

# MC10EPT20, MC100EPT20

## 3.3 V LVTTTL/LVCMOS to Differential LVPECL Translator

The MC10EPT20 is a 3.3 V TTL/CMOS to differential PECL translator. Because PECL (Positive ECL) levels are used, only +3.3 V and ground are required. The small outline SOIC-8 NB package and the single gate of the EPT20 makes it ideal for those applications where space, performance, and low power are at a premium.

The 100 Series contains temperature compensation.

### Features

- 390 ps Typical Propagation Delay
- Maximum Input Clock Frequency > 1 GHz Typical
- Operating Range:
  - ♦  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$  with  $GND = 0\text{ V}$
- PNP TTL Input for Minimal Loading
- Q Output will Default HIGH with Input Open
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



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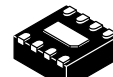
[www.onsemi.com](http://www.onsemi.com)



SOIC-8 NB  
D SUFFIX  
CASE  
751-07

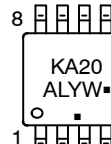
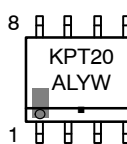
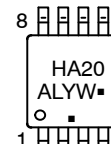
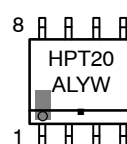


TSSOP-8  
DT SUFFIX  
CASE  
948R-02



DFN-8  
MN SUFFIX  
CASE 506AA

### MARKING DIAGRAMS\*



|    |             |   |                     |
|----|-------------|---|---------------------|
| H  | = MC10      | A | = Assembly Location |
| K  | = MC100     | L | = Wafer Lot         |
| 5W | = MC10      | Y | = Year              |
| 3Q | = MC100     | W | = Work Week         |
| M  | = Date Code | ■ | = Pb-Free Package   |

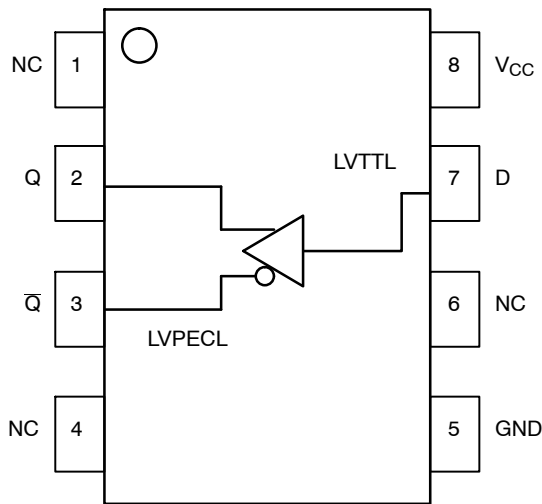
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

# MC10EPT20, MC100EPT20



**Table 1. PIN DESCRIPTION**

| PIN             | FUNCTION                                                                                                                                                                       |
|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Q, $\bar{Q}$    | Differential PECL Outputs                                                                                                                                                      |
| D               | LVTTTL Input                                                                                                                                                                   |
| V <sub>CC</sub> | Positive Supply                                                                                                                                                                |
| GND             | Ground                                                                                                                                                                         |
| NC              | No Connect                                                                                                                                                                     |
| EP              | (DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open. |

**Figure 1. 8-Lead Pinout (Top View) and Logic Diagram**

**Table 2. ATTRIBUTES**

| Characteristics                                                             | Value                         |
|-----------------------------------------------------------------------------|-------------------------------|
| Internal Input Pulldown Resistor                                            | N/A                           |
| Internal Input Pullup Resistor                                              | N/A                           |
| ESD Protection<br>Human Body Model<br>Machine Model<br>Charged Device Model | > 1.5 kV<br>> 200 V<br>> 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)               | Pb-Free Pkg                   |
| SOIC-8 NB<br>TSSOP-8<br>DFN-8                                               | Level 1<br>Level 3<br>Level 1 |
| Flammability Rating<br>Oxygen Index: 28 to 34                               | UL 94 V-0 @ 0.125 in          |
| Transistor Count                                                            | 150 Devices                   |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test                      |                               |

1. For additional information, see Application Note [AND8003/D](#).

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**Table 3. MAXIMUM RATINGS**

| Symbol           | Parameter                                | Condition 1         | Condition 2       | Rating      | Unit |
|------------------|------------------------------------------|---------------------|-------------------|-------------|------|
| $V_{CC}$         | Power Supply                             | GND = 0 V           |                   | 6           | V    |
| $V_I$            | Input Voltage                            | GND = 0 V           | $V_I \leq V_{CC}$ | 6           | V    |
| $I_{out}$        | Output Current                           | Continuous<br>Surge |                   | 50<br>100   | mA   |
| TA               | Operating Temperature Range              |                     |                   | -40 to +85  | °C   |
| T <sub>stg</sub> | Storage Temperature Range                |                     |                   | -65 to +150 | °C   |
| $\theta_{JA}$    | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm  | SOIC-8 NB         | 190<br>130  | °C/W |
| $\theta_{JC}$    | Thermal Resistance (Junction-to-Case)    | Standard Board      | SOIC-8 NB         | 41 to 44    | °C/W |
| $\theta_{JA}$    | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm  | TSSOP-8           | 185<br>140  | °C/W |
| $\theta_{JC}$    | Thermal Resistance (Junction-to-Case)    | Standard Board      | TSSOP-8           | 41 to 44    | °C/W |
| $\theta_{JA}$    | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm  | DFN-8             | 129<br>84   | °C/W |
| T <sub>sol</sub> | Wave Solder (Pb-Free)                    | <2 to 3 sec @ 260°C |                   | 265         | °C   |
| $\theta_{JC}$    | Thermal Resistance (Junction-to-Case)    | (Note 1)            | DFN-8             | 35 to 40    | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

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**Table 4. LVTTTL INPUT DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Symbol    | Characteristic                                     | Min | Typ | Max  | Unit          |
|-----------|----------------------------------------------------|-----|-----|------|---------------|
| $I_{IH}$  | Input HIGH Current ( $V_{in} = 2.7\text{ V}$ )     |     |     | 20   | $\mu\text{A}$ |
| $I_{IHH}$ | Input HIGH Current MAX ( $V_{in} = 6.0\text{ V}$ ) |     |     | 100  | $\mu\text{A}$ |
| $I_{IL}$  | Input LOW Current ( $V_{in} = 0.5\text{ V}$ )      |     |     | -0.6 | $\text{mA}$   |
| $V_{IK}$  | Input Clamp Voltage ( $I_{in} = -18\text{ mA}$ )   |     |     | -1.2 | $\text{V}$    |
| $V_{IH}$  | Input HIGH Voltage                                 | 2.0 |     |      | $\text{V}$    |
| $V_{IL}$  | Input LOW Voltage                                  |     |     | 0.8  | $\text{V}$    |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**Table 5. 10EPT PECL OUTPUT DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ,  $GND = 0\text{ V}$  (Note 1))

| Symbol   | Characteristic                | $-40^\circ\text{C}$ |      |      | $25^\circ\text{C}$ |      |      | $85^\circ\text{C}$ |      |      | Unit        |
|----------|-------------------------------|---------------------|------|------|--------------------|------|------|--------------------|------|------|-------------|
|          |                               | Min                 | Typ  | Max  | Min                | Typ  | Max  | Min                | Typ  | Max  |             |
| $I_{CC}$ | Positive Power Supply Current | 18                  | 23   | 28   | 18                 | 23   | 28   | 19                 | 24   | 29   | $\text{mA}$ |
| $V_{OH}$ | Output HIGH Voltage (Note 2)  | 2165                | 2290 | 2415 | 2230               | 2355 | 2480 | 2290               | 2415 | 2540 | $\text{mV}$ |
| $V_{OL}$ | Output LOW Voltage (Note 2)   | 1365                | 1490 | 1615 | 1430               | 1555 | 1680 | 1490               | 1615 | 1740 | $\text{mV}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Output parameters vary 1:1 with  $V_{CC}$ .
2. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

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**Table 6. 100EPT PECL OUTPUT DC CHARACTERISTICS** ( $V_{CC} = 3.3 \text{ V}$ ,  $GND = 0 \text{ V}$  (Note 1))

| Symbol   | Characteristic                | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit |
|----------|-------------------------------|-------|------|------|------|------|------|------|------|------|------|
|          |                               | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |      |
| $I_{CC}$ | Positive Power Supply Current | 20    | 25   | 30   | 22   | 27   | 32   | 23   | 28   | 33   | mA   |
| $V_{OH}$ | Output HIGH Voltage (Note 2)  | 2155  | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV   |
| $V_{OL}$ | Output LOW Voltage (Note 2)   | 1355  | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Output parameters vary 1:1 with  $V_{CC}$ .
2. All loading with  $50 \Omega$  to  $V_{CC} - 2.0 \text{ V}$ .

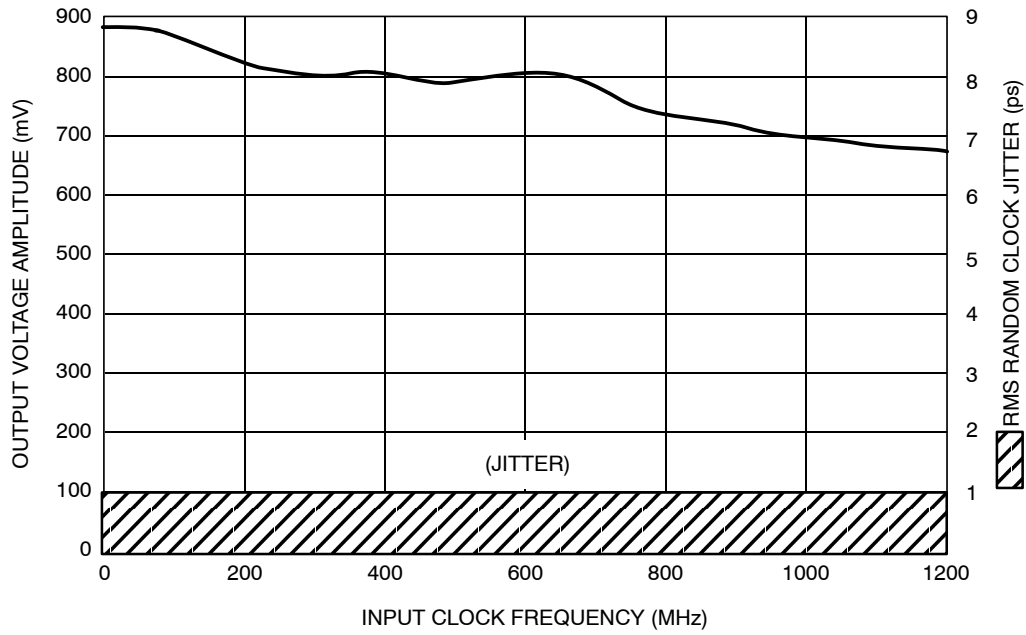
**Table 7. AC CHARACTERISTICS** ( $V_{CC} = 3.0 \text{ V}$  to  $3.6 \text{ V}$ ,  $GND = 0 \text{ V}$  (Note 1))

| Symbol                   | Characteristic                                        | -40°C |     |     | 25°C |     |     | 85°C |     |     | Unit |
|--------------------------|-------------------------------------------------------|-------|-----|-----|------|-----|-----|------|-----|-----|------|
|                          |                                                       | Min   | Typ | Max | Min  | Typ | Max | Min  | Typ | Max |      |
| $f_{max}$                | Maximum Input Clock Frequency                         |       | > 1 |     |      | > 1 |     |      | > 1 |     | GHz  |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Propagation Delay to Output Differential              | 280   | 350 | 430 | 300  | 370 | 450 | 320  | 400 | 490 | ps   |
| $t_{SKEW}$               | Device-to-Device Skew (Note 2)                        |       |     | 150 |      |     | 150 |      |     | 170 | ps   |
| $t_{JITTER}$             | RMS Random Clock Jitter                               |       | 1   | 2   |      | 1   | 2   |      | 1   | 2   | ps   |
| $t_r$ ,<br>$t_f$         | Output Rise/Fall Times<br>Q, $\bar{Q}$<br>(20% – 80%) | 70    | 100 | 170 | 80   | 120 | 180 | 90   | 140 | 190 | ps   |

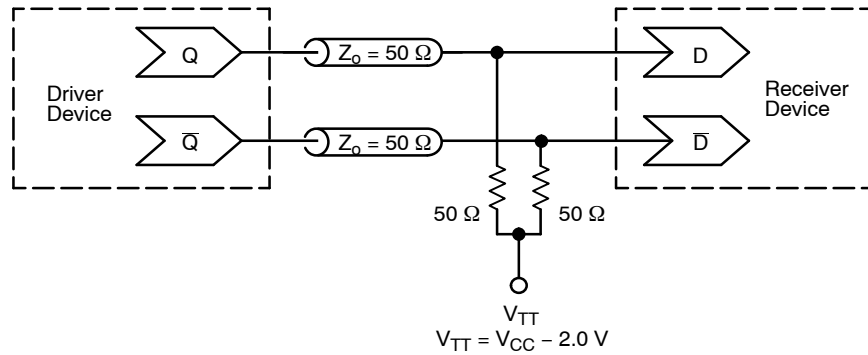
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Measured using a LVTTTL source, 50% duty cycle clock source. All loading with  $50 \Omega$  to  $V_{CC} - 2.0 \text{ V}$ .
2. Skew is measured between outputs under identical transitions.

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**Figure 2. Output Voltage Amplitude ( $V_{OUTpp}$ )/RMS Jitter vs. Input Clock Frequency at Ambient Temperature**



**Figure 3. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

## MC10EPT20, MC100EPT20

### ORDERING INFORMATION

| Device          | Package                | Shipping <sup>†</sup> |
|-----------------|------------------------|-----------------------|
| MC10EPT20DG     | SOIC-8 NB<br>(Pb-Free) | 98 Units/Rail         |
| MC10EPT20DR2G   | SOIC-8 NB<br>(Pb-Free) | 2500 / Tape & Reel    |
| MC10EPT20DTG    | TSSOP-8<br>(Pb-Free)   | 100 Units/Rail        |
| MC10EPT20DTR2G  | TSSOP-8<br>(Pb-Free)   | 2500 / Tape & Reel    |
| MC10EPT20MNR4G  | DFN-8<br>(Pb-Free)     | 1000 / Tape & Reel    |
| MC100EPT20DG    | SOIC-8 NB<br>(Pb-Free) | 98 Units/Rail         |
| MC100EPT20DR2G  | SOIC-8 NB<br>(Pb-Free) | 2500 / Tape & Reel    |
| MC100EPT20DTG   | TSSOP-8<br>(Pb-Free)   | 100 Units/Rail        |
| MC100EPT20DTR2G | TSSOP-8<br>(Pb-Free)   | 2500 / Tape & Reel    |
| MC100EPT20MNR4G | DFN-8<br>(Pb-Free)     | 1000 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

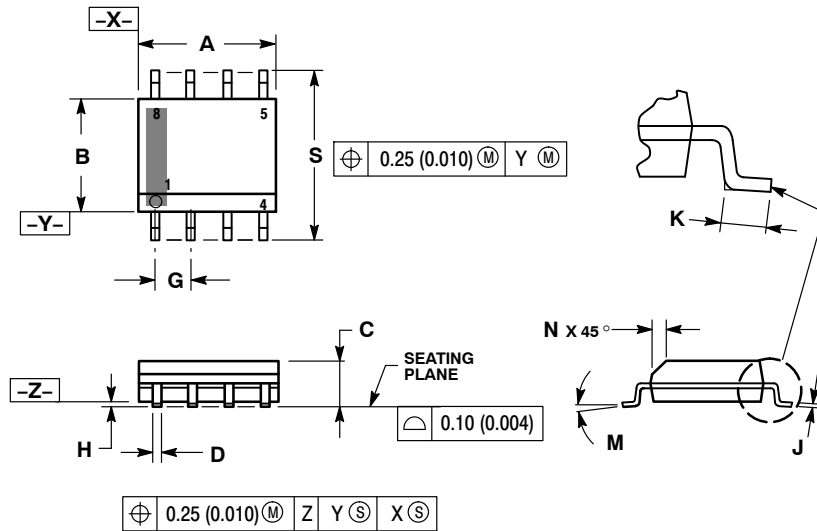
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC10EPT20, MC100EPT20

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AK

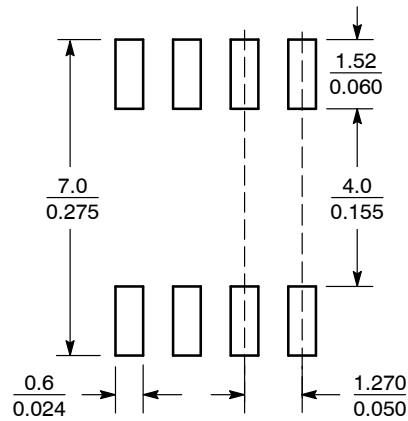


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

## SOLDERING FOOTPRINT\*



SCALE 6:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

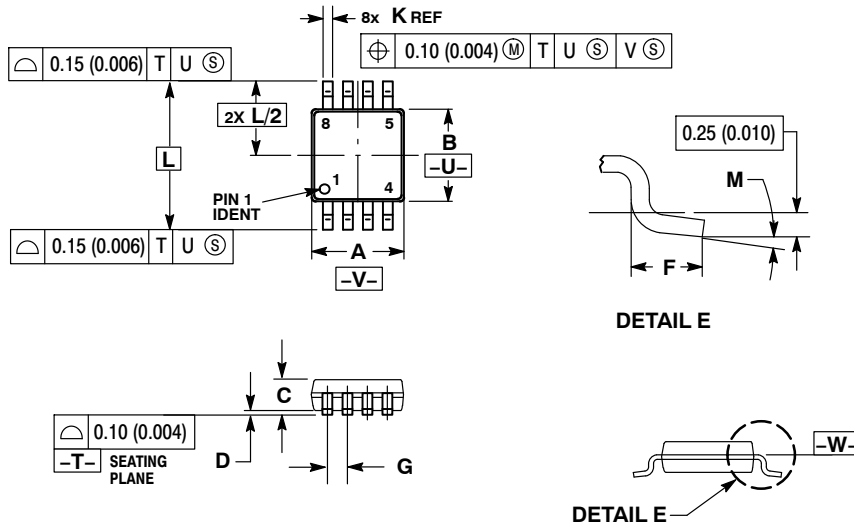
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, [SOLDERRM/D](http://www.onsemi.com/SOLDERRM/D).



# MC10EPT20, MC100EPT20

## PACKAGE DIMENSIONS

TSSOP-8  
CASE 948R-02  
ISSUE A



### NOTES:

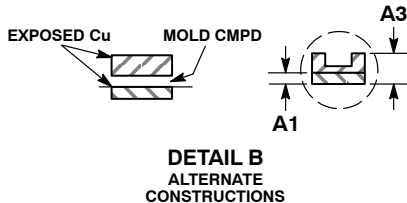
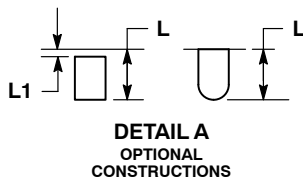
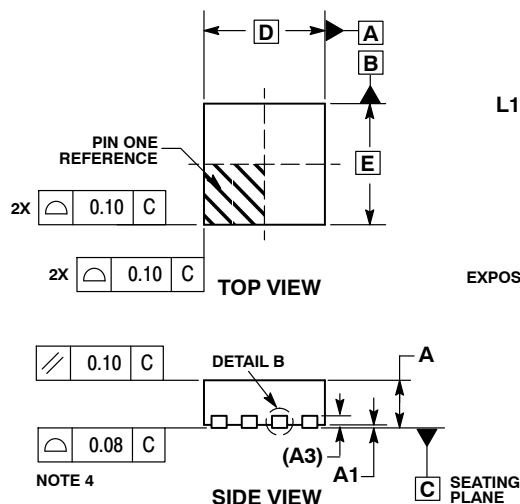
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 2.90        | 3.10 | 0.114     | 0.122 |
| B   | 2.90        | 3.10 | 0.114     | 0.122 |
| C   | 0.80        | 1.10 | 0.031     | 0.043 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.40        | 0.70 | 0.016     | 0.028 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| K   | 0.25        | 0.40 | 0.010     | 0.016 |
| L   | 4.90 BSC    |      | 0.193 BSC |       |
| M   | 0 °         | 6 °  | 0 °       | 6 °   |

# MC10EPT20, MC100EPT20

## PACKAGE DIMENSIONS

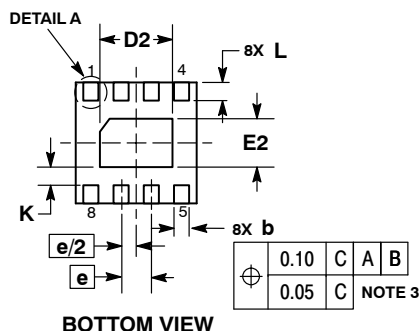
DFN-8 2x2, 0.5P  
CASE 506AA  
ISSUE F



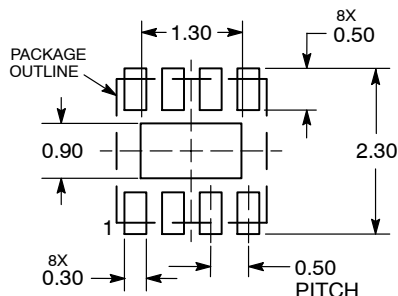
### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 0.80        | 1.00 |
| A1  | 0.00        | 0.05 |
| A3  | 0.20        | REF  |
| b   | 0.20        | 0.30 |
| D   | 2.00        | BSC  |
| D2  | 1.10        | 1.30 |
| E   | 2.00        | BSC  |
| E2  | 0.70        | 0.90 |
| e   | 0.50        | BSC  |
| K   | 0.30        | REF  |
| L   | 0.25        | 0.35 |
| L1  | ---         | 0.10 |



## RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, [SOLDDRM/D](#).

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