TEXAS INSTRUMENTS

LMH0318

SNLS508 – SEPTEMBER 2015

LMH0318 3 Gbps HD/SD SDI Reclocker with Integrated Cable Driver

1 Features

- Supports ST 424(3G), 292(HD), 259(SD), MADI, and DVB-ASI
- Locks to rates 2.97 Gbps, 1.485 Gbps, or Divided by 1.001 sub-rates, and DVB-ASI
- Reference-free Operation with Fast Lock Time covering all Supported or Selected Data Rates
- 75 Ω and 100 Ω Transmitter Outputs
- Integrated 2:1 Mux Input, 1:2 Demux/Fanout Outputs
- Automatic Slew Rate Based on Input Rate Detect
- On-chip Eye Monitor
- Low 300 mW Power Consumption With Automatic Power Down On Loss Of Input Signal
- Programmable via SPI, Or SMBus Interface
- Single 2.5 V Supply Operation
- Small 4 mm × 4 mm 24-pin QFN Package
- -40°C to +85°C Operating Temperature Range
- Footprint compatible with LMH1218 for easy upgrade to 12G

2 Applications

- SMPTE Compatible Serial Digital Interface (SDI)
- Broadcast Video Routers, Switches, and Monitors
- Digital Video Processing and Editing
- DVB-ASI and Distribution Amplifiers

3 Description

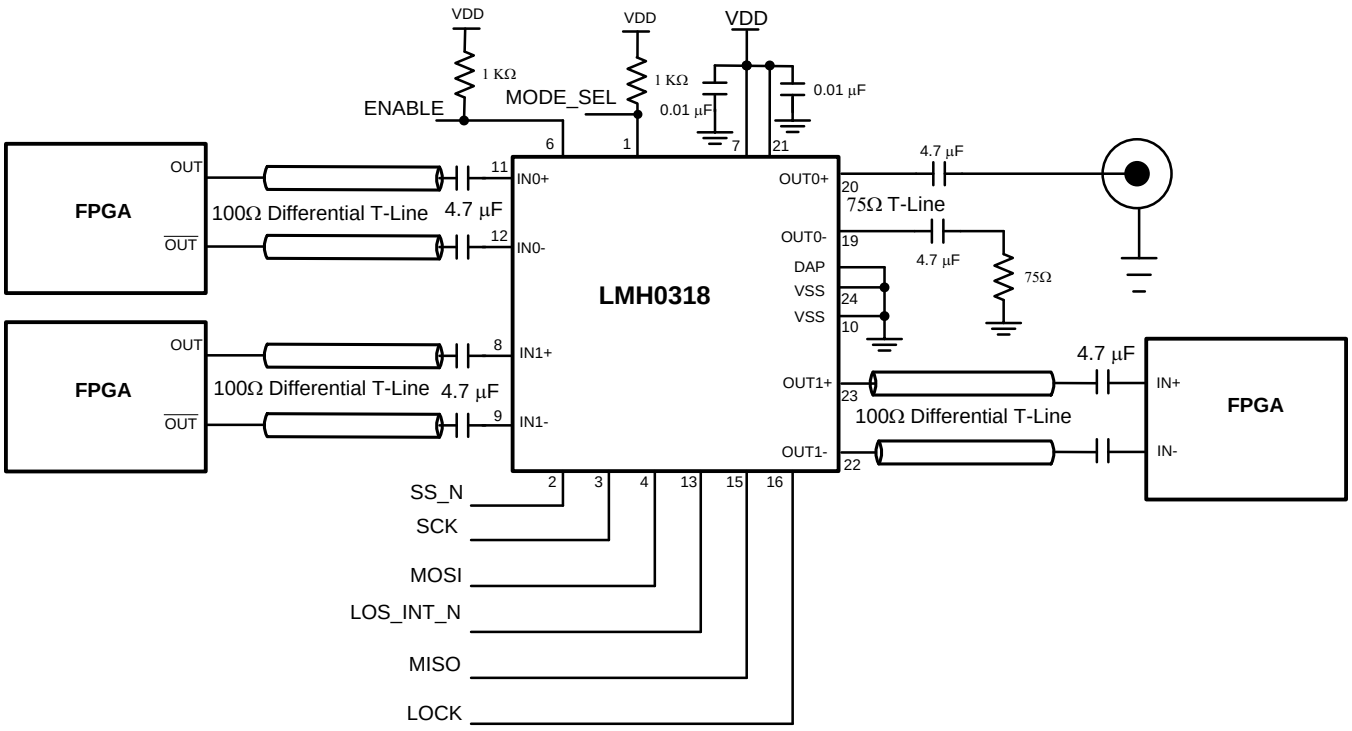
The LMH0318 is a 3 Gbps HD/SD SDI Reclocker with Integrated Cable Driver designed to drive serial video data compatible to SMPTE-SDI and DVB-ASI standards. The clock and data recovery circuit eliminates accumulated jitter and detects the incoming data rate without requiring an external reference clock. The integrated driver with 75 ohm and 50 ohm outputs enables multiple media options such as coax and FR4 PCB.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH0318	WQFN (24)	4 mm × 4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified SPI Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Description continued ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 6
7.1 Absolute Maximum Ratings ... 6
7.2 ESD Ratings ... 6
7.3 Recommended Operating Conditions ... 6
7.4 Thermal Information ... 6
7.5 Electrical Characteristics ... 7
7.6 Recommended SMBus Interface AC Timing Specifications ... 11
7.7 Serial Parallel Interface (SPI) Bus Interface AC Timing Specifications ... 11
7.8 Typical Characteristics ... 12
8 Detailed Description ... 13
8.1 Overview ... 13
8.2 Functional Block Diagram ... 13
8.3 Feature Description ... 14
8.4 Device Functional Modes ... 24
8.5 Programming ... 24
9 Application and Implementation ... 43
9.1 Application Information ... 43
9.2 Typical Application ... 43
9.3 Do's and Don'ts ... 48
9.4 Initialization Set Up ... 48
10 Power Supply Recommendations ... 48
11 Layout ... 49
11.1 Layout Guidelines ... 49
11.2 Layout Example ... 49
11.3 Solder Profile ... 50
12 Device and Documentation Support ... 51
12.1 Device Support ... 51
12.2 Documentation Support ... 51
12.3 Community Resources ... 51
12.4 Trademarks ... 51
12.5 Electrostatic Discharge Caution ... 51
12.6 Glossary ... 51
13 Mechanical, Packaging, and Orderable Information ... 51

4 Revision History

DATE	REVISION	NOTES
September 2015	*	Initial release.

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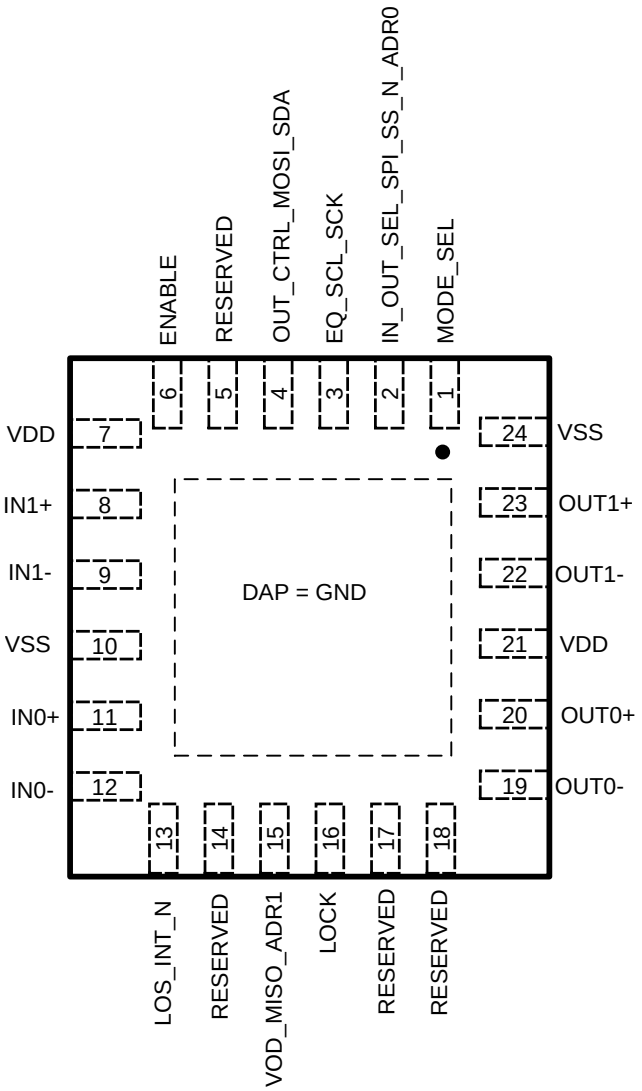
5 Description continued

The integrated 2-to-1 MUX on the input of the LMH0318 enables selection between two video sources, while the programmable equalizer compensates for the PC board loss to extend signal reach. With a wide range clock-and-data recovery (CDR) circuit, the on-chip reclocker automatically detects and locks to serial data from 270 Mbps to 2.97 Gbps without the need for an external reference clock and loop filter component, thereby simplifying board design and lowering system cost. The reclocked serial data can be routed to either the 75 Ω or 50 Ω transmitter output, or both simultaneously (1-to-2 fanout mode). The output voltage swing is compatible to ST 424, 344, 292, and 259 standards.

A non-disruptive eye monitor allows for real-time measurement of serial data to simplify system startup or field tuning. The LMH0318 is pin compatible with the LMH1218, 12 Gbps Cable Driver with Integrated Reclocker.

6 Pin Configuration and Functions

24-Pin WQFN
Package RTWA0024A
(Top View)



Pin Descriptions – SPI Mode/ Mode_SEL = 1 kΩ to VDD

PIN		I/O	DESCRIPTION
NAME	NO.		
CONTROL/INDICATOR I/O			
MODE_SEL	1	Input, 4-Level	Determines Device Configuration: SPI or SMBus 1 kΩ to VDD: • SPI mode. See *Initialization Set Up*
SS_N	2	Input, 2-Level	SPI Slave Select. . This pin has internal pull up
SCK	3	Input, 2.5V LVCMOS, 2-Level	SPI serial clock input
MOSI	4	Input, 2-Level	SPI Master Output / Slave Input. LMH0318 SPI data receive
RESERVED	5,14,17, 18		No Connect
ENABLE	6	Input, 4-Level	Powers down device when pulled low 1 kΩ to VDD: • Power down until valid signal detected Float(**Default**): • Reserved 20 kΩ to GND: • Reserved 1 kΩ to GND: • Power down including signal detects and Reset Registers upon power-up
LOS_INT_N	13	Output, LVCMOS Open Drain, 2-Level	Programmable Interrupt caused by change in LOS, violation of internal eye monitor threshold, or change in lock. External 4.7-kΩ pull-up resistor is required. This pin is 3.3 V LVCMOS tolerant.
MISO	15	Output, 2.5 V LVCMOS, 2-Level	SPI Master Input / Slave Output. LMH0318 SPI data transmit
LOCK	16	Output, 2.5V LVCMOS, 2-Level	Indicates CDR lock detect status High: • CDR locked Low: • CDR not locked
HIGH SPEED DIFFERENTIAL I/O			
IN0+	11	Input, Analog	Inverting and non-inverting differential inputs. An on-chip 100 Ω terminating resistor connects IN0+ to IN0-. Inputs require 4.7 µF AC coupling capacitors.
IN0-	12	Input, Analog	
IN1+	8	Input, Analog	Inverting and non-inverting differential inputs. An on-chip 100 Ω terminating resistor connects IN1+ to IN1-. Inputs require 4.7 µF AC coupling capacitors.
IN1-	9	Input, Analog	
OUT0+	20	Output, 75 Ω CML Compatible	Inverting and non-inverting 75 Ω outputs. An on-chip 75 Ω terminating resistor connects OUT0+ and OUT0- to VDD. Outputs require 4.7 µF AC coupling capacitors
OUT0-	19	Output, 75 Ω CML Compatible	
OUT1+	23	Output, Analog	Inverting and non-inverting differential outputs. An on-chip 100 Ω terminating resistor connects OUT1+ to OUT1-. Outputs require 4.7 µF AC coupling capacitors
OUT1-	22	Output, Analog	
POWER			
VDD	7, 21	2.5 V Supply	2.5 V ± 5%
VSS	10, 24	Ground	Connect directly to ground (GND)
DAP		Ground	Exposed DAP, connect to GND using at least 5 vias (see Figure 23)

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Pin Descriptions – SMBUS Mode/ MODE_SEL = 1 kΩ to GND

PIN		I/O	DESCRIPTION
NAME	NO.		
MODE_SEL	1	Input, 4-Level	Determines Device Configuration: SPI or SMBus 1 kΩ to GND: SMBUS mode. See *Initialization Set Up*
ADDR0	2	Input, 4-Level	4-level strap pins used to set the SMBus address of the device. The pin state is read on power-up. The multi-level nature of these pins allows for 16 unique device addresses. Note SMBus section for further details. The four strap options include: 1 kΩ to VDD: • Represents logic state 11'b Float(**Default**): Represents logic state 10'b 7-bits SMBus address = 0x17 20 kΩ to GND: • Represents logic state 01'b 1 kΩ to GND: • Represents logic state 00'b
ADDR1	15		
SCL	3	Input, 2-Level	SMBus clock input / open drain. External 2-kΩ to 5-kΩ pull-up resistor is required as per SMBus interface standard. This pin is 3.3 V LVCMOS tolerant.
SDA	4	I/O, Open Drain, 2-Level	SMBus data input / open drain. External 2-kΩ to 5-kΩ pull-up resistor is required as per SMBus interface standard. This pin is 3.3 V LVCMOS tolerant.
RESERVED	5,14,17, 18		No Connect
ENABLE	6	Input, 4-Level	Powers down device when pulled low 1 kΩ to VDD: • Power down until valid signal detected Float(**Default**): Reserved 20 kΩ to GND: • Reserved 1 kΩ to GND: • Power down including signal detects and Reset Registers upon power-up
LOS_INT_N	13	Output, LVCMOS Open Drain, 2-Level	Programmable Interrupt caused by change in LOS, violation of internal eye monitor threshold, change in lock. External 4.7-kΩ pull-up resistor is required. This pin is 3.3 V LVCMOS tolerant.
LOCK	16	Output, 2.5 V LVCMOS, 2-Level	Indicates CDR lock Status High: • CDR locked Low: • CDR not locked
HIGH SPEED DIFFERENTIAL I/O			
IN0+	11	Input, Analog	Inverting and non-inverting differential inputs. An on-chip 100 Ω terminating resistor connects IN0+ to IN0-. Inputs require 4.7 µF AC coupling capacitors.
IN0-	12	Input, Analog	
IN1+	8	Input, Analog	Inverting and non-inverting differential inputs. An on-chip 100 Ω terminating resistor connects IN0+ to IN0-. Inputs require 4.7 µF AC coupling capacitors.
IN1-	9	Input, Analog	
OUT0+	20	Output, 75 Ω CML Compatible	Inverting and non-inverting 75 Ω outputs. An on-chip 75 Ω terminating resistor connects OUT0+ and OUT0- to VDD. Outputs require 4.7 µF AC coupling capacitors
OUT0-	19	Output, 75 Ω CML Compatible	
OUT1+	23	Output, Analog	Inverting and non-inverting differential outputs. An on-chip 100 Ω terminating resistor connects OUT1+ to OUT1-. Outputs require 4.7 µF AC coupling capacitors
OUT1-	22	Output, Analog	
VDD	7, 21	2.5 V Supply	2.5V ± 5%
VSS	10, 24	Ground	Connect directly to ground (GND)
DAP		Ground	Exposed DAP, connect to GND using at least 5 vias (see Figure 23)

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply Voltage (VDD to GND)	-0.5	2.75	V
3.3 V Open drain I/O input/output voltage (SDA, SCL, LOS_INT_N)	-0.5	4.0	V
2.5V LVCMOS Input/Output Voltage	-0.5	2.75	V
High Speed input Voltage	-0.5	2.75	V
High Speed Input Current	-30	30	mA

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are ensured for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4500 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±1500 V may actually have higher performance.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage(1)	2.375	2.5	2.625	V
3.3 V Open drain I/O input/output voltage(1)	3	3.3	3.6	V
Supply noise, 50 Hz to 10 MHz, sinusoidal		40		mVpp
Ambient Temperature	-40	25	85	ºC
Source transmit differential launch amplitude	300	500	1000	mV_{P-P}
SMBus clock frequency (SCL) in SMBus slave mode		100	400	kHz
SMBUS SDA and SCL Voltage Level			3.6	V
SPI Clock Frequency		10	20	MHz

(1) DC plus AC power should not exceed these limits.

7.4 Thermal Information

THERMAL METRIC(1)(2)		RTWA0024A	UNIT
		24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	11.8	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	11.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) No heat sink is assumed for these estimations. Depending on the application, a heat sink, faster air flow, and/or reduced ambient temperature (< 85ºC) may be required in order to maintain the maximum junction temperature specified in *Electrical Characteristics*.

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7.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
PD	Power dissipation	Locked 75 Ω OUT0 only (800 mVpp), EOM powered down		300		mW
		Locked OUT1 only (600 mVpp, diff), EOM powered down		195		mW
		Transient power during CDR lock acquisition, 75 Ω OUT0 and OUT1 powered up, EOM powered down		400	500	mW
PD_RAW	Power dissipation in force RAW mode (CDR bypass)	EQ bypass, OUT0 720mVpp, OUT1 600mVpp IN0 to OUT0 and OUT1 or IN1 to OUT0 and OUT1		195		mW
		IN0 to OUT0, OUT1 powered down		160		mW
		IN1 to OUT1, OUT0 powered down		80		mW
4-LEVEL INPUT and 2.5 V LVCMOS DC SPECIFICATIONS						
V_{IH}	High level input voltage	4-level input (MODE_SEL, ADDR0/1, ENABLE pins)		0.95*VDD		V
V_{IF}	Float level input voltage	4-level input (MODE_SEL, ADDR0/1, ENABLE pins)		0.67*VDD		V
V_{I20K}	20K to GND input voltage	4-level input (MODE_SEL, ADDR0/1, ENABLE pins)		0.33*VDD		V
V_{IL}	Low level input voltage	4-level input (MODE_SEL, ADDR0/1, ENABLE pins)		0.1		V
V_{OH}	High level output voltage	IOH = -3 mA	2			V
V_{OL}	Low level output voltage	IOL = 3 mA			0.4	V
I_{IH}	Input high leakage current	V_{input} = VDD SPI Mode: LVCMOS (SPI_SCK, SPI_SS_N) pins			15	µA
		SMBus Mode: LVCMOS (SMB_SDA, SMB_SCL) pins			15	µA
		SMBus Mode: 4-Levels (ADDR0, ADDR1) pins	20	44	80	µA
		4-Levels (MODE_SEL, ENABLE) pins	20	44	80	µA
I_{IL}	Input low leakage current	Vinput = GND SPI Mode: LVCMOS (SPI_MOSI, SPI_SCK) pins	-15			µA
		Vinput = GND SPI Mode: LVCMOS (SPI_SS_N) pins	-37			µA
		SMBus Mode: LVCMOS (SMB_SDA, SMB_SCL pins	-15			µA
		SMBus Mode: 4-Levels (ADDR0, ADDR1) pins	-160	-93	-40	µA
		4-Levels (MODE_SEL, ENABLE) pins	-160	-93	-40	µA

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Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
3.3-V TOLERANT LVCMOS / LVTTL DC SPECIFICATIONS (SDA, SCL, LOS_INT_N)						
V_{IH25}	High level input voltage	2.5 V Supply Voltage	1.75		3.6	V
V_{IL}	Low level input voltage		GND		0.8	V
V_{OL}	Low level output voltage	IOL = 1.25 mA			0.4	V
I_{IH}	Input high current	VIN = 2.5 V, VDD = 2.5 V	20		40	µA
I_{IL}	Input low current	VIN = GND, VDD = 2.5 V	-10		10	µA
SIGNAL DETECT						
S_{DH}	Signal detect (default) Assert threshold level(1)(2)	2.97 Gbps, EQ Pathological Pattern		22		mV_{P-P}
		2.97 Gbps, PLL Pathological Pattern		22		mV_{P-P}
		2.97 Gbps, PRBS10 Pattern		22		mV_{P-P}
S_{DL}	Signal detect (default) De-assert threshold level(1)	2.97 Gbps EQ Pathological Pattern		16		mV_{P-P}
		2.97 Gbps, PLL Pathological Pattern		16		mV_{P-P}
		2.97 Gbps, PRBS10 Pattern		9		mV_{P-P}
HIGH SPEED RECEIVE RX INPUTS (IN_n+, IN_n-)						
R_RD	DC Input differential resistance		75	100	125	Ω
RL_{RX-SDD}	Input differential return loss(3)(4)	Measured with the device powered up. SDD11 10 MHz to 2 GHz		-14		dB
		SDD11 2 GHz to 3 GHz		-6.5		dB
RL_{RX-SCD}	Differential to common mode Input conversion(3)(4)	Measure with the device powered up.SCD11, 10 MHz to 3 GHz		-20		dB
HIGH SPEED OUTPUTS (OUT_n+, OUT_n-)						
V_{VOD_OUT1}	Output differential voltage(3)(4)	Default setting, 8T clock pattern	400	600	700	mV_{P-P}
$V_{VOD_OUT1_DE}$	De-emphasis Level	VOD = 600mV, maximum De-Emphasis with 16T clock pattern		-9		dB
$V_{VOD_OUT1_CLK}$	Clock output differential voltage	2.97 GHz,1.485 GHz, and 270 MHz		560		mV_{P-P}
V_{VOD_OUT0}	Output single ended voltage at OUT0+ with OUT0- terminated(5)(3)	Default setting	720	800	880	mV_{P-P}
R_{DIFF_OUT1}	DC output differential resistance			100		Ω

(1) Data with extraordinarily long periods of high-frequency 1010 data, and for long, lossy channels, the signal amplitude at the input to the device may be severely attenuated by the channel and may fall below the signal detect assert and/or de-assert thresholds.
(2) The voltage noise on the receiver inputs which has an amplitude larger than the signal detect assert threshold may trigger a signal detect assert condition
(3) These limits are ensured by bench characterization and are not production tested.
(4) Dependent on board layout. Characterization data was measured with LMH1218EVM evaluation board
(5) ATE Production tested using DC method. Apply differential DC signal at the input and measure OUT0P amplitude. OUT0N terminated in 75 Ohm.

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Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DIFF_OUT0}	DC output single ended resistance			75		Ω
$T_{R_F_OUT1}$	Output rise/fall time	Full Slew Rate, 20% to 80% using 8T Pattern		45		ps
$T_{R_F_OUT0}$	Output rise/fall time, PRBS15 (3)(4)	2.97 Gbps		35	45	ps
		1.485 Gbps		35	45	ps
		270 Mbps	400	900	1500	ps
$T_{R_F_OUT0_delta}$	Output rise/fall time mismatch(3)(4)	2.97 Gbps		3	18	ps
		1.485 Gbps		3	18	ps
		270 Mbps		72	500	ps
$V_{OVR_UDR_SHOOT}$	Output overshoot, undershoot(3) (4)	3G/HD/SD Measured with 8T pattern		2.4%	<10%	
V_{DC_OFFSET}	DC offset	3G/HD/SD		±0.2		V
V_{DC_WANDER}	DC wander	3G/HD/SD EQ Pathological		20		mV
RL_{OUT0_S22}	OUT0 single ended 75-Ω return loss(3)(4)(6)	S22 5 MHz to 1.485 GHz		< -15		dB
		S22 1.485 GHz to 3 GHz		< -10		dB
RL_{OUT1_SDD22}	OUT1 differential 100-Ω return loss(4)(7)	SDD22 10 MHz - 2 GHz		-20		dB
		SDD22 2 GHz - 3 GHz		-17		dB
RL_{OUT1_SCC22}	OUT1 common mode 50-Ω return loss(4)(7)	SCC22 10 MHz - 3 GHz		-11		dB
$V_{VCM_OUT1_NOISE}$	AC common mode voltage noise(4)	VOD = 0.6 Vpp, DE = 0dB, PRBS31, 2.97 Gbps		8		mV_{RMS}
$T_{RCK_LATENCY}$	Latency reclocked	Reclocked Data		1.5 UI +195		ps
$T_{RAW_LATENCY}$	Latency CDR bypass	Raw Data		230		ps
TRANSMIT OUTPUT JITTER SPECIFICATIONS						
A_{J_OUT0}	Alignment jitter(4)	OUT0, PRBS15, 2.97 Gbps		0.045		UI
T_{J_OUT1}	Total jitter (1E-12)(4)	OUT1, PRBS15 2.97 Gbps		0.06		UI
R_{J_OUT1}	Random jitter (rms)	OUT1, PRBS15, 2.97 Gbps		0.91		ps_{RMS}
D_{J_OUT1}	Deterministic jitter	OUT1, PRBS15, 2.97 Gbps		6.8		ps_{P-P}

(6) Output return loss is dependent on board design, this is measured with the LMH1218EVM evaluation board
(7) Measure with the device powered up and outputs a clock signal.

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Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK DATA RECOVERY						
D_{DATA_RATE}		SMPTE 424[8]		2.970 2.967		Gbps
		SMPTE 292[8]		1.485 1.4835		Gbps
		SMPTE 259M[8]		270		Mbps
P_{PLL_BW}	PLL bandwidth at -3 dB	Measured with 0.2UI S_J at 2.97 Gbps		5		MHz
		Measured with 0.2UI S_J at 1.485 Gbps		3		MHz
		Measured with 0.2UI S_J at 270 Mbps		1		MHz
J_{TOL}	Total input jitter tolerance	TJ = D_J + R_J + S_J, D_J+R_J = 0.15 UI S_J/P_J, low to high upward sweep (10 kHz to 10 MHz)		0.65		UI
T_{LOCK}	Lock time[3][9]	From signal detected to the lock asserted, HEO/VEO lock monitor disable, same setting for 2.97G, 1.485G and 270 MHz data rates		<5		ms
T_{TEMP_LOCK}	CDR lock with temperature ramp	Temperature Lock Range, 5ºC per minute ramp up and down, -40ºC to 85ºC operating range		125		°C

(8) Data rate tolerance is within ±1000 ppm
(9) The total CDR lock time depends on number of rate settings enabled and application data rate

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7.6 Recommended SMBus Interface AC Timing Specifications (1)(2)(3)

Over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	Bus operating frequency	MODE_SEL = 0	10	100	400	kHz
t_{BUF}	Bus free time between stop and start condition		1.3			µs
$t_{HD:STA}$	Hold time after (repeated) start condition After this period, the first clock is generated		0.6			µs
$t_{SU:STA}$	Repeated start condition setup time		0.6			µs
$t_{SU:STO}$	Stop condition setup time		0.6			µs
$t_{HD:DAT}$	Data hold time		0			ns
$t_{SU:DAT}$	Data setup time		100			ns
t_{LOW}	Clock low period		1.3			µs
t_{HIGH}	Clock high period		0.6		50	µs
t_F	SDA fall time read operation				300	ns
t_R	SDA rise time read operation				300	ns

(1) SMBus operation is available 20ms after power up
(2) These specifications support SMBus 2.0 specifications
(3) These Parameters are not production tested

7.7 Serial Parallel Interface (SPI) Bus Interface AC Timing Specifications (1)(2)(3)

Over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCK}	SCK frequency	MODE_SEL = 1		10	20	MHz
T_{SCK}	SCK period		50			ns
t_{PH}	SCK pulse width high			0.40*T_{SCK}		ns
t_{PL}	SCK pulse width low			0.40*T_{SCK}		ns
t_{SU}	MOSI setup time		4			ns
t_H	MOSI hold time		4			ns
t_{SSSu}	SS_N setup time		14	18		ns
t_{SSH}	SS_N hold time		4			ns
t_{SSOF}	SS_N off time			1		µs
t_{ODZ}	MISO driven to TRI-STATE time			20		ns
t_{OZD}	MISO TRI-STATE-to-Driven time			10		ns
t_{OD}	MISO output delay time			15		ns

(1) Typical values are parametric norms at VDD = 2.5 V, TA = 25ºC, and recommended operating conditions at the time of product characterization. Typical values are not production tested.
(2) These specifications support SPI 1.0 specifications.
(3) These Parameters are not production tested

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7.8 Typical Characteristics

Typical device characteristics at T_A = +25°C and VDD = 2.5 V, unless otherwise noted.

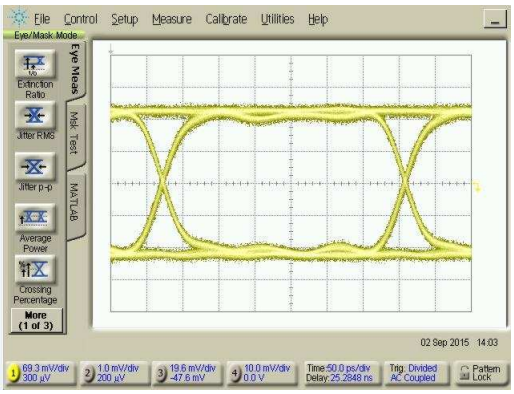


Figure 1. 75 Ω OUT0 PRBS10 at 2.97 Gbps

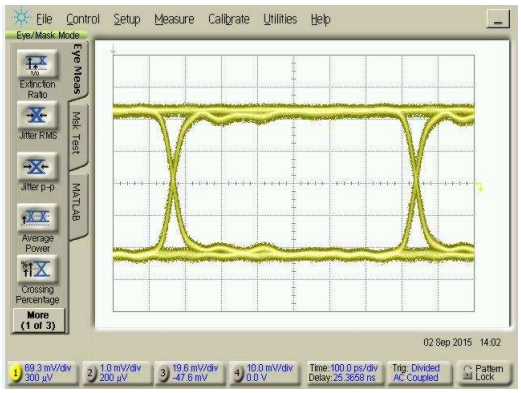


Figure 2. 75 Ω OUT0 PRBS10 at 1.485 Gbps

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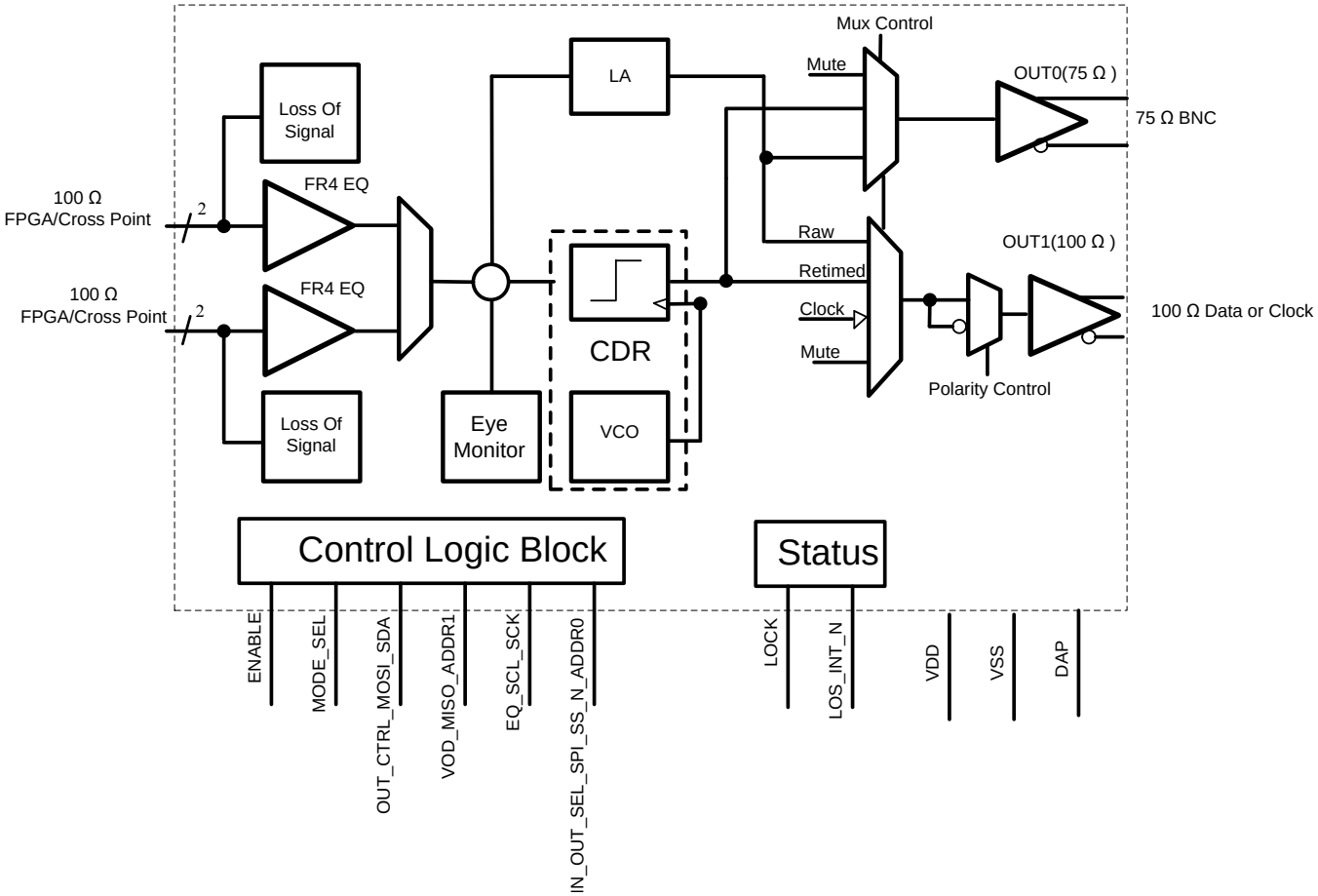
8 Detailed Description

8.1 Overview

The LMH0318 is a 2.97Gbps/1.485Gbps/0.27Gbps multi-rate serial digital video data reclocker with integrated cable driver intended for equalizing, reclocking, and driving data compatible to the SMPTE standards. It is a 2-input, 2-output single-core chip, enabling 1:2 fan-out or 2:1 MUX operations. Each input has a 100 Ω continuous time linear equalizer (CTLE) at the front-end, intended to compensate for loss over STP coax or FR-4 PCB trace. The LMH0318 OUT0 is a 75 Ω cable driver compatible to the SMPTE requirements.

The referenceless Clock-and-Data Recovery (CDR) circuit selects between the two inputs based on user choice. The reclocked output can be driven to one or two outputs. One of the outputs supports 100-Ω differential cable connection, while the other output can drive a 75 Ω SMPTE specified cable while meeting transmitter requirements as specified in SMPTE standard. The LMH0318 locks to all required SDI data rates, including 270Mbps, 1.485 Gbps, 1.4835 Gbps, 2.97 Gbps, and 2.967 Gbps. The LMH0318 is assembled in a 4 mm × 4 mm 24-pin QFN package. The chip can be programmed using SPI or SMBus interface.

8.2 Functional Block Diagram



8.3 Feature Description

The LMH0318 data path consists of several key blocks as shown in the *Functional Block Diagram*. These key circuits are:

- Loss of Signal Detector
- Continuous Time Linear Equalizer (CTLE) for FR4 Compensation
- 2:1 Multiplexer/1:2 Fanout
- CDR
- Eye Monitor
- Differential Output Selection
- 75 Ω and 100 Ω Output Drivers
- SMBus/SPI Configuration

8.3.1 Loss of Signal Detector

The LMH0318 supports two high speed differential input ports, with internal 100 Ω terminations. The inputs must be AC coupled. The external AC coupling capacitor value should take into account the pathological low frequency content. For most applications, the RC time constant of 4.7 µF AC coupling capacitor plus the 50 Ω termination resistor is capable of handing the pathological video pattern's low frequency content.

The signal detect circuit is designed to assert when data traffic with a certain minimum amplitude is present at the input of the device. It is also designed to de-assert, or remain de-asserted, when there is noise below certain amplitude at the input to the device.

The LMH0318 has two signal detect circuits, one for each input. Each signal detect threshold can be set independently. By default, both signal detects are powered on. The user selects IN1 or IN0 through SMBus/SPI interface.

8.3.2 Continuous Time Linear Equalizer (CTLE)

The LMH0318 has receive-side equalization, and a key part is the Continuous Time Linear Equalizer (CTLE). This circuit operates on the received differential signal and compensates for frequency-dependent loss due to the transmission media. The CTLE applies gain to the input signal. This gain varies over frequency: higher frequencies are boosted more than lower frequencies. The CTLE works to restore the input signal to full amplitude across a wide range of frequencies.

The CTLE consists of 4 stages with each stage having two boost control bits. This allows 256 different boost settings. CTLE boost levels are determined by summing the boost levels of the 4 stages. The CTLE is configured manually. See *LMH0318 Programming Guide* (SNLU183) on how to quickly select the most appropriate CTLE boost setting.

There are two CTLEs, one for each input, IN0 and IN1. Only one CTLE is enabled at a time, according to the user input channel selection. If IN0 is selected, the CTLE for IN0 is powered on and the IN1 CTLE is powered off. The CTLE is able to handle low loss channels without over-equalizing by bypassing the CTLE.

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Feature Description (continued)

8.3.3 2:1 Multiplexer

A 2:1 input multiplexor connects IN0 and IN1 to the CDR. By default, IN0 is selected. To select IN1, the 2:1 multiplexer must be set. See *LMH0318 Programming Guide* (SNLU183) for detailed settings.

8.3.4 Clock and Data Recovery

By default, the equalized data is fed into the CDR for clock and data recovery. The CDR consists of a reference-less Phase Frequency Detector (PFD), Charge Pump (CP), Voltage Controlled Oscillator (VCO), and Output Data Multiplexer (Mux).

The inputs to the Phase and Frequency Detector (PFD) are the data after the CTLE as well as I and Q clocks from the VCO. The LMH0318 will attempt to lock to the incoming data by tuning the VCO to phase-lock to the incoming data rate.

The supported data rates are listed in the following table. See *LMH0318 Programming Guide* (SNLU183) for further information on configuring the LMH0318 for different data rates.

Table 1. Supported Data Rates

DATA RATE RANGE	CDR MODE	COMMENT
2.97 Gbps, 2.967 Gbps	Enabled	
1.485 Gbps, 1.4835 Gbps	Enabled	
270 Mbps	Enabled	
125 Mbps	Disabled	At 125 Mbps device is in CDR bypass

8.3.5 Eye Opening Monitor (EOM)

The LMH0318 has an on-chip eye opening monitor (EOM) which can be used to analyze, monitor, and diagnose the performance of the link. The EOM operates on the post-equalized waveform, just prior to the data sampler. Therefore, it captures the effects of all the equalization circuits within the receiver before the data is reclocked. The EOM is operational for 1.485 Gbps and higher data rates.

The EOM monitors the post-equalized waveform in a time window that spans one unit interval and a configurable voltage range that spans up to ±400 mV differential. The time window and voltage range are divided into 64 steps, so the result of the eye capture is a 64 × 64 matrix of “hits,” where each point represents a specific voltage and phase offset relative to the main data sampler. The number of “hits” registered at each point needs to be taken in context with the total number of bits observed at that voltage and phase offset in order to determine the corresponding probability for that point. The number of bits observed at each point is configurable.

A common measurement performed by the EOM is the horizontal and vertical eye opening. The horizontal eye opening (HEO) represents the width of the post-equalized eye at 0 V differential amplitude, measured in unit intervals or picoseconds. The vertical eye opening (VEO) represents the height of the post-equalized eye, measured midway between the mean zero crossing of the eye. This position in time approximates the CDR sampling phase.

The resulting 64 × 64 matrix produced by the EOM can be processed by software and visualized in a number of ways. Two common ways to visualize this data are shown in Figure 20 and Figure 21. These diagrams depict examples of an eye monitor plot implemented by software. The first plot is an example of using the EOM data to plot a basic eye using ASCII characters, which can be useful for simple diagnostics software. The second plot shows the first derivative of the EOM data, revealing the density of hits and the actual waveforms and crossing that comprise the eye.

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8.3.6 Fast EOM

Fast EOM is a mechanism that provides an option to read out EOM through SPI/SMBus interfaces by reading the hits observed for each point of 64 × 64 points matrix. Since SPI interface operates at faster clock rate than SMBus interface, the SPI master will have to wait until the EOM start bit, reg 0x24[0], goes low. This indicates EOM samples are available and the SPI master can proceed to read register 0x25 and 0x26. See SPI Fast EOM Operation *and LMH0318 Programming Guide* (SNLU183) for further details of Fast EOM operation.

8.3.6.1 SMBus Fast EOM Operation

In SMBus mode, the read on register 0x26 acts as an automatic trigger to read the next EOM count value:

1. Enable EOM (power it on), and set VRANGE=0. Write reg 0x24[7] to 1 to turn on fast EOM
2. Read register 0x25 as burst of 2 bytes (EOM hit count) and discard
3. Read register 0x25 as burst of 2 bytes (EOM hit count) and discard
4. Read register 0x25 as burst of 2 bytes (EOM hit count) and save
5. Perform Step 4 4095 times (64 × 64 cells)

8.3.6.2 SPI Fast EOM Operation

To perform EOM calculation over SPI:

1. Enable EOM (power it on), and set VRANGE=0. Write reg 0x24[7] to 1 to turn on fast EOM
2. Read reg 0x26 to initialize. Discard read data
3. Read Reg 0x24[0] which is EOM start bit. Wait for this bit to go low
4. Read register 0x26 EOM hit count and discard. Read on register 0x26 will automatically trigger the next Fast Eye calculation
5. Read Reg 0x24[0]. Wait for this bit to go low
6. Do burst read on register 0x25 and 0x26 to get the EOM hit count value.
7. Repeat Steps 5 and 6 4095 times (64 × 64 cells)

8.3.7 LMH0318 Device Configuration

The control pins can be used to configure different operations depending on the functional modes as described in Table 2.

Table 2. Control Pins

		FUNCTIONAL MODES	
PIN #	**PIN NAME**	**SPI**	**SMBus_Slave**
1	MODE_SEL	1 kΩ to VDD	1 kΩ to GND
2	IN_OUT_SEL_SPI_SS_N_ADDR0	SPI_SS_N	ADDR0
3	EQ_SCL_SCK	SPI_SCK	SMBUS_SCL
4	OUT_CTRL_MOSI_SDA	SPI_MOSI	SMBUS SDA
6	ENABLE	ENABLE	ENABLE
13	LOS_INT_N	LOS_INT_N	LOS_INT_N
15	VOD_MISO_ADDR1	SPI_MISO	ADDR1
16	LOCK	LOCK	LOCK

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8.3.7.1 MODE_SEL

This pin can be configured in 4 possible ways:

1. 1 kΩ to VDD: This puts the part in SPI mode
2. Float (Default): Reserved
3. 20 kΩ to GND: Reserved
4. 1 kΩ to GND: This puts the part in SMBus mode

8.3.7.2 ENABLE

Normal operation when ENABLE is pulled high, and powers down the device when pulled low.

Table 3. ENABLE Selection

ENABLE	POWER CONDITION
1 kΩ to GND	Power down device (signal detectors powered down, registers at reset state)
20 kΩ to GND	Reserved
Float	Reserved
1 kΩ to VDD	Normal Operation

8.3.7.3 LOS_INT_N

LOS_INT_N pin is an open drain output. When the channel that has been selected cannot detect a signal at the high-speed input pins (as defined by the assert levels), the pin pulls low. Pin 13 can be configured through share register 0xFF[5] for interrupt functionality.

In SMBus/SPI mode, this pin can be configured as an interrupt. This pin is asserted low when there is an interrupt and goes back high when the interrupt status register is read. There are 7 separate masks for different interrupt sources. These interrupt sources are:

1. If there is a LOS transition on IN0, irrespective of the input channel selected (2 separate masks).
2. If there is a LOS transition on IN1, irrespective of the input channel selected (2 separate masks).
3. HEO or VEO goes below a certain threshold as specified in the registers (1 mask).
4. Lock transition, whether it is asserted or de-asserted – disabled by default (2 mask).

8.3.7.4 LOCK

Indicates the lock status of the CDR. When CDR is locked this pin is asserted high.

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8.3.7.5 SMBus MODE

The SMBus interface can also be used to control the device. If pin 1 (MODE_SEL) is pulled low through 1 kΩ to GND, then Pins 3, 4 are configured as the SMBUS_SCL and SMBUS_SDA respectively. Pins 2, 15 are address straps, **ADDR0/ADDR1** respectively, during power up.

The maximum operating speed supported on the SMBus pins is 400 kHz.

Table 4. SMBus MODE

ADDR0	ADDR1	ADDR0 [BINARY]	ADDR1 [BINARY]	7-Bit SLAVE ADDRESS [HEX]	8-Bit WRITE COMMAND [HEX]
1 kΩ to GND	1 kΩ to GND	00	00	0D	1A
1 kΩ to GND	20 kΩ to GND	00	01	0E	1C
1 kΩ to GND	Float	00	10	0F	1E
1 kΩ to GND	1 kΩ to VDD	00	11	10	20
20 kΩ to GND	1 kΩ to GND	01	00	11	22
20 kΩ to GND	20 kΩ to GND	01	01	12	24
20 kΩ to GND	Float	01	10	13	26
20 kΩ to GND	1 kΩ to VDD	01	11	14	28
Float	1 kΩ to GND	10	00	15	2A
Float	20 kΩ to GND	10	01	16	2C
Float	Float	10	10	17	2E
Float	1 kΩ to VDD	10	11	18	30
1 kΩ to VDD	1 kΩ to GND	11	00	19	32
1 kΩ to VDD	20 kΩ to GND	11	01	1A	34
1 kΩ to VDD	Float	11	10	1B	36
1 kΩ to VDD	1 kΩ to VDD	11	11	1C	38

Note: These are 7 bit addresses. Therefore, the LSB must be added to indicate read/write. LSB equal to zero indicates write and 1 indicates SMBus read operation. For example, for 7 bit hex address 0x0D, the I2C hex address byte is 0x1A to write and 0X1B to read.

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8.3.7.6 SMBus READ/WRITE Transaction

The System Management Bus (SMBus) is a two-wire serial interface through which various system component chips can communicate with the master. Slave devices are identified by having a unique device address. The two-wire serial interface consists of SCL and SDA signals. SCL is a clock output from the Master to all of the Slave devices on the bus. SDA is a bidirectional data signal between the Master and Slave devices. The LMH0318 SMBUS SCL and SDA signals are open drain and require external pull up resistors.

Start and Stop:

The Master generates Start and Stop conditions at the beginning and end of each transaction.

- Start: High to low transition (falling edge) of SDA while SCL is high
- Stop: Low to high transition (rising edge) of SDA while SCL is high

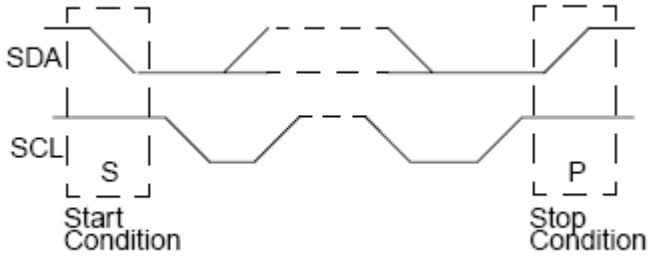


Figure 3. Start and Stop Conditions

The Master generates 9 clock pulses for each byte transfer. The 9th clock pulse constitutes the ACK cycle. The transmitter releases SDA to allow the receiver to send the ACK signal. An ACK is when the device pulls SDA low, while a NACK is recorded if the line remains high.

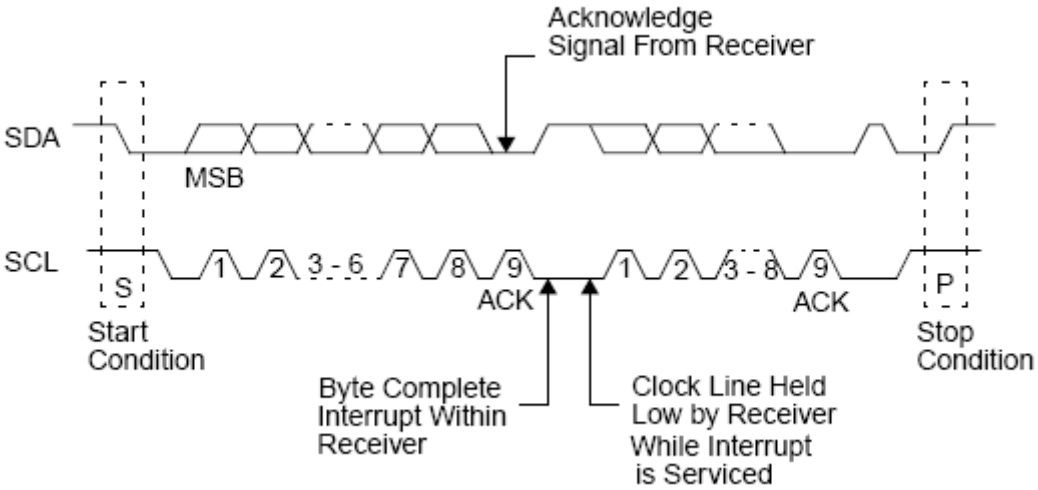


Figure 4. Acknowledge (ACK)

Writing data from a master to a slave comprises of 3 parts as noted in figure Figure 5

- The master begins with start condition followed by the slave device address with the R/W bit cleared
- The 8-bit register address that will be written
- The data byte to write

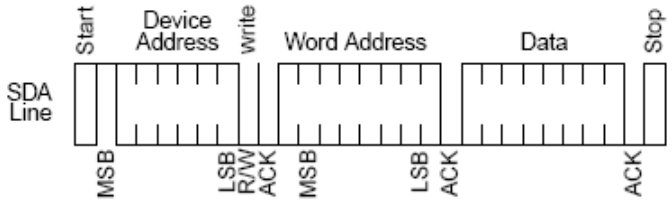


Figure 5. SMBus Write Operation

SMBus read operation consists of four parts

- The master initiates the read cycle with start condition followed by slave device address with the R/W bit cleared
- The 8-bit register address that is to be read
- After acknowledgment from the slave, the master initiates a re-start condition
- The slave device address is resent followed with R/W bit set
- After acknowledgment from the slave, the data is read back from the slave to the master. The last ACK is high if there are no more bytes to read

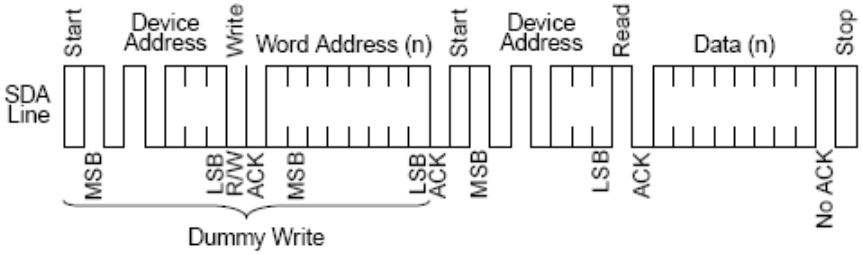


Figure 6. SMBus Read Operation

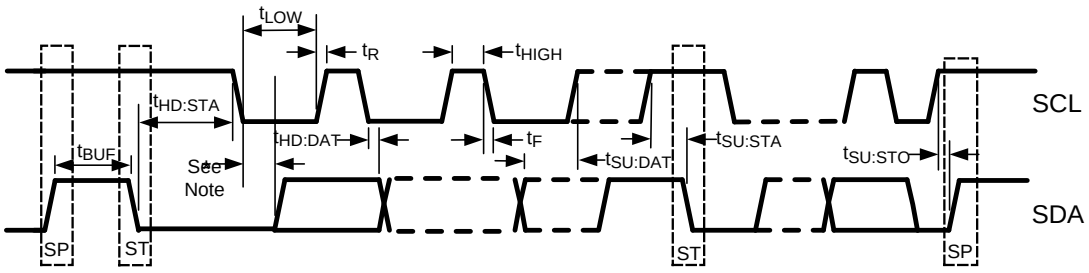


Figure 7. SMBus Timing Parameters

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8.3.7.7 SPI Mode

The SPI (Serial Peripheral Interface) bus standard can be used to control the device. The SPI Mode is enabled when MODE_SEL Pin 1 is pulled high through the 1-kΩ resistor. The SPI bus comprises of 4 pins: Pin 2, Pin 3, Pin 4, and Pin 15:

1. MOSI Pin 4: Master Output Slave Input. Configured as toggling input.
2. MISO Pin 15: Master Input, Slave Output: Configured as a toggling output
3. SS_N Pin 2: Slave Select (active low). Configured as toggling input.
4. SCK Pin 3: Serial clock (output from master). Configured as toggling input.

The maximum operating speed supported on the SPI bus is 20 MHz.

8.3.7.7.1 SPI READ/WRITE Transaction

Each SPI transaction to a single device is 17 bits long and is framed by SS_N asserted low. The MOSI input is ignored and the MISO output is floated whenever SS_N is de-asserted (High).

The bits are shifted in left-to-right. The first bit is R/W, so it is 1 for reads and 0 for writes. Bits A7-A0 are the 8-bit register address, and bits D7-D0 are the 8-bit read or write data. The prior SPI command, address, and data are shifted out on MISO as the current command, address, and data are shifted in on MOSI. In all SPI transactions, the MISO output signal is enabled asynchronously when SS_N becomes asserted.

R/W	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Figure 8. MOSI Format

8.3.7.7.2 SPI Write Transaction Format

For SPI writes, the R/W bit is 0. SPI write transactions are 17 bits per device, and the command is executed on the rising edge of SS_N, as shown in Figure 9. The SPI transaction always starts on the rising edge of the clock.

Figure 9. MOSI Write Sequence

0	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

The signal timing for a SPI Write transaction is shown in Figure 10. The “prime” values on MISO (for example, A7") reflect the contents of the shift register from the previous SPI transaction, and are a "don’t-care" for the current transaction.

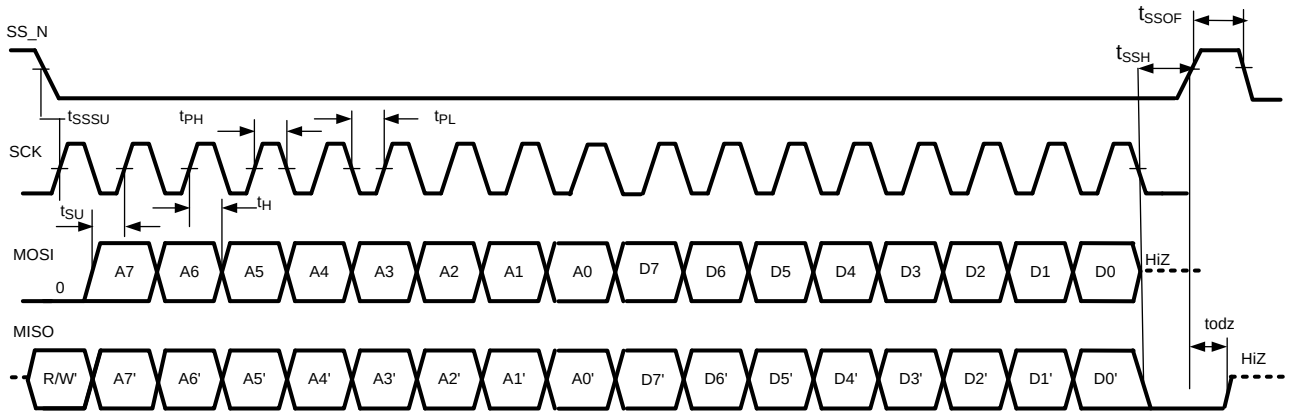


Figure 10. Signal Timing for a SPI Write Transaction

8.3.7.7.3 SPI Read Transaction Format

An SPI read transaction is 34 bits per device consisting of two 17-bit frames. The first 17-bit read transaction, first frame, shifts in the address to be read, followed by a dummy transaction, second frame, to shift out the 17-bit read data. The R/W bit is 1 for the read transaction, as shown in Figure 11.

The first 17 bits from the read transaction specifies 1-bit of RW and 8-bits of address A7-A0. The eight 1's following the address are ignored. The second dummy transaction acts like a read operation on address 0xFF and needs to be ignored. However, the transaction is necessary in order to shift out the read data D7-D0 in the last 8 bits of the MISO output.

The signal timing for a SPI read transaction is shown in Figure 11. As with the SPI write, the "prime" values on MISO during the first 16 clocks are a don't-care for this portion of the transaction. Note, that the values shifted out on MISO during the last 17 clocks reflect the read address and 8-bit read data for the current transaction.

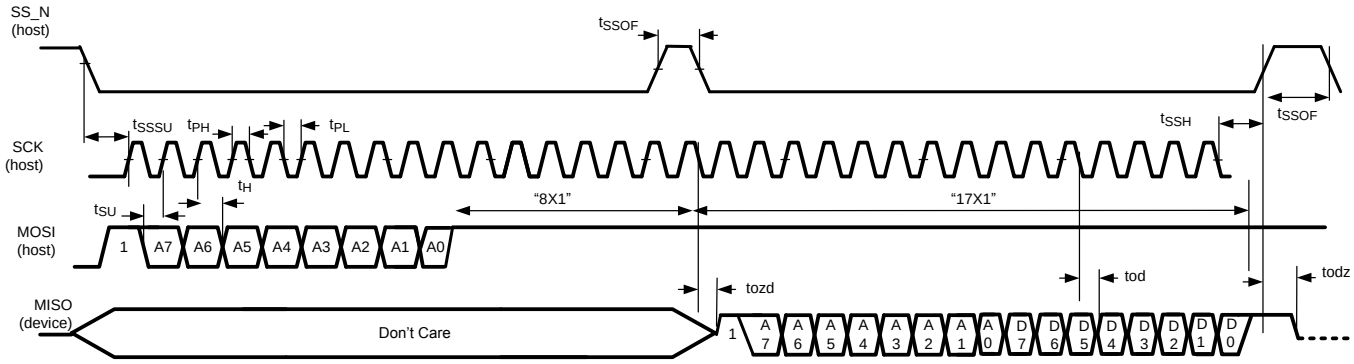


Figure 11. Signal Timing for a SPI Read Transaction

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8.3.7.8 SPI Daisy Chain

The LMH0318 includes an enhanced SPI controller that supports daisy-chaining the serial configuration data among multiple LMH0318 devices. The LMH0318 device supports SPI Daisy Chain between devices with an 8-bit SPI addressing scheme. Each LMH0318 device is directly connected to the SCK and SS_N pins of the Host. However, only the first LMH0318 device in the chain is connected to the Host's MOSI pin, and only the last device in the chain is connected to the Host's MISO pin. The MOSI pin of each intermediate LMH0318 device in the chain is connected to the MISO pin of the previous LMH0318 device, thereby creating a serial shift register. This architecture is shown in Figure 12.

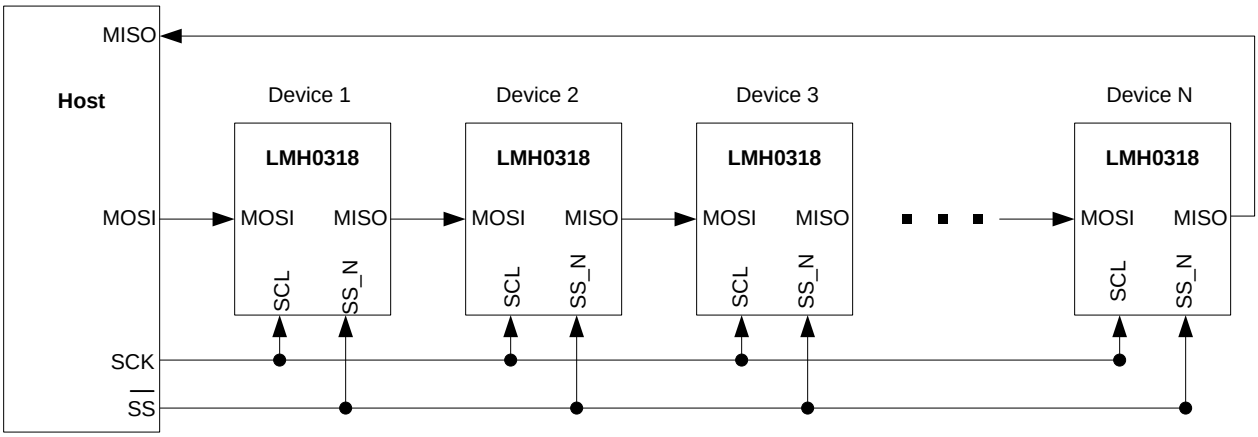


Figure 12. Daisy-Chain Configuration

In a daisy-chain configuration of N LMH0318 devices, the Host conceptually sees a long shift register of length 17xN. Therefore the length of a Basic SPI Transaction, as described above, is 17xN; in other words, SS_N is asserted for 17xN clock cycles.

8.3.7.8.1 SPI Daisy Chain Write Example

The following example make some assumptions:

The daisy-chain is 3 LMH0318 devices long, comprising Devices 1, 2, and 3 as shown in Figure 12. Therefore, each Basic SPI Transaction is 17x3 = 51 clocks long.

In Figure 13, the following occurs at the end of the transaction:

- Write 0x5A to register 0x12 in Device 3
- Write 0x3C to register 0x34 in Device 2
- Write 0x00 to register 0x56 in Device 1

Note that the bits are shifted out of MOSI left to right. The MISO pin is not shown as it reflects shift register contents from a prior transaction.

MOSI (Write)	0	0x12	0x5A	0	0x34	0x3C	0	0x56	0x00

Figure 13. MOSI Write Example

8.3.7.8.2 SPI Daisy Chain Write Read Example

In Figure 14 and Figure 15, the following occurs at the end of the first transaction:

- Write 0x22 to register 0x01 in Device 3
- Latch the data from register 0x34 in Device 2
- Write 0x44 to register 0x76 in Device 1

MOSI (Host)	0	0x01	0x22	1	0x34	0xFF	0	0x76	0x44

Figure 14. SPI Daisy Chain Write Read First Frame Illustration

MOSI (Host)	1	0xFF	0xFF	1	0xFF	0xFF	1	0xFF	0xFF
MISO (Host)	0	0x01	0x22	1	0x34	0x3C	0	0x76	0x44

Figure 15. SPI Daisy Chain Write Read second Frame Illustration

8.3.7.8.2.1 SPI Daisy Chain Length of Daisy Chain Illustration

A useful operation for the Host may be to detect the length of the daisy-chain. This is a simple matter of shifting in a series of known data values (0x7F, 0xAA) in the example in Figure 16. After N+1 writes, the known data value will begin to appear on the Host's MISO pin.

MOSI (Host)	1	0x7F	0xAA	1	0x7F	0xAA	1	0x7F	0xAA
MISO (Host)	x	xx	xx	x	xx	xx	1	0x7F	0xAA

Figure 16. MOSI (Host)

8.3.8 Power-On Reset

The LMH0318 has an internal power-on reset (PoR) circuitry which initiates a self-clearing reset after the power is applied to the VDD pins.

8.4 Device Functional Modes

The LMH0318 features can be programmed via SPI, or SMBus interface. *LMH0318 Device Configuration* describes detailed operation using SPI, or SMBus interface.

8.5 Programming

For more information on device programming, See *LMH0318 Programming Guide* (SNLU183). Register initialization is required at power-up or after reset. See *Initialization Set Up*

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Programming (continued)

8.5.1 Register Maps

The LMH0318 register set definition is organized into four groups:

1. Global Registers: Chip ID, Interrupt status, LOS registers
2. Receiver Registers: Equalizer boost settings and signal detect setting
3. CDR Registers: PLL control
4. Transmitter Registers: OUT0 and OUT1 parameter setting

The typical device initialization sequence for the LMH0318 includes the followings. For detailed register settings See *LMH0318 Programming Guide* (SNLU183).

1. Shared Register Configuration
   (a) Reading device ID
   (b) Selecting interrupt on to LOS pin
   (c) Settings up the register to access the channel registers
2. Channel Register Configuration
   (a) CDR Reset
   (b) Interrupt register configuration
   (c) Optional Input/Output selection
   (d) Optional VOD selection
   (e) CDR Reset and Release

8.5.2 Global Registers

Table 5. Global Registers

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
SMBus Observation		Reg_0x00 Share	0x00		SMBus Address Observation
	7	SMBUS_addr3	0	R	SMBus strap observation
	6	SMBUS_addr2	0	R	
	5	SMBUS_addr1	0	R	
	4	SMBUS_addr0	0	R	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
Reset Shared Regs		Reg 0x04 Share	0x01		Shared Register Reset
	7	Reserved	0	RW	
	6	rst_i2c_regs	0	RW	1: Reset Shared Registers 0: Normal operation
	5	Reserved	0	RW	
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	1	RW	
Enable SMBus Strap		Reg 0x06 Share	0x00		Allow SMBus strap observation
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	

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Programming (continued)

Table 5. Global Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
	3	Test control[3]	0	RW	Set to >9 to allow strap observation on share reg 0x00
	2	Test control[2]	0	RW	
	1	Test control[1]	0	RW	
	0	Test control[0]	0	RW	
Device Version		Reg 0xF0 Share	0x01		Device Version
	7	VERSION[7]	0	RW	Device revision
	6	VERSION[6]	0	RW	
	5	VERSION[5]	0	RW	
	4	VERSION[4]	0	RW	
	3	VERSION[3]	0	RW	
	2	VERSION[2]	0	RW	
	1	VERSION[1]	0	RW	
	0	VERSION[0]	1	RW	
Channel Control		Reg 0xFF Control	0x00		Enable Channel Control
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	los_int_bus_sel	0	RW	1: Selects interrupt onto LOS pin 0: Selects signal detect onto LOS pin
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	en_ch_Access	0	RW	1: Enables access to channel registers 0: Enables access to share registers
	1	Reserved	0	RW	
	0	Reserved	0	RW	
Reset_Channel_Regs		Reg_0x00 Channel	0x00		Reset all Channel Registers to Default Values
	7	Reserved	0		
	6	Reserved	0		
	5	Reserved	0		
	4	Reserved	0		
	3	Reserved	0		
	2	Rst_regs	0		1: Reset Channel Registers (self clearing) 0: Normal operation
	1	Reserved	0		
	0	Reserved	0		
LOS_status		Reg_0x01 Channel	0x00		Signal Detect Status
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	LOS1	0	R	1: Loss of signal on IN1 0: Signal present on IN1
	0	LOS0	0	R	1: Loss of signal on IN0 0: Signal present on IN0

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Programming (continued)

Table 5. Global Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
CDR_Status_1		Reg_0x02 Channel	0x00		CDR Status
	7	Reserved	0	R	
	6	Reserved	0	R	
	5	Reserved	0	R	
	4	cdr_status[4]	0	R	11: CDR locked 00: CDR not locked
	3	cdr_status[3]	0	R	
	2	Reserved	0	R	
	1	Reserved	0	R	
	0	Reserved	0	R	
Interrupt Status Register		Reg 0x54 Channel	0x00		Interrupt Status (clears upon read)
	7	Sigdet	0	R	1: Signal Detect from the selected input asserted 0: Signal Detect from the selected input de-asserted
	6	cdr_lock_int	0	R	1: CDR Lock interrupt 0: No interrupt from CDR Lock
	5	signal_det1_int	0	R	1: IN1 Signal Detect interrupt 0: No interrupt from IN1 Signal Detect
	4	signal_det0_int	0	R	1: IN0 Signal Detect interrupt 0: No interrupt from IN0 Signal Detect
	3	heo_veo_int	0	R	1: HEO_VEO Threshold reached interrupt 0: No interrupt from HEO_VEO
	2	cdr_lock_loss_int	0	R	1: CDR loss of lock interrupt 0: No interrupt from CDR lock
	1	signal_det1_loss_int	0	R	1: IN1 Signal Detect loss interrupt 0: No interrupt from IN1 Signal Detect
	0	signal_det0_loss_int	0	R	1: IN0 Signal Detect loss interrupt 0: No interrupt from IN0 Signal Detect

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Programming (continued)

Table 5. Global Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
Interrupt Control		Reg 0x56 Channel	0x00		Interrupt Mask
	7	Reserved	0	RW	
	6	cdr_lock_int_en	0	RW	1: Enable Interrupt if CDR lock is achieved 0: Disable interrupt if CDR lock is achieved
	5	signal_det1_int_en	0	RW	1: Enable interrupt if IN1 Signal Detect is asserted 0: Disable interrupt if IN1 Signal Detect is asserted
	4	signal_det0_int_en	0	RW	1: Enable interrupt if IN0 Signal Detect is asserted 0: Disable interrupt if IN0 Signal Detect is asserted
	3	heo_veo_int_en	0	RW	1: Enable interrupt if HEO-VEO threshold is reached 0: Disable interrupt due to HEO-VEO threshold
	2	cdr_lock_loss_int_en	0	RW	1: Enable interrupt if CDR loses lock 0: Disable interrupt if CDR loses lock
	1	signal_det1_loss_int_en	0	RW	1: Enable interrupt if there is loss of signal on IN1 0: Disable interrupt if there is loss of signal on IN1
	0	signal_det0_loss_int_en	0	RW	1: Enable interrupt if there is loss of signal on IN0 0: Disable interrupt if there is loss of signal on IN0

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8.5.3 Receiver Registers

Table 6. Receiver Registers

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
EQ_Boost		Reg 0x03 Channel	0x80		4 Stage EQ Boost Levels. Read-back value going to CTLE in reg_0x52. Used for setting EQ value when reg_0x2D[3] is high
	7	eq_BST0[1]	1	RW	2 Bits control for stage 0 of the CTLE. Adapts during CTLE adaptation
	6	eq_BST0[0]	0	RW	
	5	eq_BST1[1]	0	RW	2 Bits control for stage 1 of the CTLE. Adapts during CTLE adaptation
	4	eq_BST1[0]	0	RW	
	3	eq_BST2[1]	0	RW	2 Bits control for stage 2 of the CTLE. Adapts during CTLE adaptation
	2	eq_BST2[0]	0	RW	
	1	eq_BST3[1]	0	RW	2 Bits control for stage 3 of the CTLE. Adapts during CTLE adaptation
	0	eq_BST3[0]	0	RW	
SD_EQ		Reg_0x0D Channel	0x00		270 Mbps EQ Boost Setting
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Mr_auto_eq_en_bypass	0	RW	1: EQ Bypass for 270 Mbps 0: Use EQ Settings in reg0x03[7:0] for 270 Mbps Note: If 0x13[1] mr_eq_en_bypass is set, bypass would be set and auto-bypass has no significance.
EQ_SD_CONFIG		Reg 0x13 Channel	0x90		Channel EQ Bypass and Power Down
	7	Reserved	1	RW	
	6	sd_0_PD	0	RW	1: Power Down IN0 Signal Detect 0: IN0 Signal Detect normal operation
	5	sd_1_PD	0	RW	1: Power Down IN1 Signal Detect 0: IN1 Signal Detect normal operation
	4	Reserved	1	RW	
	3	eq_PD_EQ	0	RW	Controls the power-state of the selected channel. The un-selected channel is always powered-down 1: Powers down selected channel EQ stage 0: Powers up EQ of the selected channel
	2	Reserved	0	RW	
	1	eq_en_bypass	0	RW	1: Bypass stage 3 and 4 of CTLE 0: Enable Stage 3 and 4 of CTLE
	0	Reserved	0	RW	

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Table 6. Receiver Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
SD0_CONFIG		Reg 0x14 Channel	0x00		IN0 Signal Detect Threshold Setting
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	sd_0_refa_sel[1]	0	RW	Controls signal detect S_{DH}- Assert [5:4], S_{DL}- De-Assert [3:2], thresholds for IN0 0000: Default levels (nominal) 0101: Nominal -2 mV 1010: Nominal +5 mV 1111: Nominal +3 mV
	4	sd_0_refa_sel[0]	0	RW	
	3	sd_0_refd_sel[1]	0	RW	
	2	sd_0_refd_sel[0]	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
SD1_CONFIG		Reg_0x15 Channel	0x00		IN1 Signal Detect Threshold Setting
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	sd_1_refa_sel[1]	0	RW	Controls signal detect S_{DH}- Assert [5:4], S_{DL}- De-Assert [3:2], thresholds for IN1 0000: Default levels (nominal) 0101: Nominal -2 mV 1010: Nominal +5 mV 1111: Nominal +3 mV
	4	sd_1_refa_sel[0]	0	RW	
	3	sd_1_refd_sel[1]	0	RW	
	2	sd_1_refd_sel[0]	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
EQ_BOOST_OV		Reg_0x2D Channel	0x88		EQ Boost Override
	7	Reserved	1	RW	
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	
	3	reg_eq_bst_ov	1	RW	1: Enable EQ boost over ride See *LMH0318 Programming Guide* (SNLU183) 0: Disable EQ boost over ride
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
CTLE Setting		Reg_0x31 Channel	0x00		CTLE Mode of Operation and Input/Output Mux Selection
	7	Reserved	0	RW	
	6	adapt_mode[1]	00	RW	00: Normal Operation - Manual CTLE Setting 01: Test Mode - See the *LMH0318 Programming Guide* (SNLU183) for details Other Settings - Invalid
	5	adapt_mode[0]			
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	input_mux_ch_sel[1]	0	RW	IN0/1 and OUT0/1 selection 00: selects IN0 and OUT0/1 01: selects IN0 and OUT0 10: selects IN1 and OUT1 11: selects IN1 and OUT0/1
	0	input_mux_ch_sel[0]	0	RW	

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Table 6. Receiver Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
LOW_RATE_ EQ_BST		Reg 0x3A Channel	0x00		HD and SD EQ Level
	7	fixed_eq_BST0[1]	0	RW	When CTLE is operating in test mode, Reg 0x3A[7:0] forces fixed EQ setting. In normal operating manual mode Reg_0x03 forces EQ boost. See *LMH0318 Programming Guide* (SNLU183) for details
	6	fixed_eq_BST0[0]	0	RW	
	5	fixed_eq_BST1[1]	0	RW	
	4	fixed_eq_BST1[0]	0	RW	
	3	fixed_eq_BST2[1]	0	RW	
	2	fixed_eq_BST2[0]	0	RW	
	1	fixed_eq_BST3[1]	0	RW	
	0	fixed_eq_BST3[0]	0	RW	
BST_Indx0		Reg_0x40 Channel	0x00		Index0 4 Stage EQ Boost. See *LMH0318 Programming Guide* (SNLU183)
	7	I0_BST0[1]	0	RW	Index 0 Boost Stage 0 bit 1
	6	I0_BST0[0]	0	RW	Index 0 Boost Stage 0 bit 0
	5	I0_BST1[1]	0	RW	Index 0 Boost Stage 1 bit 1
	4	I0_BST1[0]	0	RW	Index 0 Boost Stage 1 bit 0
	3	I0_BST2[1]	0	RW	Index 0 Boost Stage 2 bit 1
	2	I0_BST2[0]	0	RW	Index 0 Boost Stage 2 bit 0
	1	I0_BST3[1]	0	RW	Index 0 Boost Stage 3 bit 1
	0	I0_BST3[0]	0	RW	Index 0 Boost Stage 3 bit 0
BST_Indx1		Reg 0x41 Channel	0x40		Index1 4 Stage EQ Boost.
	7	I1_BST0[1]	0	RW	Index 1 Boost Stage 0 bit 1
	6	I1_BST0[0]	1	RW	Index 1 Boost Stage 0 bit 0
	5	I1_BST1[1]	0	RW	Index 1 Boost Stage 1 bit 1
	4	I1_BST1[0]	0	RW	Index 1 Boost Stage 1 bit 0
	3	I1_BST2[1]	0	RW	Index 1 Boost Stage 2 bit 1
	2	I1_BST2[0]	0	RW	Index 1 Boost Stage 2 bit 0
	1	I1_BST3[1]	0	RW	Index 1 Boost Stage 3 bit 1
	0	I1_BST3[0]	0	RW	Index 1 Boost Stage 3 bit 0
BST_Indx2		Reg 0x42 Channel	0x80		Index2 4 Stage EQ Boost.
	7	I2_BST0[1]	1	RW	Index 2 Boost Stage 0 bit 1
	6	I2_BST0[0]	0	RW	Index 2 Boost Stage 0 bit 0
	5	I2_BST1[1]	0	RW	Index 2 Boost Stage 1 bit 1
	4	I2_BST1[0]	0	RW	Index 2 Boost Stage 1 bit 0
	3	I2_BST2[1]	0	RW	Index 2 Boost Stage 2 bit 1
	2	I2_BST2[0]	0	RW	Index 2 Boost Stage 2 bit 0
	1	I2_BST3[1]	0	RW	Index 2 Boost Stage 3 bit 1
	0	I2_BST3[0]	0	RW	Index 2 Boost Stage 3 bit 0

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Table 6. Receiver Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
BST_Indx3		Reg 0x43 Channel	0x50		Index3 4 Stage EQ Boost.
	7	I3_BST0[1]	0	RW	Index 3 Boost Stage 0 bit 1
	6	I3_BST0[0]	1	RW	Index 3 Boost Stage 0 bit 0
	5	I3_BST1[1]	0	RW	Index 3 Boost Stage 1 bit 1
	4	I3_BST1[0]	1	RW	Index 3 Boost Stage 1 bit 0
	3	I3_BST2[1]	0	RW	Index 3 Boost Stage 2 bit 1
	2	I3_BST2[0]	0	RW	Index 3 Boost Stage 2 bit 0
	1	I3_BST3[1]	0	RW	Index 3 Boost Stage 3 bit 1
	0	I3_BST3[0]	0	RW	Index 3 Boost Stage 3 bit 0
BST_Indx4		Reg 0x44 Channel	0xC0		Index4 4 Stage EQ Boost.
	7	I4_BST0[1]	1	RW	Index 4 Boost Stage 0 bit 1
	6	I4_BST0[0]	1	RW	Index 4 Boost Stage 0 bit 0
	5	I4_BST1[1]	0	RW	Index 4 Boost Stage 1 bit 1
	4	I4_BST1[0]	0	RW	Index 4 Boost Stage 1 bit 0
	3	I4_BST2[1]	0	RW	Index 4 Boost Stage 2 bit 1
	2	I4_BST2[0]	0	RW	Index 4 Boost Stage 2 bit 0
	1	I4_BST3[1]	0	RW	Index 4 Boost Stage 3 bit 1
	0	I4_BST3[0]	0	RW	Index 4 Boost Stage 3 bit 0
BST_Indx5		Reg 0x45 Channel	0x90		Index5 4 Stage EQ Boost.
	7	I5_BST0[1]	1	RW	Index 5 Boost Stage 0 bit 1
	6	I5_BST0[0]	0	RW	Index 5 Boost Stage 0 bit 0
	5	I5_BST1[1]	0	RW	Index 5 Boost Stage 1 bit 1
	4	I5_BST1[0]	1	RW	Index 5 Boost Stage 1 bit 0
	3	I5_BST2[1]	0	RW	Index 5 Boost Stage 2 bit 1
	2	I5_BST2[0]	0	RW	Index 5 Boost Stage 2 bit 0
	1	I5_BST3[1]	0	RW	Index 5 Boost Stage 3 bit 1
	0	I5_BST3[0]	0	RW	Index 5 Boost Stage 3 bit 0
BST_Indx6		Reg 0x46 Channel	0x54		Index6 4 Stage EQ Boost.
	7	I6_BST0[1]	0	RW	Index 6 Boost Stage 0 bit 1
	6	I6_BST0[0]	1	RW	Index 6 Boost Stage 0 bit 0
	5	I6_BST1[1]	0	RW	Index 6 Boost Stage 1 bit 1
	4	I6_BST1[0]	1	RW	Index 6 Boost Stage 1 bit 0
	3	I6_BST2[1]	0	RW	Index 6 Boost Stage 2 bit 1
	2	I6_BST2[0]	1	RW	Index 6 Boost Stage 2 bit 0
	1	I6_BST3[1]	0	RW	Index 6 Boost Stage 3 bit 1
	0	I6_BST3[0]	0	RW	Index 6 Boost Stage 3 bit 0
BST_Indx7		Reg 0x47 Channel	0xA0		Index7 4 Stage EQ Boost.
	7	I7_BST0[1]	1	RW	Index 7 Boost Stage 0 bit 1
	6	I7_BST0[0]	0	RW	Index 7 Boost Stage 0 bit 0
	5	I7_BST1[1]	1	RW	Index 7 Boost Stage 1 bit 1
	4	I7_BST1[0]	0	RW	Index 7 Boost Stage 1 bit 0
	3	I7_BST2[1]	0	RW	Index 7 Boost Stage 2 bit 1
	2	I7_BST2[0]	0	RW	Index 7 Boost Stage 2 bit 0
	1	I7_BST3[1]	0	RW	Index 7 Boost Stage 3 bit 1
	0	I7_BST3[0]	0	RW	Index 7 Boost Stage 3 bit 0

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Table 6. Receiver Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
BST_Indx8		Reg 0x48 Channel	0xB0		Index8 4 Stage EQ Boost.
	7	I8_BST0[1]	1	RW	Index 8 Boost Stage 0 bit 1
	6	I8_BST0[0]	0	RW	Index 8 Boost Stage 0 bit 0
	5	I8_BST1[1]	1	RW	Index 8 Boost Stage 1 bit 1
	4	I8_BST1[0]	1	RW	Index 8 Boost Stage 1 bit 0
	3	I8_BST2[1]	0	RW	Index 8 Boost Stage 2 bit 1
	2	I8_BST2[0]	0	RW	Index 8 Boost Stage 2 bit 0
	1	I8_BST3[1]	0	RW	Index 8 Boost Stage 3 bit 1
	0	I8_BST3[0]	0	RW	Index 8 Boost Stage 3 bit 0
BST_Indx9		Reg 0x49 Channel	0X95	0x95	Index9 4 Stage EQ Boost.
	7	I9_BST0[1]	1	RW	Index 9 Boost Stage 0 bit 1
	6	I9_BST0[0]	0	RW	Index 9 Boost Stage 0 bit 0
	5	I9_BST1[1]	0	RW	Index 9 Boost Stage 1 bit 1
	4	I9_BST1[0]	1	RW	Index 9 Boost Stage 1 bit 0
	3	I9_BST2[1]	0	RW	Index 9 Boost Stage 2 bit 1
	2	I9_BST2[0]	1	RW	Index 9 Boost Stage 2 bit 0
	1	I9_BST3[1]	0	RW	Index 9 Boost Stage 3 bit 1
	0	I9_BST3[0]	1	RW	Index 9 Boost Stage 3 bit 0
BST_Indx10		Reg 0x4A Channel	0x69		Index10 4 Stage EQ Boost.
	7	I10_BST0[1]	0	RW	Index 10 Boost Stage 0 bit 1
	6	I10_BST0[0]	1	RW	Index 10 Boost Stage 0 bit 0
	5	I10_BST1[1]	1	RW	Index 10 Boost Stage 1 bit 1
	4	I10_BST1[0]	0	RW	Index 10 Boost Stage 1 bit 0
	3	I10_BST2[1]	1	RW	Index 10 Boost Stage 2 bit 1
	2	I10_BST2[0]	0	RW	Index 10 Boost Stage 2 bit 0
	1	I10_BST3[1]	0	RW	Index 10 Boost Stage 3 bit 1
	0	I10_BST3[0]	1	RW	Index 10 Boost Stage 3 bit 0
BST_Indx11		Reg 0x4B Channel	0xD5		Index11 4 Stage EQ Boost.
	7	I11_BST0[1]	1	RW	Index 11 Boost Stage 0 bit 1
	6	I11_BST0[0]	1	RW	Index 11 Boost Stage 0 bit 0
	5	I11_BST1[1]	0	RW	Index 11 Boost Stage 1 bit 1
	4	I11_BST1[0]	1	RW	Index 11 Boost Stage 1 bit 0
	3	I11_BST2[1]	0	RW	Index 11 Boost Stage 2 bit 1
	2	I11_BST2[0]	1	RW	Index 11 Boost Stage 2 bit 0
	1	I11_BST3[1]	0	RW	Index 11 Boost Stage 3 bit 1
	0	I11_BST3[0]	1	RW	Index 11 Boost Stage 3 bit 0
BSTIndx12		Reg 0x4C Channel	0x99		Index12 4 Stage EQ Boost.
	7	I12_BST0[1]	1	RW	Index 12 Boost Stage 0 bit 1
	6	I12_BST0[0]	0	RW	Index 12 Boost Stage 0 bit 0
	5	I12_BST1[1]	0	RW	Index 12 Boost Stage 1 bit 1
	4	I12_BST1[0]	1	RW	Index 12 Boost Stage 1 bit 0
	3	I12_BST2[1]	1	RW	Index 12 Boost Stage 2 bit 1
	2	I12_BST2[0]	0	RW	Index 12 Boost Stage 2 bit 0
	1	I12_BST3[1]	0	RW	Index 12 Boost Stage 3 bit 1
	0	I12_BST3[0]	1	RW	Index 12 Boost Stage 3 bit 0

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Table 6. Receiver Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
BST_Indx13		Reg 0x4D Channel	0xA5		Index13 4 Stage EQ Boost.
	7	I13_BST0[1]	1	RW	Index 13 Boost Stage 0 bit 1
	6	I13_BST0[0]	0	RW	Index 13 Boost Stage 0 bit 0
	5	I13_BST1[1]	1	RW	Index 13 Boost Stage 1 bit 1
	4	I13_BST1[0]	0	RW	Index 13 Boost Stage 1 bit 0
	3	I13_BST2[1]	0	RW	Index 13 Boost Stage 2 bit 1
	2	I13_BST2[0]	1	RW	Index 13 Boost Stage 2 bit 0
	1	I13_BST3[1]	0	RW	Index 13 Boost Stage 3 bit 1
	0	I13_BST3[0]	1	RW	Index 13 Boost Stage 3 bit 0
BST_Indx14		Reg 0x4E Channel	0xE6		Index14 4 Stage EQ Boost.
	7	I14_BST0[1]	1	RW	Index 14 Boost Stage 0 bit 1
	6	I14_BST0[0]	1	RW	Index 14 Boost Stage 0 bit 0
	5	I14_BST1[1]	1	RW	Index 14 Boost Stage 1 bit 1
	4	I14_BST1[0]	0	RW	Index 14 Boost Stage 1 bit 0
	3	I14_BST2[1]	0	RW	Index 14 Boost Stage 2 bit 1
	2	I14_BST2[0]	1	RW	Index 14 Boost Stage 2 bit 0
	1	I14_BST3[1]	1	RW	Index 14 Boost Stage 3 bit 1
	0	I14_BST3[0]	0	RW	Index 14 Boost Stage 3 bit 0
BST_Indx15		Reg 0x4F Channel	0xF9		Index15 4 Stage EQ Boost.
	7	I15_BST0[1]	1	RW	Index 15 Boost Stage 0 bit 1
	6	I15_BST0[0]	1	RW	Index 15 Boost Stage 0 bit 0
	5	I15_BST1[1]	1	RW	Index 15 Boost Stage 1 bit 1
	4	I15_BST1[0]	1	RW	Index 15 Boost Stage 1 bit 0
	3	I15_BST2[1]	1	RW	Index 15 Boost Stage 2 bit 1
	2	I15_BST2[0]	0	RW	Index 15 Boost Stage 2 bit 0
	1	I15_BST3[1]	0	RW	Index 15 Boost Stage 3 bit 1
	0	I15_BST3[0]	1	RW	Index 15 Boost Stage 3 bit 0
Active_EQ		Reg 0x52 Channel	0x00		Active CTLE Boost Setting Read Back
	7	eq_bst_to_ana[7]	0	R	Read-back returns CTLE boost settings
	6	eq_bst_to_ana[6]	0	R	
	5	eq_bst_to_ana[5]	0	R	
	4	eq_bst_to_ana[4]	0	R	
	3	eq_bst_to_ana[3]	0	R	
	2	eq_bst_to_ana[2]	0	R	
	1	eq_bst_to_ana[1]	0	R	
	0	eq_bst_to_ana[0]	0	R	
EQ_Control		Reg 0x55 Channel	0x00		EQ Adaptation Control
	7	Reserved	0	R	
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	INIT_CDR_SM_4	0	RW	At power-up, this bit needs to be set to 1'b. See initialization set up
	0	Reserved	0	RW	

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8.5.4 CDR Registers

Table 7. CDR Registers

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
Output_Mux_OV		Reg 0x09 Channel	0x00		Output Data Mux Override
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	Reg_bypass_pfd_ovd	0	RW	1: Enable values from 0x1E[7:5] & 0x1C[7:5] to control output mux 0: Register 0x1C[3:2] determines the output selection
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
CDR_Reset		Reg 0x0A Channel	0x50		CDR State Machine Reset
	7	Reserved	0	RW	
	6	Reserved	1	RW	
	5	Reserved	0	RW	
	4	Reserved	1	RW	
	3	reg_cdr_reset_ov	0	RW	1: Enable 0x0A[2] to control CDR Reset 0: Disable CDR Reset
	2	reg_cdr_reset_sm	0	RW	1: Enable CDR Reset if 0x0A[3] = 1'b 0: Disable CDR Reset if 0x0A[3] = 1'b
	1	Reserved	0	RW	
	0	Reserved	0	RW	
CDR_Status		Reg 0x0C Channel	0x08		CDR Status Control
	7	reg_sh_status_control[3]	0	RW	Determines what is shown in Reg 0x02. See *LMH0318 Programming Guide* (SNLU183)
	6	reg_sh_status_control[2]	0	RW	
	5	reg_sh_status_control[1]	0	RW	
	4	reg_sh_status_control[0]	0	RW	
	3	Reserved	1	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
EOM_Vrange		Reg 0x11 Channel	0xE0		EOM Vrange Setting and EOM Power Down Control
	7	eom_sel_vrange[1]	11	RW	Sets eye monitor ADC granularity if 0x2C[6] =0'b 00: 3.125 mV 01: 6.25 mV 10: 9.375 mV 11: 12.5 mV
	6	eom_sel_vrange[0]			
	5	eom_PD	1	RW	0: EOM Operational 1: Power down EOM
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	

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Table 7. CDR Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
Full Temperature Range		Reg 0x16 Channel	0x7A		Temperature Range Setting
	7	INIT_CDR_SM_27	0	RW	At power-up, this register needs to be set to 0x25. See initialization set up
	6	INIT_CDR_SM_26	1	RW	
	5	INIT_CDR_SM_25	1	RW	
	4	INIT_CDR_SM_24	1	RW	
	3	INIT_CDR_SM_23	1	RW	
	2	INIT_CDR_SM_22	0	RW	
	1	INIT_CDR_SM_21	1	RW	
	0	INIT_CDR_SM_20	0	RW	
HEO_VEO_OV		Reg 0x23 Channel	0x40		
	7	eom_get_heo_veo_ov	0	RW	1: Enable reg 0x24[1] to acquire HEO/VEO 0: Disable reg 0x24[1] to acquire HEO/VEO
	6	Reserved	1	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
EOM_CNTL		Reg 0x24 Channel	0x00	0x00	Eye Opening Monitor Control Register
	7	fast_eom	0	R	1: Enable Fast EOM mode 0: Disable fast EOM mode
	6	Reserved	0	R	
	5	get_heo_veo_error_no_hits	0	R	1: No zero crossing in the eye diagram observed 0: Zero crossing in the eye diagram detected
	4	get_heo_veo_error_no_opening	0	R	1: Eye diagram is completely closed 0: Open eye diagram detected
	3	Reserved	0	R	
	2	Reserved	0	R	
	1	eom_get_heo_veo	0	RW	1: Acquire HEO & VEO(self-clearing) 0: Normal operation
	0	eom_start	0	R	1: Starts EOM counter(self-clearing) 0: Normal operation
EOM_MSB		Reg 0x25 Channel	0x00		Eye opening monitor hits(MSB)
	7	eom_count[15]	0	RW	MSBs of EOM counter
	6	eom_count[14]	0	RW	
	5	eom_count[13]	0	RW	
	4	eom_count[12]	0	RW	
	3	eom_count[11]	0	RW	
	2	eom_count[10]	0	RW	
	1	eom_count[9]	0	RW	
	0	eom_count[8]	0	RW	

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Table 7. CDR Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
EOM_LSB		Reg 0x26 Channel	0x00		Eye opening monitor hits(LSB)
	7	eom_count[7]	0	RW	LSBs of EOM counter
	6	eom_count[6]	0	RW	
	5	eom_count[5]	0	RW	
	4	eom_count[4]	0	RW	
	3	eom_count[3]	0	RW	
	2	eom_count[2]	0	RW	
	1	eom_count[1]	0	RW	
	0	eom_count[0]	0	RW	
HEO		Reg 0x27 Channel	0x00		Horizontal Eye Opening
	7	heo[7]	0	R	HEO value. This is measured in 0-63 phase settings. To get HEO in UI, read HEO, convert hex to dec, then divide by 64.
	6	heo[6]	0	R	
	5	heo[5]	0	R	
	4	heo[4]	0	R	
	3	heo[3]	0	R	
	2	heo[2]	0	R	
	1	heo[1]	0	R	
	0	heo[0]	0	R	
VEO		Reg 0x28 Channel	0x00		Vertical Eye Opening
	7	veo[7]	0	R	This is measured in 0-63 vertical steps. To get VEO in mV, read VEO, convert hex to dec, then multiply by 3.125mV
	6	veo[6]	0	R	
	5	veo[5]	0	R	
	4	veo[4]	0	R	
	3	veo[3]	0	R	
	2	veo[2]	0	R	
	1	veo[1]	0	R	
	0	veo[0]	0	R	
Auto_EOM _Vrange		Reg 0x29 Channel	0x00		EOM Vrange Readback
	7	Reserved	0	RW	
	6	eom_vrange_setting[1]	00	R	Auto Vrange readback of eye monitor granularity 00: 3.125mV 01: 6.25mV 10: 9.375mV 11: 12.5mV
	5	eom_vrange_setting[0]			
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	

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Table 7. CDR Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
EOM_Timer_Thr		Reg 0x2A Channel	0x30		EOM Hit Timer
	7	eom_timer_thr[7]	0	RW	EOM timer for how long to check each phase/voltage setting
	6	eom_timer_thr[6]	0	RW	
	5	eom_timer_thr[5]	1	RW	
	4	eom_timer_thr[4]	1	RW	
	3	eom_timer_thr[3]	0	RW	
	2	eom_timer_thr[2]	0	RW	
	1	eom_timer_thr[1]	0	RW	
	0	eom_timer_thr[0]	0	RW	
VEO_Scale		Reg 0x2C Channel	0x32		VEO_Scale
	7	Reserved	0	RW	
	6	veo_scale	0	RW	1: Enable Auto VEO scaling 0: VEO scaling based on Vrange Setting (0x11[7:6])
	5	Reserved	1	RW	
	4	Reserved	1	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	1	RW	
	0	Reserved	0	RW	
HEO VEO Threshold		Reg 0x32 Channel	0x11		HEO/VEO Interrupt Threshold
	7	heo_int_thresh[3]	0	RW	Compares HEO value, 0x27[7:0], vs threshold 0x32[7:4] * 4
	6	heo_int_thresh[2]	0	RW	
	5	heo_int_thresh[1]	0	RW	
	4	heo_int_thresh[0]	1	RW	
	3	veo_int_thresh[3]	0	RW	Compares VEO value, 0x28[7:0], vs threshold 0x32[3:0 * 4
	2	veo_int_thresh[2]	0	RW	
	1	veo_int_thresh[1]	0	RW	
	0	veo_int_thresh[0]	1	RW	

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Table 7. CDR Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
CDR State Machine Control		Reg 0x3E Channel	0x80		CDR State Machine Setting
	7	INIT_CDR_SM_3	1	RW	At power-up, this bit needs to be set to 0'b. See initialization set up
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
HEO_VEO_Lock		Reg 0x69 Channel	0x0A		HEO/VEO Interval Monitoring
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	
	3	hv_lckmon_cnt_ms[3]	1	RW	While monitoring lock, this sets the interval time. Each interval is 6.5 ms. At default condition, HEO_VEO Lock Monitor occurs once every 65 ms.
	2	hv_lckmon_cnt_ms[2]	0	RW	
	1	hv_lckmon_cnt_ms[1]	1	RW	
	0	hv_lckmon_cnt_ms[0]	0	RW	
CDR State Machine Control		Reg 0x6A Channel	0x44		CDR State Machine Control
	7	INIT_CDR_SM_57	0	RW	At power-up, this register should be set to 0x00. See initialization set up
	6	INIT_CDR_SM_56	1	RW	
	5	INIT_CDR_SM_55	0	RW	
	4	INIT_CDR_SM_54	0	RW	
	3	INIT_CDR_SM_53	0	RW	
	2	INIT_CDR_SM_52	1	RW	
	1	INIT_CDR_SM_51	0	RW	
	0	INIT_CDR_SM_50	0	RW	
SMPTE_Rate_Enable		Reg 0xA0 Channel	0x1f		SMPTE_Data_Rate_Lock_Restriction
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	dvb_enable	1	RW	1: Enable CDR Lock to 270 Mbps 0: Disable CDR Lock to 270 Mbps
	3	hd_enable	1	RW	1: Enable CDR Lock to 1.485/1.4835 Gbps 0: Disable CDR Lock to 1.485/1.4835 Gbps
	2	3G_enable	1	RW	1: Enable CDR Lock to 2.97/2.967 Gbps 0: Disable CDR Lock to 2.97/2.967 Gbps
	1	Reserved	1	RW	Reserved
	0	Reserved	1	RW	Reserved

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8.5.5 Transmitter Registers

Table 8. Transmitter Registers

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
Out0_Mux_Select		Reg 0x1C Channel	0x18		OUT0 Mux Selection
	7	pfd_sel0_data_mux[2]	0	RW	When 0x09[5] = 1'b OUT0 Mux Selection can be controlled as follows: 000: Mute 001: 10 MHz Clock 010: Raw Data 100: Retimed Data Other Settings - Invalid
	6	pfd_sel0_data_mux[1]	0	RW	
	5	pfd_sel0_data_mux[0]	0	RW	
	4	vco_clk_sel	1	RW	When 0x09[5] = 1'b and 0x1E[[7:5] = 101'b OUT1 clock selection can be controlled as follows: 1: OUT1 puts out line rate clock 0: OUT1 puts out 10MHz clock
	3	mr_drv_out_ctrl[1]	1	RW	Controls both OUT0 and OUT1: 00: OUT0: Mute OUT1: Mute 01: OUT0: Locked Reclocked Data / Unlocked Raw Data OUT1: Locked Output Clock / Unlocked Mute 10: OUT0: Locked Reclocked Data / Unlocked RAW OUT1: Locked Reclocked Data / Unlocked Raw 11: OUT0: Forced Raw OUT1: Forced Raw
	2	mr_drv_out_ctrl[0]	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
OUT1_Mux_Select		Reg 0x1E Channel	0xE9		OUT1 Mux Selection
	7	pfd_sel_data_mux[2]	1	RW	When 0x09[5] = 1'b OUT0 Mux Selection can be controlled as follows: 111: Mute 101: 10MHz Clock if reg 0x1c[4]=0 and full rate clock if reg 0x1c[4] = 1 010: Full Rate Clock 001: Retimed Data 000: Raw Data Other Settings - Invalid
	6	pfd_sel_data_mux[1]	1	RW	
	5	pfd_sel_data_mux[0]	1	RW	
	4	Reserved	0	RW	
	3	Reserved	1	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	1	RW	

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Table 8. Transmitter Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
OUT1 Invert		Reg 0x1F Channel	0x10		Invert OUT1 Polarity
	7	pfd_sel_inv_out1	0	RW	1: Inverts OUT1 polarity 0: OUT1 Normal polarity
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	1	RW	
	3	Reserved	0	RW	
	2	Reserved	0	RW	
	1	Reserved	0	RW	
	0	Reserved	0	RW	
OUT0_VOD		Reg 0x80 Channel	0x54		OUT0 VOD_PD
	7	drv_0_sel_vod[3]	0	RW	Controls OUTDriver 0 VOD Setting 0011: Nominal - 10% 0100: Nominal - 5% 0101: Nominal 800 mV 0110: Nominal + 5% 0111: Nominal + 10% Other Settings - Invalid
	6	drv_0_sel_vod[2]	1	RW	
	5	drv_0_sel_vod[1]	0	RW	
	4	drv_0_sel_vod[0]	1	RW	
	3	Reserved	0	RW	
	2	Reserved	1	RW	
	1	mr_drv_0_ov	0	RW	1: Enable 0x80[0] to override pin/sm control 0: Disable 0x80[0] to override pin/sm control
	0	sm_drv_0_PD	0	RW	1: Power down OUT0 0: OUT1 in normal operating mode
OUT1_VOD		Reg 0x84 Channel	0x04		OUT1 VOD Control
	7	Reserved	0	RW	
	6	drv_1_sel_vod[2]	0	RW	OUTDriver1 VOD Setting 000: 570 mVDifferential(Diff) Peak to Peak(PP) 010: 730 mV(Diff PP) 100: 900 mV(Diff PP) 110: 1035 mV(Diff PP)
	5	drv_1_sel_vod[1]	0	RW	
	4	drv_1_sel_vod[0]	0	RW	
	3	Reserved	0	RW	
	2	drv_1_sel_scp	1	RW	1: Enables short circuit protection on OUT1 0: Disable short circuit protection on OUT1
	1	mr_drv_1_ov	0	RW	1: Enable 0x80[0] to override pin/sm control 0: Disable 0x80[0] to override pin/sm control
	0	sm_drv_1_PD	0	RW	1: Power down OUT1 driver 0: OUT1 in normal operating mode
OUT1_DE		Reg 0x85	0x00		OUT1 DE Control
	7	Reserved	0	RW	
	6	Reserved	0	RW	
	5	Reserved	0	RW	
	4	Reserved	0	RW	

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Table 8. Transmitter Registers (continued)

REGISTER NAME	BITS	FIELD REGISTER ADDRESS	DEFAULT	R/RW	DESCRIPTION
	3	drv_1_dem_range	0	RW	Controls de-emphasis of 50 Ω Driver 0000: DE Disabled 0001: 0.2 dB 0010: 1.8 dB ..... 0111: 11 dB
	2	drv_1_dem[2]	0	RW	
	1	drv_1_dem[1]	0	RW	
	0	drv_1_dem[0]	0	RW	

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMH0318 is a single channel SDI reclocker with integrated cable driver that supports different application spaces. The following sections describe the typical use cases and common implementation practices.

9.1.1 General Guidance for All Applications

The LMH0318 supports two modes of configuration: SPI Mode, and SMBus Mode. Once one of these two control mechanism is chosen, pay attention to the PCB layout for the high speed signals. The LMH0318 has strong equalization capabilities that allow it to recover data over lossy channels. As a result, the optimal placement for the LMH0318 is with the higher loss channel at its input and lower loss channel segment at the output in order to meet the various SMPTE requirements. The SMPTE specifications also define the use of AC coupling capacitors for transporting uncompressed serial data streams with heavy low frequency content. This specification requires the use of a 4.7 µF AC coupling capacitor to avoid low frequency DC wander. The 75 Ω signal is also required to meet certain rise/fall timing to facilitate highest eye opening for the receiving device. The LMH0318 built-in 75 Ω termination minimizes parasitic, improving overall signal integrity. Note: When the FPGA is not transmitting valid SMPTE data, the FPGA output should be muted (P=N).

9.2 Typical Application

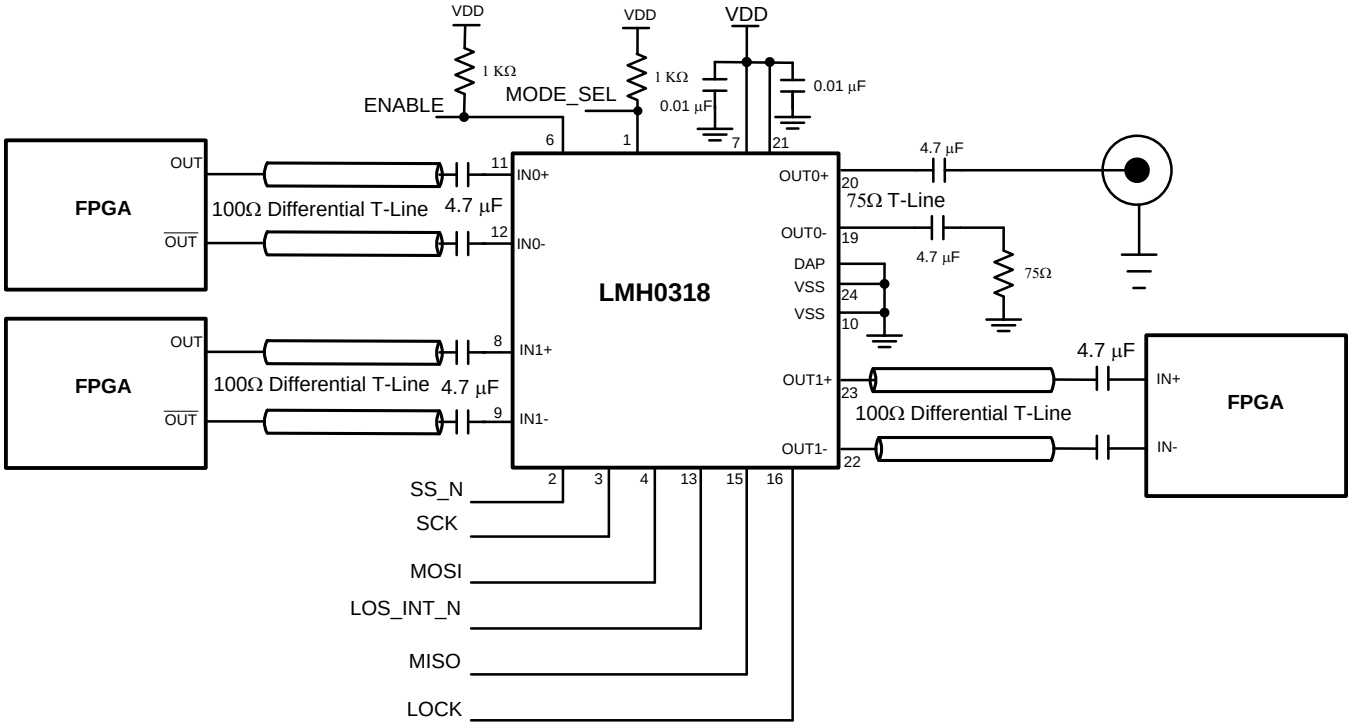


Figure 17. LMH0318 SPI Mode Configuration

Typical Application (continued)

SMPTE specifies the requirements for the Serial Digital Interface to transport digital video at SD, HD, 3Gb/s and higher data rates over coaxial cables. One of the requirements is meeting the required return loss. This requirement specifies how closely the port resembles 75 Ω impedance across a specified frequency band. Output return loss is dependent on board design. The LMH0318 meets this requirement. To gain additional return loss margin, a return loss network, as shown in Figure 18, can be used on the output .

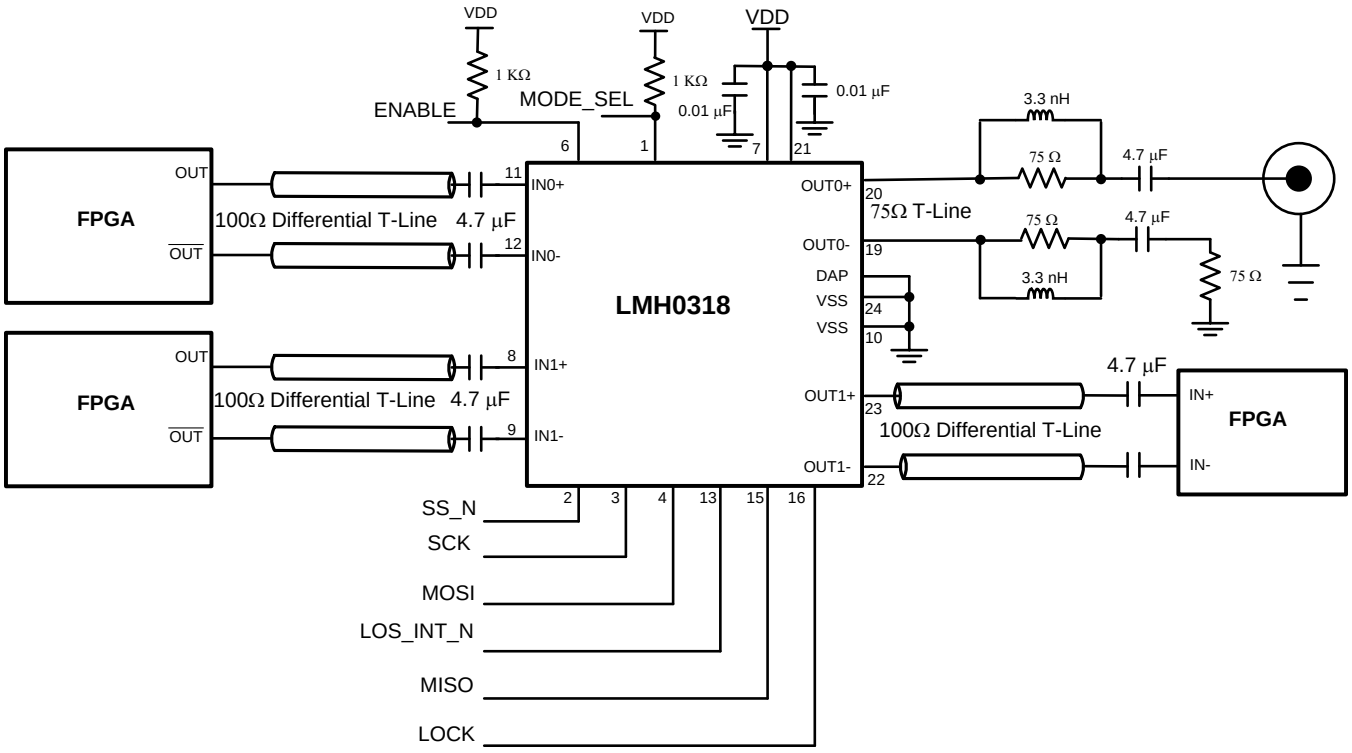


Figure 18. LMH0318 SPI Mode Configuration with Return Loss Network

9.2.1 Design Requirements

For the LMH0318 design example, the requirements noted in Table 9 apply.

Table 9. LMH0318 Design Parameters

DESIGN PARAMETER	REQUIREMENT
Input AC coupling capacitors	Required. 4.7 µF AC coupling capacitors are recommended. Capacitors may be implemented on the PCB or in the connector.
Output AC coupling capacitors	Required. Both OUT0 and OUT1 require AC coupling capacitors. OUT0 AC Coupling capacitors is expected to be 4.7 µF to comply with SMPTE wander requirement.
DC Power Supply Coupling Capacitors	To minimize power supply noise, use 0.01 µF capacitors as close to the device VDD pins as possible.
Distance from Device to BNC	Keep this distance as short as possible.
High Speed IN0, IN1, OUT0, and OUT1 trace impedance	Design differential trace impedance of IN0, IN1, and OUT1 with 100 Ω ± 5%, single-ended trace impedance for OUT0 with 75 Ω ± 5%

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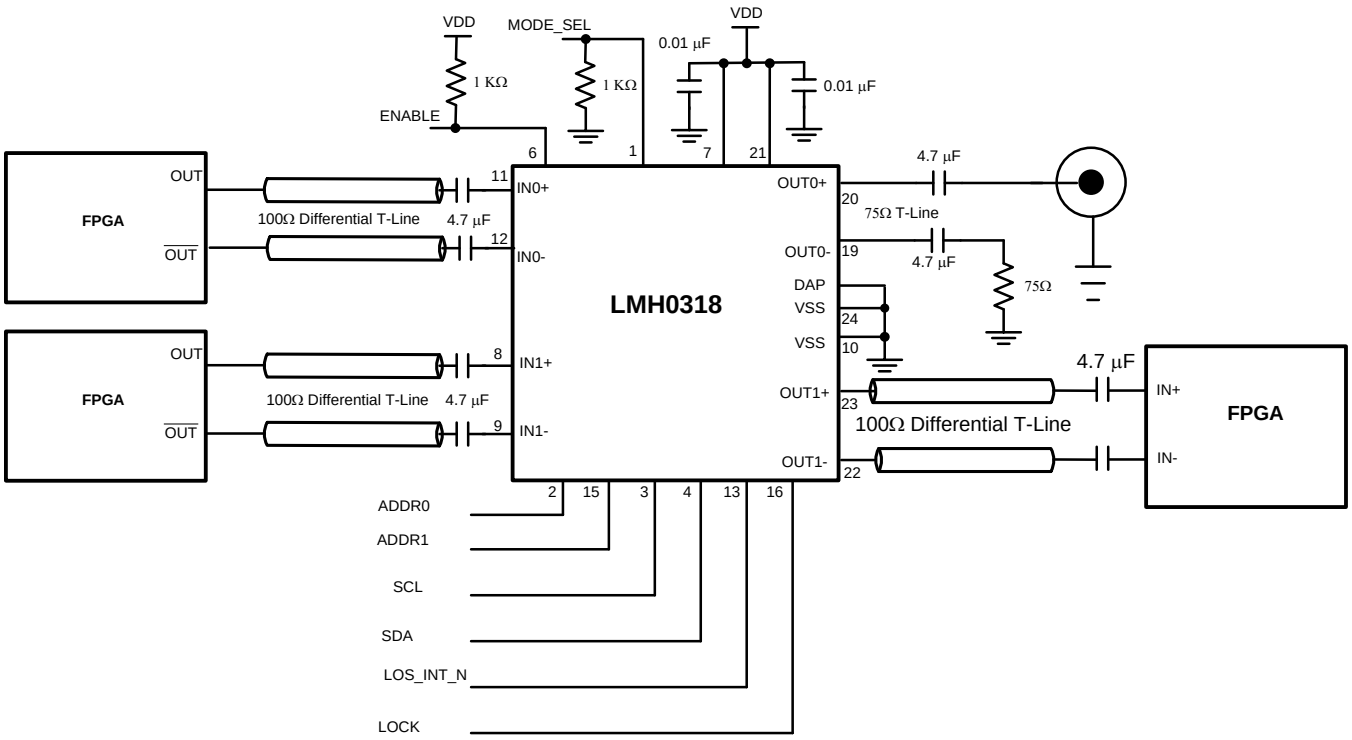


Figure 19. LMH0318 SMBus Mode Configuration

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

1. Maximum power draw for PCB regulator selection. In this case, use the transient CDR power (during acquisition) specified in the datasheet, multiplied by the number of channels.
2. Maximum operational power for thermal calculation. For thermal calculation, use the locked power number. Transient power consumption is only observed during lock acquisition, which typically lasts for <5ms. Additional margin can be applied in case of unsupported data rates being applied which extend the lock time. Note that the CDR should operate in bypass mode for any unsupported data rates.
3. Consult the BNC vendor for optimum BNC landing pattern.
4. Use IBIS-AMI model for simple channel simulation before PCB layout.
5. Closely compare schematic against typical connection diagram in the data sheet.
6. Plan out the PCB layout and component placement to minimize parasitic.

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9.2.3 Application Curves

Two common ways to visualize this data are shown in Figure 20 and Figure 21. These diagrams depict examples of eye monitor plot implemented by software. The first plot is an example of using the EOM data to plot a basic eye using ASCII characters, which can be useful for simple diagnostics software. The second plot shows the first derivative of the EOM data, revealing the density of hits and the actual waveforms and crossing that comprise the eye. Measurements were done at default operating conditions.

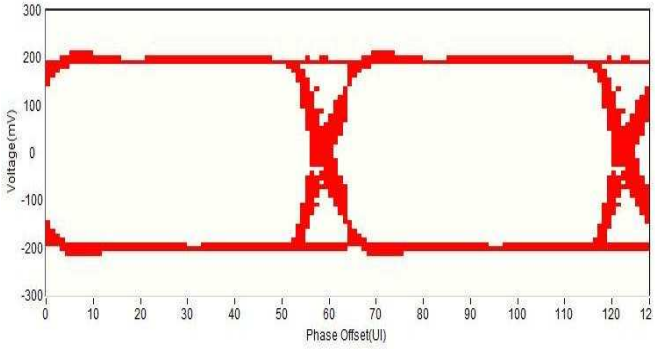


Figure 20. Internal Input Eye Monitor Plot at 2.97 Gbps, PRBS10

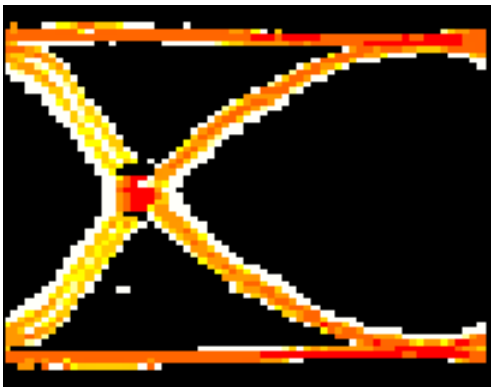


Figure 21. Internal Eye Monitor Hit Density Plot at 2.97 Gbps, PRBS10

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9.3 Do's and Don'ts

In order to meet SMPTE standard requirements for jitter, AC timing, and return loss use the following guidelines:

1. Do place BNC as close to the device as possible.
2. Do consult BNC vendor to provide optimum landing pad for the BNC to comply with the required specifications.
3. Place return loss network as close to the device as possible.
4. Do pay attention to the recommended solder paste to ensure reliable GND connection to DAP.
5. Do use control impedance for both 100 Ω and 75 Ω for IN0/1 and OUT0/1.

9.4 Initialization Set Up

After power up or register reset write the initialization sequences in Table 10.

Table 10. LMH0318 Register Initialization

DESCRIPTION	ADDRESS [Hex]	VALUE [Hex]
Enable Channel Registers	0xFF	0x04
Enable Full Temperature Range	0x16	0x25
Initialize CDR State Machine Control	0x3E	0x00
	0x55	0x02
	0x6A	0x00
Restore media CTLE setting(1)	0x03	xx (2)
Reset CDR	0x0A	0x5C
Release Reset	0x0A	0x50

(1) See *LMH0318 Programming Guide* (SNLU183) on how to quickly select the most appropriate CTLE boost setting.
(2) xx Value depends on media loss characteristics

10 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the recommended operating conditions in terms of DC voltage, AC noise, and start-up ramp time.
2. The maximum current draw for the LMH0318 is provided in the data sheet. This figure can be used to calculate the maximum current the supply must provide. Current consumption can be derived from the typical power consumption specification in the data sheet.
3. The LMH0318 does not require any special power supply filtering, provided the recommended operating conditions are met. Only standard supply decoupling is required.

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11 Layout

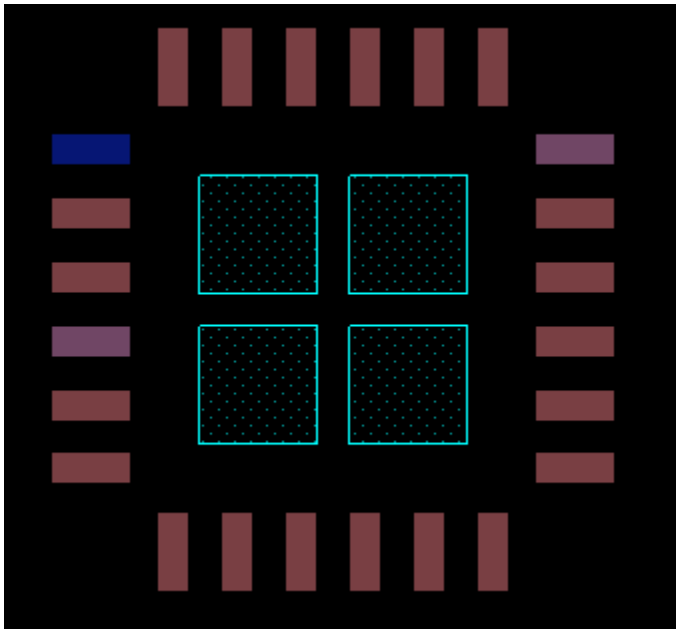
11.1 Layout Guidelines

The following guidelines should be followed when designing the layout:

1. Set trace impedances to 75 Ω ± 5% single ended, 100 Ω ± 5% differential.
2. Maintain the same signal reference plane for 75 Ω single-end trace, and reference plane for 100 Ω differential traces.
3. Use the smallest size surface mount components.
4. Use solid planes. Provide GND or VDD relief under the component pads to minimize parasitic capacitance.
5. Select trace widths that minimize the impedance mismatch along the signal path.
6. Select a board stack-up that supports 75 Ω or 50 Ω single-end trace, 100 Ω coupled differential traces.
7. Use surface mount ceramic capacitors.
8. Place return loss network as close to the device as possible.
9. Maintain symmetry on the complimentary signals.
10. Route 100 Ω traces uniformly (keep trace widths and trace spacing uniform along the trace).
11. Avoid sharp bends; use 45-degree or radial bends.
12. Walk along the signal path, identify geometry changes and estimate their impedance changes.
13. Maintain 75 Ω impedance with a well-designed connectors' footprint.
14. Consult a 3-D simulation tool to guide layout decisions.
15. Use the shortest path for VDD and Ground hook-ups; connect pin to planes with vias to minimize or eliminate trace.
16. When a high speed trace changes layer, provide at least 2 return vias to improve current return path.

11.2 Layout Example

The following example layout demonstrates how the thermal pad should be laid out using standard WQFN board routing guidelines.

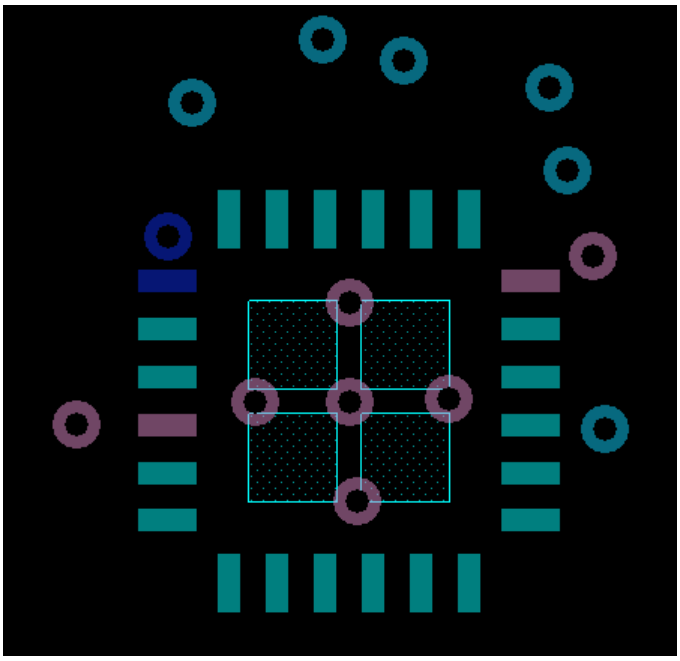


Note: Thermal pad is divided into 4 squares with solder paste

Figure 22. LMH0318 Recommended Four Squares Solder Paste

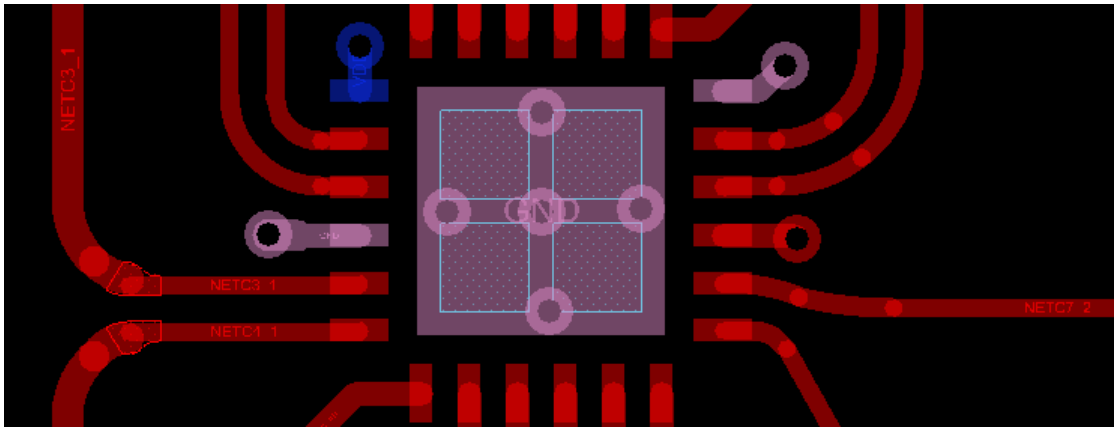
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Layout Example (continued)



5 Vias without solder paste are located between 4 squares solder paste

Figure 23. LMH0318 Recommended Solder Paste Mask and vias



Top etch plus traces

Figure 24. Example Layout

11.3 Solder Profile

The LMH0318 RTW024A Package solder profile and solder paste material can be found at the following link: SNOA401

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

For additional support, see the following:

- TI's E2E community: http://e2e.ti.com/
- High-Speed Interface forum in E2E community: http://e2e.ti.com/support/interface/high_speed_interface/

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- *LMH0318 Programming Guide* SNLU183
- *Leadless Leadframe Package* Application Note SNOA401

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH0318RTWR	ACTIVE	WQFN	RTW	24	3000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	L0318A1	Samples
LMH0318RTWT	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	L0318A1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

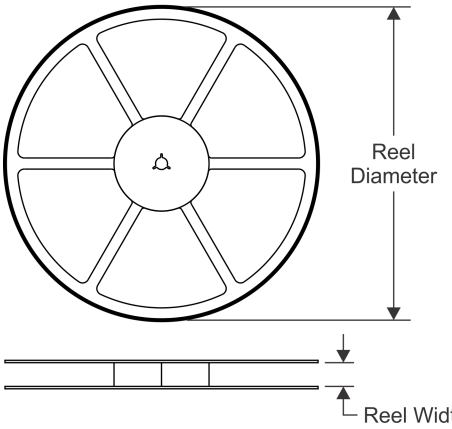
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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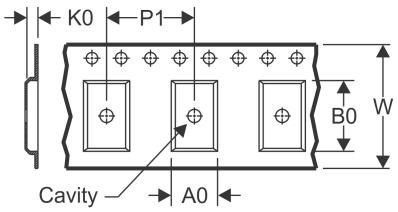
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

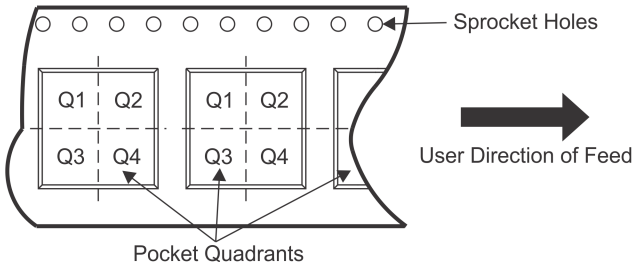


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

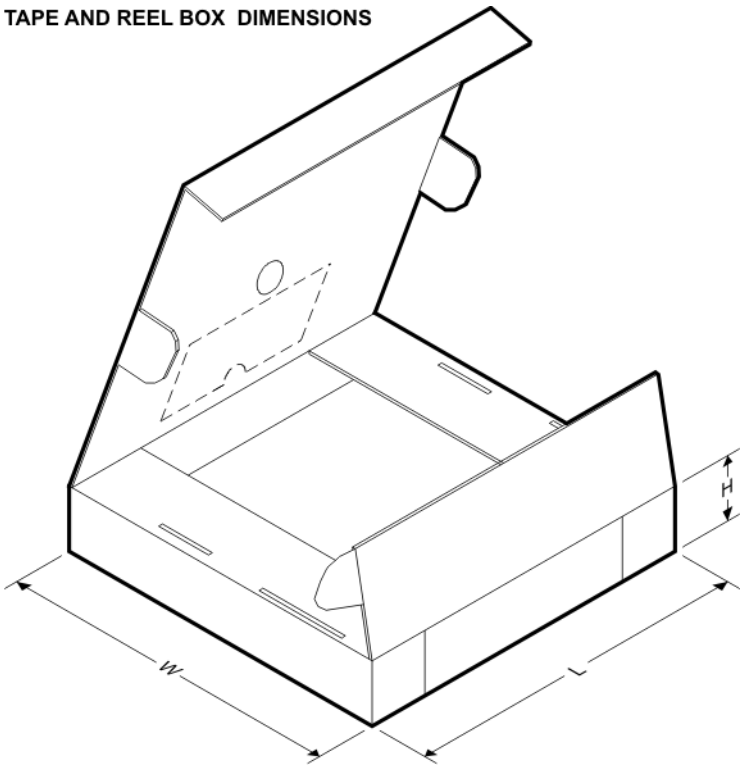
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH0318RTWR	WQFN	RTW	24	3000	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0318RTWT	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

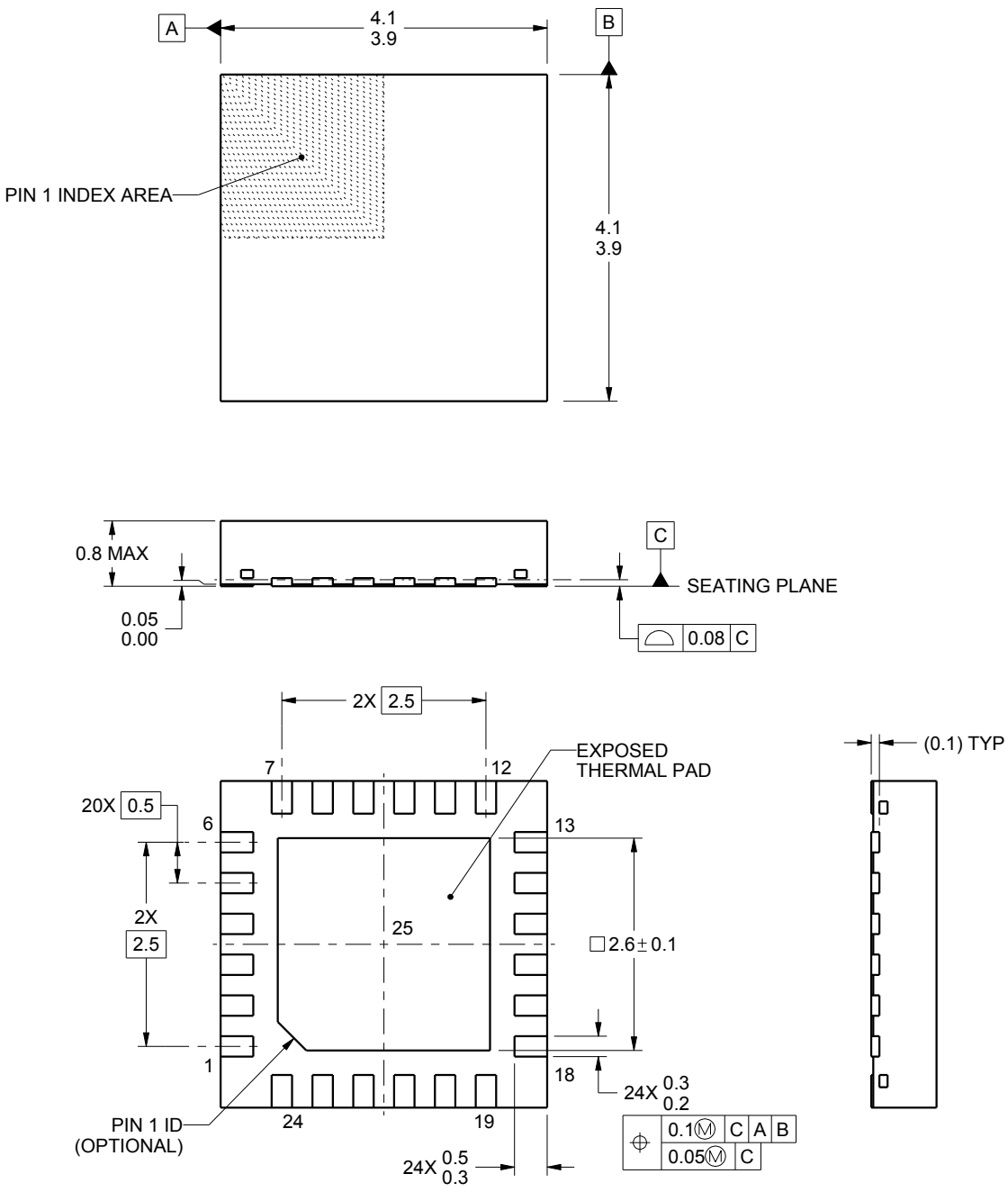
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH0318RTWR	WQFN	RTW	24	3000	367.0	367.0	35.0
LMH0318RTWT	WQFN	RTW	24	250	210.0	185.0	35.0

PACKAGE OUTLINE

RTW0024A

WQFN - 0.8 mm max height

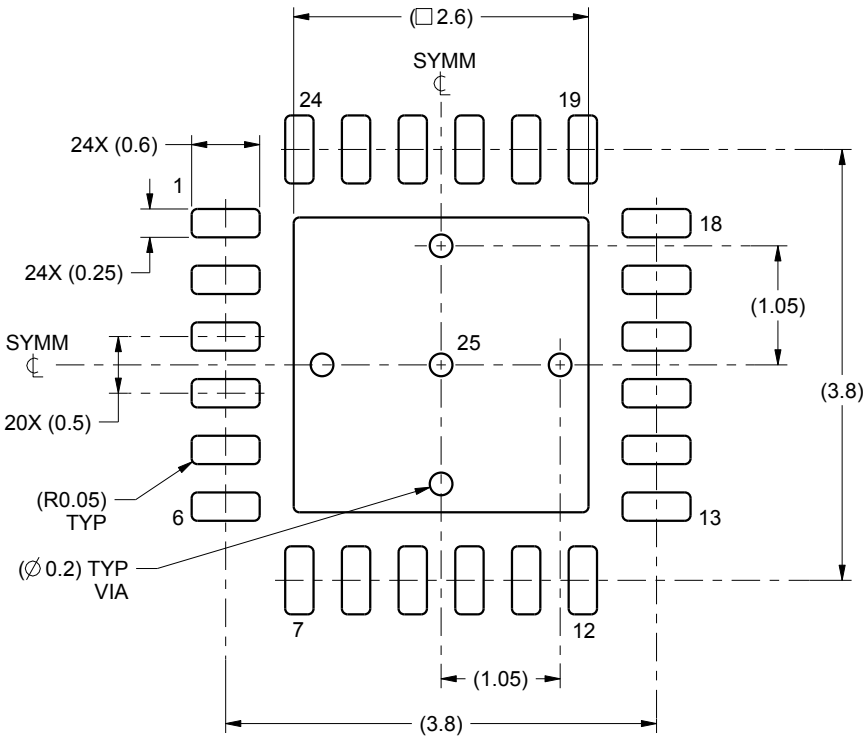
PLASTIC QUAD FLATPACK - NO LEAD



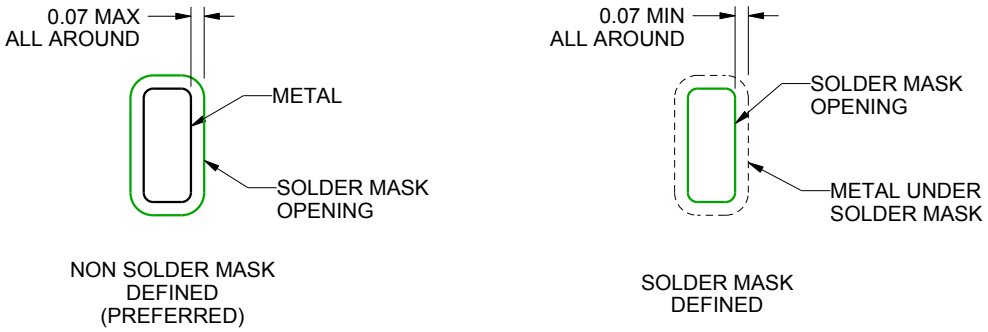
4222815/A 03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

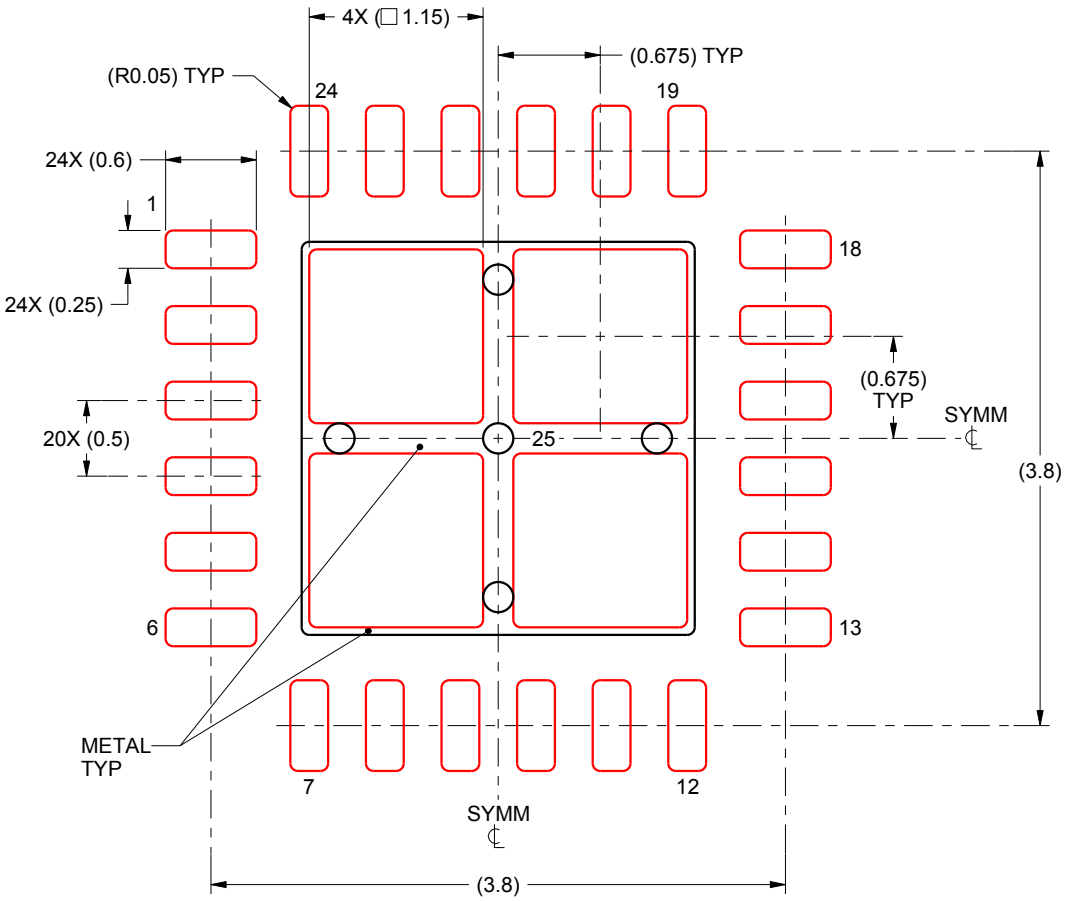


SOLDER MASK DETAILS

4222815/A 03/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222815/A 03/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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