

DESCRIPTION

Demonstration circuit 859 is a Multiple Output PD featuring the LTC4267. The board provides a complete IEEE 802.3af power device (PD) interface and isolated power supply solution for use in Power over Ethernet (PoE) applications. It generates 1.8V @ 2.5A, 2.5V @ 1.5A and 3.3V @ 0.5A.

The LTC4267 integrates the 25k Ω signature resistor, classification current source, thermal overload protection, signature disable and power good signal along with an undervoltage lockout optimized for use with the IEEE required diode bridge. The precision dual level input current limit allows the LTC4267 to charge load capacitors and interface with legacy PoE systems.

The LTC4267 combines the above features with a current mode switching controller designed for driving a 6V rated N-channel MOSFET. It features programmable slope compensation, soft-start, and constant frequency operation, minimizing electrical noise even with light loads.

Design files for this circuit board are available. Call the LTC factory.

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Table 1. Performance Summary ($T_A = 25^\circ\text{C}$)

PARAMETER	CONDITION	VALUE
Turn-on Voltage	Input from PSE	-36V maximum
Maximum Turn-off Voltage	Input from PSE, PD switch turns off	-32V
Power Converter Input operating range	$V_{OUT}=3.3\text{V}$, $I_{OUT} = 0$ to 2.6A	-37V to -57V
Maximum Input Current	Input from PSE, PD high level current limit	375 mA, typical
Maximum Output Current	$V_{OUT1}=1.8\text{V}$	2.5A
	$V_{OUT2}=2.5\text{V}$	1.5A
	$V_{OUT3}=3.3\text{V}$	0.5A
Output Voltage	$V_{IN}=48\text{VDC}$ from PSE	1.79V, typical
		2.5V, typical
		3.3V, typical
Output Regulation	$V_{OUT1} = 1.8\text{V}$, $V_{IN} = -37$ to -57VDC, zero to full load	$\pm 5\%$
	$V_{OUT2} = 2.5\text{V}$, $V_{IN} = -37$ to -57VDC, zero to full load	$\pm 2\%$
	$V_{OUT3} = 3.3\text{V}$, $V_{IN} = -37$ to -57VDC, zero to full load	$\pm 5\%$

QUICK START PROCEDURE

Demonstration circuit 859 is easy to set up to evaluate the performance of the LTC4267. For proper equipment setup, refer to figure 1 and follow the procedure below:

1. With the power source to the PSE turned off, connect the input power supply to the board through the J1 filtered Ethernet connector.
2. In addition to a PSE, the DC859 board can be powered by an alternate input power supply through the V+ (TP5) and VPORTN (TP14) terminals. Do not connect more than one power source.
3. Set the SIGNATURE jumper (JP1) to the ENABLE position.
4. Turn on the PSE or alternate input power supply and increase the voltage until the power converter turns on. Be careful not to exceed 57VDC. NOTE: Make sure that the input voltage does not exceed 57VDC. If a higher voltage is required, power components with higher voltage ratings should be used.
5. Verify proper classification and signature detection.
6. Check the output voltages. They should be as listed in table 1. If there is no output, temporarily disconnect the load to make sure that the load is not set too high.
7. Once the proper output voltage is established, adjust the load current within the appropriate range and observe the output regulation, ripple voltage, efficiency and other parameters.

OPERATION

Demonstration circuit 859 interfaces with a customer's Power-Over-Ethernet test setup per Figure 1. The front end of the demo circuit implements the required Ethernet input interface transformer coupling and common-mode termination through the integrated connector J1. The demonstration circuit is set up to allow data to pass in and back out of the demo circuit while the DC859 performs IEEE 802.3af interface functions. The Power Sourcing Equipment (PSE) is connected to J1 and the PHY is optionally connected to J2.

The PD is required to have 0.1 μ F of capacitance during detection; this is provided by C2. It is also required to have at least 5 μ F of capacitance after the in-rush circuit, provided by capacitors C1 and C9.

This demo circuit allows detection and power classification of the PD per the IEEE 802.3af specification. During the detection process of a PD, the LTC4267

displays the proper 25k Ω signature resistor. Signature detection may be disabled, if so desired, by setting the SIGNATURE jumper (JP1) to the DISABLE position. If signature classification is disabled, all interface functions of the LTC4267 are disabled. Signature detection, classification and the internal power MOSFET switch are all disabled.

Classification is programmed by the selection of a single external resistor, RClass, connected to the RCLASS pin on the LTC4267.

After detection and classification, the PD is powered up when the input voltage exceeds the LTC4267 turn-on under-voltage lock out (UVLO) through a dual-level current-limited power switch. While the voltage between POUT and VPORTN is above the Power Good trip point, the amperage through the power switch is held below the low-level current limit. When the voltage between POUT and VPORTN falls below the Power

Good trip point, the Power Good signal goes active low and the amperage through the power switch is held below the high-level current limit.

For the PD to remain powered on, it must present to the PSE both AC and DC components of the Maintain Power Signature (MPS). The PD must hold the DC MPS by drawing at least 10mA or the PSE may disconnect power. The DC859 demo board does not implement a discrete minimum load. The synchronous switching design satisfies the requirement.

The synchronous Flyback converter operates at a typical switching frequency of 200kHz, controlled by the current mode controller portion of the LT4267. Galvanic isolation is achieved through transformer T1 and opto-isolator ISO2.

The primary side power path is comprised of C1, C9, $\frac{1}{2}$ of T1, Q2, and R11. These components should be as close to each other as possible when laying out the printed circuit board. The secondary side power path for the 1.8V output is made up of part of T1, Q5, and C4. The 2.5V power path is made up of part of T1, Q4, C6 and C7. The 3.3V power path is made up of part of T1, Q6, C11 and C12. These parts, as grouped in the above description, should also be laid out as close to each other as possible, without overlapping any of the circuitry or traces of the primary side.

IN ORDER TO ENSURE PROPER OPERATION, THE DESIGNER MUST ENSURE THAT THE PD INPUT CURRENT REQUIREMENT DOES NOT EXCEED THE LTC4267 CURRENT LIMIT OVER THE UNIT'S OPERATING VOLTAGE RANGE.

QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 859

MULTIPLE OUTPUT PD

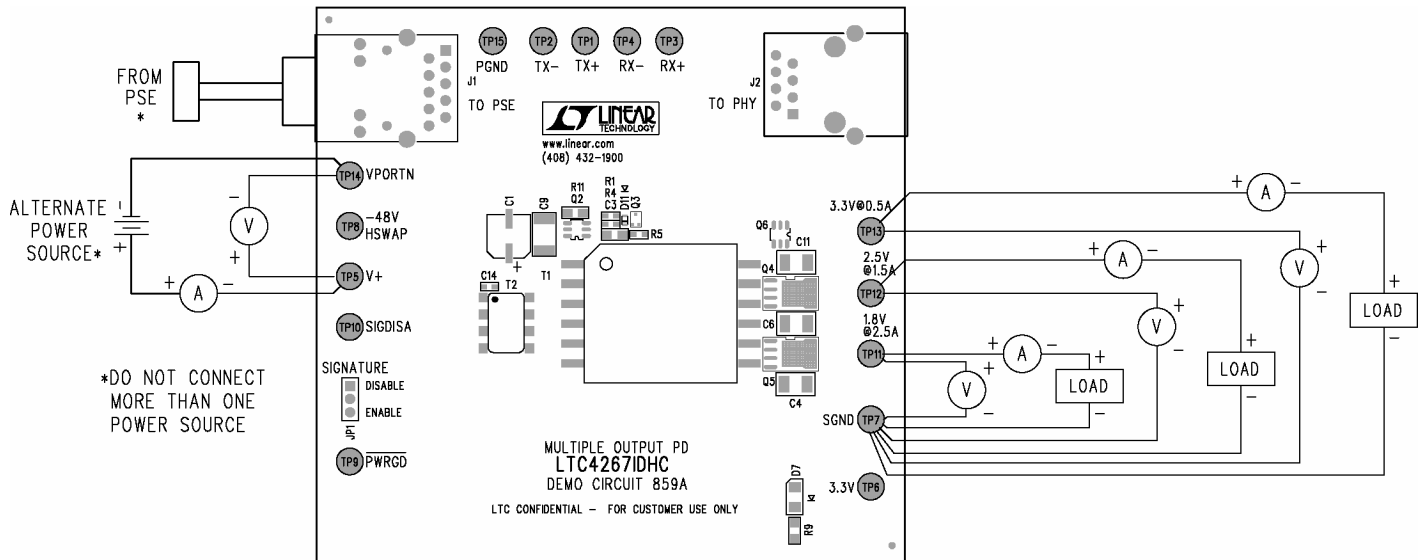


Figure 1. Proper Measurement Equipment Setup

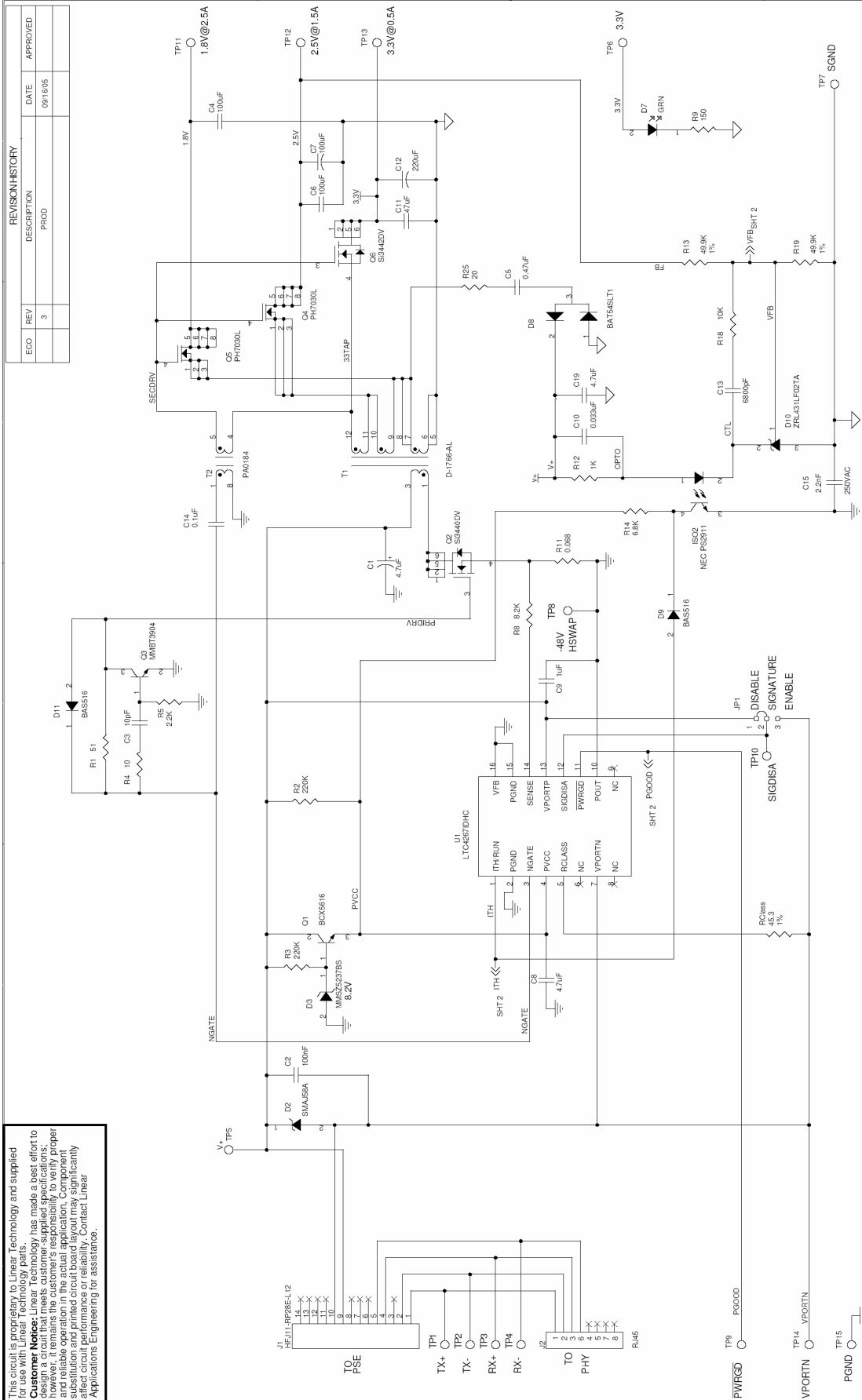
QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 859

MULTIPLE OUTPUT PD

This circuit is proprietary to Linear Technology and supplied for use with Linear Technology parts.

Customer Notice: Linear Technology has made a best effort to design a circuit that meets customer-supplied specifications; however, it remains the customer's responsibility to verify proper operation of the circuit. Linear Technology does not warrant the substitution and printed circuit board layout may significantly affect circuit performance or reliability. Contact Linear Applications Engineering for assistance.

REVISION HISTORY			
ECO	REV	DESCRIPTION	DATE
	3	PROD	09/16/05

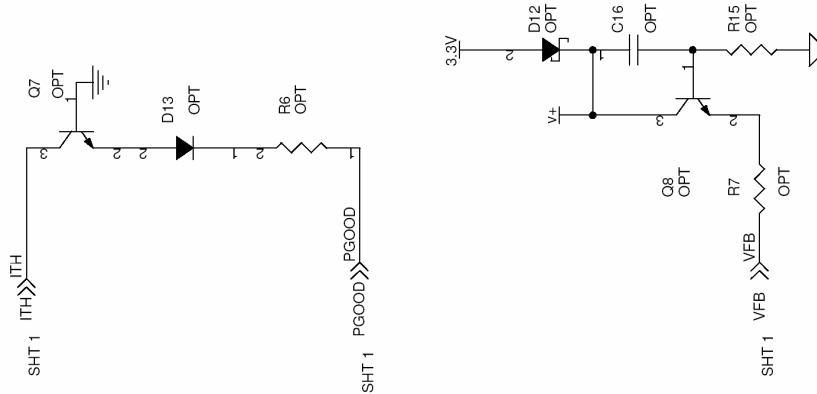


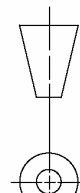
CONTRACT NO.		DATE	
APPROVALS		DATE	
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TITLE		SCH. LTC4267IDHC, MULTIPLE OUTPUT PD	
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QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 859

MULTIPLE OUTPUT PD

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	APPROVALS	DATE	TITLE SCH, LTC4267IDHC, MULTIPLE OUTPUT PD			
	DRAWN MEI	02/28/05				
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DO NOT SCALE DRAWING	SCALE: NONE		FILENAME: 859A-3.DSN		SHEET	2
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Tooling Holes

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