CDCEL824 Programmable 2-PLL Clock Synthesizer

1 Features

- Flexible Clock Driver
  - Three User-Definable Control Inputs [S0/S1/S2]: for example, Frequency Switching, Output Enable, or Power Down
  - Enables 0-PPM Clock Generation
- In-System Programmability and EEPROM
  - Serial Programmable Volatile Register
  - Nonvolatile EEPROM to Store Customer Settings
- Flexible Input Clocking Concept
  - External Crystal: 20 MHz to 30 MHz
  - Single-Ended LVCMOS up to 130 MHz
- Selectable Output Frequency up to 201 MHz
- Low-Noise PLL Core
  - PLL Loop Filter Components Integrated
  - Low Period Jitter (Typical 80 ps)
- 1.8-V Device Power Supply
- Temperature Range –40°C to 85°C
- Packaged in TSSOP

2 Applications

Laser Distance Measurement Applications

3 Description

The CDCEL824 is a modular PLL-based low-cost, high-performance, programmable clock synthesizer, multiplier, and divider. It generates up to four output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 201 MHz, using up to two independent configurable PLLs.

The CDCEL824 has a separate output supply pins, V_{DDOUT}, which are 1.8 V.

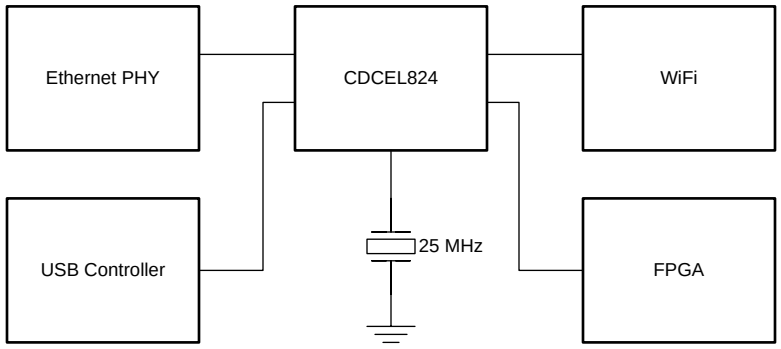
The input accepts an external crystal or LVCMOS clock signal. In case of a crystal input, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 pF to 20 pF.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCEL824	TSSOP (16)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2015) to Revision A	Page
• Changed custom to catalog data sheet	1
• Changed order of pin function rows to be by number per format rules	3
• Changed *Thermal Information* table format; move *EEPROM Spec* table per format rules	5

5 Description (continued)

The deep M/N divider ratio allows the generation of zero-ppm audio/video, networking (WLAN, *Bluetooth*, Ethernet, GPS) or interface (USB, IEEE1394, memory stick) clocks from a 27-MHz reference input frequency, for example.

Based on the PLL frequency and the divider settings, the internal loop filter components are automatically adjusted to achieve high stability and optimized jitter transfer characteristic of each PLL.

The device supports nonvolatile EEPROM programming for easy customization of the device in the application. It is preset to a factory default configuration and can be reprogrammed to a different application configuration before it goes onto the PCB or reprogrammed by in-system programming. All device settings are programmable through the SDA/SCL bus, a 2-wire serial interface.

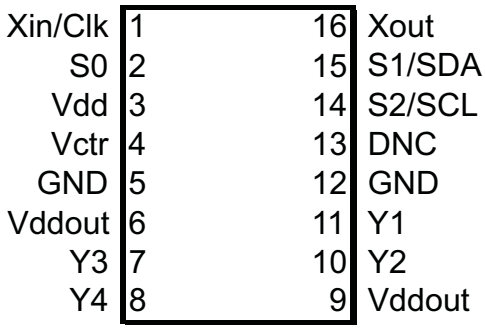
Three free programmable control inputs, S0, S1, and S2, can be used to select different frequencies, or other control features like outputs disable to low, outputs in high-impedance state, power down, PLL bypass, and so forth.

The CDCx824 operates in a 1.8-V environment in a temperature range of –40°C to 85°C.

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6 Pin Configuration and Functions

PW Package
20-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	Xin/CLK	I	Crystal oscillator input or LVCMOS clock Input (selectable via SDA/SCL bus).
2	S0	I	User-programmable control input S0; LVCMOS inputs; internal pullup.
3	V_{DD}	Power	1.8-V power supply for the device
4	V_{Ctrl}	I	VCXO control voltage (leave open or pull up when not used).
5, 12	GND	Ground	Ground
6, 9	V_{DDOUT}	Power	1.8-V supply for all outputs
7	Y3	O	LVCMOS outputs
8	Y4	O	LVCMOS outputs
10	Y2	O	LVCMOS outputs
11	Y1	O	LVCMOS outputs
13	DNC	O	Reserved pin, do not connect
14	SCL/S2	I	SCL: Serial clock input (default configuration), LVCMOS; internal pullup. S2: User-programmable control input; LVCMOS inputs; internal pullup.
15	SDA/S1	I/O or I	SDA: Bidirectional serial data input/output (default configuration), LVCMOS; internal pullup S1: User-programmable control input; LVCMOS inputs; internal pullup.
16	Xout	O	Crystal oscillator output (leave open or pull up when not used).

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage range	–0.5	2.5	V
V_I	Input voltage range(2) (3)	–0.5	V_{DD} + 0.5	V
V_O	Output voltage range(2)	–0.5	V_{DD} + 0.5	V
I_I	Input current (V_I < 0, V_I > V_{DD})		20	mA
I_O	Continuous output current		50	mA
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) SDA and SCL can go up to 3.6V as stated in the *Recommended Operating Conditions* table.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Device supply voltage	1.7	1.8	1.9	V
V_{DDOUT}	Output Yx supply voltage for CDCEL824	1.7		1.9	V
V_{IL}	Low-level input voltage LVCMOS			0.3 V_{DD}	V
V_{IH}	High-level input voltage LVCMOS	0.7 V_{DD}			V
$V_{I(thresh)}$	Input voltage threshold LVCMOS		0.5 V_{DD}		V
$V_{I(S)}$	Input voltage range S0	0		1.9	V
	Input voltage range S1, S2, SDA, SCL; $V_{(Ithresh)}$ = 0.5 V_{DD}	0		3.6	
$V_{I(CLK)}$	Input voltage range CLK	0		1.9	V
I_{OH} /I_{OL}	Output current (V_{DDOUT} = 1.8 V)			±8	mA
C_L	Output load LVCMOS			15	pF
T_A	Operating free-air temperature	–40		85	°C
RECOMMENDED CRYSTAL/VCXO SPECIFICATIONS(1)					
f_{Xtal}	Crystal input frequency range (fundamental mode)	10		30	MHz
ESR	Effective series resistance			100	Ω
f_{PR}	Pulling range (0 V ≤ V_{Ctrl} ≤ 1.8 V)(2)	±120	±150		ppm
V_{Ctrl}	Frequency control voltage	0		V_{DD}	V
C_0/C_1	Pullability ratio			220	
C_L	On-chip load capacitance at Xin and Xout	0		20	pF

(1) For more information about VCXO configuration, and crystal recommendation, see application report (SCAA085).
(2) Pulling range depends on crystal-type, on-chip crystal load capacitance and PCB stray capacitance; pulling range of min ±120 ppm applies for crystal listed in the application report (SCAA085).

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7.4 Thermal Information

THERMAL METRIC[1][2]		AIRFLOW (lfm)	CDCEL824 PW (TSSOP) 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	0	101	°C/W
		150	85	°C/W
		200	84	°C/W
		250	82	°C/W
		500	74	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		42	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		58	°C/W
ψ_{JB}	Junction-to-board characterization parameter		64	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		1.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

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7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
OVERALL PARAMETER							
I_{DD}	Supply current (see Figure 1)	All outputs off, f_{CLK} = 27 MHz, f_{VCO} = 135 MHz; f_{OUT} = 27 MHz	All PLLS on		20		mA
			Per PLL		9		
I_{DDOUT}	Supply current (see Figure 2)	No load, all outputs on, f_{OUT} = 27 MHz	V_{DDOUT} = 1.8 V		1		mA
I_{DDPD}	Power-down current. Every circuit powered down except SDA/SCL	f_{IN} = 0 MHz,	V_{DD} = 1.9 V		30		µA
V_{PUC}	Supply voltage V_{DD} threshold for power-up control circuit			0.85		1.45	V
f_{VCO}	VCO frequency range of PLL			80		201	MHz
f_{OUT}	LVCMOS output frequency	V_{DDOUT} = 1.8 V		201			MHz
LVCMOS PARAMETER							
V_{IK}	LVCMOS input voltage	V_{DD} = 1.7 V; I_S = –18 mA				–1.2	V
I_I	LVCMOS input current	V_I = 0 V or V_{DD}; V_{DD} = 1.9 V				±5	µA
I_{IH}	LVCMOS input current for S0/S1/S2	V_I = V_{DD}; V_{DD} = 1.9 V				5	µA
I_{IL}	LVCMOS Input current for S0/S1/S2	V_I = 0 V; V_{DD} = 1.9 V				–4	µA
C_I	Input capacitance at Xin/Clk	V_{IClk} = 0 V or V_{DD}			6		pF
	Input capacitance at Xout	V_{IXout} = 0 V or V_{DD}			2		
	Input capacitance at S0/S1/S2	V_{IS} = 0 V or V_{DD}			3		
LVCMOS PARAMETER for V_{DDOUT} = 1.8 V – MODE							
V_{OH}	LVCMOS high-level output voltage	V_{DDOUT} = 1.7 V, I_{OH} = –0.1 mA		1.6			V
		V_{DDOUT} = 1.7 V, I_{OH} = –4 mA		1.4			
		V_{DDOUT} = 1.7 V, I_{OH} = –8 mA		1.1			
V_{OL}	LVCMOS low-level output voltage	V_{DDOUT} = 1.7 V, I_{OL} = 0.1 mA				0.1	V
		V_{DDOUT} = 1.7 V, I_{OL} = 4 mA				0.3	
		V_{DDOUT} = 1.7 V, I_{OL} = 8 mA				0.6	
t_{PLH}, t_{PHL}	Propagation delay	All PLL bypass			2.6		ns
t_r/t_f	Rise and fall time	V_{DDOUT} = 1.8 V (20%–80%)			0.7		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter (2) (3)	1 PLL switching, Y1-to-Y2			80	110	ps
		2 PLL switching, Y1-to-Y4			130	200	
$t_{jit(per)}$	Peak-to-peak period jitter (3)	1 PLL switching, Y1-to-Y2			100	130	ps
		2 PLL switching, Y1-to-Y4			150	220	
$t_{sk(o)}$	Output skew(4)	f_{OUT} = 50 MHz; Y1-to-Y2				50	ps
		f_{OUT} = 50 MHz; Y1-to-Y4				110	
odc	Output duty cycle(5)	f_{VCO} = 100 MHz; Pdiv = 1		45%		55%	
SDA/SCL PARAMETER							
V_{IK}	SCL and SDA input clamp voltage	V_{DD} = 1.7 V; I_I = –18 mA				–1.2	V
I_{IH}	SCL and SDA input current	V_I = V_{DD}; V_{DD} = 1.9 V				±10	µA
V_{IH}	SDA/SCL input high voltage(6)			0.7 V_{DD}			V
V_{IL}	SDA/SCL input low voltage(6)					0.3 V_{DD}	V
V_{OL}	SDA low-level output voltage	I_{OL} = 3 mA V_{DD} = 1.7 V				0.2 V_{DD}	V
C_I	SCL/SDA Input capacitance	V_I = 0 V or V_{DD}			3	10	pF

(1) All typical values are at respective nominal V_{DD}.
(2) 10,000 cycles
(3) Jitter depends on configuration. Jitter data is for input frequency = 27 MHz, f_{VCO} = 135 MHz, f_{OUT} = 27 MHz. f_{OUT} = 3.072 MHz or input frequency = 27 MHz, f_{VCO} = 108 MHz, f_{OUT} = 27 MHz. f_{OUT} = 16.384 MHz, f_{OUT} = 25 MHz, f_{OUT} = 74.25 MHz, f_{OUT} = 48 MHz
(4) The tsk(o) specification is only valid for equal loading of each bank of outputs, and the outputs are generated from the same divider, data sampled on rising edge (t_r).
(5) odc depends on output rise- and fall time (t_r/t_f).
(6) SDA and SCL pins are 3.3-V tolerant.

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7.6 CLK_IN Timing Requirements

over recommended ranges of supply voltage, load, and operating free-air temperature

			MIN	NOM	MAX	UNIT
f_{CLK}	LVCMOS clock input frequency	PLL bypass mode	0		130	MHz
		PLL mode	8		130	
t_r / t_f	Rise and fall time CLK signal (20% to 80%)				3	ns
$duty_{CLK}$	Duty cycle CLK at V_{DD} / 2		40%		60%	

7.7 SDA/SCL Timing Requirements

(See Figure 5)		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{su(START)}$	START setup time (SCL high before SDA low)	4.7		0.6		µs
$t_{h(START)}$	START hold time (SCL low after SDA low)	4		0.6		µs
$t_{w(SCLL)}$	SCL low-pulse duration	4.7		1.3		µs
$t_{w(SCLH)}$	SCL high-pulse duration	4		0.6		µs
$t_{h(SDA)}$	SDA hold time (SDA valid after SCL low)	0	3.45	0	0.9	µs
$t_{su(SDA)}$	SDA setup time	250		100		ns
t_r	SCL/SDA input rise time		1000		300	ns
t_f	SCL/SDA input fall time		300		300	ns
$t_{su(STOP)}$	STOP setup time	4		0.6		µs
t_{BUS}	Bus free time between a STOP and START condition	4.7		1.3		µs

7.8 EEPROM Specification

		MIN	TYP	MAX	UNIT
EEcyc	Programming cycles of EEPROM	100	1000		cycles
EEret	Data retention	10			years

7.9 Typical Characteristics

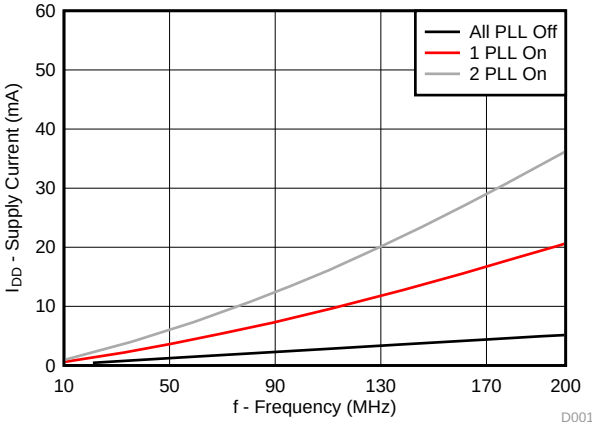


Figure 1. Supply Current vs PLL Frequency

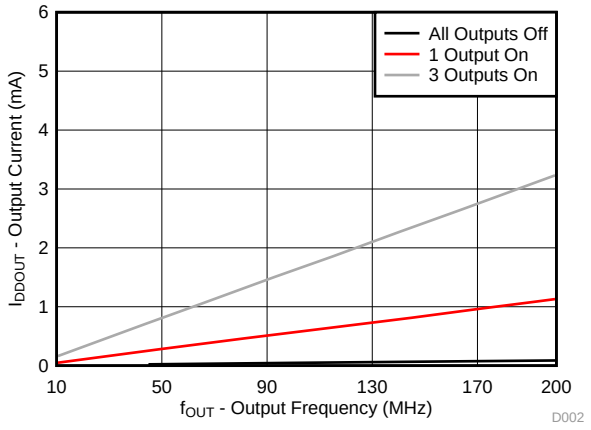


Figure 2. Output Current vs Output Frequency

8 Parameter Measurement Information

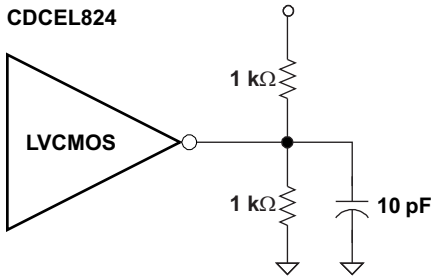


Figure 3. Test Load

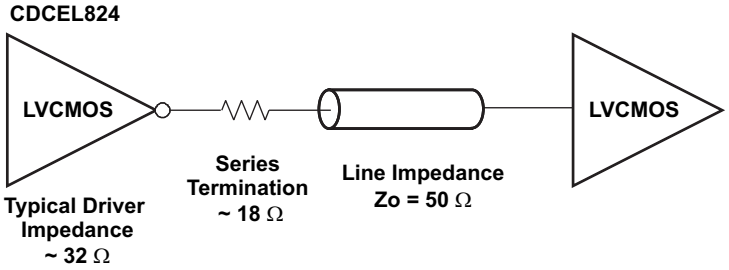


Figure 4. Test Load for 50-Ω Board Environment

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9 Detailed Description

9.1 Overview

The CDCEL824 is a modular PLL-based low-cost, high-performance, programmable clock synthesizer, multiplier, and divider. It generates up to four output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 201 MHz, using up to two independent configurable PLLs.

The CDCEL824 has a separate output supply pins, V_{DDOUT}, which are 1.8 V.

The input accepts an external crystal or LVCMOS clock signal. In case of a crystal input, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 pF to 20 pF.

The deep M/N divider ratio allows the generation of zero-ppm audio/video, networking (WLAN, *Bluetooth*, Ethernet, GPS) or interface (USB, IEEE1394, memory stick) clocks from a 27-MHz reference input frequency, for example.

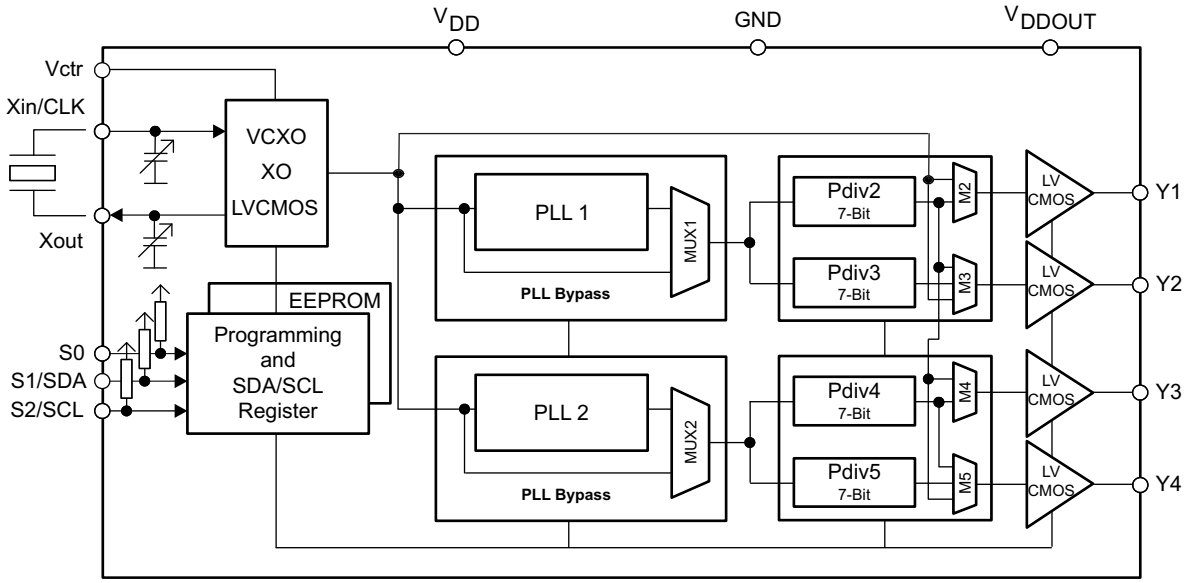
Based on the PLL frequency and the divider settings, the internal loop filter components are automatically adjusted to achieve high stability and optimized jitter transfer characteristic of each PLL.

The device supports nonvolatile EEPROM programming for easy customization of the device in the application. It is preset to a factory default configuration and can be reprogrammed to a different application configuration before it goes onto the PCB or reprogrammed by in-system programming. All device settings are programmable through the SDA/SCL bus, a 2-wire serial interface.

Three, free programmable control inputs, S0, S1, and S2, can be used to select different frequencies, or other control features like outputs disable to low, outputs in high-impedance state, power down, PLL bypass, and so forth.

The CDCx824 operates in a 1.8-V environment. It operates in a temperature range of –40°C to 85°C.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Control Pins Settings

The CDCEL824 has three user-definable control pins (S0, S1, and S2) which allow external control of device settings. They can be programmed to any of the following settings:

- Frequency selection → switching between any of two user-defined frequencies
- Output state selection → output configuration and power-down control

The user can predefine up to eight different control settings. Table 1 and Table 2 explain these settings.

Table 1. Control Pin Definition

EXTERNAL CONTROL BITS	PLL1 SETTING			PLL2 SETTING			RSVD SETTING
Control function	PLL frequency selection	Reserved	Output Y1/Y2 selection	PLL frequency selection	Reserved	Output Y3/Y4 selection	Reserved

Table 2. PLL Setting (Can Be Selected for Each PLL Individual)(1)

FREQUENCY SELECTION(2)	
FSx	**FUNCTION**
0	Frequency0
1	Frequency1
OUTPUT SELECTION(3) (Y1 ... Y4)	
YxYx	**FUNCTION**
0	State0
1	State1

(1) Center/down-spread, Frequency0/1 and State0/1 are user-definable in the PLLx configuration register.
(2) Frequency0 and Frequency1 can be any frequency within the specified f_{VCO} range.
(3) State0/1 selection is valid for both outputs of the corresponding PLL module and can be power down, high-impedance state, low, or active

SDA/S1 and SCL/S2 pins of the CDCEL824 are dual-function pins. In the default configuration, they are predefined as the SDA/SCL serial programming interface. They can be programmed to control pins (S1/S2) by setting the relevant bits in the EEPROM. Note that the changes of the bits in the control register (bit [6] of byte 02h) have no effect until they are written into the EEPROM.

Once they are set as control pins, the serial programming interface is no longer available. However, if V_{DDOUT} is forced to GND, the two control pins, S1 and S2, temporally act as serial programming pins (SDA/SCL).

S0 is not a multi-use pin; it is a control pin only.

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9.3.2 SDA/SCL Serial Interface

This section describes the SDA/SCL interface of the CDCEL824 device. The CDCEL824 operates as a slave device of the 2-wire serial SDA/SCL bus, compatible with the popular SMBus or I^2C specification. It operates in the standard-mode transfer (up to 100 kbit/s) and fast-mode transfer (up to 400 kbit/s) and supports 7-bit addressing.

The SDA/S1 and SCL/S2 pins of the CDCEL824 are dual-function pins. In the default configuration they are used as SDA/SCL serial programming interface. They can be reprogrammed as general-purpose control pins, S1 and S2, by changing the corresponding EEPROM setting, byte 02h, bit [6].

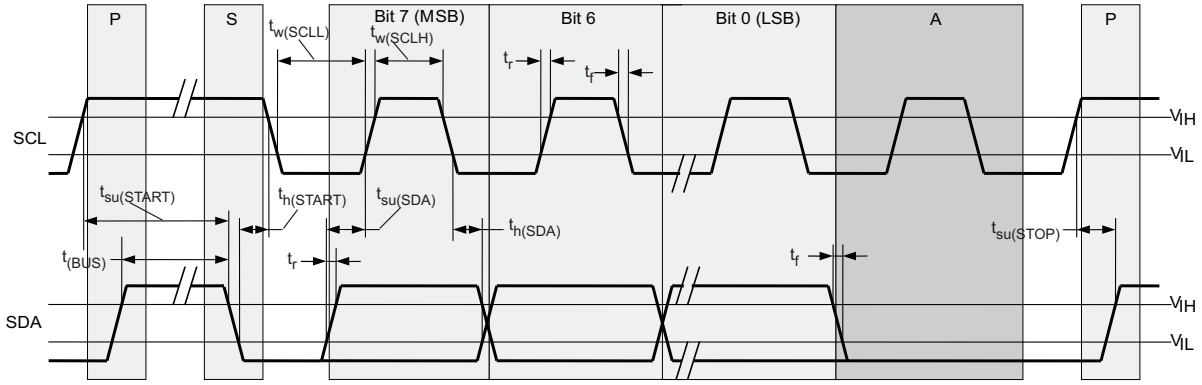


Figure 5. Timing Diagram for SDA/SCL Serial Control Interface

9.3.3 SDA/SCL Hardware Interface

Figure 6 shows how the CDCEL824 clock synthesizer is connected to the SDA/SCL serial interface bus. Multiple devices can be connected to the bus, but the speed may need to be reduced (400 kHz is the maximum) if many devices are connected.

Note that the pullup resistors (R_P) depend on the supply voltage, bus capacitance, and number of connected devices. The recommended pullup value is 4.7 kΩ. It must meet the minimum sink current of 3 mA at V_{OLmax} = 0.4 V for the output stages (for more details see the SMBus or I^2C Bus specification).

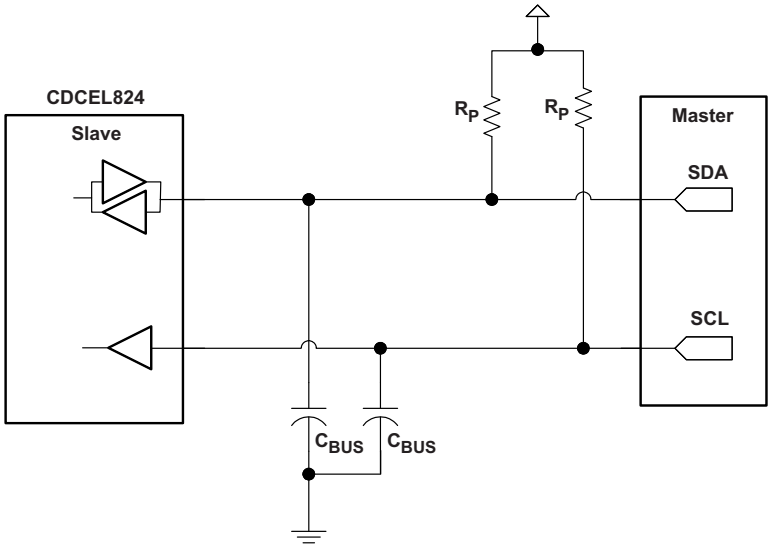


Figure 6. SDA/SCL Hardware Interface

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9.4 Device Functional Modes

9.4.1 Default Device Setting

The internal EEPROM of CDCEL824 is preconfigured as shown in Figure 7. The input frequency is passed through the output as a default. This allows the device to operate in default mode without the extra production step of programming it. The default setting appears after power is supplied or after a power-down/up sequence until it is reprogrammed by the user to a different application configuration. A new register setting is programmed via the serial SDA/SCL interface.

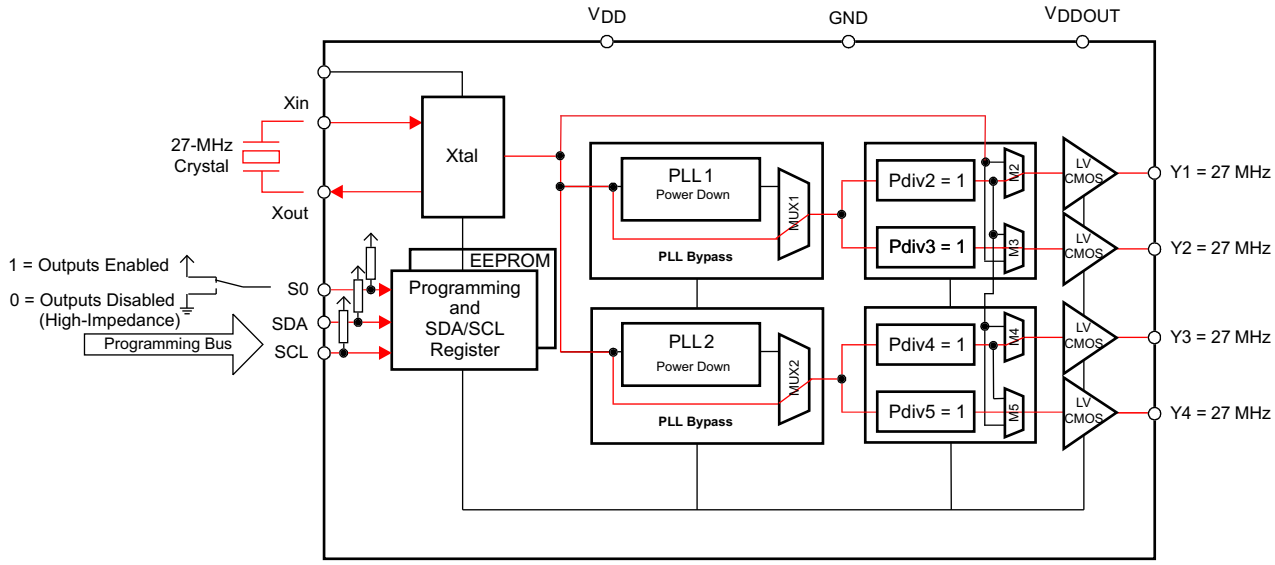


Figure 7. Preconfiguration of CDCEL824 Internal EEPROM

Table 3 shows the factory default setting for the control terminal register (external control pins). Note that even though eight different register settings are possible, in default configuration, only the first two settings (0 and 1) can be selected with S0, as S1 and S2 are configured as programming pins in the default mode.

Table 3. Factory Default Settings for Control Terminal Register(1)

			PLL1 SETTINGS		PLL2 SETTINGS	
EXTERNAL CONTROL PINS			FREQUENCY SELECTION	OUTPUT SELECTION	FREQUENCY SELECTION	OUTPUT SELECTION
S2	*S1*	**S0**	*FS1*	**Y1Y2**	*FS2*	**Y2Y3**
SCL (I2C)	SDA (I^2C)	**0**	f_{VCO1_0}	**High-impedance state**	f_{VCO2_0}	**High-impedance state**
SCL (I2C)	SDA (I^2C)	**1**	f_{VCO1_0}	**Enabled**	f_{VCO2_0}	**Enabled**

(1) S1 is SDA and S2 is SCL in default mode or when programmed (SPICON bit 6 of register 2 set to 0). They do not have any control-pin function but they are internally interpreted as if S1 = 0 and S2 = 0. S0, however, is a control pin which in the default mode switches all outputs ON or OFF (as previously predefined).

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9.5 Programming

9.5.1 Data Protocol

The device supports *Byte Write and Byte Read* and *Block Write and Block Read* operations.

For *Byte Write/Read* operations, the system controller can individually access addressed bytes.

For *Block Write/Read* operations, the bytes are accessed in sequential order from lowest to highest byte (with most-significant bit first) with the ability to stop after any complete byte has been transferred. The numbers of bytes read out are defined by byte count in the generic configuration register. At the *Block Read* instruction, all bytes defined in the byte count must be read out to finish the read cycle correctly.

Once a byte has been sent, it is written into the internal register and is effective immediately. This applies to each transferred byte regardless of whether this is a *Byte Write* or a *Block Write* sequence.

If the EEPROM write cycle is initiated, the internal SDA registers are written into the EEPROM. During this write cycle, data is not accepted at the SDA/SCL bus until the write cycle is completed. However, data can be read out during the programming sequence (*Byte Read* or *Block Read*). The programming status can be monitored by *EEPIP*, byte 01h–bit 6.

The offset of the indexed byte is encoded in the command code, as described in Table 4.

Table 4. Slave Receiver Address (7 Bits)

DEVICE	A6	A5	A4	A3	A2	A1(1)	A0(1)	R/$\overline{W}$
CDCEL824	1	1	0	0	1	0	0	1/0

(1) Address bits A0 and A1 are programmable via the SDA/SCL bus (byte 01, bit [1:0]. This allows addressing up to four devices connected to the same SDA/SCL bus. The least-significant bit of the address byte designates a write or read operation.

9.5.2 Command Code Definition

Table 5. Command Code Definition

BIT	DESCRIPTION
7	0 = *Block Read* or *Block Write* operation 1 = *Byte Read* or *Byte Write* operation
(6:0)	Byte offset for *Byte Read*, *Block Read*, *Byte Write* and *Block Write* operations.

9.5.3 Generic Programming Sequence

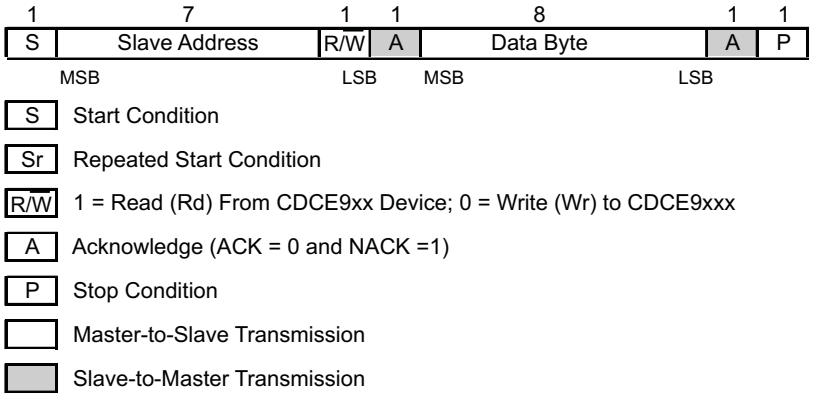


Figure 8. Generic Programming Sequence

9.5.4 Byte Write Programming Sequence

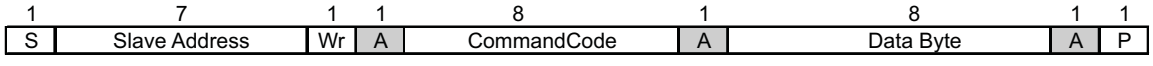


Figure 9. Byte Write Protocol

9.5.5 Byte Read Programming Sequence

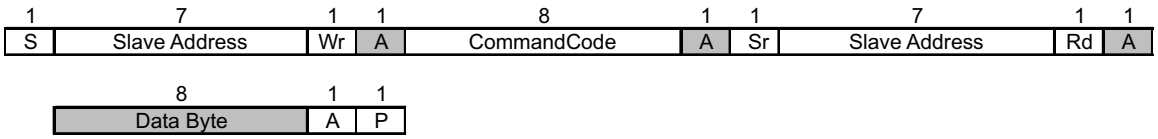
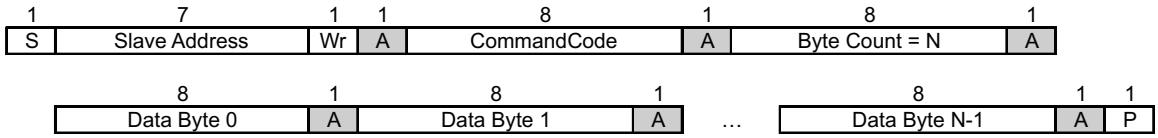


Figure 10. Byte Read Protocol

9.5.6 Block Write Programming Sequence



(1) Data byte 0 bits [7:0] is reserved for Revision Code and Vendor Identification. Also, it is used for internal test purpose and should not be overwritten.

Figure 11. Block Write Protocol

9.5.7 Block Read Programming Sequence

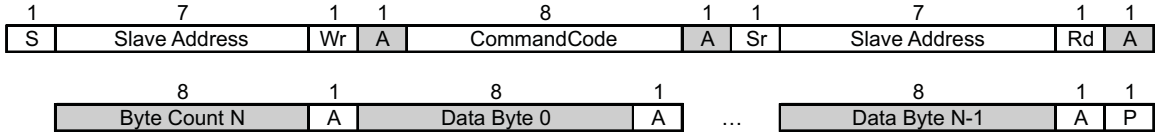


Figure 12. Block Read Protocol

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9.6 Register Maps

9.6.1 SDA/SCL Configuration Registers

The clock input, control pins, PLLs, and output stages are user configurable. The following tables and explanations describe the programmable functions of the CDCEL824. All settings can be manually written into the device via the SDA/SCL bus or easily programmed by using the TI Pro-Clock™ software.

Table 6. SDA/SCL Registers

ADDRESS OFFSET	REGISTER DESCRIPTION	TABLE
00h	Generic configuration register	Table 8
10h	PLL1 configuration register	Table 9
20h	PLL2 configuration register	Table 10

The grey-highlighted bits, described in the Configuration Registers tables in the following pages, belong to the Control Terminal Register. The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2. Table 7 explains the corresponding bit assignment between the Control Terminal Register and the Configuration Registers.

Table 7. Configuration Register, External Control Terminals

				PLL1 SETTINGS		PLL2 SETTINGS	
	EXTERNAL CONTROL PINS			FREQUENCY SELECTION	OUTPUT SELECTION	FREQUENCY SELECTION	OUTPUT SELECTION
	S2	S1	S0	FS1	Y1Y2	FS2	Y3Y4
0	0	0	0	FS1_0	Y1Y2_0	FS2_0	Y3Y4_0
1	0	0	1	FS1_1	Y1Y2_1	FS2_1	Y3Y4_1
2	0	1	0	FS1_2	Y1Y2_2	FS2_2	Y3Y4_2
3	0	1	1	FS1_3	Y1Y2_3	FS2_3Reserved	Reserved
4	1	0	0	FS1_4	Y1Y2_4	FS2_4Reserved	Reserved
5	1	0	1	FS1_5	Y1Y2_5	FS2_5	Y3Y4_5
6	1	1	0	FS1_6	Y1Y2_6	FS2_6	Y3Y4_6
7	1	1	1	FS1_7	Y1Y2_7	FS2_7	Y3Y4_7
	Address offset(1)			13h	15h	23h	25h

(1) Address offset refers to the byte address in the configuration register in Table 8, Table 9, and Table 10.

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Table 8. Generic Configuration Register

OFFSET[1]	BIT[2]	ACRONYM	DEFAULT[3]	DESCRIPTION
00h	7	E_EL	0b	Device identification (read-only): 0 is CDCEL824 (1.8 V out)
	6:4	RID	Xb	Revision identification number (read-only)
	3:0	VID	1h	Vendor identification number (read-only)
01h	7	–	0b	Reserved – always write 0
	6	EEPIP	0b	EEPROM programming Status4:[4] (read-only) 0 – EEPROM programming is completed 1 – EEPROM is in programming mode
	5	EELOCK	0b	Permanently lock EEPROM data[5] 0 – EEPROM is not locked 1 – EEPROM is permanently locked
	4	PWDN	0b	Device power down (overwrites S0/S1/S2 setting; configuration register settings are unchanged) Note: PWDN cannot be set to 1 in the EEPROM. 0 – Device active (all PLLs and all outputs are enabled) 1 – Device power down (all PLLs in power down and all outputs in high-impedance state)
	3:2	INCLK	00b	Input clock selection: 00 – Xtal 01 – VCXO 10 – LVCMOS 1 – Reserved
	1:0	SLAVE_ADR	00b	Address bits A0 and A1 of the slave receiver address
02h	7	M1	0b	RSVD 0 – Input clock 1 – PLL1 clock
	6	SPICON	0b	Operation mode selection for pins 14/15[6] 0 – Serial programming interface SDA (pin 15) and SCL (pin 14) 1 – Control pins S1 (pin 15) and S2 (pin 14)
	5:4	RSVD	01b	RSVD Reserved
	3:2	RSVD	01b	
	1:0	RSVD	001h	RSVD Reserved
03h	7:0	RSVD		
04h	7	Reserved	0b	RSVD Reserved
	6	Reserved	0b	
	5	Reserved	0b	
	4	Reserved	0b	
	3	Reserved	0b	
	2	Reserved	0b	
	1	Reserved	0b	

(1) Writing data beyond 30h may affect device function.
(2) All data transferred with the MSB first
(3) Unless customer-specific setting
(4) During EEPROM programming, no data is allowed to be sent to the device via the SDA/SCL bus until the programming sequence is completed. Data, however, can be read out during the programming sequence (*Byte Read* or *Block Read*).
(5) If this bit is set to high in the EEPROM, the actual data in the EEPROM is permanently locked. No further programming is possible. Data, however can still be written via the SDA/SCL bus to the internal register to change device function on the fly. But new data can no longer be saved to the EEPROM. EELOCK is effective only if written into the EEPROM.
(6) Selection of *control pins* is effective only if written into the EEPROM. Once written into the EEPROM, the serial programming pins are no longer available. However, if V_{DDOUT} is forced to GND, the two control pins, S1 and S2, temporally act as serial programming pins (SDA/SCL), and the two slave receiver address bits are reset to A0 = 0 and A1 = 0.

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Table 8. Generic Configuration Register (continued)

OFFSET[1]	BIT[2]	ACRONYM	DEFAULT[3]	DESCRIPTION	
05h	7:3	XCSEL	0Ah	Crystal load-capacitor selection[7]	00h – 0 pF 01h – 1 pF 02h – 2 pF : 14h to 1Fh – 20 pF
	2:0		0b	Reserved – do not write other than 0.	
06h	7:1	BCOUNT	30h	7-bit byte count (defines the number of bytes which will be sent from this device at the next *Block Read* transfer); all bytes must be read out to correctly finish the read cycle.	
	0	EEWRITE	0b	Initiate EEPROM write cycle[8]	0 – No EEPROM write cycle 1 – Start EEPROM write cycle (internal registers are saved to the EEPROM)
07h-0Fh		—	0h	Reserved – do not write other than 0	

(7) The internal load capacitor (C1, C2) must be used to achieve the best clock performance. External capacitors should be used only to finely adjust C_L by a few picofarads. The value of C_L can be programmed with a resolution of 1 pF for a crystal load range of 0 pF to 20 pF. For CL > 20 pF, use additional external capacitors. Also, the value of the device input capacitance has to be considered which always adds 1.5 pF (6 pF/2 pF) to the selected C_L. For more information about VCXO configuration and crystal recommendation, see application report SCAA085.

(8) Note: The EEPROM WRITE bit must be sent last. This ensures that the content of all internal registers are stored in the EEPROM. The EEWRITE cycle is initiated with the rising edge of the EEWRITE bit. A static level-high does not trigger an EEPROM WRITE cycle. The EEWRITE bit must be reset to low after the programming is completed. The programming status can be monitored by reading out EEPIP. If EELOCK is set to high, no EEPROM programming is possible.

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Table 9. PLL1 Configuration Register

OFFSET(1)	BIT(2)	ACRONYM	DEFAULT(3)	DESCRIPTION	
10h	7:0	Reserved	00000000b	Reserved	
11h	7:0	Reserved	00000000b	Reserved	
12h	7:0	Reserved	00000000b	Reserved	
13h	7	FS1_7	0b	FS1_x: PLL1 frequency selection(4)	
	6	FS1_6	0b	0 – f_{VCO1_0} (predefined by PLL1_0 – multiplier/divider value) 1 – f_{VCO1_1} (predefined by PLL1_1 – multiplier/divider value)	
	5	FS1_5	0b		
	4	FS1_4	0b		
	3	FS1_3	0b		
	2	FS1_2	0b		
	1	FS1_1	0b		
	0	FS1_0	0b		
14h	7	MUX1	1b	PLL1 multiplexer:	0 – PLL1 1 – PLL1 bypass (PLL1 is in power down)
	6	M2	1b	Output Y1 multiplexer:	0 – bypass 1 – Pdiv2
	5:4	M3	10b	Output Y2 multiplexer:	00 – bypass 01 – Pdiv2-divider 10 – Pdiv3-divider 11 – Reserved
	3:2	Y1Y2_ST1	11b	Y1, Y2-state0/1definition:	00 – Y1/Y2 disabled to high-impedance state (PLL1 is in power down) 01 – Y1/Y2 disabled to high-impedance state (PLL1 on) 10 – Y1/Y2 disabled to low (PLL1 on) 11 – Y1/Y2 enabled (normal operation, PLL1 on)
	1:0	Y1Y2_ST0	01b		

(1) Writing data beyond 30h may adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used

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Table 9. PLL1 Configuration Register (continued)

OFFSET[1]	BIT[2]	ACRONYM	DEFAULT[3]	DESCRIPTION
15h	7	Y1Y2_7	0b	Y1Y2_x output state selection[4] 0 – state0 (predefined by Y1Y2_ST0) 1 – state1 (predefined by Y1Y2_ST1)
	6	Y1Y2_6	0b	
	5	Y1Y2_5	0b	
	4	Y1Y2_4	0b	
	3	Y1Y2_3	0b	
	2	Y1Y2_2	0b	
	1	Y1Y2_1	1b	
	0	Y1Y2_0	0b	
16h	7	Reserved	0b	RSVD Reserved
	6:0	Pdiv2	01h	7-bit Y1-output-divider Pdiv2: 0 – Reset and in standby 1 to 127 – Divider value
17h	7	—	0b	Reserved – do not write others than 0
	6:0	Pdiv3	01h	7-bit Y2-output-divider Pdiv3: 0 – Reset and in standby 1 to 127 – Divider value
18h	7:0	PLL1_0N [11:4	004h	PLL1_0[4]: 30-bit multiplier/divider value for frequency f_{VCO1_0} (for more information, see the *PLL Multiplier/Divider Definition* paragraph).
19h	7:4	PLL1_0N [3:0]		
	3:0	PLL1_0R [8:5]	000h	
1Ah	7:3	PLL1_0R[4:0]		
	2:0	PLL1_0Q [5:3]	10h	
1Bh	7:5	PLL1_0Q [2:0]		
	4:2	PLL1_0P [2:0]	010b	
	1:0	VCO1_0_RANGE	00b	f_{VCO1_0} range selection: 00 – f_{VCO1_0} < 125 MHz 01 – 125 MHz ≤ f_{VCO1_0} < 150 MHz 10 – 150 MHz ≤ f_{VCO1_0} < 175 MHz 11 – f_{VCO1_0} ≥ 175 MHz
1Ch	7:0	PLL1_1N [11:4]	004h	PLL1_1[4]: 30-bit multiplier/divider value for frequency f_{VCO1_1} (for more information see the *PLL Multiplier/Divider Definition* paragraph)
1Dh	7:4	PLL1_1N [3:0]		
	3:0	PLL1_1R [8:5]	000h	
1Eh	7:3	PLL1_1R[4:0]		
	2:0	PLL1_1Q [5:3]	10h	
1Fh	7:5	PLL1_1Q [2:0]		
	4:2	PLL1_1P [2:0]	010b	
	1:0	VCO1_1_RANGE	00b	f_{VCO1_1} range selection: 00 – f_{VCO1_1} < 125 MHz 01 – 125 MHz ≤ f_{VCO1_1} < 150 MHz 10 – 150 MHz ≤ f_{VCO1_1} < 175 MHz 11 – f_{VCO1_1} ≥ 175 MHz

(4) PLL settings limits: $16 \le q \le 63$, $0 \le p \le 7$, $0 \le r \le 511$, $0 < N < 4096$

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Table 10. PLL2 Configuration Register

OFFSET[1]	BIT[2]	ACRONYM	DEFAULT[3]	DESCRIPTION	
20h	7:0	Reserved	0000000b	Reserved	
21h	7:0	Reserved	0000000b	Reserved	
22h	7:0	Reserved	0000000b	Reserved	
23h	7	FS2_7	0b	FS2_x: PLL2 frequency selection[4] 0 – f_{VCO2_0} (predefined by PLL2_0 – multiplier/divider value) 1 – f_{VCO2_1} (predefined by PLL2_1 – multiplier/divider value)	
	6	FS2_6	0b		
	5	FS2_5	0b		
	4	FS2_4	0b		
	3	FS2_3	0b		
	2	FS2_2	0b		
	1	FS2_1	0b		
	0	FS2_0	0b		
24h	7	MUX2	1b	PLL2 multiplexer:	0 – PLL2 1 – PLL2 bypass (PLL2 is in power down)
	6	M4	1b	Output Y3 multiplexer:	0 – Pdiv2 1 – Pdiv4
	5:4	M5	10b	Output Y4 multiplexer:	00 – Pdiv2-divider 01 – Pdiv4-divider 10 – Pdiv5-divider 11 – Reserved
	3:2	Y3Y4_ST1	11b	Y3, Y4-State0/1definition:	00 – Y3/Y4 disabled to high-impedance state (PLL2 is in power down) 01 – Y3/Y4 disabled to high-impedance state (PLL2 on) 10–Y3/Y4 disabled to low (PLL2 on) 11 – Y3/Y4 enabled (normal operation, PLL2 on)
	1:0	Y3Y4_ST0	01b		

(1) Writing data beyond 30h may adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used

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Table 10. PLL2 Configuration Register (continued)

OFFSET[1]	BIT[2]	ACRONYM	DEFAULT[3]	DESCRIPTION
25h	7	Y3Y4_7	0b	Y3Y4_x output state selection[4] 0 – state0 (predefined by Y3Y4_ST0) 1 – state1 (predefined by Y3Y4_ST1)
	6	Y3Y4_6	0b	
	5	Y3Y4_5	0b	
	4	Y3Y4_4	0b	
	3	Y3Y4_3	0b	
	2	Y3Y4_2	0b	
	1	Y3Y4_1	1b	
	0	Y3Y4_0	0b	
26h	7	Reserved	0b	Reserved 0 – Down 1 – Center
	6:0	Pdiv4	01h	7-Bit Y3-output-divider Pdiv4: 0 – Reset and in standby 1 to 127 – Divider value
27h	7	—	0b	Reserved – do not write others than 0
	6:0	Pdiv5	01h	7-bit Y4-output-divider Pdiv5: 0 – Reset and in standby 1 to 127 – Divider value
28h	7:0	PLL2_0N [11:4	004h	PLL2_0[4]: 30-Bit Multiplier/Divider value for frequency f_{VCO2_0} (for more information see the *PLL Multiplier/Divider Definition* paragraph)
29h	7:4	PLL2_0N [3:0]		
	3:0	PLL2_0R [8:5]	000h	
2Ah	7:3	PLL2_0R[4:0]		
	2:0	PLL2_0Q [5:3]	10h	
2Bh	7:5	PLL2_0Q [2:0]		
	4:2	PLL2_0P [2:0]	010b	
	1:0	VCO2_0_RANGE	00b	f_{VCO2_0} range selection: 00 – f_{VCO2_0} < 125 MHz 01 – 125 MHz ≤ f_{VCO2_0} < 150 MHz 10 – 150 MHz ≤ f_{VCO2_0} < 175 MHz 11 – f_{VCO2_0} ≥ 175 MHz
2Ch	7:0	PLL2_1N [11:4]	004h	PLL2_1[4]: 30-bit multiplier/divider value for frequency f_{VCO2_1} (for more information see the *PLL Multiplier/Divider Definition* paragraph)
2Dh	7:4	PLL2_1N [3:0]		
	3:0	PLL2_1R [8:5]	000h	
2Eh	7:3	PLL2_1R[4:0]		
	2:0	PLL2_1Q [5:3]	10h	
2Fh	7:5	PLL2_1Q [2:0]		
	4:2	PLL2_1P [2:0]	010b	
	1:0	VCO2_1_RANGE	00b	f_{VCO2_1} range selection: 00 – f_{VCO2_1} < 125 MHz 01 – 125 MHz ≤ f_{VCO2_1} < 150 MHz 10 – 150 MHz ≤ f_{VCO2_1} < 175 MHz 11 – f_{VCO2_1} ≥ 175 MHz

(4) PLL settings limits: 16 ≤ q ≤ 63, 0 ≤ p ≤ 7, 0 ≤ r ≤ 511, 0 < N < 4096

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

CDCEL824 is an easy to use low-cost, programmable CMOS clock synthesizer. it can be used as a crystal buffer, clock synthesizer with separate output supply pin. CDCEL824 features on-chip loop filter. Programming can be done through SPI, pin-mode, or using on-chip EEPROM. This section shows some examples of using CDCEL824 in various applications.

10.2 Typical Application

CDCEL824 is ideal clock generator for medium-range phase-shift laser distance meter. Having two separate PLLs allows for achieving as low intermediate frequency as required as well as high maximum modulation frequency, hence increasing the accuracy of the measurement device. Moreover, a fast settling PLL supports faster switching between multiple modulation frequencies required by a single measurement. this results in higher measurement rates for the device. Low power consumption and low cost position CDCEL824 as an ideal device for commercial laser distance metering equipment.

Figure 13 shows a typical application concept for the CDCEL824, where the outputs of the PLL1, Y1 and Y2 are used to generate the modulation and the counter frequency respectively. Y3 coming out of the PLL2 is carrying the shifted modulation frequency for down mixing. all three frequencies are programmable and dynamically switchable.

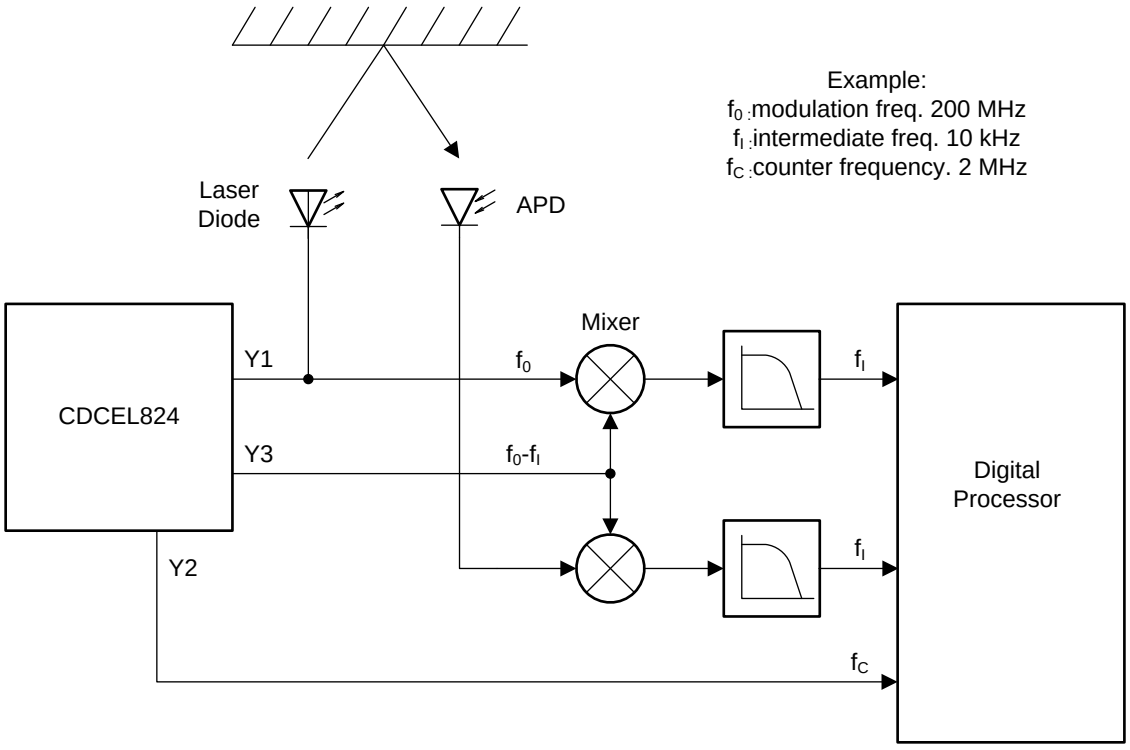


Figure 13. Heterodyne Phase-Shift Laser Distance Meter Concept

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Typical Application (continued)

10.2.1 Design Requirements

For Laser distance meter applications, if heterodyne technique is used as mentioned in *Typical Application* , it is shown that:

Maximum Measurement Range equals: $$R = \frac{c}{2f_o} \quad (1)$$

And best error achievable in measurement: $$\Delta d = \frac{c}{2} \frac{f_I}{f_o} \frac{1}{f_c} \quad (2)$$

That means lower RF frequency allows for longer range, while lower ratio $\frac{f_I}{f_o}$ (higher RF frequency and lower IF frequency) gives lower error.

The values of intermediate, RF, and counter frequency should be chosen according to design targets of the maximum range and maximum tolerable error. Typically multiple consecutive measurements with multiple RF frequencies are carried on to resolve the trade-off between the accuracy and the maximum range.

10.2.2 Detailed Design Procedure

10.2.2.1 PLL Multiplier/Divider Definition

At a given input frequency (f_{IN}), the output frequency (f_{OUT}) of the CDCEL824 can be calculated:

$$f_{OUT} = \frac{f_{IN}}{Pdiv} \times \frac{N}{M} \quad (3)$$

where

- M (1 to 511) and N (1 to 4095) are the multiplier/divide values of the PLL
- Pdiv (1 to 127) is the output divider.

The target VCO frequency (f_{VCO}) of each PLL can be calculated:

$$f_{VCO} = f_{IN} \times \frac{N}{M} \quad (4)$$

The PLL internally operates as fractional divider and needs the following multiplier/divider settings:

$$NP = 4 - \text{int}\left(\log_2 \frac{N}{M}\right) \text{ [if } P < 0 \text{ then } P = 0] \qquad Q = \text{int}\left(\frac{N'}{M}\right) \qquad R = N' - M \times Q$$

where

$N' = N \times 2^P$
$N \geq M$
$80\ MHz \leq f_{VCO} \leq 200\ MHz$
$16 \leq q \leq 63$
$0 \leq p \leq 4$
$0 \leq r \leq 511$

Example:

for f_{IN} = 27 MHz; M = 1; N = 4; Pdiv = 2;

→ f_{OUT} = 54 MHz
→ f_{VCO} = 108 MHz
→ P = 4 – int($\log_2$4) = 4 – 2 = 2
→ N″ = 4 × 2^2 = 16
→ Q = int(16) = 16
→ R = 16 – 16 = 0

for f_{IN} = 27 MHz; M = 2; N = 11; Pdiv = 2;

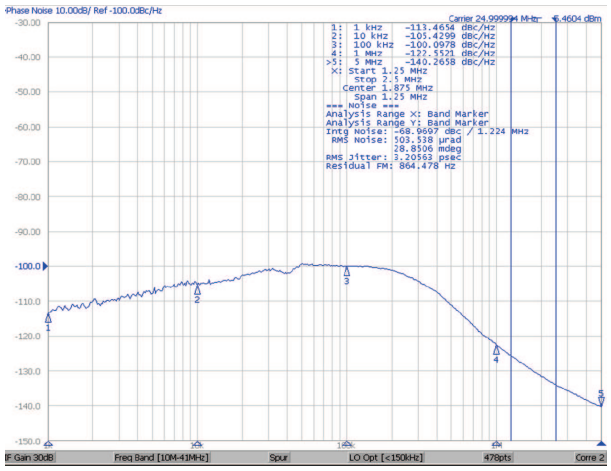
→ f_{OUT} = 74.25 MHz
→ f_{VCO} = 148.50 MHz
→ P = 4 – int($\log_2$5.5) = 4 – 2 = 2
→ N″ = 11 × 2^2 = 44
→ Q = int(22) = 22
→ R = 44 – 44 = 0

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Typical Application (continued)

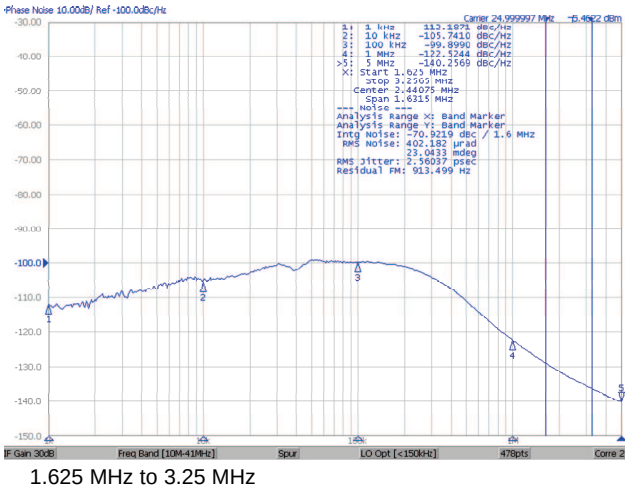
The values for P, Q, R, and N' are automatically calculated when using TI Pro-Clock™ software.

10.2.3 Application Curves



1.5 MHz to 2.5 MHz

Figure 14. Phase Noise and RMS Jitter



1.625 MHz to 3.25 MHz

Figure 15. Phase Noise and RMS Jitter

11 Power Supply Recommendations

There is no restriction on the power-up sequence. In case VDDOUT is applied first, it is recommended to ground VDD. In case VDDOUT is powered while VDD is floating, there is a risk of high current flowing on the VDDOUT.

The device has a power-up control that is connected to the 1.8-V supply. This keeps the whole device disabled until the 1.8-V supply reaches a sufficient voltage level. Then the device switches on all internal components, including the outputs. If there is a VDDOUT available before the V_{DD} supply, the outputs will stay disabled until the VDD supply has reached a certain level.

12 Layout

12.1 Layout Guidelines

When the CDCEL824 is used as a crystal buffer, any parasitics across the crystal affects the pulling range of the VCXO. Therefore, care must be taken in placing the crystal units on the board. Crystals should be placed as close to the device as possible, ensuring that the routing lines from the crystal terminals to X_{IN} and X_{OUT} have the same length.

If possible, cut out both ground plane and power plane under the area where the crystal and the routing to the device are placed. In this area, always avoid routing any other signal line, as it could be a source of noise coupling.

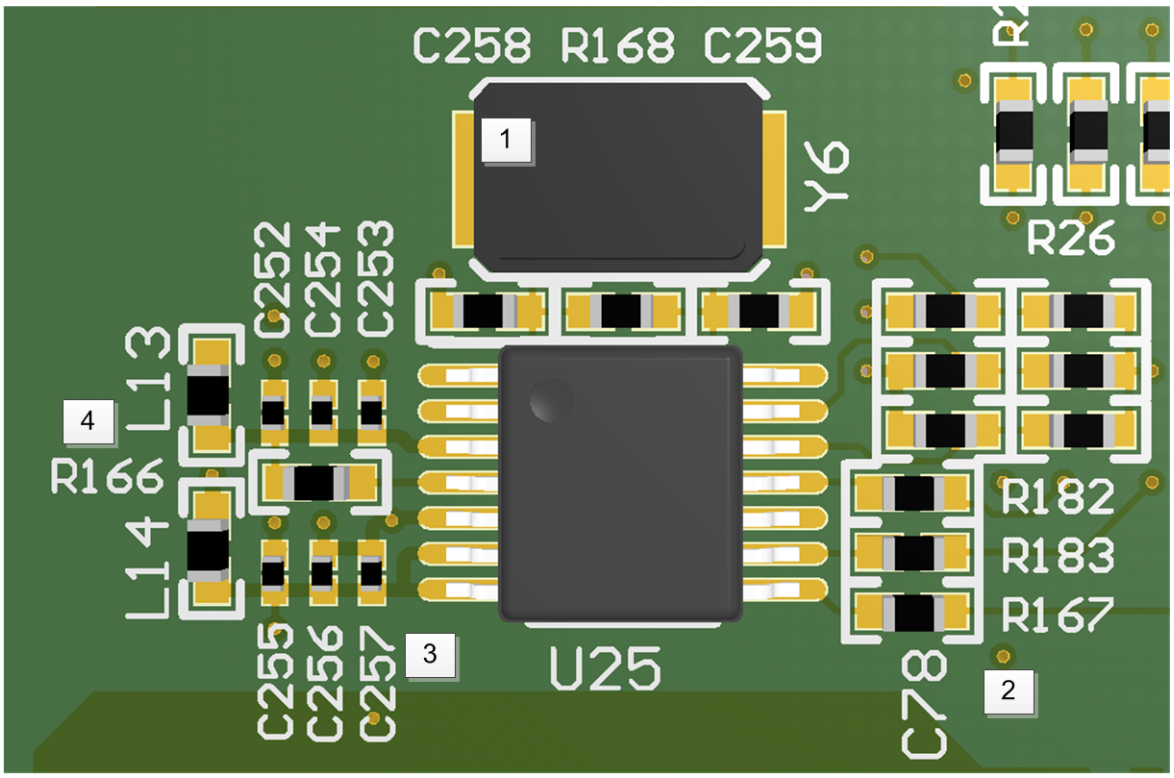
Additional discrete capacitors can be required to meet the load capacitance specification of certain crystal. For example, a 10.7-pF load capacitor is not fully programmable on the chip, because the internal capacitor can range from 0 pF to 20 pF with steps of 1 pF. The 0.7-pF capacitor therefore can be discretely added on top of an internal 10 pF.

To minimize the inductive influence of the trace, it is recommended to place this small capacitor as close to the device as possible and symmetrically with respect to XIN and XOUT.

Figure 16 shows a conceptual layout detailing recommended placement of power supply bypass capacitors. For component side mounting, use 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

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12.2 Layout Example



1 Place crystal with associated load caps as close to the chip	2 Place series termination resistors at Clock outputs to improve signal integrity
3 Place bypass caps close to the device pins, ensure wide freq. range	4 Use ferrite beads to isolate the device supply pins from board noise sources

Figure 16. Board Layout

13 Device and Documentation Support

13.1 Documentation Support

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

Pro-Clock, E2E are trademarks of Texas Instruments.

13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCEL824PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKEL824	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

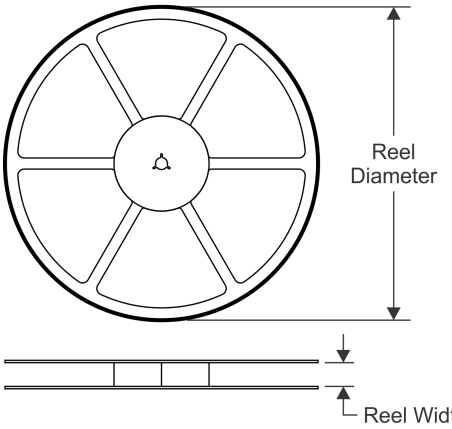
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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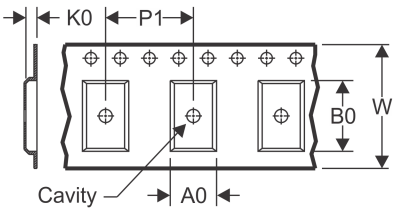
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

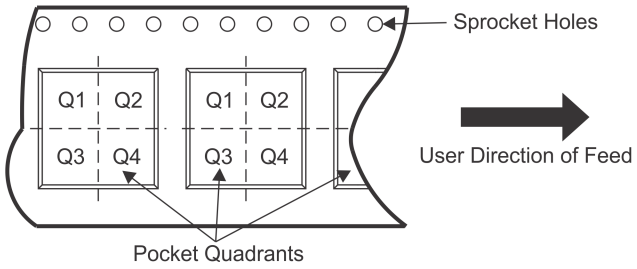


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

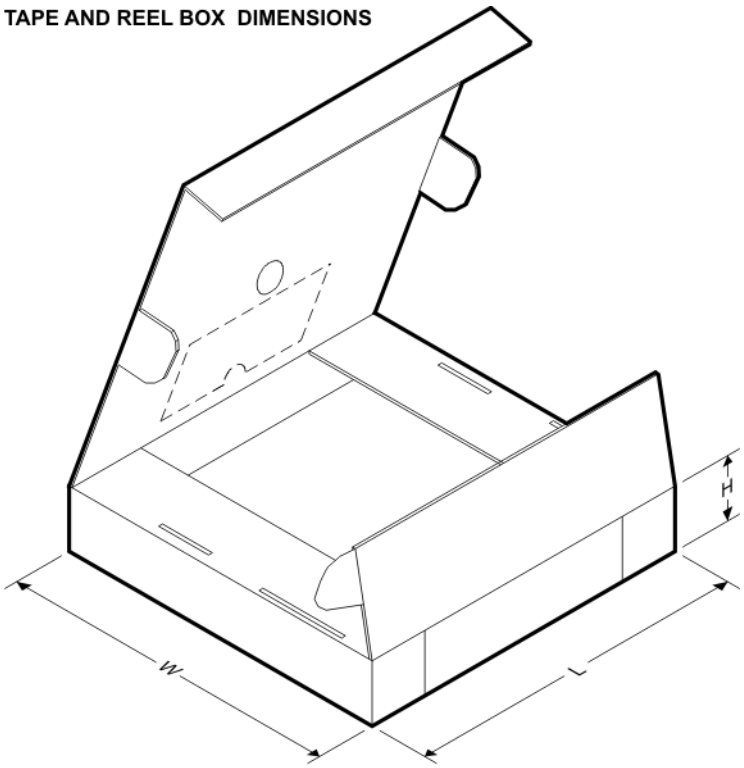
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCEL824PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

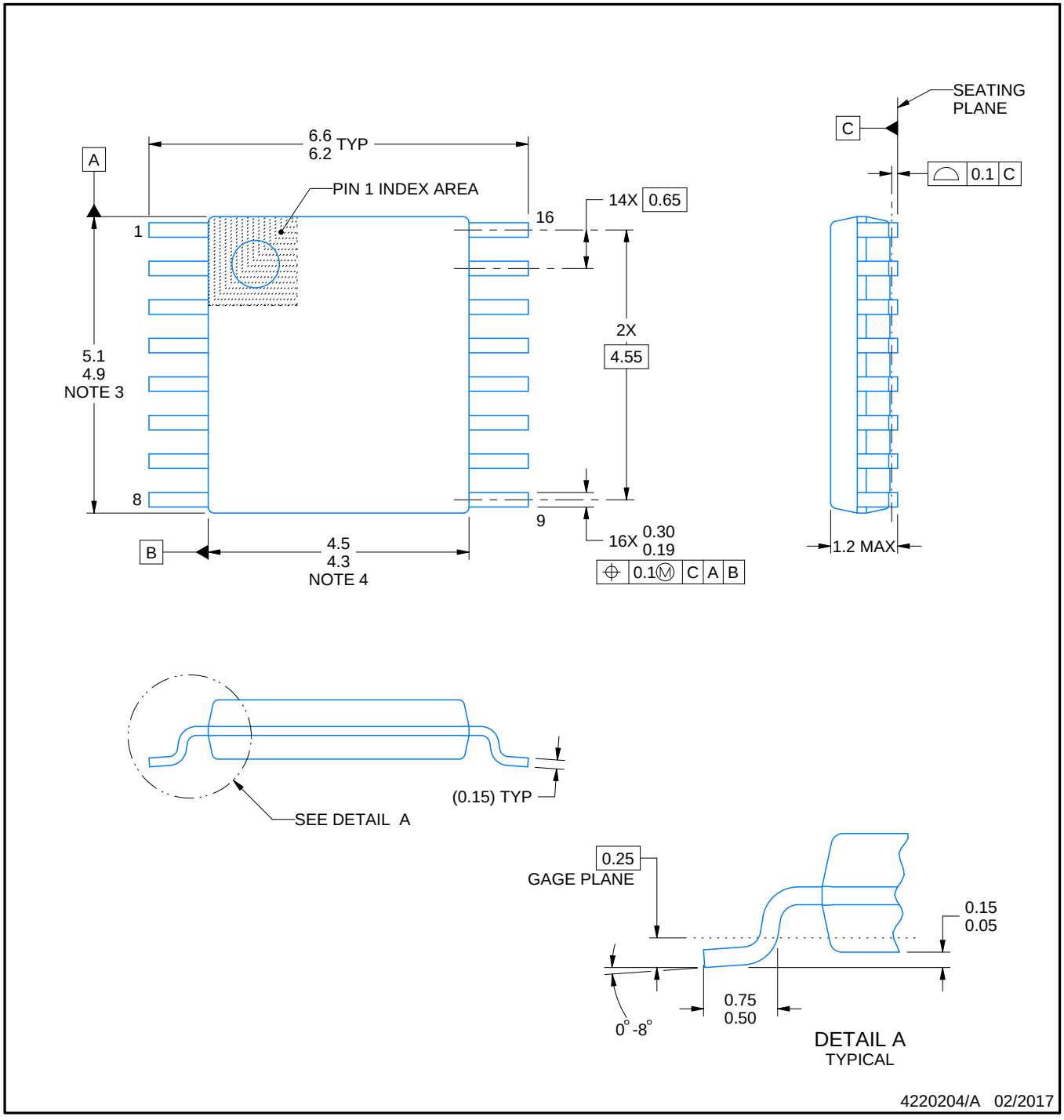
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCEL824PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

PACKAGE OUTLINE

PW0016A

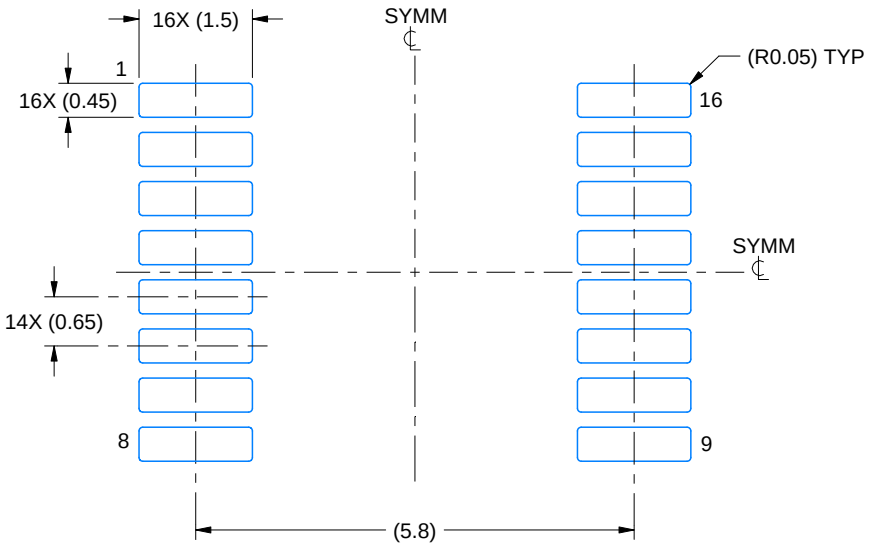
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

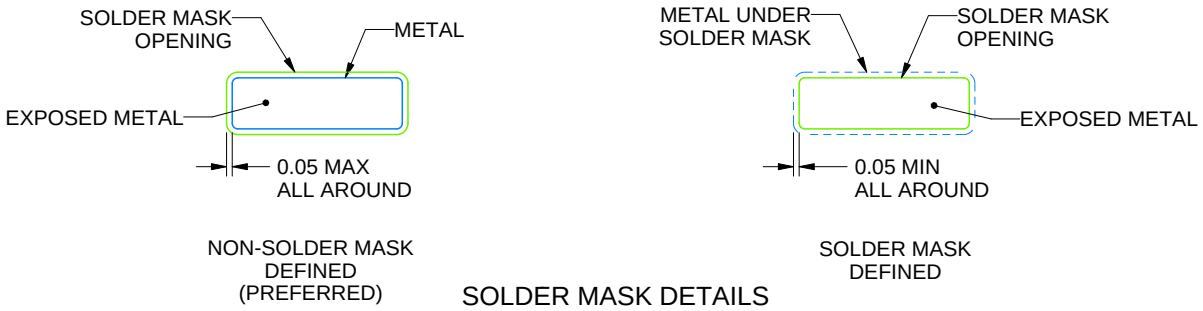


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

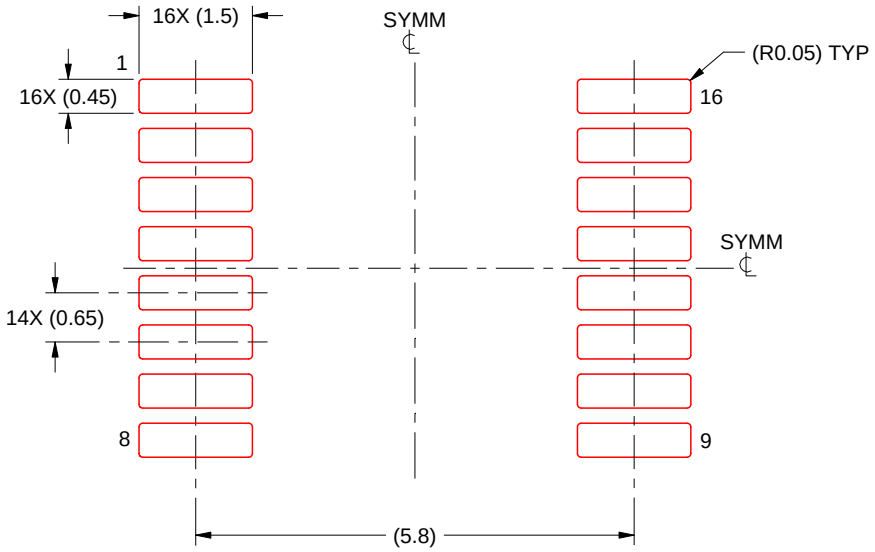


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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