LC75056PE

ON Semiconductor®

www.onsemi.com

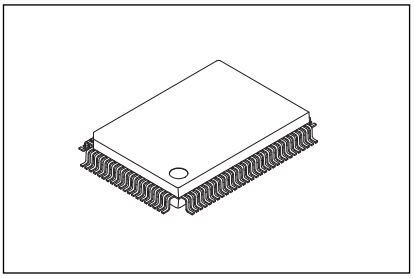
CMOS LSI

Car Audio DSP with Bongiovi DPS

Overview

LC75056PE is a Digital Sound Processor which integrates audio signal processor, A/D, D/A, and volume into a single chip which are the prerequisites for car audio DSP.
Programs are downloaded from internal Flash ROM into DSP RAM.

(Caution)
On-board programming to the Flash ROM of LC75056PE is not available.
(Data is programmable only before delivery by Our company.)



PQFP100 14x20 / QIP100E

Hardware overview specification

Parameter	Note
Analog input (stereo)	Balanced x2, Single x1 or Balanced x1, Single x3
Analog input (monaural)	Balanced x2, Single x1 or Balanced x1, Single x3
ADC 24bit	2 stereo ch, 2 monaural ch
DAC 24bit + EVR	3 stereo ch
Digital input (IIS)	Maximum 5 stereo ch (slave)
Digital output (IIS)	Maximum 4 stereo ch (master) Input through output 1 stereo ch
Sampling rate converter (SRC)	Maximum 4 stereo ch (3 or 4 ch Synchronous input)
Main microcontroller serial interface	Serial interface (I^2C or SPI)
DSP (24bit)	220MIPS (DSP 2 Core: operation at 110MHz)

Supply voltage

- Logic (DSP) : 1.5V
- PLL circuit : 3.3V
- Crystal oscillation, digital I/O power supply : 3.3V
- CODEC analog power supply : 3.3V

* I^2C Bus is a trademark of Philips Corporation.

* This product is licensed from Bongiovi Acoustics, Inc. and Silicon Storage Technology, Inc. (USA).

ORDERING INFORMATION
See detailed ordering and shipping information on page 28 of this data sheet.

© Semiconductor Components Industries, LLC, 2015

Specifications

Absolute Maximum Ratings at Ta = 25°C, DV_{SS}_1 to 3 = $COAV_{SS}$1 to 6 =AVB = XV_{SS} = $AVCOV_{SS}$ = 0V

Parameter	Symbol	Applicable pins	Ratings	Unit
Maximum supply voltage	V_{DD} max1	CODEC power supply pin	–0.3 to +3.9	V
	V_{DD} max2	Power supply pin for oscillation circuit	–0.3 to +3.9	V
		Digital 3.3V power supply pin	–0.3 to +3.9	V
	V_{DD} max3	Logic (DSP)	–0.3 to +1.8	V
Maximum input voltage	V_{IN}1	CODEC Analog input pin	–0.3 to V_{DD} max1 +0.3	V
	V_{IN}2	Oscillation circuit input pin, TEST setting input pin	–0.3 to V_{DD} max2 +0.3	V
	V_{IN}3	Digital input pin	–0.3 to +6.0	V
Maximum output current	I_O	All output pin	6.0	mA
Allowable power dissipation	Pd max	Ta = 85°C (Note 1)	900	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

Note 1: For a chip mounted on a reference board. (board size: 105 × 75 × 1.6mm 4-layer)

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Range at Ta = –40 to 85°C, DV_{SS}_1 to 3 = $COAV_{SS}$1 to 6 =AVB = XV_{SS} = $AVCOV_{SS}$ = 0V

Parameter	Symbol	Applicable pins	min	typ	max	Unit
Supply voltage CODEC ANALOG	AV_{DD}	CODEC power supply pin	3.14	3.3	3.47	V
Supply voltage XTAL, DSP_IO	DV_{DD}33	Power supply pin for oscillation circuit Digital 3.3V power supply pin	3.14	3.3	3.47	V
Supply voltage PLL	$AVCOV_{DD}$	Power supply pin for PLL	3.14	3.3	3.47	V
Supply voltage Logic	DV_{DD}	Power supply pin for Logic	1.43	1.5	1.58	V
Input high level voltage	V_{IH}1	All digital input pin except for XIN	2.0		5.5 *1	V
Input high level voltage	V_{IH}2	XIN	2.0		DV_{DD}33	V
Input low level voltage	V_{IL}1	All digital input pin	0		0.8	V
Crystal oscillation frequency (256fs)	Fosc	XIN, XOUT (fs = 44.1kHz) *2		11.2896		MHz

*1) Only when power is supplied to all the power supplies, you can supply power to input pin up to 5.5V.
When the power is turned off, only supply the power up to 3.6V.

*2) Crystal for oscillator CI value: CI ≤ 150Ω
The evaluation by the crystal supplier is recommended.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC Electrical Characteristics at Ta = –40 to 85°C, DV_{SS}_1 to 3 = $COAV_{SS}$1 to 6 =AVB = XV_{SS} = $AVCOV_{SS}$ = 0V

Parameter	Symbol	Conditions and applicable pin	min	typ	max	Unit
Input high level current	I_{IH}	All digital input pin			10	μA
Input low level current	I_{IL}	All digital input pin	–10			μA
Output high level voltage	V_{OH}	I_{OH} = –2mA: Digital output pin except for DSPIO4, SDAS	2.4			V
		I_{OH} = –4mA: DSPIO4, SDAS	2.4			V
Output low level voltage	V_{OL}	I_{OL} = 2mA: Digital output pin except for DSPIO4, SDAS			0.4	V
		I_{OL} = 4mA: DSPIO4, SDAS			0.4	V
Output OFF leak current	IOFF	Unloaded: All digital output pin	–10		10	μA
Crystal oscillator feedback resistance	Rf	XIN, XOUT		1.0		MΩ
CODEC reference voltage	VREF	ADC_REF, ADC_REF		0.5×AV_{DD}		V
Power supply current	I_{DD}A33	$COAV_{DD}$1, 2, 3, 4, 5, 6 $AVCOAV_{DD}$		110	157	mA
	I_{DD}D33	DV_{DD}33, XV_{DD}		10	12.5	mA
	I_{DD}D15	DV_{DD}_1, 2		120	173	mA

AC Electrical Characteristics

at AV_{DD} = DV_{DD}33 = $AVCOV_{DD}$ = 3.3V, DV_{SS}_1 to 3 = $COAV_{SS}$1 to 6 =AVB = XV_{SS} = $AVCOV_{SS}$ = 0V
Ta = 25°C, fs = 44.1kHz, signal frequency 1kHz, measurement band = 10Hz to 20kHz

Parameter	Symbol	Conditions and applicable pin	min	typ	max	Unit
(Input selector + ADC)						
Full-scale analog input level					0.85×AV_{DD}	Vp-p
Analog block input impedance			20	30		kΩ
Gain setting level			–12		+19	dB
Gain setting step				1		dB
Error between gain setting steps			–0.5		+0.5	dB
S/N		w/ A-weighted	90	95		dB
		w/o A-weighted	87	92		dB
Dynamic range		w/ A-weighted	90	95		dB
		w/o A-weighted	87	92		dB
THD+N		Input condition: –3dBFS		–90	–80	dB
Cross talk 1		Input condition: –3dBFS, 1kHz Cross talk between AUX Lch and Rch when AUX differential input is used.		–75	–65	dB
Cross talk 2		Input condition: –3dBFS, 1kHz Other than cross talk1		–90	–80	dB
(ADC digital filter)						
Pass band frequency			0		0.4535	fs
Stop band frequency			0.5465			fs
Pass band ripple					±0.04	dB
Stop band attenuation			–69			dB
HPF cutoff frequency DC for offset cancellation		fs: 44.1kHz		0.86		Hz
(Audio DAC)						
Full-scale analog output level					0.85×AV_{DD}	Vp-p
S/N		w/ A-weighted	94	100		dB
		w/o A-weighted	91	97		dB
Dynamic range		w/ A-weighted	94	100		dB
		w/o A-weighted	91	97		dB
THD+N		–3dBFS		–91	–80	dB
Cross talk		Input condition: full-scale, 1kHz		–100	–85	dB
Mute level		w/ A-weighted	94	100		dB

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Conditions and applicable pin	min	typ	max	Unit
(ADC digital filter)						
Pass band frequency			0		0.4535	fs
Stop band frequency			0.5465			fs
Pass band ripple					±0.015	dB
Stop band attenuation			−62			dB
HPF cutoff frequency for DC offset cancellation		fs: 44.1kHz		1.7		Hz
(EVR)						
Input impedance	ZEVRI		20	25		kΩ
Volume setting range			−70		0	dB
Mute level			85	95		dB
Volume step				1		dB
Volume setting step error			−0.5		0.5	dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1.5V reference level characteristics

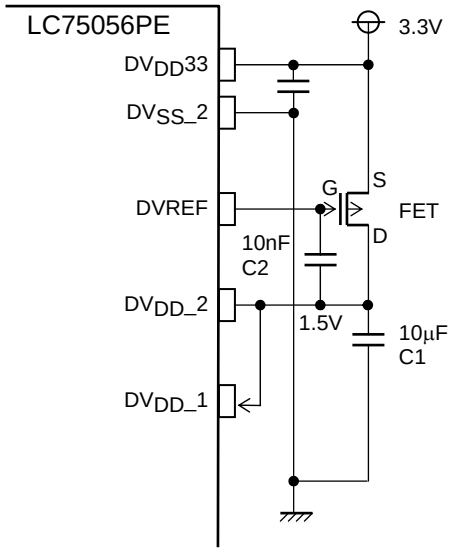
at Ta = –40 to 85°C, $DV_{DD}33$ = 3.3V, DV_{SS}_1 to 3 = $COAV_{SS}1$ to 6 =AVB = XV_{SS} = $AVCOV_{SS}$ = 0V

Parameter	Symbol	Condition	min	typ	max	Unit
FET Control Output voltage	DVREF	$DV_{DD}33$ = 3.3V	0		3.3	V

<Addition>

- 1.5V reference level circuit is a circuit that prepared 1.5V power-supply voltage needed in this LSI to be easily generable. The power supply of 1.5V is enabled by using recommendation FET shown in Figure 5-1.

<Figure 5-1> 1.5V reference level circuit peripheral block



* FET Recommended Device No.
NTR2101P (ON Semiconductor)

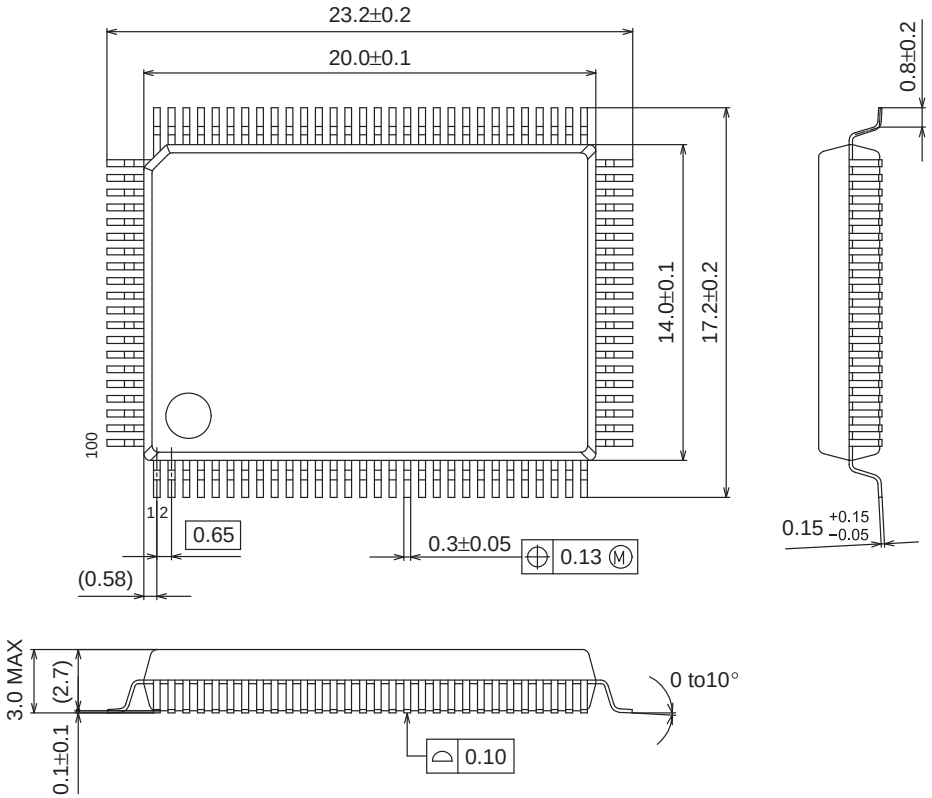
* C1 is the capacitor to prevent oscillation.
In the range of operating temperature, make sure to maintain low ESR and the capacitance recommended value is 10μF because oscillation may occur when the capacitance value changes due to the change of temperature.

- As for power supply ON, the order of $DV_{DD}33$ power supply voltage (3.3V) to FET source supply voltage (3.3V) is recommended.

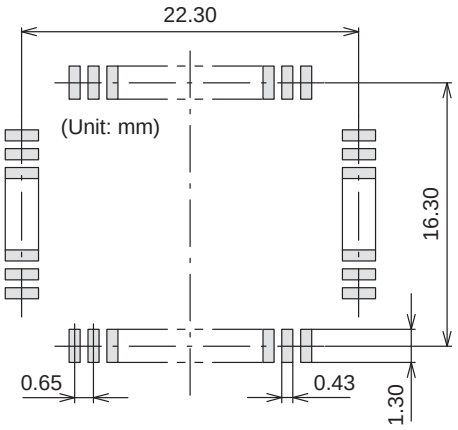
Package Dimensions

unit : mm

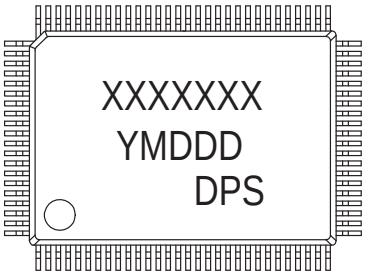
PQFP100 14x20 / QIP100E
CASE 122BV



SOLDERING FOOTPRINT*



MARKING DIAGRAM

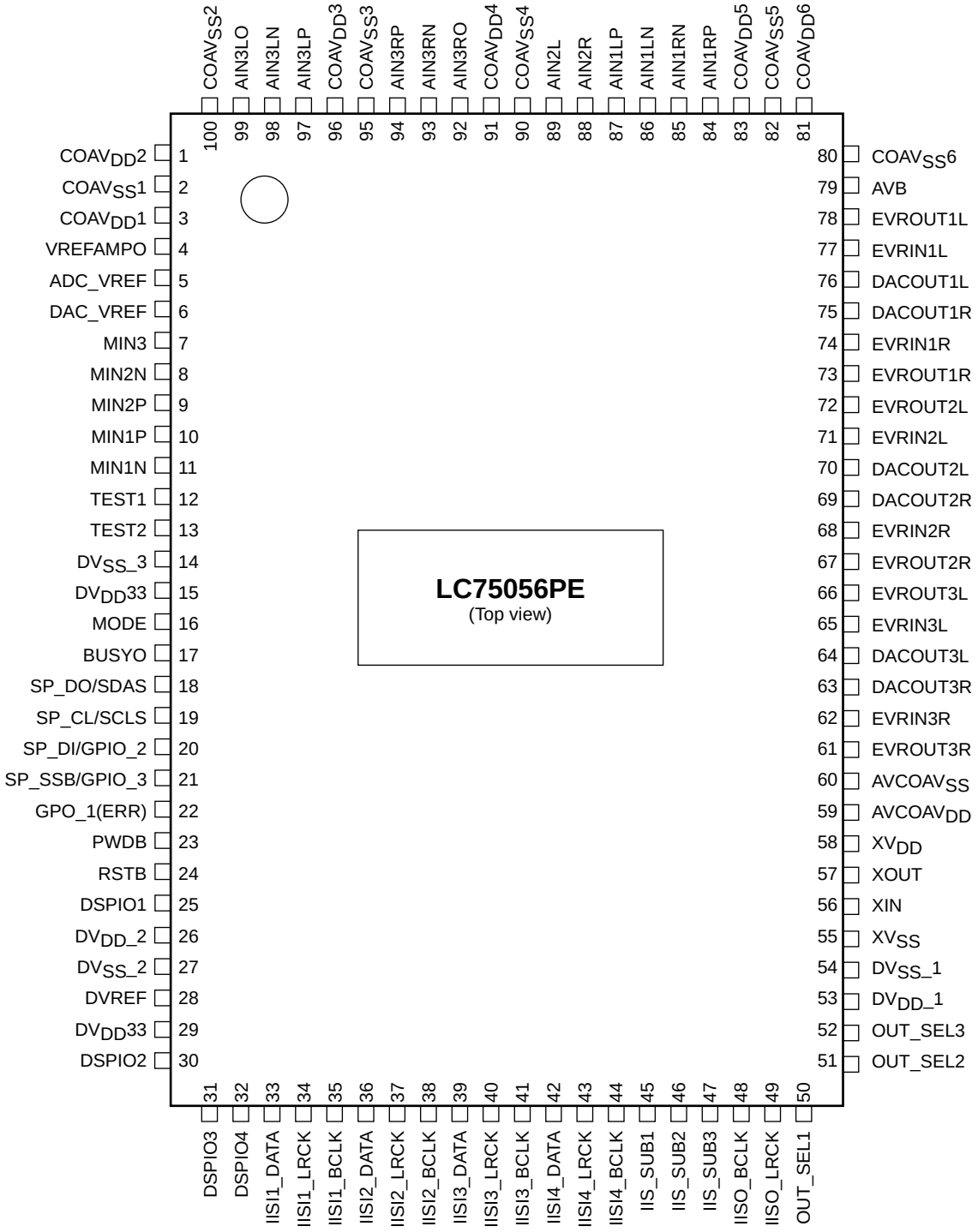


XXXXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data
DPS = Digital Power Station (DPS)

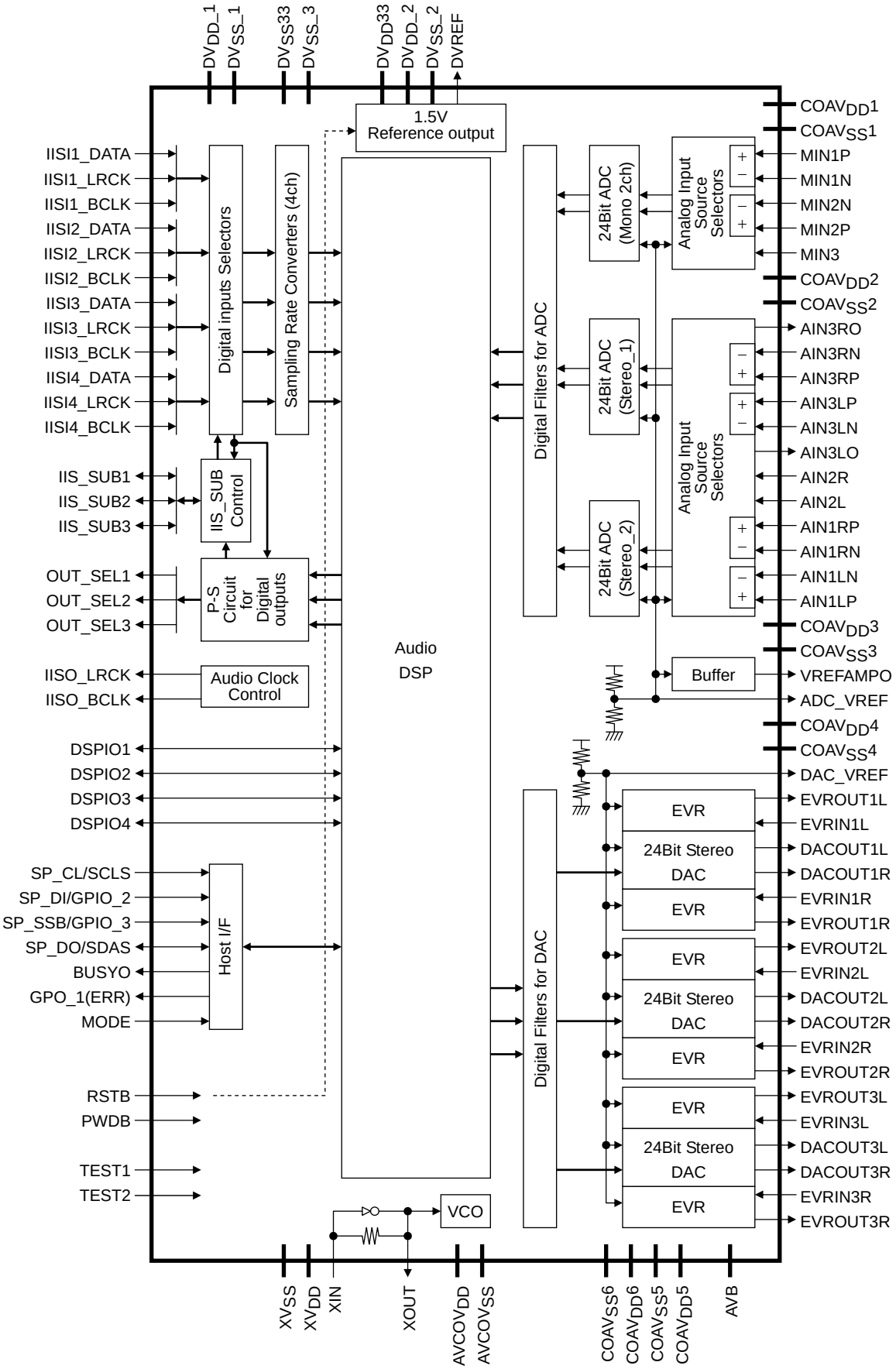
NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pin Assignment



Block Diagram



Pin functions

No	Pin name	Input/output	Input/output (RSTB=L)	Functions
1	$COAV_{DD}2$			Power supply for CODEC analog (3.3V)
2	$COAV_{SS}1$			Power supply for CODEC analog (GND)
3	$COAV_{DD}1$			Power supply for CODEC analog (3.3V)
4	VREFAMPO	AO	AO	Reference voltage buffer output pin, used as external reference voltage
5	ADC_VREF	AO	AO	Reference voltage output pin for CODEC ADC A coupling capacitor is required between this pin and GND.
6	DAC_VREF	AO	AO	Reference voltage output pin for CODEC DAC A coupling capacitor is required between this pin and GND.
7	MNI3	AI	AI	Analog single-end input pin for monaural3 When this pin is unused, connect it to GND via capacitor.
8	MNI2N	AI	AI	Negative analog input pin for monaural 2 or Analog single-end input pin for monaural 5. When this pin is unused, connect it to GND via capacitor.
9	MNI2P	AI	AI	Positive analog input pin for monaural 2 or Analog single-end input pin for monaural 4. When this pin is unused, connect it to GND via capacitor.
10	MNI1P	AI	AI	Positive analog input pin for monaural 1 When this pin is unused, connect it to GND via capacitor.
11	MNI1N	AI	AI	Negative analog input pin for monaural 1 When this pin is unused, connect it to GND via capacitor.
12	TEST1	I	I	Test mode setting input pin1. Normally connected to GND
13	TEST2	I	I	Test mode setting input pin2. Normally connected to GND
14	DV_{SS}_3			Power supply for digital (GND)
15	$DV_{DD}33$			Power supply for digital (3.3V)
16	MODE	I		Select pin for serial communication mode (“0”: I^2C, “1”: SPI)
17	BUSYO	O	O (H)	System busy signal output pin for HOST CPU communication (High level: the system is busy)
18	SP_DO/SDAS	I/O	I	Data output pin for SPI (slave) communication or data input/ output pin for IIC (Slave) communication
19	SP_CL/SCLS	I	I	Clock input pin for data transfer for SPI (slave) communication or data transfer clock input pin for IIC (Slave) communication
20	SP_DI/GPIO_2	I/O	I	Data input pin for SPI (slave) communication or General-purpose input/output pin2 for Audio DSP
21	SP_SSB/GPIO_3	I/O	I	Enable signal input pin for SPI (slave) communication (Active: low level) or General-purpose input/output pin3 for audio DSP
22	GPO_1 (ERR)	O	O(L)	General-purpose output pin 1 for integrated DSP (will be designed to correspond to communication error signal output)
23	PWDB	I	I	Power-down mode setting pin. Normally high level.
24	RSTB	I	I	System reset pin. Make sure to set to low level when turning on power.
25	DSPIO1	I/O	I	Audio DSP general input/output pin 1
26	DV_{DD}_2			Power supply for internal logic (1.5V)
27	DV_{SS}_2			Power supply for digital (GND)
28	DVREF	O		Control output pin for 1.5V level
29	$DV_{DD}33$			Power supply for digital (3.3V)
30	DSPIO2	I/O	I	Audio DSP general-purpose input/output pin2
31	DSPIO3	I/O	I	Audio DSP general-purpose input/output pin3
32	DSPIO4	I/O	I	Audio DSP general-purpose input/output pin4 or 256fs_clock out pin.
33	IISI1_DATA	I	I	IIS data input pin1
34	IISI1_LRCK	I	I	IIS word clock input pin1
35	IISI1_BCLK	I	I	IIS bit clock input pin1
36	IISI2_DATA	I	I	IIS data input pin2
37	IISI2_LRCK	I	I	IIS word clock input pin2
38	IISI2_BCLK	I	I	IIS bit clock input pin2
39	IISI3_DATA	I	I	IIS data input pin3
40	IISI3_LRCK	I	I	IIS word clock input pin3
41	IISI3_BCLK	I	I	IIS bit clock input pin3
42	IISI4_DATA	I	I	IIS data input pin4

Continued on next page.

Continued from preceding page.

No	Pin name	Input/output	Input/output (RSTB=L)	Functions
43	IISI4_LRCK	I	I	IIS word clock input pin4
44	IISI4_BCLK	I	I	IIS bit clock input pin4
45	IIS_SUB1	I/O	I	IIS data input pin5 or IIS data output pin1 or IIS data output pin4
46	IIS_SUB2	I/O	I	IIS data input pin6 or IIS word clock input pin5 or IIS data output pin2 or IIS word clock output pin4
47	IIS_SUB3	I/O	I	IIS data input pin7 or IIS bit clock input pin5 or IIS data output pin3 or IIS bit clock output pin4
48	IISO_BCLK	O	O (L)	IIS bit clock output pin (for IIS data output 1 to 3)
49	IISO_LRCK	O	O (L)	IIS word clock output pin (for IIS data output 1 to 3)
50	OUT_SEL1	O	O (L)	IIS data output pin1 or IIS data output pin4 or internal signal output pin1 (During reset, this pin is fixed to low level output.)
51	OUT_SEL2	O	O (L)	IIS data output pin2 or IIS word clock output pin4 or internal signal output pin2 (During reset, this pin is fixed to low level output.)
52	OUT_SEL3	O	O (L)	IIS data output pin3 or IIS bit clock output pin4 or internal signal output pin3 (During reset, this pin is fixed to low level output.)
53	DV_{DD}_1			Power supply for internal logic (1.5V)
54	DV_{SS}_1			Power supply for digital (GND)
55	XV_{SS}			Crystal for oscillation circuit power supply. (GND)
56	XIN		Oscillation	Crystal oscillation circuit input (11.2896MHz or 12.288MHz)
57	XOUT		Oscillation	Crystal oscillation circuit output
58	XV_{DD}			Crystal for oscillation circuit power supply (3.3V)
59	$AVCOAV_{DD}$			VCO analog power supply for CODEC main clock generation(3.3V)
60	$AVCOAV_{SS}$			VCO analog power supply for CODEC main clock generation (GND)
61	EVROUT3R	AO	AO	Electronic volume output pin. When output of EVR3 is OFF, EVRIN3R input signal output to EVROUT3R via 50kΩ register.
62	EVRIN3R	AI	AI	Electronic volume input pin. Make sure to connect this pin with DACOUT3R (DAC output) via coupling capacitor. When this pin is unused, leave it open or connect it to GND via capacitor.
63	DACOUT3R	AO	AO	DAC analog output pin. (R-channel output) When output of DAC3 is OFF, pin output becomes GND.
64	DACOUT3L	AO	AO	DAC analog output pin. (L-channel output) When output of DAC3 is OFF, pin output becomes GND.
65	EVRIN3L	AI	AI	Electronic volume input pin. Make sure to connect this pin with DACOUT3L (DAC output) via coupling capacitor. When this pin is unused, leave it open or connect it to GND via capacitor.
66	EVROUT3L	AO	AO	Electronic volume output pin. When output of EVR3 is OFF, EVRIN3L input signal output to EVROUT3L via 50kΩ register.
67	EVROUT2R	AO	AO	Electronic volume output pin. When output of EVR2 OFF, EVRIN2R input signal output to EVROUT2R via 50kΩ register.
68	EVRIN2R	AI	AI	Electronic volume input pin. Make sure to connect this pin with DACOUT2R (DAC output) via coupling capacitor. When this pin is unused, leave it open or connect it to GND via capacitor.
69	DACOUT2R	AO	AO	DAC analog output pin. (R-channel output) When output of DAC2 is OFF, pin output becomes GND.
70	DACOUT2L	AO	AO	DAC analog output pin. (L-channel output) When output of DAC2 is OFF, pin output becomes GND.
71	EVRIN2L	AI	AI	Electronic volume input pin. Make sure to connect this pin with DACOUT2L (DAC output) via coupling capacitor. When this pin is unused, leave it open or connect it to GND via capacitor.
72	EVROUT2L	AO	AO	Electronic volume output pin. When output of EVR2 is OFF, EVRIN2L input signal output to EVROUT2L via 50kΩ register.
73	EVROUT1R	AO	AO	Electronic volume output pin. When output of EVR1 is OFF, EVRIN1R input signal output to EVROUT1R via 50kΩ register.

Continued on next page.

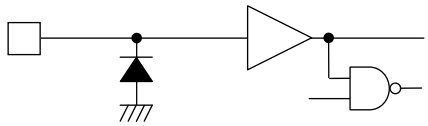
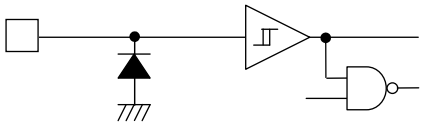
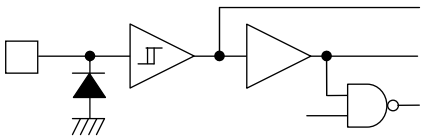
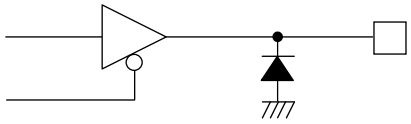
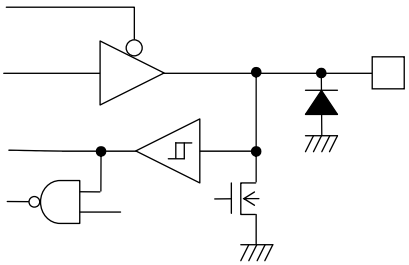
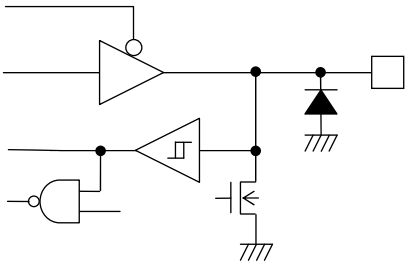
Continued from preceding page.

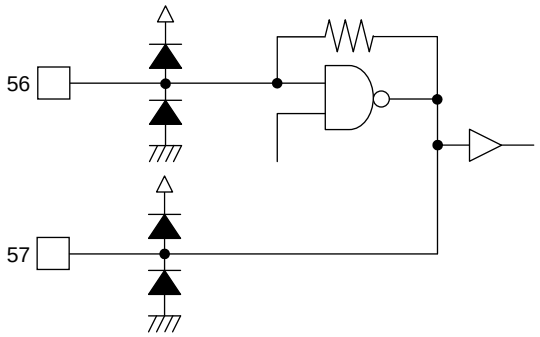
No	Pin name	Input/output	Input/output (RSTB=L)	Functions
74	EVRIN1R	AI	AI	Electronic volume input pin. Make sure to connect this pin with DACOUT1R (DAC output) via coupling capacitor. When this pin is unused, leave it open or connect it to GND via capacitor.
75	DACOUT1R	AO	AO	DAC analog output pin. (R-channel output) When the output setting of DAC1 is OFF, the pin output becomes GND.
76	DACOUT1L	AO	AO	DAC analog output pin. (L-channel output) When the output setting of DAC1 is OFF, the pin output becomes GND.
77	EVRIN1L	AI	AI	Electronic volume input pin. Make sure to connect this pin with DACOUT1L (DAC output) via coupling capacitor. When this pin is unused, leave it open or connect it to GND via capacitor.
78	EVROUT1L	AO	AO	Electronic volume output pin. When the output setting of EVR1 is OFF, EVRIN1L input signal output to EVROUT1L via 50kΩ register.
79	AVB			CODEC Substrate GND pin. Make sure to connect this pin to GND with low impedance. Note that when the pin is open, latch-up may occur.
80	$COAV_{SS}6$			Power supply for CODEC analog (GND)
81	$COAV_{DD}6$			Power supply for CODEC analog (3.3V)
82	$COAV_{SS}5$			Power supply for CODEC analog (GND)
83	$COAV_{DD}5$			Power supply for CODEC analog (3.3V)
84	AIN1RP	AI	AI	R-channel for stereo1 Positive analog input pin. or R-channel for stereo 4 analog input pin. When this pin is unused, connect it to GND via capacitor.
85	AIN1RN	AI	AI	R-channel for stereo 1 Negative analog input pin. or L-channel for stereo 4 analog input pin. When this pin is unused, connect it to GND via capacitor.
86	AIN1LN	AI	AI	L-channel for stereo 1 Negative analog input pin. or R-channel for stereo 5 analog input pin. When this pin is unused, connect it to GND via capacitor.
87	AIN1LP	AI	AI	L-channel for stereo1 Positive analog input pin. or L-channel for stereo 5 analog input pin. When this pin is unused, connect it to GND via capacitor.
88	AIN2R	AI	AI	R-channel for stereo 2 analog input pin. When this pin is unused, connect it to GND via capacitor.
89	AIN2L	AI	AI	L-channel for stereo 2 analog input pin. When this pin is unused, connect it to GND via capacitor.
90	$COAV_{SS}4$			Power supply for CODEC analog (GND)
91	$COAV_{DD}4$			Power supply for CODEC analog (3.3V)
92	AIN3RO	AO	AO	R-channel for stereo 3 Op Amp output pin
93	AIN3RN	AI	AI	R-channel for stereo 3 Op Amp inverting input pin. When this pin is unused, connect it to GND via capacitor.
94	AIN3RP	AI	AI	R-channel for stereo 3 Op Amp non-inverting input pin. When this pin is unused, connect it to GND via capacitor.
95	$COAV_{SS}3$			Power supply for CODEC analog (GND)
96	$COAV_{DD}3$			Power supply for CODEC analog (3.3V)
97	AIN3LP	AI	AI	L-channel for stereo 3 Op Amp non-inverting input pin. When this pin is unused, connect it to GND via capacitor.
98	AIN3LN	AI	AI	L-channel for stereo 3 Op Amp inverting input pin. When this pin is unused, connect it to GND via capacitor.
99	AIN3LO	AO	AO	L-channel for stereo 3 Op Amp output pin
100	$COAV_{SS}2$			Power supply for CODEC analog (GND)

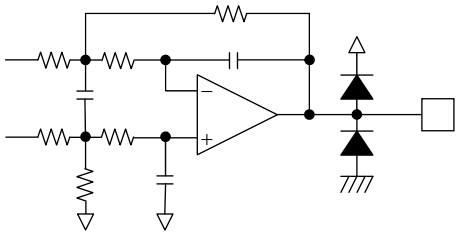
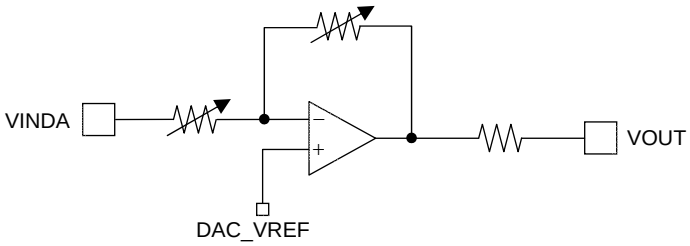
(Caution)

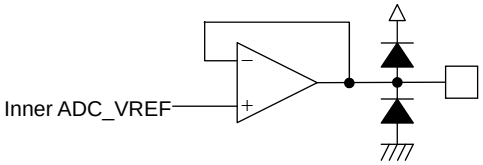
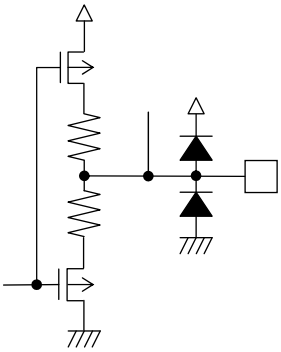
* Make sure to connect decoupling capacitor between V_{DD} and V_{SS}.
* The unused input pins that are not particularly specified above should be connected to GND.
* The unused output pins that are not particularly specified above should be left open (do not connect to anything else).
* Make sure to connect AVB (#79) to GND.(When the pin is open, latch-up may occur).

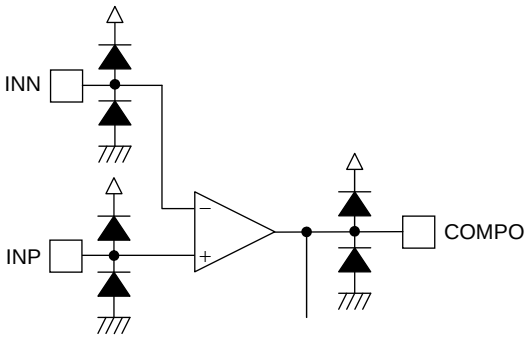
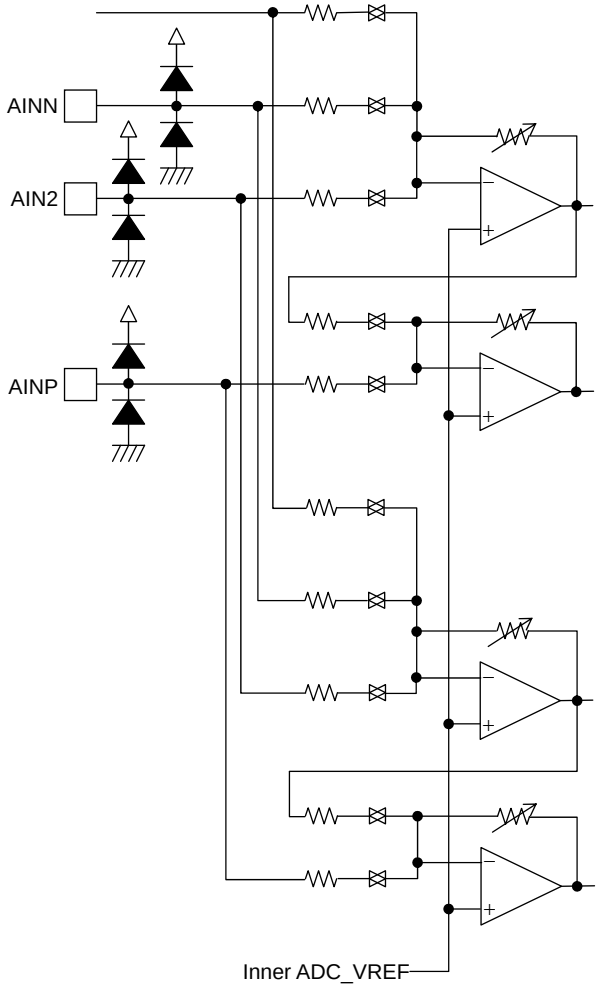
Input/Output PIN equivalent circuit

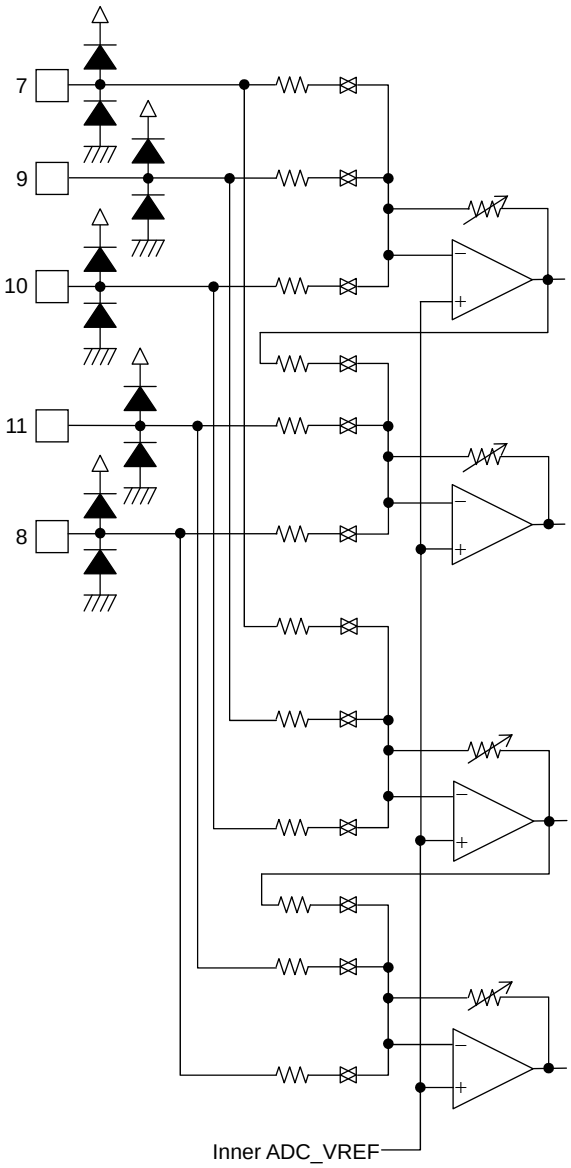
I/O	Equivalent circuit	Pin	Comment
Digital input		TEST1 : 12 TEST2 : 13 MODE : 16	5V-Tolerant
Digital input		SP_CL/SCLS : 19 PWDB : 23 IISI1_DATA : 33 IISI1_LRCK : 34 IISI1_BCLK : 35 IISI2_DATA : 36 IISI2_LRCK : 37 IISI2_BCLK : 38 IISI3_DATA : 39 IISI3_LRCK : 40 IISI3_BCLK : 41 IISI4_DATA : 42 IISI4_LRCK : 43 IISI4_BCLK : 44	5V-Tolerant
Digital input		RSTB : 24	5V-Tolerant 3.3V Output (Inverting)
Digital output		BUSYO : 17 GPO_1(ERR) : 22 IISO_BCLK : 48 IISO_LRCK : 49 OUT_SEL1 : 50 OUT_SEL2 : 51 OUT_SEL3 : 52	5V-Tolerant
Digital input/output		SP_DI/GPIO_2 : 20 SP_SSB/GPIO_3 : 21 DSPIO1 : 25 DSPIO2 : 30 DSPIO3 : 31 IIS_SUB1 : 45 IIS_SUB2 : 46 IIS_SUB3 : 47	5V-Tolerant
Digital input/output		SP_DO/SDAS : 18 DSPIO4 : 32	5V-Tolerant

I/O	Equivalent circuit	Pin
Oscillation circuit		XIN : 56 XOUT : 57

I/O	Equivalent circuit	Pin
DAC		DACOUT3R : 63 DACOUT3L : 64 DACOUT2R : 69 DACOUT2L : 70 DACOUT1R : 75 DACOUT1L : 76
EVR In/Out		VINDA EVRIN3R : 62 EVRIN3L : 65 EVRIN2R : 68 EVRIN2L : 71 EVRIN1R : 74 EVRIN1L : 77 VOUT EVROUT3R : 61 EVROUT3L : 66 EVROUT2R : 67 EVROUT2L : 72 EVROUT1R : 73 EVROUT1L : 78

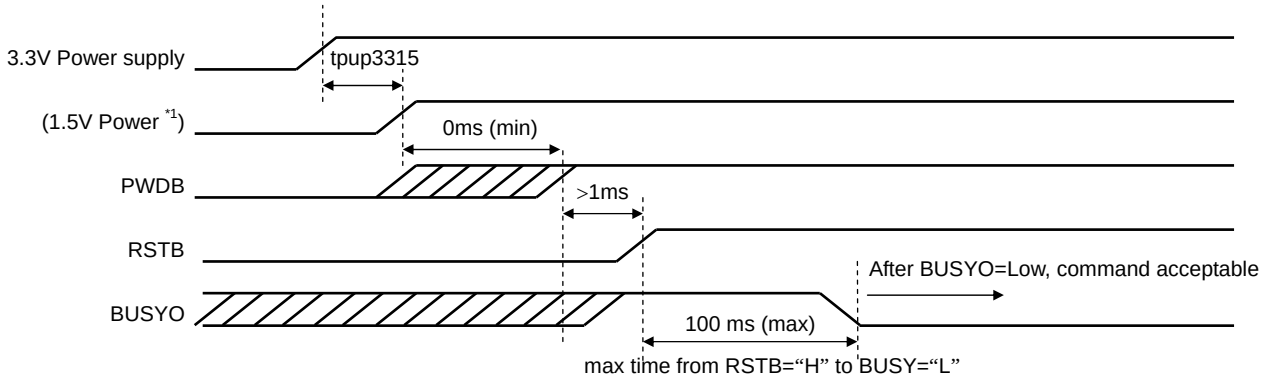
I/O	Equivalent circuit	Pin
VREF AMP Output		VREFAMPO : 4
VREF Output		ADC_VREF : 5 DAC_VREF : 6

I/O	Equivalent circuit	Pin
Analog input (differential)		INN AIN3RN : 93 AIN3LN : 98 INP AIN3RP : 94 AIN3LP : 97 COMPO AIN3RO : 92 AIN3LO : 99
Analog Selector input (stereo)		AINN AIN1RN : 85 AIN1LN : 86 AIN2 AIN2R : 88 AIN2L : 89 AINP AIN1RP : 84 AIN1LP : 87

I/O	Equivalent circuit	Pin
Analog Selector input (monaural)		MIN3 : 7 MIN2P : 9 MIN1P : 10 MIN1N : 11 MIN2N : 8

Power On/Off Timing

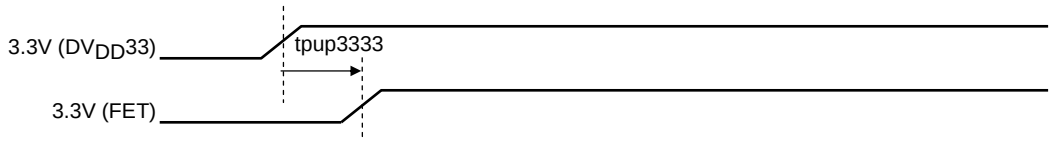
(1) Power supply ON timing order



*1) When a 1.5V power supply is applied in external power source directly, Please refer to this sequential order.

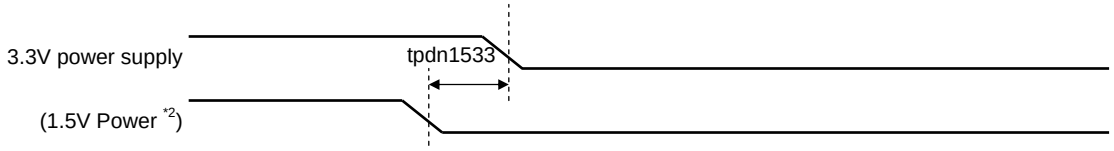
RSTB signal should be set in Low level more than 1ms from either late power supply turned on or positive edge of the PWDB signal.. In addition, the reset time is less than 100msec.

When a 1.5V power supply is produced using a onchip 1.5V reference level and external FET, It is recommended that 3.3V power supply of LC75056 ($DV_{DD}33$) and 3.3V power of external FET are turned on the following order.



Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power on (3.3V → 1.5V)	tpup3315		0		100	msec
Power on (3.3V → 3.3V)	tpup3333		0			

(2) Power supply OFF timing order



*2) When a 1.5V power supply is applied in external power source directly, Please refer to this sequential order.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power off (1.5V → 3.3V)	tpdn1533		0		100	msec

In addition, 5V-Tolerant input pin of LC75056 can input 3.6V voltage even if in power supply OFF condition. Furthermore, it can be applied to 5V after regular voltage was applied to each power supply. Be careful because the I/O direction of the pin is not decided before a 1.5V power supply being input.

In the voltage of each power supply, the voltage of the 3.3V power supply must be higher than the voltage of the 1.5V power supply.

Audio input Function

(1) Digital audio input

LC75056 has 4ch sampling rate converter as digital audio input, and Implement an independent selector circuitry every channel.

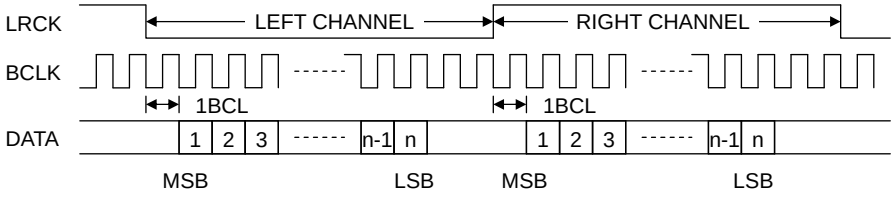
(2) Digital input format

1) Pin Name	IISI1_DATA, IISI1_LRCK, IISI1_BCLK, IISI2_DATA, IISI2_LRCK, IISI2_BCLK, IISI3_DATA, IISI3_LRCK, IISI3_BCLK, IISI4_DATA, IISI4_LRCK, IISI4_BCLK, IIS_SUB1(*1), IIS_SUB2(*1), IIS_SUB3(*1)
2) Mode	MASTER MODE, SLAVE MODE
3) Format	IIS MODE, LEFT JUSTIFIED MODE, RIGHT JUSTIFIED MODE (*2)
4) Bit length	16bit, 20bit, 24bit (*2)
5) BCLK Frequency	max 64fs (selectable from 32fs, 48fs, 64fs)
6) Input fs	8kHz to 96kHz (Internal automatic distinction)

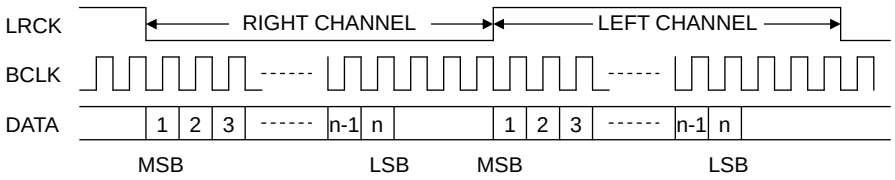
(*1) As for the pin of IIS_SUB1/2/3, input or output is selectable.

(*2) These modes can be set independently in IIS1 and IIS2. The setting method is shown in software specifications.

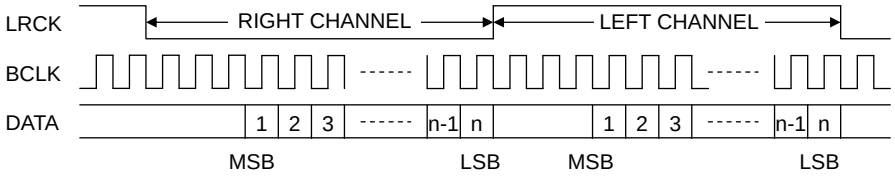
(3) IIS MODE input timing



(4) LEFT JUSTIFIED MODE Input Timing



(5) RIGHT JUSTIFIED MODE Input Timing



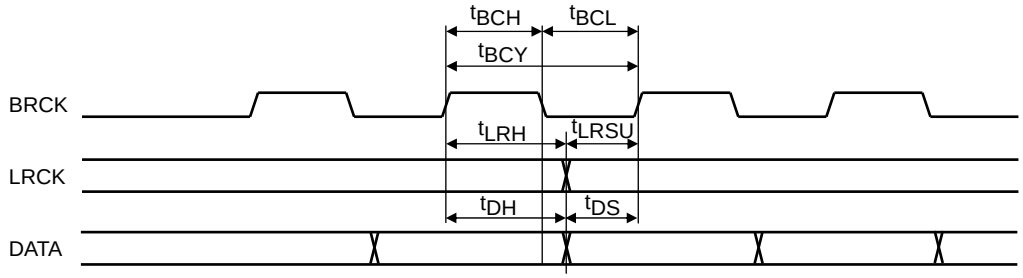
(6) Combination of IIS Input/Output

About IIS application pin, the following configurations are enabled.

- 4 independent input and 4 output
- 5 independent input and 3 output
- 3 independent input and 3 multi-channel input and 3 output

The setting method is shown in software specifications.

(7) Input timing chart



Parameter	symbol	Conditions	Min	Typ	Max	Unit
LRCK Cycle Time	-		8		96	kHz
BCLK Cycle Time	t_{BCY}	BCLK : 64FS	512		6144	kHz
		BCLK : 32FS	256		3072	
BCLK pulse width “H”	t_{BCH}		60			nsec
BCLK pulse width “L”	t_{BCL}		60			nsec
LRCK setup time to BCLK rising edge	t_{LRSU}		30			nsec
LRCK hold time to BCLK rising edge	t_{LRH}		30			nsec
DATA setup time to BCLK rising edge	t_{DS}		30			nsec
DATA hold time to BCLK rising edge	t_{DH}		30			nsec

(8) Sampling rate Converter (SRC)

The sampling rate converter converts the sampling frequency into internal 44.1kHz or 48kHz for IIS digital input. It is decided which frequency it is converted into by crystal to use.

In the case of 44.1kHz Crystal oscillator is 11.2896MHz (44.1kHz × 256)

In the case of 48kHz: Crystal oscillator is 12.288MHz (48kHz × 256)

Setting of the control information is necessary. About the setting method, it is shown in software specification.

1) Input sampling frequency 8kHz to 96kHz
2) Output sampling frequency 44.1kHz or 48kHz
3) number of the channels: 4 stereo channel (8 channel)

It takes 2782fs (based on fs of either slow input or output) period after starting input and output of the digital audio before SRC output is stable (THD+N is stable). Because noise may occur during this period, please do mute processing.

(9) Analog audio input

LC75056 has 2 ADCs (main/sub) for stereo sounds and 2 ADCs (INTA/INTB) for interruption monaural voices as analog audio in. In addition, a source select circuitry with gain setting is implemented in each ADC.

As stereo input, one of single end input or op-amp input or the differential input can be chosen.
As monaural voice inputting, one of single end input or the differential input can be chosen.

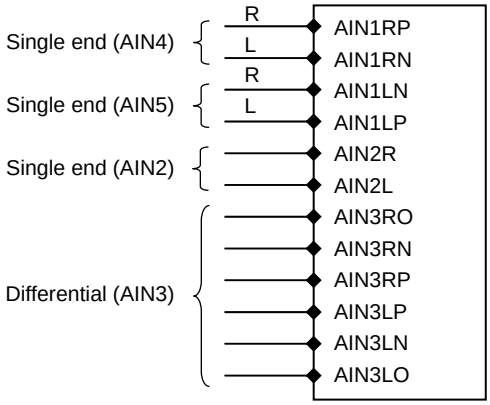
1) Main and Sub ADC input

In audio main/sub ADC, a source selector of the single end input/op-amp input/differential input, and the Amp that can set a gain for each input individually are implemented. The gain set point of the main/sub is settable every each input source. Each amplifier gain is settable independently in the range of -12dB to +19dB (1dB step).
In addition, please do mute processing because a noise may occur when gain setting is changed. About the setting command, it is shown on software specifications.

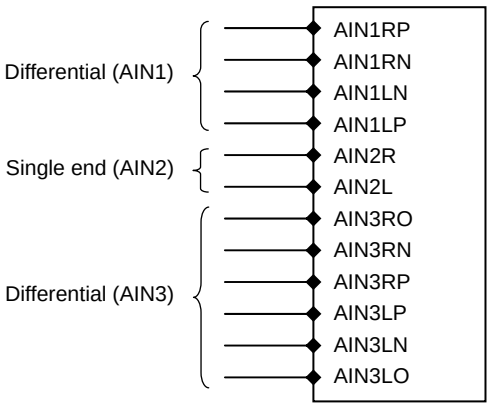
	single end input		differential input	
	Lch	Rch	Lch	Rch
Single end: 3 Differential: 1	AIN1LP	AIN1LN	AIN3LP, AIN3LN	AIN3RP, AIN3RN
	AIN1RN	AIN1RP		
	AIN2L	AIN2R		
Single end: 1 Differential: 2	AIN2L	AIN2R	AIN1LP, AIN1LN	AIN1RP, AIN1RN
			AIN3LP, AIN3LN	AIN3RP, AIN3RN

About the method of these setting, it is appointed on software specifications.

(i) Single end input: 3, differential input: 1



(ii) Single end input: 1, differential input: 2



2) Monaural ADC input

Audio system ADC for interrupt sound (INTA/INTB) has the amplifier which can set a gain for a source selector of the single-end input/differential input and each input individually. The gain setting of INTA/INTB is settable every each input source. The range of the gain is -12 to +19dB (1dB steps), and set from the outside.

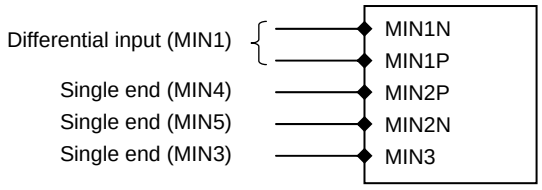
In addition, perform mute processing by all means because the noise outbreak is possible at the time of the gain setting change. About the method of the gain setting change, it is appointed on software specifications.

By a number and the kind of the interrupt sound, the following combination is enabled.

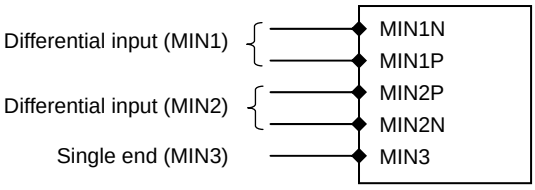
Combination	single end input	differential input
Single end: 3 Differential: 1	MIN2N	MIN1P, MIN1N
	MIN2P	
	MIN3	
Single end: 1 Differential: 2	MIN3	MIN1P, MIN1N
		MIN2P, MIN2N

About the method of these setting, it is appointed on software specifications.

(i) Single end input: 3, differential input: 1

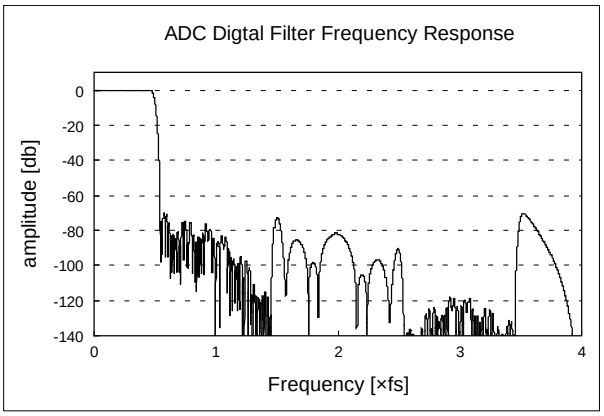


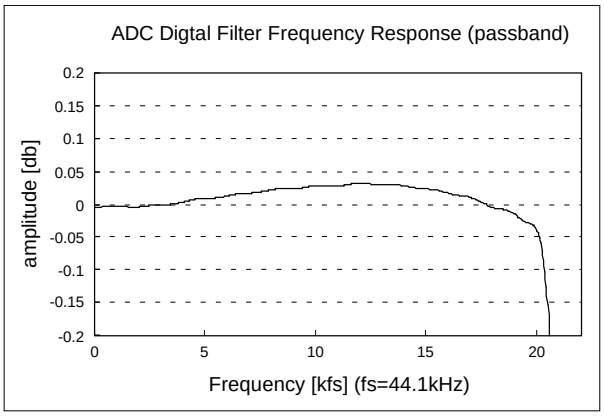
(ii) Single end input: 1, differential input: 2



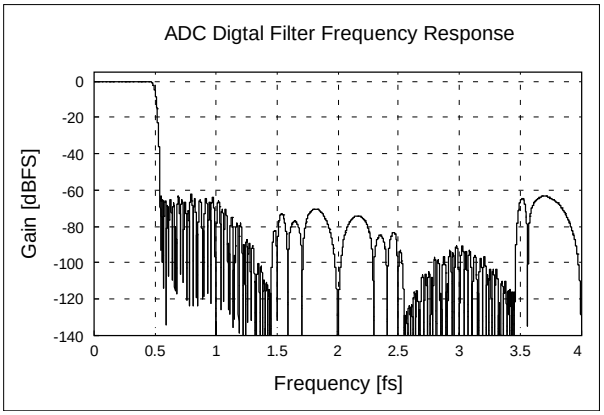
(10) Internal digital filter characteristic in A/D and D/A converter block

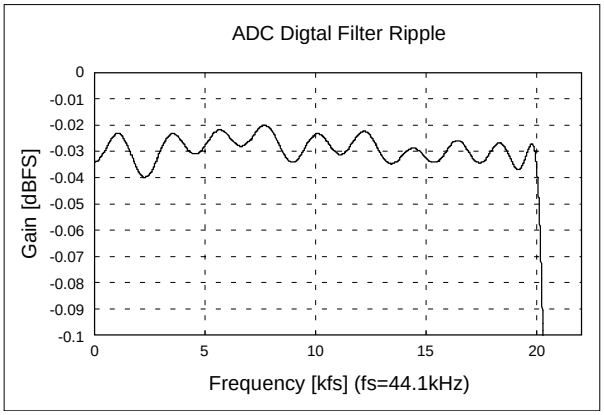
1) A/D converter block





2) D/A converter block (8- TIMES OVER SAMPLING DIGITAL FILTER)





Audio output Function

Digital audio output

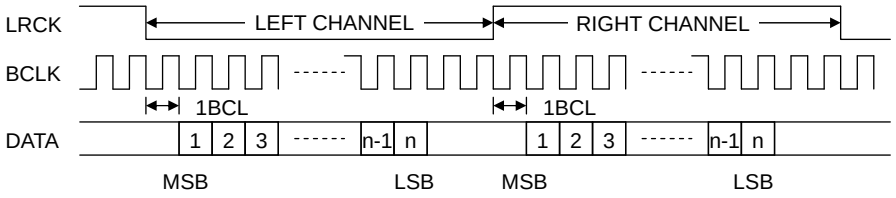
LC75056 has the digital output function of up to four systems. The digital output is fixed with IIS24bit/64fs format.

(1) IIS output format (DSP processing)

1) Pin Name	IISO_BCLK, IISO_LRCK, OUT_SEL1, OUT_SEL2, OUT_SEL3, IIS_SUB1(*1), IIS_SUB2(*1), IIS_SUB3(*1)
2) Format	IIS MODE
3) Mode	MASTER mode
4) Bit length	24bit
5) BCLK Frequency	64fs

(*1) As for the pin of IIS_SUB1/2/3, input or output is selectable.

Timing Chart



(2) Through output format

LC75056 has a digital through output function other than four above digital output. With this mode, input data are output from the OUT_SEL1/2/3 terminal regardless of DSP processing. It is set from the outside which data are output from these terminals.

1) Selectable data	IISI1_DATA, IISI1_LRCK, IISI1_BCLK, IISI2_DATA, IISI2_LRCK, IISI2_BCLK, IISI3_DATA, IISI3_LRCK, IISI3_BCLK, IISI4_DATA, IISI4_LRCK, IISI4_BCLK, IIS_SUB1(*1), IIS_SUB2(*1), IIS_SUB3(*1)
2) Pin Assign	OUT_SEL1 : DATA OUT_SEL2 : LRCK OUT_SEL3 : BCLK
3) Format	As for the IIS output, an input signal is just output. When it is used by the through output, there are not the rules such as formats in particular.

(*1) It is only on the condition that IIS_SUB1/2/3 is used as input.

MICON Interface

As communication interface of a host microcomputer and this LSI, one of IIC method or SPI methods is selectable. The choice of the communication mode is decided by MODE pin.

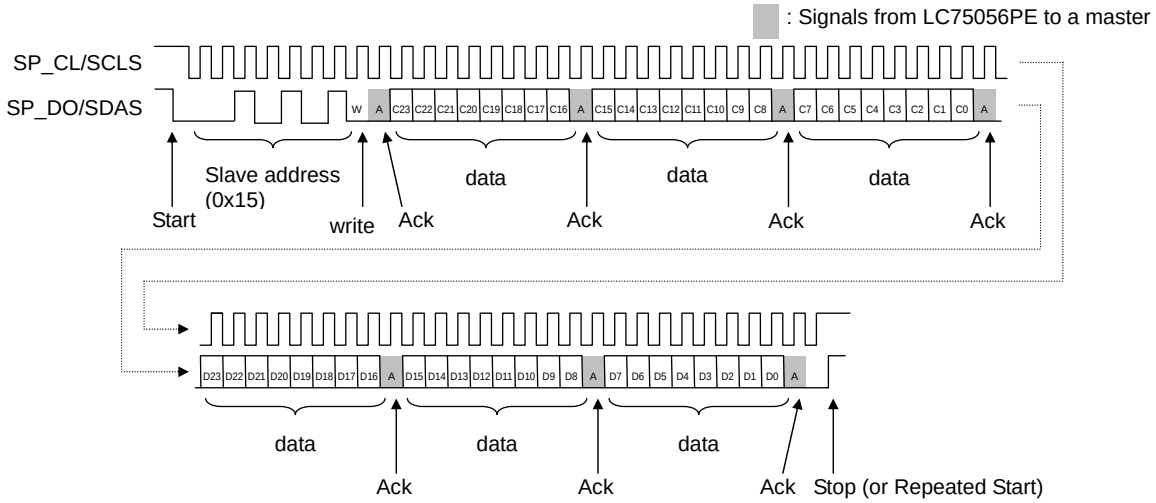
MODE: "0": IIC Interface
"1": SPI Interface

(1) I^2C Interface

The IIC slave transmission and reception interface of this LSI is based on IIC Interface Specification ver.2.1. (Standard mode: 100Kbps, High speed mode: 400Kbps)

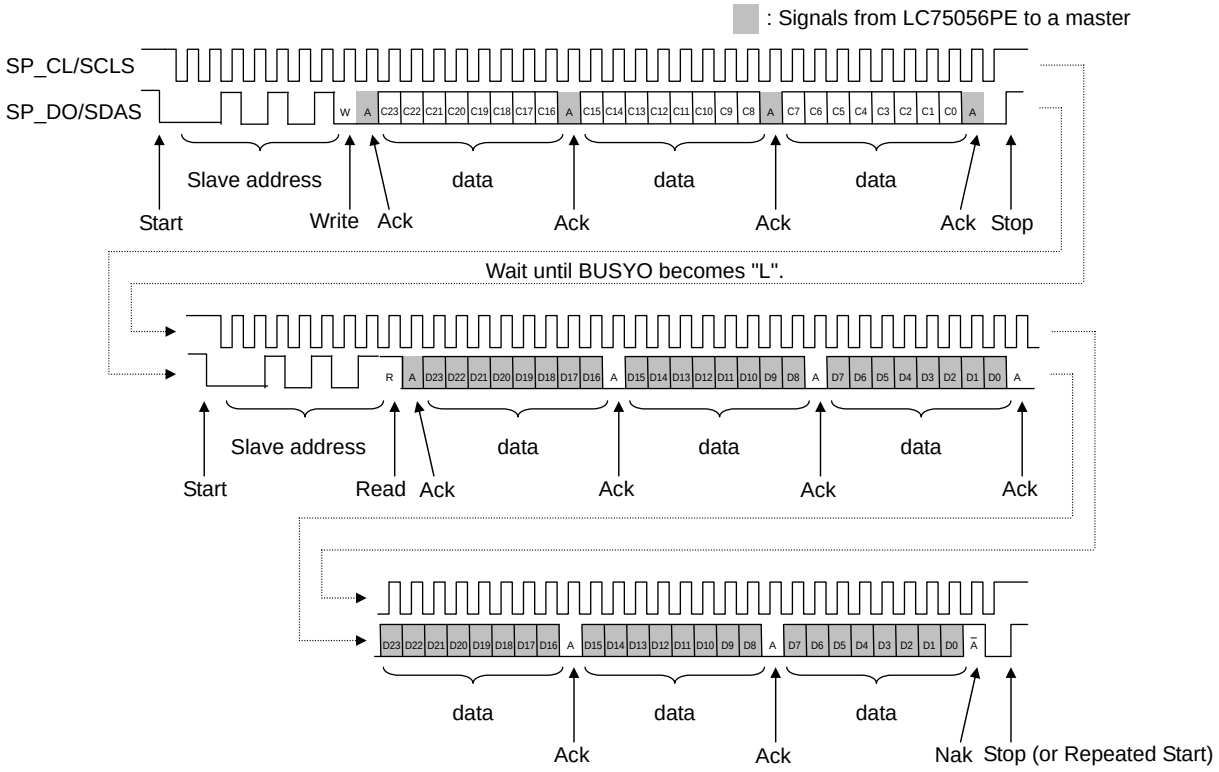
The slave address of this LSI is 0x15 (value of upper 7 bits). The data to transfer assume 8 bits 1 unit. The format of the data transmission is performed according to the following. In addition, each byte data are the MSB first.

Data write (6byte transmission example)



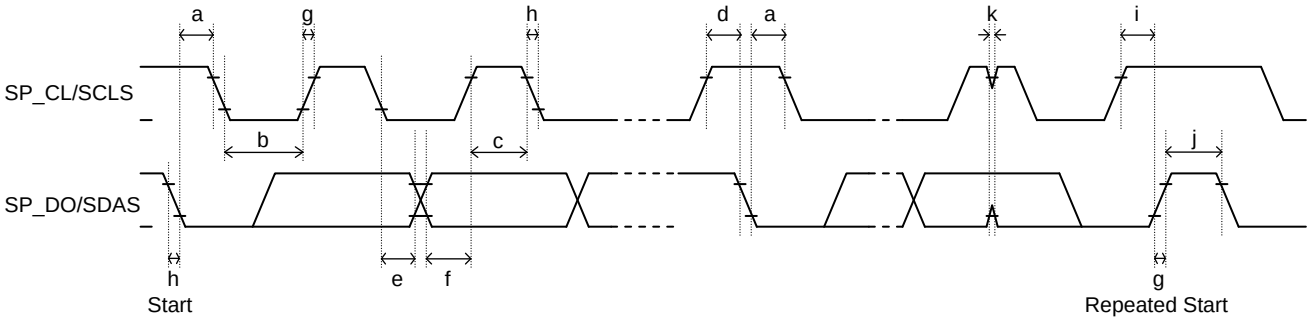
Make sure to perform communication when BUSYO pin is "L". If communication is started when BUSYO pin is "H", the operation of LC75056 will not be guaranteed.

Data read



The content of each data is specified by the software specification.

Data access timing



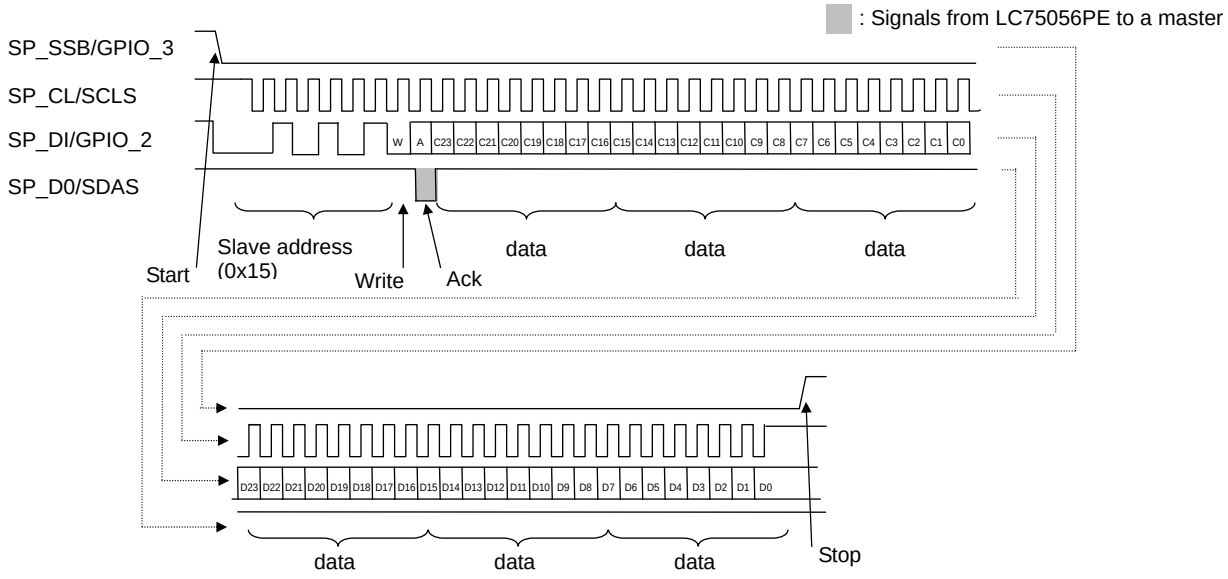
Symbol	Timing Parameter	Standard mode (100kbps)		Fast mode (400kbps)		unit
		Min	Max	Min	Max	
a	Start (Repeated-Start) condition hold time	4000		600	-	ns
b	SP_CL/SCLS “P_ level pulse width	4700		1300	-	ns
c	SP_CL/SCLS “HP level pulse width	4000		600	-	ns
d	Start (Repeated-Start) condition setup time	4700		600	-	ns
e	SP_DO/SDAS hold time	0	3450	0	900	ns
f	SP_DO/SDAS setup time	250		100	-	ns
g	SP_CL/SCLS, SP_DO/SDAS rise time	-	1000	20+0.1Cb(1)	300	ns
h	SP_CL/SCLS, SP_DO/SDAS fall time	-	300	20+0.1Cb(1)	300	ns
i	Stop condition setup time	4000		600	-	ns
j	Bus release time	4700		1300	-	ns
k	Allowable spikes pulse width	-		0	-	ns

Cb = total capacitance of one bus line in pF.

(2) SPI Interface

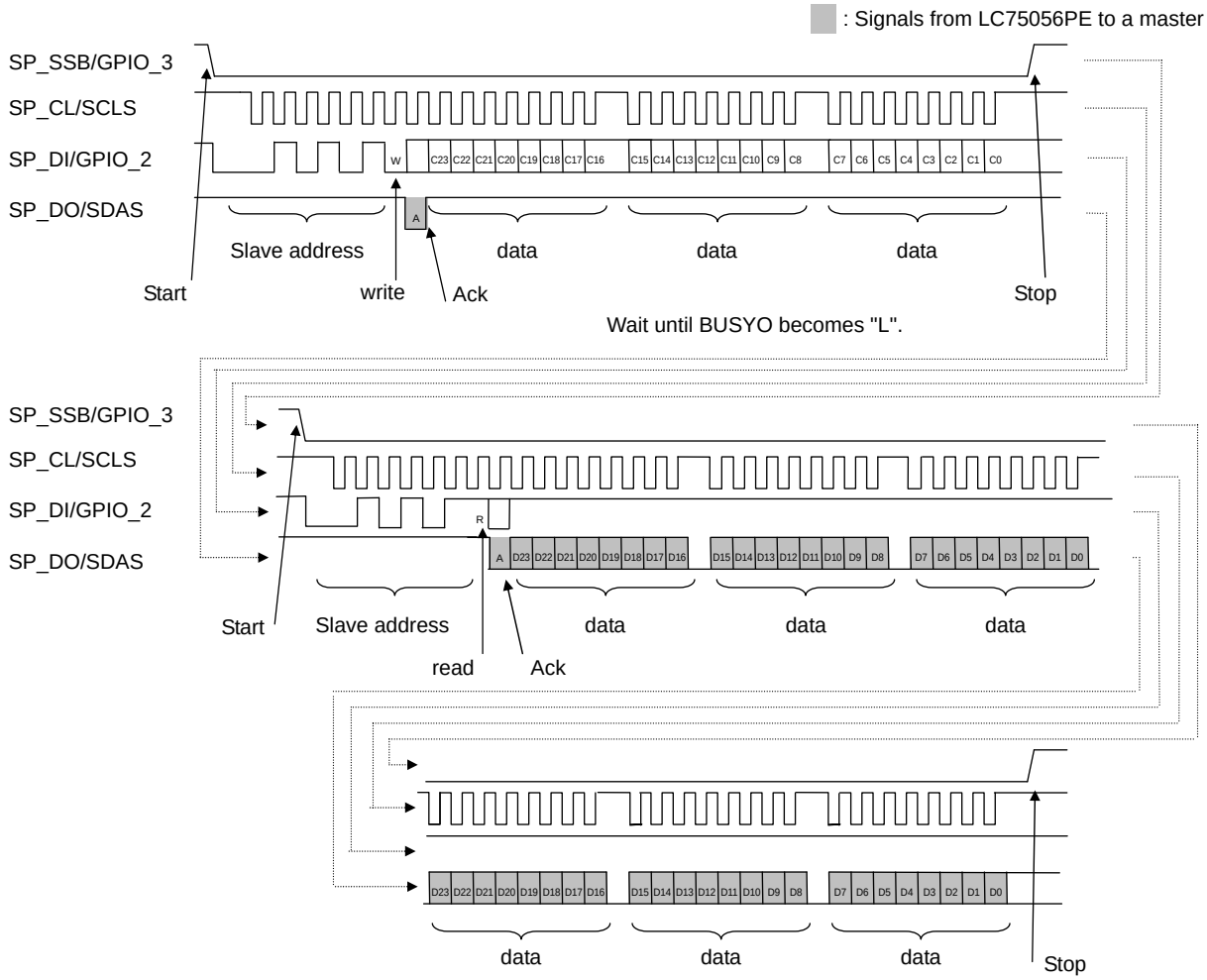
The SPI slave sending and receiving interface of this LSI communicates by using four terminals (SP_SSB/GPIO_3, SP_CL/SCLS, SP_DI/GPIO_2, and SP_DO/SDAS). The fast transfer in 2Mbps or less is possible unlike I2C method. The slave address is 0x15 (six bit value) when the data transfer is done to this LSI, and one unit of data is 8 bits. The data transfer is formatted as follows. Each byte data are the MSB first.

Data write (Ex. 6byte transmission)



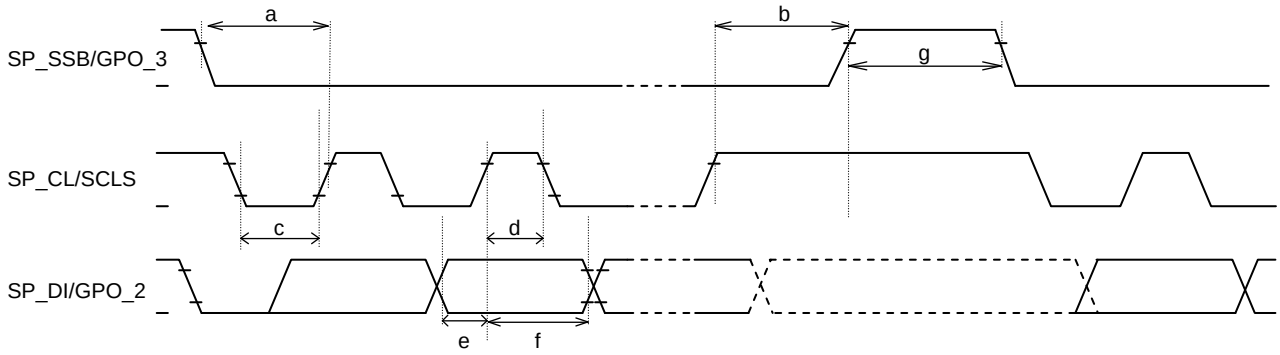
Make sure to perform communication when BUSYO pin is “L”. If communication is started when BUSYO pin is “H”, the operation of LC75056 will not be guaranteed.

Data read

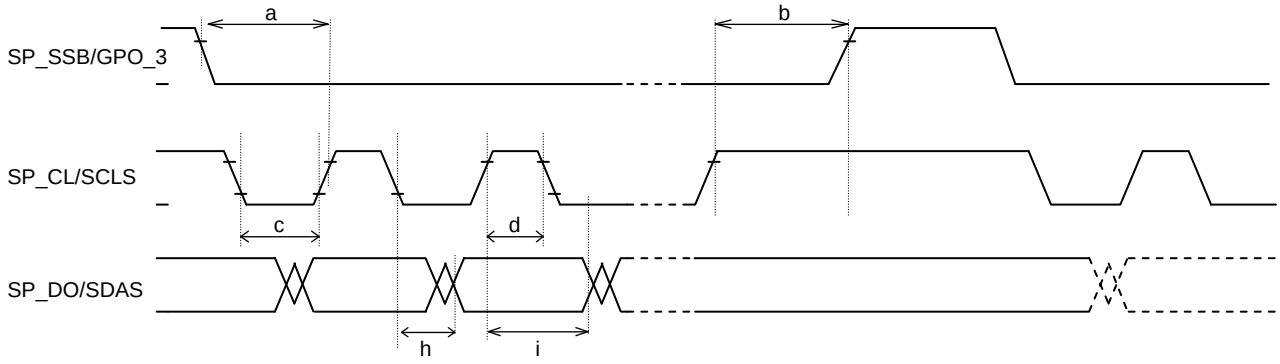


The content of each data is specified by the software specification.

Data write timing

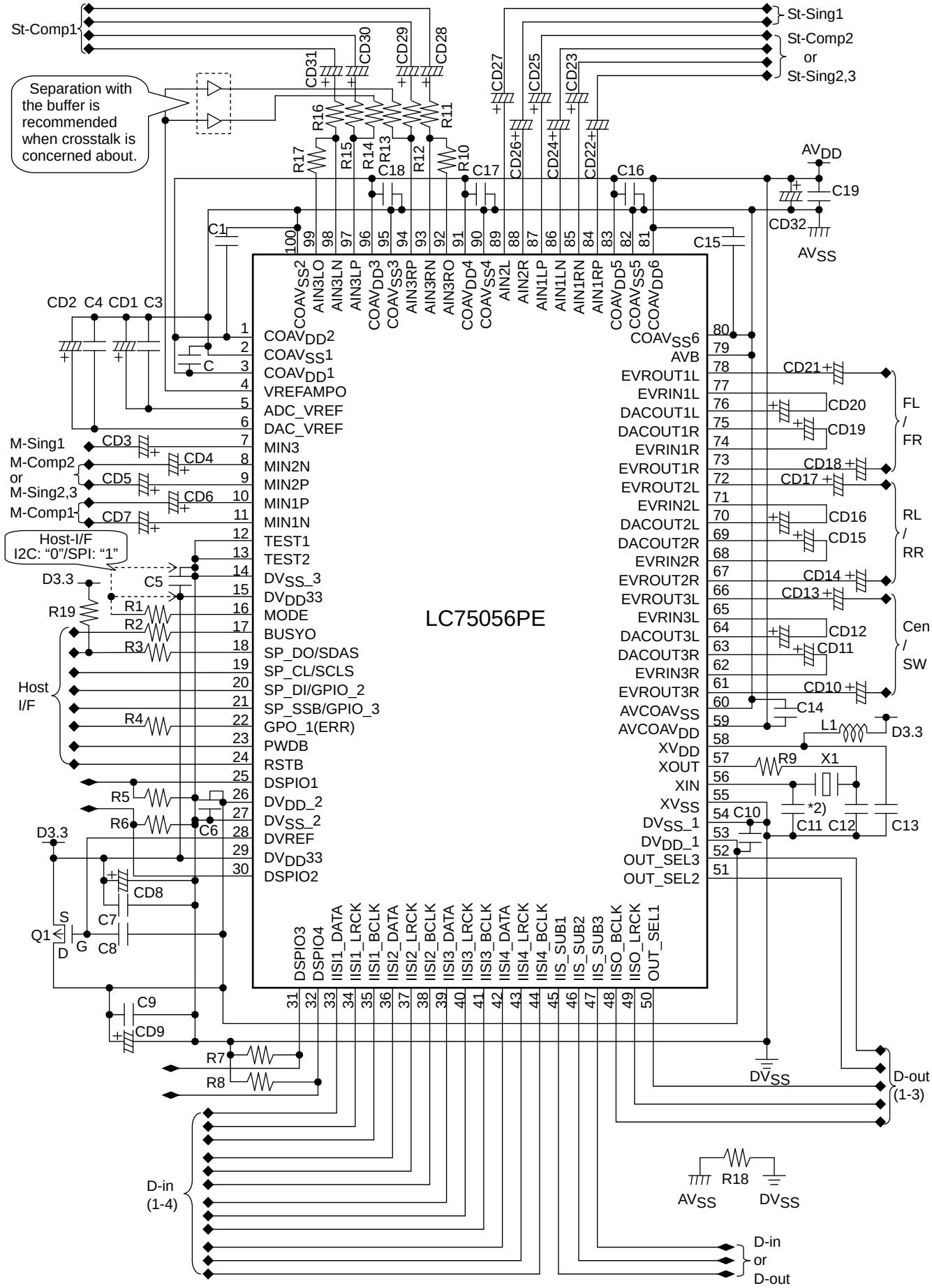


Data read timing



Symbol	Parametre	Min	Typ	Max	Unit
a	SP_SSB setup time	500			ns
b	SP_SSB hold time	250			ns
c	SP_CL Low level pulse width	250			ns
d	SP_CL High level pulse width	250			ns
e	SP_DI setup time	100			ns
f	SP_DI hold time	100			ns
g	Command transfer interval	500			ns
h	SP_DO access time	0		100	ns
i	SP_DO hold time	120			ns

Application Schematics



Note 1) This application schematics is just for reference and the characteristics are not guaranteed.
Note 2) The confirmation of the constant for the oscillator and the evaluation request to the oscillator vendor are recommended.

BOM for Application Schematics

Name	Parameter	Condition	Model	Locations	Notice
Ceramic Capacitor	0.1μF		1608	C1, C2, C3, C4, C5, C6, C7, C10, C13, C14, C15, C16, C17, C18, C19	
Ceramic Capacitor	10μF		3216	C9	
Ceramic Capacitor	18pF		1608	C11, C12	The confirmation of the constant for the oscillator and the evaluation request to the oscillator vendor are recommended.
Ceramic Capacitor	10nF		1608	C8	
Electrolytic Capacitor	47μF	DC50V±20 %		CD1, CD2, CD8, CD9, CD32	
Electrolytic Capacitor	4.7μF	DC50V±20 %		CD10, CD11, CD12, CD13, CD14, CD15, CD16, CD17, CD18, CD19, CD20, CD21	The polarity depends on the constitution of other circuits.
Electrolytic Capacitor	2.2μF	DC50V±20 %		CD3, CD4, CD5, CD6, CD7, CD22, CD23, CD24, CD25, CD26, CD27, CD28, CD29, CD30, CD31	
Chip Resistor	10kΩ		1608	R1, R5, R6, R7, R8, R19	
Chip Resistor	30kΩ		1608	R11, R16	
Chip Resistor	30kΩ		1608	R12, R15	
Chip Resistor	15kΩ		1608	R13, R14	
Chip Resistor	15kΩ		1608	R10, R17	
Chip Resistor	0		1608	R9, R18	
Chip Resistor	100Ω		1608	R2, R4	
Chip Resistor	33Ω		1608	R3	
Chip Bead	MPZ1608R39 1A		1608	L1	
FET			NTR2101P	Q1	
Cristal Oscillator	11.2896MHz 12.288MHz		CX8045GA	X1	Selectable by System constitution.

Notice:

*) The locations of the bypass capacitors (C1, C2, C5, C6, C10, C14, C15, C16, C17, C18) must be arranged close to the each LSI pin and in the aspect of the same side as the LC75056PE.

*) The location of the Q1 (FET) must be arranged close to the LC75056PE.

*) The locations of C7, CD8, C9, and CD9 must be arranged close to the Q1 (FET).

*) The length of the Lch and Rch of each Audio input/output wiring same as much as possible is recommended. (It is similar in the case of the length of the +ch and –ch of each differential input/output.)

(Appendix : Audio processing mode)

This software has nine modes of operation as following table.
Depending on the number of the channels processing Bongiovi DPS and another function to use, please select one mode.
A channel name (ex. FL/FR/RL/RR/CE/SW, RSEL/RSER, IntA/IntB) listing in each cell is the processing channel of each function.

Audio processing mode

Function	DPS OFF		DPS 2 channel		DPS 4 channel			DPS 5 channel	DPS 6 channel
	Mode(0)	Mode(1)	Mode(2)	Mode(3)	Mode(4)	Mode(5)	Mode(6)	Mode(7)	Mode(8)
Input Selector	Enable	Enable	Enable	Enable	Enable	Enable	Enable	Enable	Enable
Input Gain	Enable	Enable	Enable	Enable	Enable	Enable	Enable	Enable	Enable
DownMix	Enable	Enable	Enable	Enable	Enable	Enable	Enable	Enable	Enable
High band retriever (HBR)	FL/FR	FL/FR	FL/FR	FL/FR	disable	disable	disable	disable	disable
Selector Int Selector	Enable	Enable	Enable	Enable	Enable	Enable	Enable	Enable	Enable
Noise Gate	disable	disable	6 channel FL/FR/RL/RR/ CE/SW	6 channel FL/FR/RL/RR/ CE/SW	6 channel FL/FR/RL/RR/ CE/SW	6 channel FL/FR/RL/RR/ CE/SW	6 channel FL/FR/RL/RR/ CE/SW	6 channel FL/FR/RL/RR/ CE/SW	6 channel FL/FR/RL/RR/ CE/SW
Bongiovi DPS	disable	disable	2 channel FL/FR	2 channel FL/FR	4 channel FL/FR/RL/RR	4 channel FL/FR/RL/RR	4 channel FL/FR/RL/RR	5 channel FL/FR/RL/RR CE	6 channel FL/FR/RL/RR/ CE/SW
Input ATT(2)	FL/FR/RL/RR/ CE/SW	FL/FR/RL/RR/C E/SW	FL/FR	FL/FR	FL/FR/RL/RR	FL/FR/RL/RR	FL/FR/RL/RR	FL/FR/RL/RR	disable
Tone Control	FL/FR/RL/RR/ CE/SW Bas/Mid/Tre (3Band)	FL/FR/RL/RR/C E/SW Bas/Mid/Tre (3Band)	FL/FR Bas/Mid/Tre (3Band)	FL/FR Bas/Mid/Tre (3Band)	FL/FR/RL/RR Bas/Tre (2Band)	FL/FR/RL/RR Bas/Mid/Tre (3Band)	FL/FR/RL/RR Bas/Mid/Tre (3Band)	disable	disable
Loudness	FL/FR/RL/RR/ CE/SW low/high (2Band)	FL/FR/RL/RR/C E/SW low/high (2Band)	FL/FR low/high (2Band)	FL/FR low/high (2Band)	disable	FL/FR/RL/RR low/high (2Band)	FL/FR/RL/RR low/high (2Band)	disable	disable
Input ATT(3)	FL/FR/RL/RR/ CE/SW	FL/FR/RL/RR/C E/SW	FL/FR	FL/FR	disable	FL/FR/RL/RR	disable	disable	disable
Equalizer	FL/FR/RL/RR/ CE/SW 7Band	FL/FR/RL/RR/C E/SW 7Band	FL/FR 7Band	FL/FR 7Band	disable	FL/FR/RL/RR 7Band	disable	disable	disable
Surround	FL/FR/RL/RR	FL/FR/RL/RR	FL/FR	FL/FR	disable	disable	disable	disable	disable
Bass Enhancement (NewSlive)	FL/FR/RL/RR	disable	FL/FR	disable	FL/FR/RL/RR	disable	disable	disable	disable
SW generator	disable	FL/FR/RL/RR	disable	FL/FR	disable	disable	FL/FR/RL/RR	disable	disable
Volume(1): Main Volume	IntA/IntB FL/FR/RL/RR/ CE/SW RSEL/RSER	IntA/IntB FL/FR/RL/RR/C E/SW RSEL/RSER	IntA/IntB FL/FR RSEL/RSER	IntA/IntB FL/FR RSEL/RSER	IntA/IntB FL/FR/RL/RR RSEL/RSER	IntA/IntB FL/FR/RL/RR RSEL/RSER	IntA/IntB FL/FR/RL/RR RSEL/RSER	IntA/IntB FL/FR/RL/RR/ CE/SW RSEL/RSER	IntA FL/FR/RL/RR/ CE/SW
Delay	FL/FR/RL/RR/ CE/SW	FL/FR/RL/RR/C E/SW	FL/FR	FL/FR	FL/FR/RL/RR	FL/FR/RL/RR	FL/FR/RL/RR	FL/FR/RL/RR/ CE/SW	FL/FR/RL/RR/ CE/SW
Volume(2) Balance/Fader	FL/FR/RL/RR/ CE/SW	FL/FR/RL/RR/C E/SW	FL/FR	FL/FR	FL/FR/RL/RR	FL/FR/RL/RR	FL/FR/RL/RR	FL/FR/RL/RR/ CE/SW	FL/FR/RL/RR/ CE/SW
Mute	IntA/IntB FL/FR/RL/RR/ CE/SW RSEL/RSER	IntA/IntB FL/FR/RL/RR/C E/SW RSEL/RSER	IntA/IntB FL/FR RSEL/RSER	IntA/IntB FL/FR RSEL/RSER	disable	IntA/IntB FL/FR/RL/RR RSEL/RSER	IntA/IntB FL/FR/RL/RR RSEL/RSER	IntA/IntB FL/FR/RL/RR/ CE/SW RSEL/RSER	disable
Limiter	FL/FR/RL/RR/ CE/SW	FL/FR/RL/RR/C E/SW	FL/FR	FL/FR	disable	disable	disable	FL/FR/RL/RR/ CE/SW	disable
Volume(3) Fixed Level Control	IntA/IntB FL/FR/RL/RR/ CE/SW RSEL/RSER	IntA/IntB FL/FR/RL/RR/C E/SW RSEL/RSER	IntA/IntB FL/FR RSEL/RSER	IntA/IntB FL/FR RSEL/RSER	IntA/IntB FL/FR/RL/RR RSEL/RSER	IntA/IntB FL/FR/RL/RR RSEL/RSER	IntA/IntB FL/FR/RL/RR RSEL/RSER	IntA/IntB FL/FR/RL/RR/ CE/SW RSEL/RSER	disable
Mixing	FL/FR/RL/RR/ CE/SW	FL/FR/RL/RR/C E/SW	FL/FR	FL/FR	FL/FR/RL/RR	FL/FR/RL/RR	FL/FR/RL/RR	FL/FR/RL/RR/ CE/SW	FL/FR/RL/RR/ CE/SW
Output Selector	Enable	Enable	Enable	Enable	Enable	Enable	Enable	Enable	Enable

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC75056PE-H	PQFP100 14x20 / QIP100E (Pb-Free / Halogen Free)	50 / Tray Foam

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.