ANALOG DEVICES

EVAL-ADM3053EBZ User Guide
UG-234

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Evaluating the ADM3053 Signal and Power Isolated CAN Transceiver with Integrated Isolated DC-to-DC Converter

FEATURES

- Signal and power isolated ADM3053 CAN transceiver with *iso*Power integrated isolated dc-to-dc converter
- PCB layout optimized for low radiated emissions; passes EN55022 Class B (certification available)
- Standard 4-layer PCB solution for radiated emissions
- Screw terminal connectors for prototyping
  - Logic signals RXD and TXD
  - Power supply VCC and VIO
  - Bus signals CANH and CANL
  - PCB ground GND1 and GND2
- SMA connectors for TXD and RXD
- On-board LDO for 6 V to 9 V supply, providing 5 V on ADM3053 V_{CC} pin
- 5 V or 3.3 V operation on VIO
- Test points for logic signals, power supplies, grounds, and bus signals
- On-board 30 Ω + 30 Ω termination resistors to simulate full bus load (60 Ω)

EVALUATION KIT CONTENTS

EVAL–ADM3053EBZ evaluation board

DOCUMENTS NEEDED

ADM3053 data sheet

GENERAL DESCRIPTION

The EVAL-ADM3053EBZ allows for the simple evaluation of the ADM3053 signal and power isolated controller area network (CAN) transceivers. The evaluation board allows all of the input and output functions to be exercised without the need for external components.

The EVAL-ADM3053EBZ device employs Analog Devices, Inc., *i*Coupler® technology to combine a 2-channel isolator, a CAN transceiver, and an Analog Devices *iso*Power® dc-to-dc converter into a single small outline IC (SOIC) surface-mount package. An on-chip oscillator outputs a pair of square waveforms that drive an internal transformer to provide isolated power. The device is powered by a single 5 V supply, realizing a fully isolated CAN solution.

The ADM3053 contains *iso*Power technology that uses high frequency switching elements to transfer power through the transformer. For layout guidelines, see the AN-0971 Application Note.

For full details, see the ADM3053 data sheet, which must be used in conjunction with this user guide when using the evaluation board.

EVAL-ADM3053EBZ EVALUATION BOARD PHOTOGRAPH

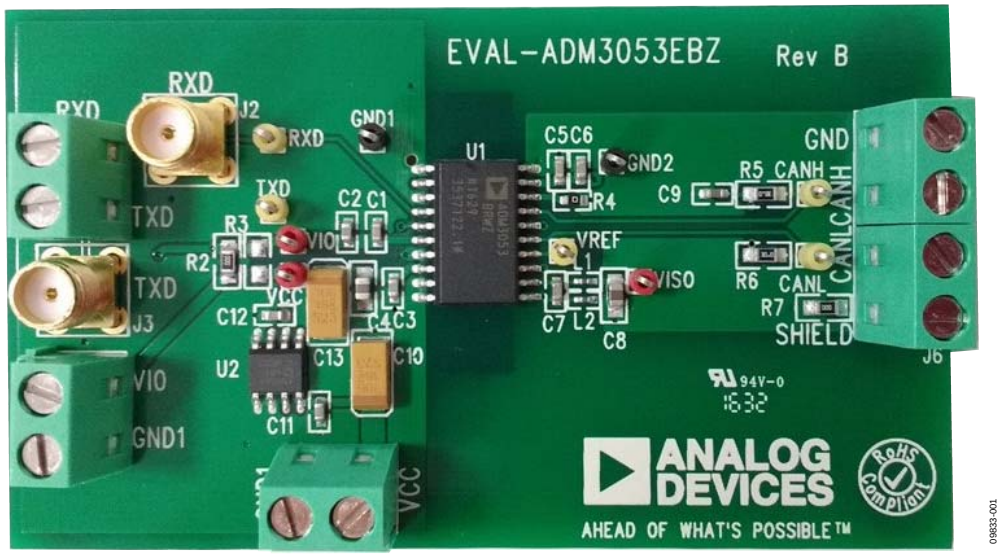


Figure 1.

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REVISION HISTORY

7/2017—Rev. 0 to Rev. A

Deleted ADM3053 Applications Section, Equipment Needed Section, and Functional Block Diagram Section 1
Changes to Features Section and Figure 1 1
Added Evaluation Kit Contents Section, Documents Needed Section, and Evaluation Board Photograph Section 1
Changes to Setting Up the Evaluation Board Section and Figure 3 3
Added Table 1, Renumbered Sequentially 3
Added Overlapping Stitching Capacitors Section, PCB Layout Recommendations Section, EN55022 Radiated Emissions Test Results Section, and Figure 4; Renumbered Sequentially 4
Added Figure 5, Figure 6, and Table 2 5
Changes to Figure 7 6
Deleted Figure 9 and Figure 10 6
Changes to Figure 8 and Figure 10 7
Added to Figure 9 7
Changes to Figure 11, Figure 12, and Figure 13 8
Changes to Table 3 and Related Links Section 9

7/2011—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

SETTING UP THE EVALUATION BOARD

The EVAL-ADM3053EBZ evaluation board default configuration is shown in Figure 3. In the default configuration, R2 is fitted with a 0 Ω resistor, and R3 is open, which allows VIO to be powered by 3.3 V or 5 V on J4, corresponding to the logic levels required for TXD and RXD. A power supply with a voltage of 6 V to 9 V is required on the input supply, Pin 8 (IN) of the on-board low dropout regulator, LDO (V_{CC} on J5). The on-board LDO generates the required 5 V to the ADM3053 V_{CC} pin. By fitting R3 with a 0 Ω resistor and removing R2, VIO of the EVAL-ADM3053EBZ is connected to the ADM3053 V_{CC} pin, and the complete board can be powered by a 9 V battery (for example, for electromagnetic current (EMC) testing).

VCC supplies power to the *iso*Power circuitry, and VIO supplies the *i*Coupler circuitry. Decoupling capacitors of values 0.1 µF and 10 µF are fitted to C3 and C4 between V_{CC} and GND1 and of values 0.01 µF and 0.1 µF to C1 and C2 between V_{IO} and GND1. On the bus side, it is required that V_{ISOIN} connect to V_{ISOOUT}. A 10 µF reservoir capacitor (C8) and a 0.1 µF decoupling capacitor (C7) are fitted between V_{ISOOUT} and GND2. Two 0.1 µF and 0.01 µF decoupling capacitors (C5 and C6) are fitted between V_{ISOIN} and GND2.

Resistor R4 connects the ADM3053 R_S pin to GND2 to adjust the slope of the CANH and CANL signals, as required. Resistor R4, by default, is a 0 Ω resistor for full speed operation. Replacing R4 with a 47 kΩ resistor (or similar) limits the slew rate of the CANH and CANL signals. By default, the R5 and R6 resistors load the ADM3053 CANH pin and CANL pin with 60 Ω (30 Ω + 30 Ω) to simulate a double terminated bus. If connecting two boards together, replace these values with 60 Ω + 60 Ω, or if connecting one board to a double terminated bus, remove both resistors (R5 and R6 not fitted). Table 1 shows parameters set by the on-board resistors.

Figure 3 shows an example operation of the EVAL–ADM3053EBZ. Connect a clock generator on TXD and set up a 500 kHz square wave clock with the output swinging between 0 V and 5 V. Connect the scope probes to the test points: TXD, RXD, CANH, and CANL. Figure 2 shows an example oscilloscope plot; Channel 1 shows the TXD signal, and Channel 2 and Channel 3 show the CANH and CANL signals.

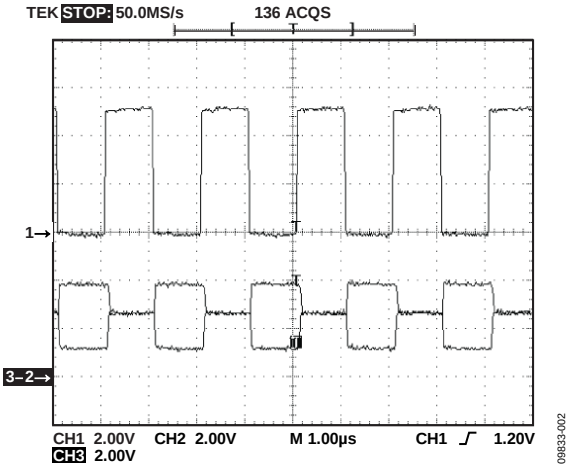


Figure 2. ADM3053 TXD, CANH, and CANL Signals

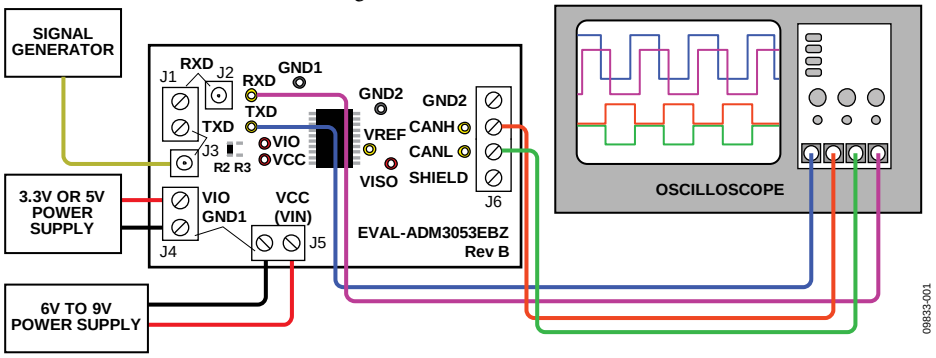


Figure 3. Basic Isolated CAN Transceiver Evaluation Board Operation

Table 1. Parameters Set by On-Board Resistors

Resistor(s)	Values	Default	Test Conditions/Comments
R2, R3	0 Ω for R2, R3 not fitted	Yes	V_{IO} connected to J4
	R2 not fitted, 0 Ω for R3	No	V_{IO} connected to the ADM3053 V_{CC}/5 V LDO output (J4 V_{IO} unconnected)
R4	0 Ω	Yes	ADM3053 in full speed mode
	47 kΩ	No	ADM3053 in slope control mode
R5, R6	Both 30 Ω	Yes	Simulates double terminated bus
	Both 60 Ω	No	Allows another node with 120 Ω termination to be connected
	Both not fitted	No	Allows a double terminated bus to be connected

OVERLAPPING STITCHING CAPACITOR

The evaluation board implements an embedded stitching capacitor structure. A printed circuit board (PCB) embedded stitching capacitor is created when two metal planes in a PCB overlap each other and are separated by dielectric material. This overlap is formed by extending the internal reference planes from the primary and secondary layers across the area that is used for creepage on the PCB surface. This capacitor provides a return path for high frequency common-mode noise currents across the isolation gap. The overlapping area is 24.9 mm × 6.3 mm, the distance between overlapping layers is ~0.7 mm; therefore, the plate capacitor is around 8.9 pF. For full details on the layout and implementation of embedded stitching capacitors, see the AN-0971 Application Note, *Recommendations for Control of Radiated Emissions with isoPower Devices*.

PCB LAYOUT RECCOMENDATIONS

The ADM3053 evaluation board reduces emissions generated by the high frequency switching elements used by the *iso*Power technology to transfer power through the integrated isolated dc-to-dc power supply. The layout of the evaluation board is generated using guidelines similar to those in the AN-1349 Application Note, *PCB Implementation Guidelines to Minimize Radiated Emissions on the ADM2582E/ADM2587E RS-485/ RS-422 Transceivers*.

To pass EN55022 Class B on a 4-layer PCB, the following layout guidelines are recommended:

- Best practice decoupling on the PCB per the ADM3053 data sheet.
- Place ferrite beads between the PCB trace/plane connections and the ADM3053 V_{ISOOUT} pin (Pin 12) and GND2 pins (Pin 11 and Pin 13).
- Do not connect the V_{ISOOUT} pin to a power plane; connect between the V_{ISOOUT} pin and the V_{ISOIN} pin using a PCB trace. Ensure V_{ISOOUT} (Pin 12) is connected first through the L1 ferrite before connecting to V_{ISOIN} (Pin 19), as shown in Figure 4.
- An embedded stitching capacitor between the GND1 PCB plane and GND2 Pin 11 and Pin 13 (inside L2 ferrite) using internal layers of the PCB planes as highlighted in the area around U1 in Figure 4 (see the Overlapping Stitching Capacitor section).

The following additional notes apply to the PCB layout; refer to the schematic and artwork in Figure 7 to Figure 13.

- Ensure that GND2 (Pin 13) is connected to GND2 (Pin 11) on the inside (device side) of the C7 100 nF capacitor.
- Ensure that the C7 capacitor is connected between V_{ISOOUT} (Pin 12) and GND2 (Pin 11) on the device side of the L1 and L2 ferrite beads.
- Ensure that GND2 (Pin 16) is connected to the main bus side PCB ground plane outside of the L2 ferrite, as shown in Figure 4.
- Ensure that there is a keep out area in the PCB layout around the L1 and L2 ferrites (no PCB planes under or alongside L1 and L2).

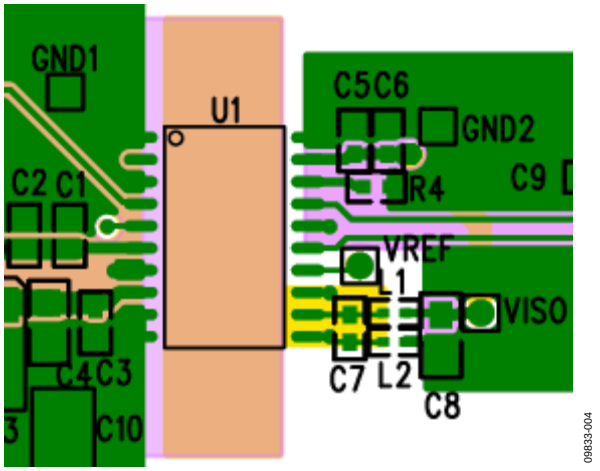


Figure 4. Layout Notes for EVAL-ADM3053EBZ

- Locate the power delivery circuit in close proximity to the ADM3053 device, to ensure that the V_{CC} trace is as short as possible. The EVAL-ADM3053EBZ PCB has a power delivery circuit located at the bottom of the PCB with a short trace from the ADP667ARZ regulator output (U3) to V_{CC} (Pin 8). This layout example minimizes the loop area in which high frequency current can flow. An increase in the loop area results in an increase in the emissions levels.

EN55022 RADIATED EMISSIONS TEST RESULTS

The EVAL-ADM3053EBZ evaluation board is tested and certified to pass EN55022 Class B with a 2.48 dB µV/m margin. EN55022 certification documents for the EVAL-ADM3053EBZ evaluation board is available to users upon request from Analog Devices. Table 2 provides a summary of the results. All EN55022 radiated emissions tests are performed with the PCB schematic and layout as described in Figure 7 to Figure 13.

The EVAL-ADM3053EBZ evaluation boards are configured and tested with 5.0 V power supplied to the ADM3053 V_{IO} pin and V_{CC} pin, with the power supplied from the ADP667ARZ regulator output. The ADP667ARZ regulator input is supplied from a standard 9 V battery. Testing is performed with an active 500 kbps clock on the TXD pin supplied by an on-board oscillator fitted to U2. The ADM3053 CAN bus pins are loaded with a 60 Ω termination resistor (per a double terminated bus). Measurements are carried out in an anechoic chamber at 10 m from 30 MHz to 3 GHz. Figure 5 and Figure 6 show the results of the peak horizontal and vertical scans, and Table 2 shows the tabulated quasi-peak (QP) results.

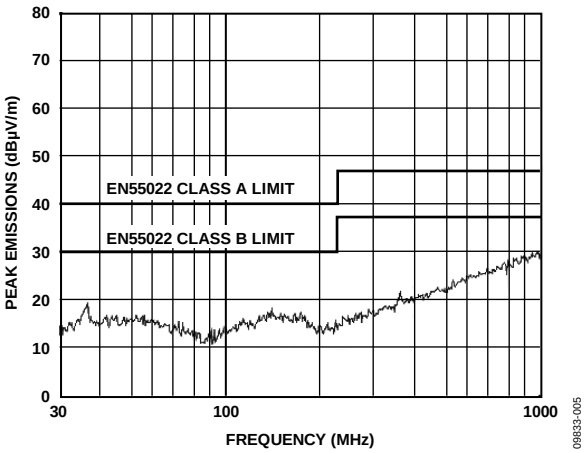


Figure 5. Horizontal Scan From 30 MHz to 1000 MHz

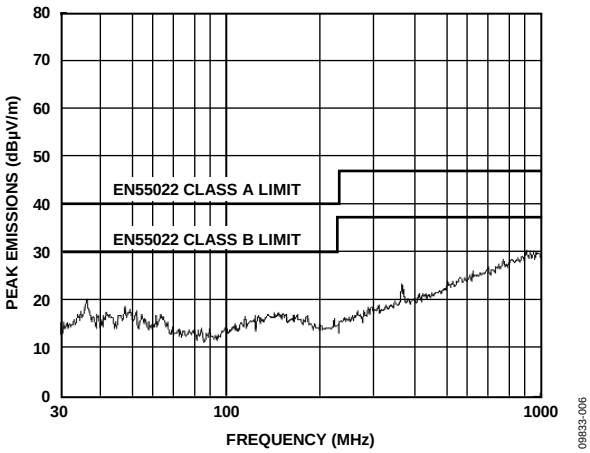


Figure 6. Vertical Scan from 30 MHz to 1000 GHz

Table 2. ADM3053 Test Results (Quasi-Peak Measurements)

Frequency (MHz)	QP Level dB (µV/m)	EN55022 Class B dB (µV/m)	Antenna Position	Antenna Height (m)	Pass/Fail
182.330	17.5	30	Horizontal	4.00	Pass
364.902	31.9	37	Horizontal	2.50	Pass
182.027	12.0	30	Vertical	1.00	Pass
364.058	22.1	37	Vertical	1.50	Pass

EVALUATION BOARD SCHEMATICS AND ARTWORK

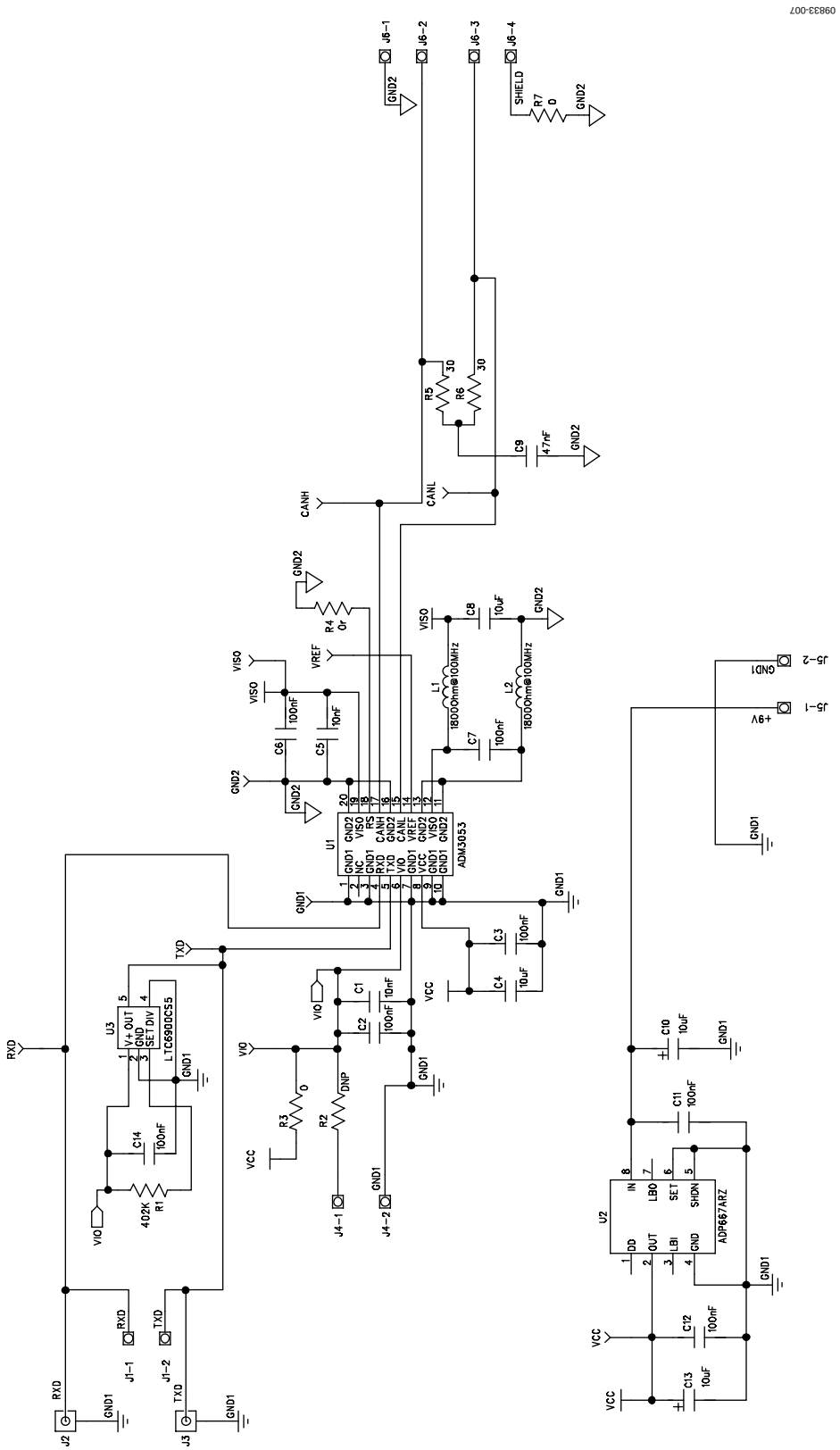


Figure 7. EVAL-ADM3053EBZ Evaluation Board Schematic

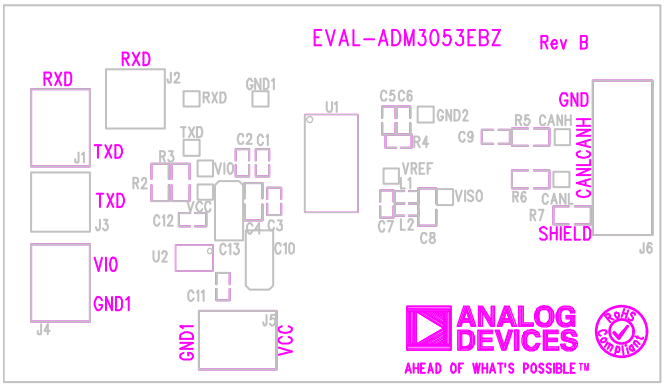


Figure 8. EVAL-ADM3053EBZ Evaluation Board Silkscreen (Top)

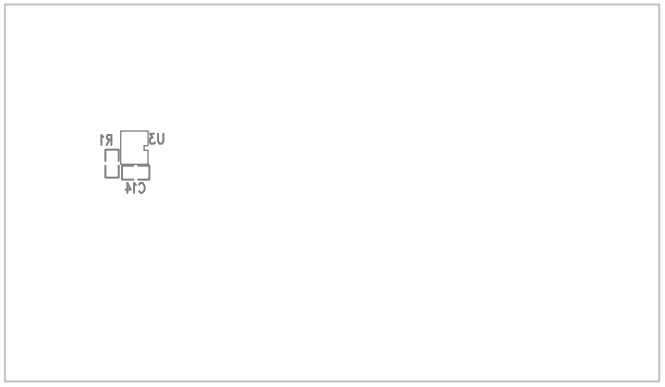


Figure 9. EVAL-ADM3053EBZ Evaluation Board Silkscreen (Bottom)

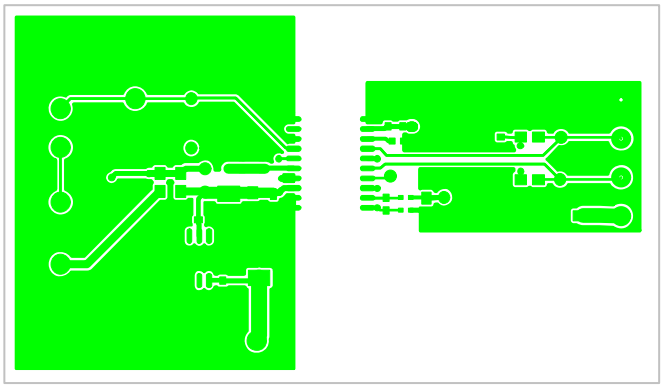


Figure 10. EVAL-ADM3053EBZ Evaluation Board Component Side

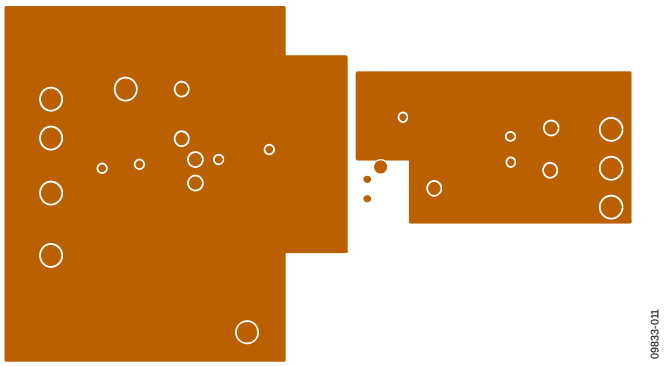


Figure 11. EVAL-ADM3053EBZ Evaluation Board Layer 2

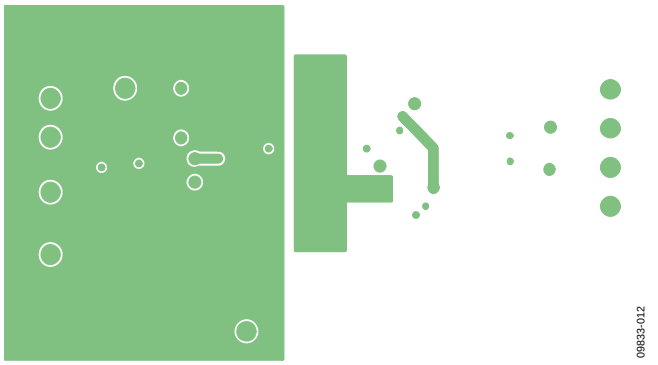


Figure 12. EVAL-ADM3053EBZ Evaluation Board Layer 3

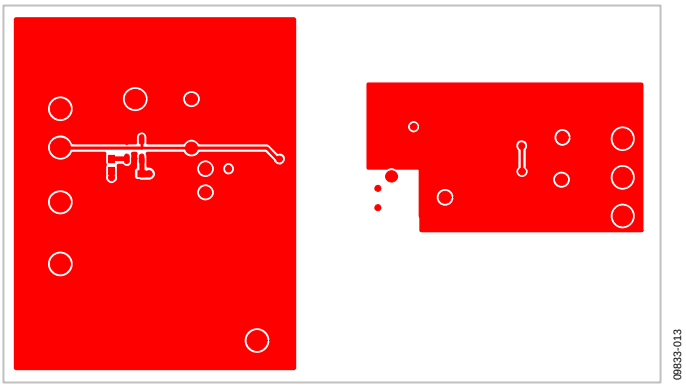


Figure 13. EVAL-ADM3053EBZ Evaluation Board Solder Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Quantity	Name	Description	Supplier	Part No.
2	C1, C5	Capacitor, X7R, 10 nF, 0603	Multicomp	MC0603B103K160CT
6	C2, C3, C6, C7, C11, C12	Capacitor, X7R, 100 nF, 0603	Multicomp	MC0603B104K160CT
2	C4, C8	Capacitor, X7R, 10 µF, 0805	AVX	0805ZC106KAT2A
1	C9	Capacitor, X7R, 47 nF, 0603	Multicomp	MC0603B473K500CT
2	C10, C13	Capacitor, tantalum, 10 µF, Case C	Kemet	B45196E3106K309
1	C14 (not placed)	Capacitor, X7R, 100 nF (optional)	Multicomp	MC0603B104K160CT
3	J1, J4, J5	2-pin terminal block	Lumberg	KRM 02
2	J2, J3	SMA, straight jack	TE Connectivity	5-1814832-1
1	J6	4-pin terminal block	Lumberg	KRM 04
2	L1, L2	Ferrite bead, 1.8 kΩ at 100 MHz	Murata	BLM15HD182SN1D
1	R1 (not placed)	Resistor, 402 kΩ, 0603 (optional)	Multicomp	MC0063W06031402K
1	R2, R7	Resistor, 0 Ω, 0805	Vishay Draloric	CRCW08050000ZSTA
1	R3 (not placed)	Resistor, 0 Ω, 0805 (optional)	Vishay Draloric	CRCW08050000ZSTA
1	R4	Resistor, 0 Ω, 0603	Multicomp	MC0063W06030R
2	R5, R6	Resistor, thick film, 30 Ω, 0.5 W, 0805	Panasonic	ERJP06F30R0V
5	CANH, CANL, RXD, TXD, VREF	Test point, yellow	Vero	20-313140
2	GND1, GND2	Test point, black	Vero	20-2137
3	VCC, VIO, VISO	Test point, red	Vero	20-313137
1	U1	ADM3053 isolated CAN transceiver with *iso*Power integrated dc-to-dc converter	Analog Devices	ADM3053BRWZ
1	U2	5 V fixed, adjustable low dropout linear voltage regulator	Analog Devices	ADP667ARZ
1	U3 (not placed)	Oscillator, 1 kHz to 20 MHz (optional)	Linear Technology	LTC6900CS5#TRMPBF

RELATED LINKS

Resource	Description
ADM3053	Signal and Power isolated CAN Transceiver with Integrated Isolated DC-to-DC Converter
AN-1349	PCB Implementation Guidelines to Minimize Radiated Emissions on the ADM2582E/ADM2587E RS-485/RS-422 Transceivers
AN-1123	Controller Area Network (CAN) Implementation Guide
AN-0971	Recommendations for Control of Radiated Emissions with *iso*Power Devices

NOTES



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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