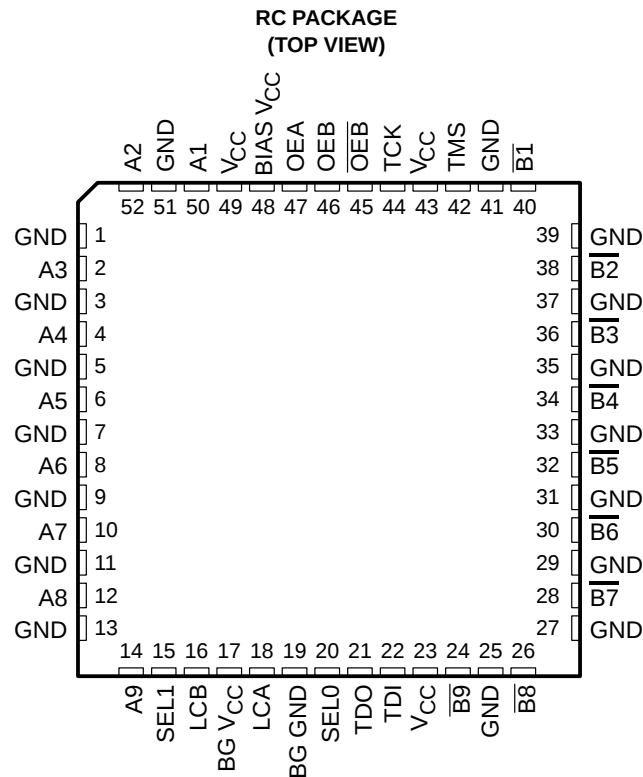


SN74FB2031 9-BIT TTL/BTL ADDRESS/DATA TRANSCEIVER

SCBS176N – NOVEMBER 1991 – REVISED JUNE 2001

- Compatible With IEEE Std 1194.1-1991 (BTL)
- TTL A Port, Backplane Transceiver Logic (BTL) $\bar{B}$ Port
- Open-Collector $\bar{B}$ -Port Outputs Sink 100 mA
- High-Impedance State During Power Up and Power Down
- BIAS V_{CC} Minimizes Signal Distortion During Live Insertion or Withdrawal
- $\bar{B}$ -Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage
- TTL-Input Structures Incorporate Active Clamping to Aid in Line Termination



description

The SN74FB2031 is a 9-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments. The device is designed specifically to be compatible with IEEE Std 1194.1-1991.

The $\bar{B}$ port operates at BTL-signal levels. The open-collector $\bar{B}$ ports are specified to sink 100 mA. Two output enables (OEB and $\overline{OEB}$) are provided for the $\bar{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is less than 2.1 V, the $\bar{B}$ port is turned off.

The A port operates at TTL signal levels. The A outputs reflect the inverse of the data at the $\bar{B}$ port when the A-port output enable (OEA) is high. When OEA is low or V_{CC} is less than 2.1 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE Std 1149.1 (JTAG) test bus, although currently there are no plans to release a JTAG-featured version. TMS and TCK are not connected and TDI is shorted to TDO.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN74FB2031

9-BIT TTL/BTL ADDRESS/DATA TRANSCEIVER

SCBS176N – NOVEMBER 1991 – REVISED JUNE 2001

description (continued)

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFP – RC	Tube	SN74FB2031RC	FB2031

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

TRANSCEIVER

INPUTS			FUNCTION
OEA	OEB	$\overline{OEB}$	
L	H	L	$\overline{A}$ data to B bus
H	L	X	$\overline{B}$ data to A bus
H	X	H	
H	H	L	$\overline{A}$ data to B bus, $\overline{B}$ data to A bus
L	L	X	Isolation
L	X	H	

STORAGE MODE

LCA, LCB	RESULT
0	Transparent
1	Latches latched
↑	Flip-flops triggered

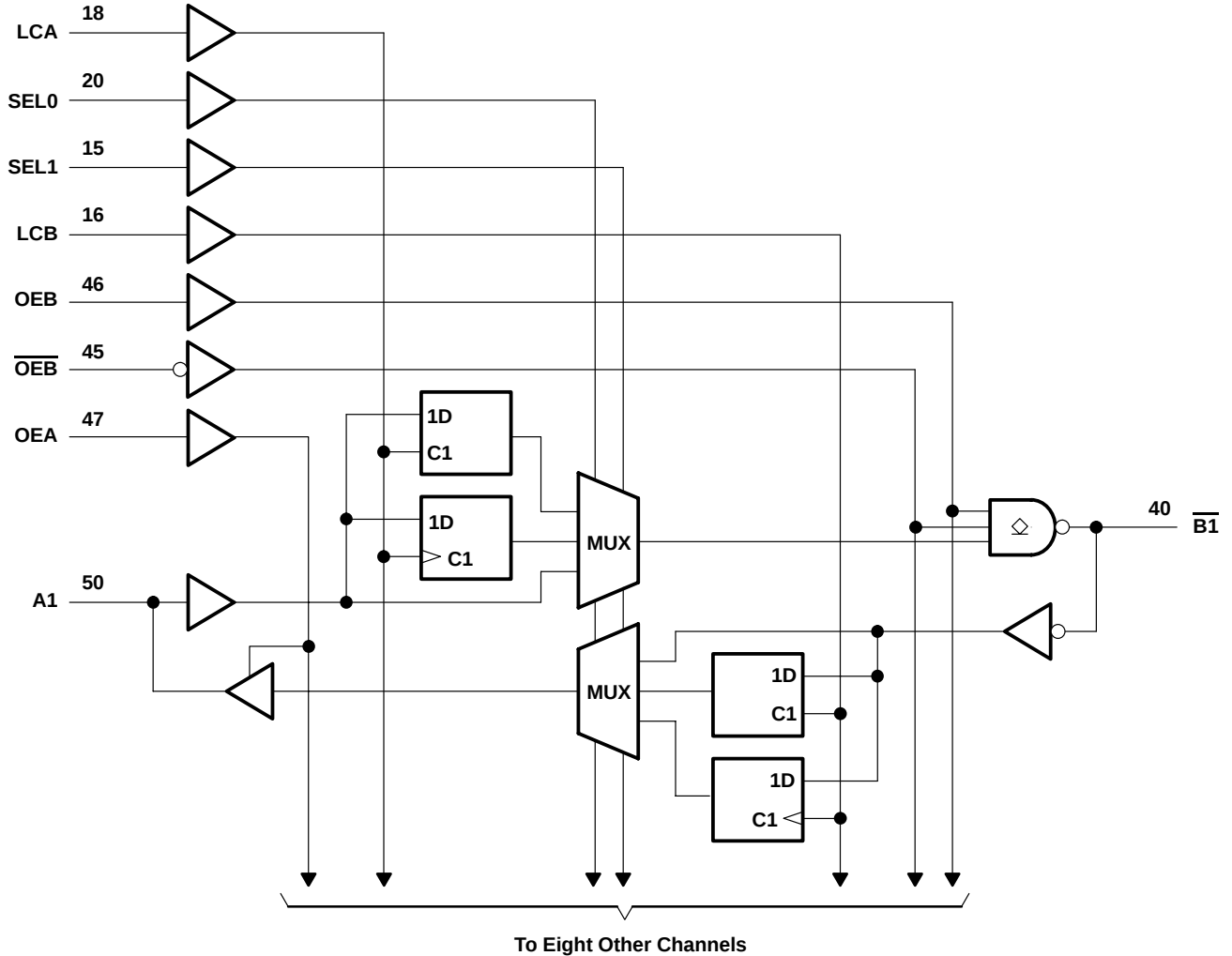
SELECT

SEL1	SEL0	MUX A→B	MUX B→A
0	0	Latch	Latch
0	1	Through	Through
1	0	Flip-flop	Flip-flop
1	1	Flip-flop	Latch



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functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I : Except $\overline{B}$ port	–1.2 V to 7 V
$\overline{B}$ port	–1.2 V to 3.5 V
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, V_O	–0.5 V to 3.5 V
Voltage range applied to any output in the high state, V_O	–0.5 V to V_{CC}
Input clamp current, I_{IK} : Except $\overline{B}$ port	–40 mA
$\overline{B}$ port	–18 mA
Current applied to any single output in the low state, I_O : A port	48 mA
$\overline{B}$ port	200 mA
Package thermal impedance, θ_{JA} (see Note 1)	44°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

SN74FB2031

9-BIT TTL/BTL ADDRESS/DATA TRANSCEIVER

SCBS176N – NOVEMBER 1991 – REVISED JUNE 2001

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC} , BIAS V_{CC} , BG V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port Except $\overline{B}$ port	1.62 2	2.3	V
V_{IL}	Low-level input voltage	$\overline{B}$ port Except $\overline{B}$ port	0.75 0.8	1.47	V
I_{OH}	High-level output current	A port		–3	mA
I_{OL}	Low-level output current	A port $\overline{B}$ port		24 100	mA
T_A	Operating free-air temperature	0		70	°C

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to V_{CC} (5 V) or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{IK}	$\overline{B}$ port	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			–1.2	V
	Except $\overline{B}$ port	$V_{CC} = 4.5$ V,	$I_I = -40$ mA			–0.5	
V_{OH}	A port	$V_{CC} = 4.5$ V,	$I_{OH} = -3$ mA	2.5	3.3		V
V_{OL}	A port	$V_{CC} = 4.5$ V,	$I_{OL} = 24$ mA		0.35	0.5	V
	$\overline{B}$ port	$V_{CC} = 4.5$ V	$I_{OL} = 80$ mA	0.75		1.1	
			$I_{OL} = 100$ mA			1.15	
I_I	Except $\overline{B}$ port	$V_{CC} = 5.5$ V,	$V_I = 5.5$ V			50	μA
$I_{IH}^{\ddagger}$	Except $\overline{B}$ port	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			50	μA
$I_{IL}^{\ddagger}$	Except $\overline{B}$ port	$V_{CC} = 5.5$ V,	$V_I = 0.5$ V			–50	μA
	$\overline{B}$ port	$V_{CC} = 5.5$ V,	$V_I = 0.75$ V			–100	μA
I_{OZH}	A port	$V_{CC} = 2.1$ V to 5.5 V,	$V_O = 2.7$ V			50	μA
I_{OZL}	A port	$V_{CC} = 2.1$ V to 5.5 V,	$V_O = 0.5$ V			–50	μA
I_{OZPU}	A port	$V_{CC} = 0$ to 2.1 V,	$V_O = 0.5$ V to 2.7 V			50	μA
I_{OZPD}	A port	$V_{CC} = 2.1$ V to 0,	$V_O = 0.5$ V to 2.7 V			–50	μA
I_{OH}	$\overline{B}$ port	$V_{CC} = 0$ to 5.5 V,	$V_O = 2.1$ V			100	μA
$I_{OS}^{\S}$	A port	$V_{CC} = 5.5$ V,	$V_O = 0$	–30		–150	mA
I_{CC}	A port to $\overline{B}$ port	$V_{CC} = 5.5$ V,	$I_O = 0$			78	mA
	$\overline{B}$ port to A port					78	
C_i		$V_I = 0.5$ V or 2.5 V			4.5		pF
C_{io}	A port	$V_O = 0.5$ V or 2.5 V			8.5		pF
	$\overline{B}$ port per IEEE Std 1194.1-1991	$V_{CC} = 0$ to 5.5 V				6	

[†] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I _{CC} (BIAS V _{CC})		V _{CC} = 0 to 4.5 V	V _B = 0 to 2 V, V _I (BIAS V _{CC}) = 4.5 V to 5.5 V	450		μA
		V _{CC} = 4.5 V to 5.5 V		10		
V _O	B̄ port	V _{CC} = 0, V _I (BIAS V _{CC}) = 5 V		1.62	2.1	V
I _O	B̄ port	V _{CC} = 0, V _B = 1 V, V _I (BIAS V _{CC}) = 4.5 V to 5.5 V		−1		μA
		V _{CC} = 0 to 5.5 V, OEB = 0 to 0.8 V		100		
		V _{CC} = 0 to 2.2 V, OEB = 0 to 5 V		100		

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				MIN	MAX	UNIT
f _{clock}	Clock frequency			150		MHz
t _w	Pulse duration		LCA or LCB		3.3	ns
t _{su}	Setup time		Clock mode	Data before LCA↑	1.4	ns
				Data before LCB↑	2.8	
			Latch mode	Data before LCA↑	1.1	
				Data before LCB↑	2.4	
t _h	Hold time		Clock mode	Data after LCA↑	0.6	ns
				Data after LCB↑	0	
			Latch mode	Data after LCA↑	0.9	
				Data after LCB↑	0	

SN74FB2031

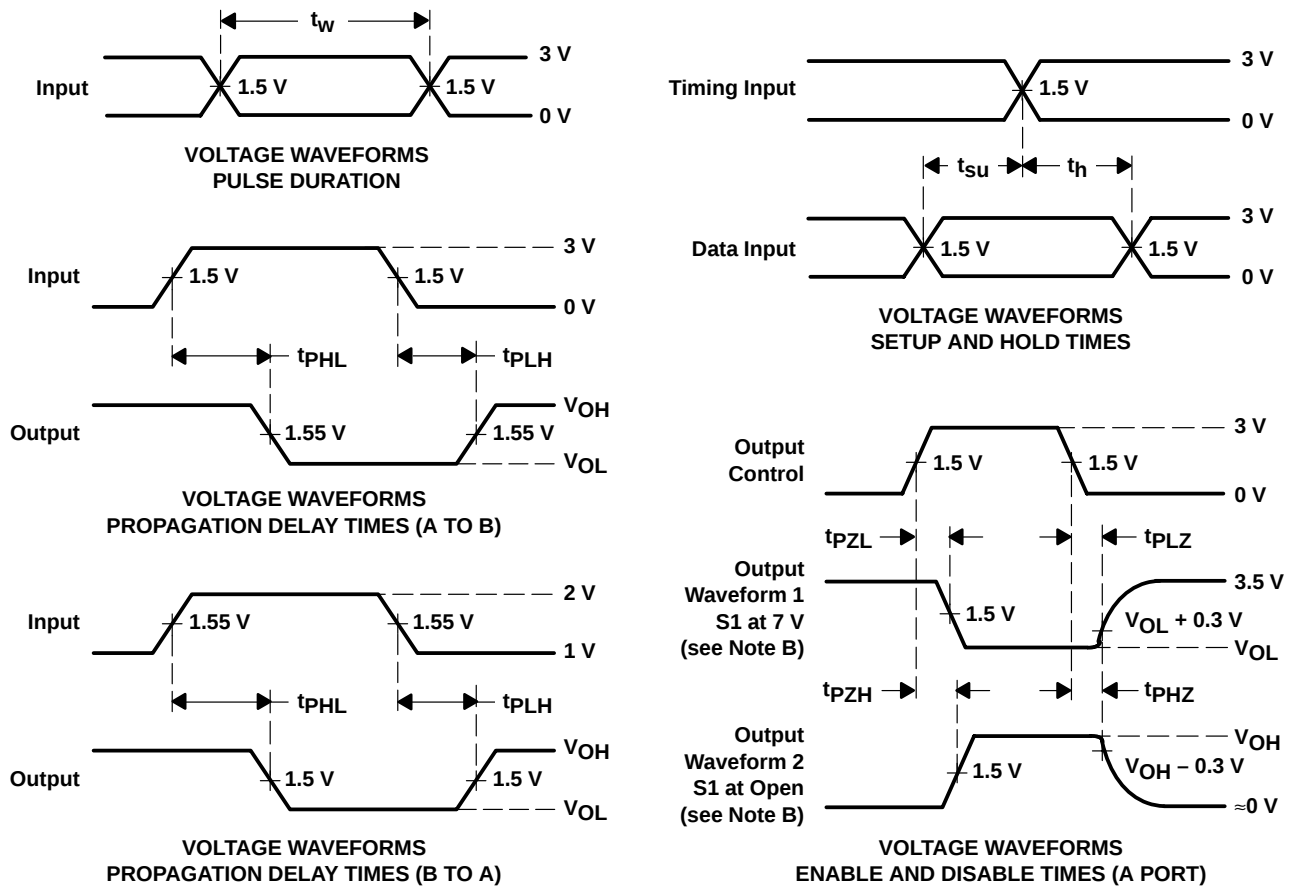
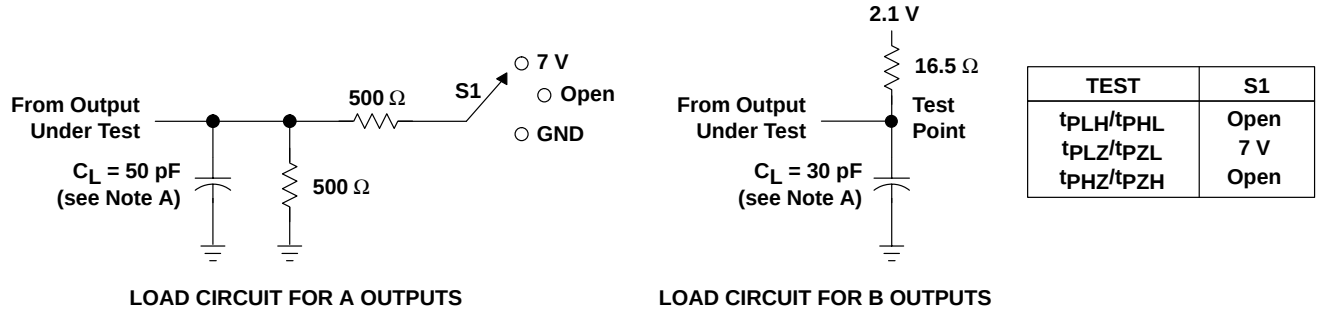
9-BIT TTL/BTL ADDRESS/DATA TRANSCEIVER

SCBS176N – NOVEMBER 1991 – REVISED JUNE 2001

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V},$ $T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$f_{\max}$			150			150		MHz
t_{PLH}	A (through mode)	$\overline{B}$	3.7	4.5	5.9	3.2	6.6	ns
t_{PHL}			2.9	4	5.7	2.6	5.9	
t_{PLH}	A (transparent)	$\overline{B}$	4.1	5	6.5	3.6	7.3	ns
t_{PHL}			3.3	4.5	6.1	3	6.5	
t_{PLH}	LCA	$\overline{B}$	4.5	5.4	7	3.9	7.8	ns
t_{PHL}			4	5.1	6.7	3.4	7.4	
t_{PLH}	LCB	A	2.8	3.7	4.7	1.9	6	ns
t_{PHL}			2.5	3.4	4.9	1.8	5.5	
t_{PLH}	SEL1 or SEL0	A	2.5	3.8	5.3	1.9	6.3	ns
t_{PHL}			2.2	3.5	5.1	1.6	5.6	
t_{PLH}	SEL1 or SEL0	$\overline{B}$	4.1	5.3	6.9	3.7	7.8	ns
t_{PHL}			3.7	5.2	6.9	3.3	7.7	
t_{PLH}	$\overline{B}$ (through mode)	A	3.1	4	5.6	2.2	7.1	ns
t_{PHL}			2.6	3.4	4.9	1.4	5.7	
t_{PLH}	$\overline{B}$ (transparent)	A	3.3	4.2	5.9	2.4	7.6	ns
t_{PHL}			2.8	3.9	5.5	1.8	6.3	
t_{PLH}	OEB or $\overline{OEB}$	$\overline{B}$	3.7	4.6	6.1	3.2	6.7	ns
t_{PHL}			2.9	4.3	5.8	2.5	6.4	
t_{PZH}	OEA	A	2.3	3.1	4.5	1.6	5	ns
t_{PZL}			1.9	2.7	4.1	1.6	4.4	
t_{PHZ}	OEA	A	2.2	3.1	4.5	1.5	5.2	ns
t_{PLZ}			2.5	3.3	4.9	2	5.2	
$t_{sk(p)}$ Pulse skew	A	$\overline{B}$	0.5					ns
	$\overline{B}$	A	0.3					
$t_{sk(o)}$ Output skew	A	$\overline{B}$	0.2					ns
	$\overline{B}$	A	0.3					
t_t	Transition time, $\overline{B}$ outputs (1.3 V to 1.8 V)		0.6	2	2.8	0.4	2.9	ns
	Transition time, A outputs (10% to 90%)		0.5	3.5	4.7	0	5.4	
$t_{(pr)}$	$\overline{B}$ -port input pulse rejection		1			1		ns

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: TTL inputs: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$; BTL inputs: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74FB2031RCRG3	NRND	QFP	RC	52	500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	0 to 70	FB2031	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74FB2031RCRG3	QFP	RC	52	500	330.0	24.4	14.2	14.2	2.6	24.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

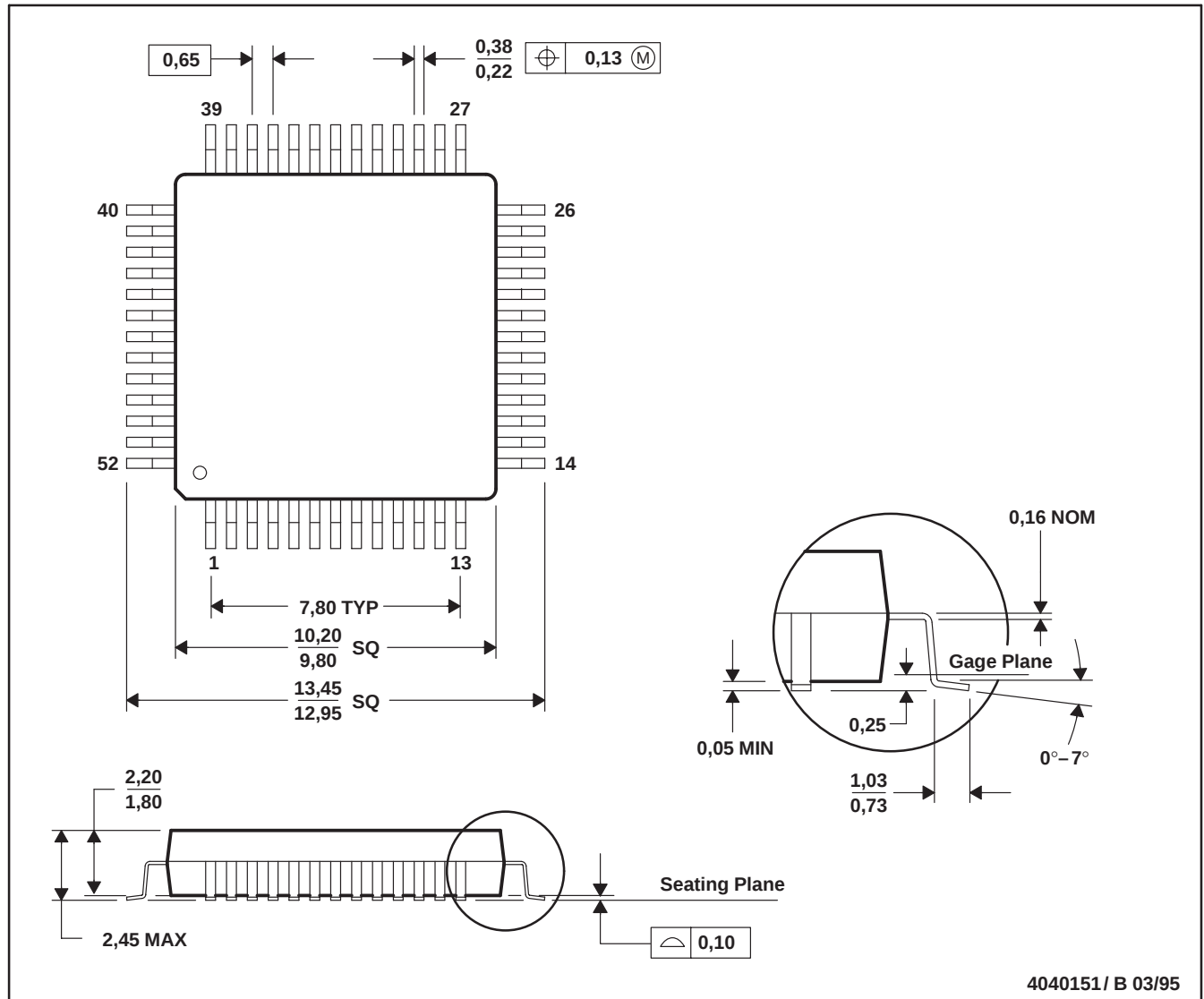


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74FB2031RCRG3	QFP	RC	52	500	350.0	350.0	43.0

RC (S-PQFP-G52)

PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-022

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