L99DZ70XP

Door actuator driver

Features

- One full bridge for 6 A load (R_{on} = 150 mΩ)
- Two half bridges for 3 A load (R_{on} = 300 mΩ)
- Two half bridges for 0.75 A load (R_{on} = 1600 mΩ)
- One highside driver for 6 A load (R_{on} = 90 mΩ)
- Two configurable highside drivers for up to 1.5 A load (R_{on} = 500 mΩ) or 0.4 A (R_{on} = 1800 mΩ)
- Two highside drivers for 0.5 A load (R_{on} = 1600 mΩ)
- Programmable softstart function to drive loads with higher inrush currents as current limitation value
- Very low current consumption in standby mode (I_S < 6 µA typ; $T_j \leq 85$ °C; I_{CC} < 5 µA typ; $T_j \leq 85$ °C)
- Current monitor output for all highside drivers
- Device contains temperature warning and protection
- Openload detection for all outputs
- Over-current protection for all otputs
- Separated half bridges for door lock motor
- PWM control of all outputs
- Charge pump output for reverse polarity protection
- STM standard serial peripheral interface (ST-SPI 3.0)
- Control block for electrochromic element



PowerSSO-36

Applications

- Door actuator driver with 6 bridges for double door lock control, mirror fold and mirror axis control, highside driver for mirror defroster, bulbs and LEDs (replacement for L9950). Control block with external MOS transistor for charging / discharging of electrochromic glass.

Description

The L99DZ70XP is a microcontroller driven multifunctional door actuator driver for automotive applications. Up to five DC motors and five grounded resistive loads can be driven with six half bridges and five highside drivers. An electrochromic mirror glass can be controlled using the integrated SPI-driven module in conjunction with an external MOS transistor. The integrated SPI controls all operating modes (forward, reverse, brake and high impedance). Also all diagnostic information is available via SPI read.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36	L99DZ70XP	L99DZ70XPTR

Contents

1 **Block diagram and pin description 6**

2 **Electrical specifications 10**

2.1 Absolute maximum ratings 10

2.2 ESD protection 10

2.3 Thermal data 11

2.4 Electrical characteristics 11

2.4.1 Outputs OUT1 - OUT11, ECV 13

2.5 SPI - Electrical characteristics 18

3 **Application information 24**

3.1 Dual power supply: VS and VCC 24

3.2 Wake up and active mode / standby mode 24

3.3 Charge pump 24

3.4 Diagnostic functions 24

3.5 Overvoltage and undervoltage detection at V_S 25

3.6 Overvoltage and undervoltage detection at V_{CC} 25

3.7 Temperature warning and thermal shutdown 25

3.8 Inductive loads 25

3.9 Open load detection 26

3.10 Over-load detection 26

3.11 Current monitor 26

3.12 PWM inputs 26

3.13 Cross-current protection 27

3.14 Programmable soft-start function to drive loads with higher inrush current 27

3.15 Controller for electrochromic glass 28

4 **Functional description of the SPI 29**

4.1 General description 29

4.1.1 Chip Select Not (CSN) 29

4.1.2 Serial Data In (DI) 29

4.1.3 Serial Clock (CLK) 29
4.1.4 Serial Data Out (DO) 29
4.1.5 SPI communication flow 30
4.2 Command byte 31
4.2.1 Operation code definition 31
4.3 Global status byte 32
4.4 Address mapping 33

5 SPI - control and status registers 34
5.1 Control register 0 34
5.2 Control register 1 35
5.3 Control register 2 36
5.4 Control register 3 37
5.5 Status register 0 38
5.6 Status register 1 39
5.7 Status register 2 40
5.8 Configuration register 41

6 Packages thermal data 42

7 Package and packing information 43
7.1 ECOPACK® packages 43
7.2 PowerSSO-36 package information 43
7.3 PowerSSO-36 packing information 45

8 Revision history 46

List of tables

Table 1. Device summary . . . 1
Table 2. Pin definition and functions . . . 6
Table 3. Absolute maximum ratings . . . 10
Table 4. ESD protection . . . 10
Table 5. Operating junction temperature . . . 11
Table 6. Temperature warning and thermal shutdown . . . 11
Table 7. Supply . . . 11
Table 8. Overvoltage and under voltage detection . . . 12
Table 9. Current monitor output CM / PWM 2 . . . 12
Table 10. Charge pump output CP . . . 13
Table 11. On-resistance and switching times . . . 13
Table 12. Current monitoring . . . 16
Table 13. Electrochrome control . . . 17
Table 14. Delay time from standby to active mode . . . 19
Table 15. Inputs: CSN, CLK, PWM1/2 and DI . . . 19
Table 16. SDI timing . . . 19
Table 17. DO . . . 20
Table 18. DO timing . . . 20
Table 19. CSN timing . . . 21
Table 20. SPI frame . . . 31
Table 21. Operation code definition . . . 31
Table 22. Global status byte . . . 32
Table 23. RAM memory map . . . 33
Table 24. ROM memory map . . . 33
Table 25. Control register 0 (read/write) . . . 34
Table 26. Control register 1 (read/write) . . . 35
Table 27. Control register 2 (read/write) . . . 36
Table 28. Control register 3 (read/write) . . . 37
Table 29. Status register 0 (read) . . . 38
Table 30. Status register 1 (read) . . . 39
Table 31. Status register 2 (read) . . . 40
Table 32. Configuration register (read/write) . . . 41
Table 33. PowerSSO-36 mechanical data . . . 44
Table 34. Document revision history . . . 46

List of figures

Figure 1. Block diagram . . . 6
Figure 2. Configuration diagram (top view) . . . 9
Figure 3. Electrochrome control block diagram . . . 18
Figure 4. SPI - Transfer timing diagram . . . 21
Figure 5. SPI - Input timing . . . 21
Figure 6. SPI - DO valid data delay time and valid time . . . 22
Figure 7. SPI - DO enable and disable time . . . 22
Figure 8. SPI - driver turn on/off timing, minimum CSN HI time . . . 23
Figure 9. Example of programmable soft-start function for inductive loads . . . 27
Figure 10. Write and read SPI . . . 30
Figure 11. Global error flag definition . . . 33
Figure 12. Packages thermal data . . . 42
Figure 13. PowerSSO-36 package dimensions . . . 43
Figure 14. PowerSSO-36 tube shipment (no suffix) . . . 45
Figure 15. PowerSSO-36 tape and reel shipment (suffix “TR”) . . . 45

1 Block diagram and pin description

Figure 1. Block diagram

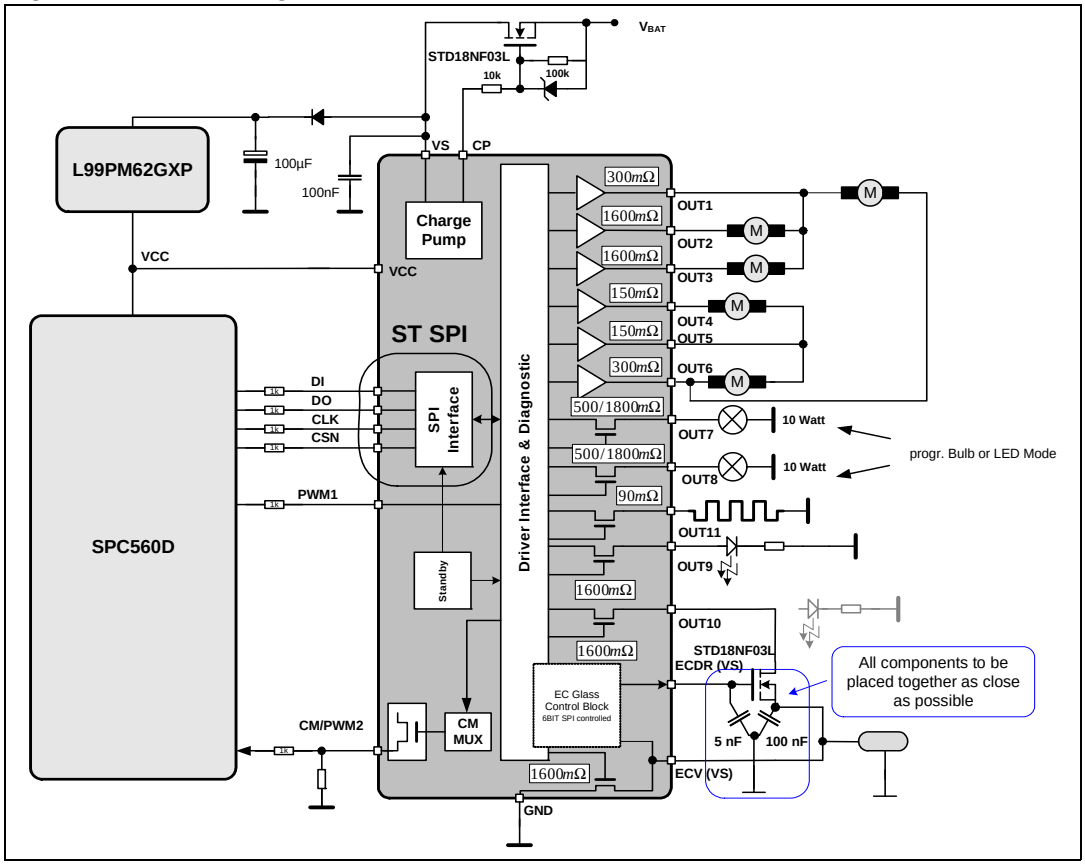


Table 2. Pin definition and functions

Pin	Symbol	Function
1, 18, 19, 36	GND	Ground: reference potential. *Important:* For the capability of driving the full current at the outputs all pins of GND must be externally connected!
2, 35	OUT11	Highside driver output 11. The output is built by a highside switch and is intended for resistive loads, therefore the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present, but the energy which can be dissipated is limited. The highside driver is a power DMOS transistor with an internal parasitic reverse diode from the output to VS (bulk-drain-diode). The output is over-current protected. *Important:* for the capability of driving the full current at the outputs both pins of OUT11 must be externally connected!

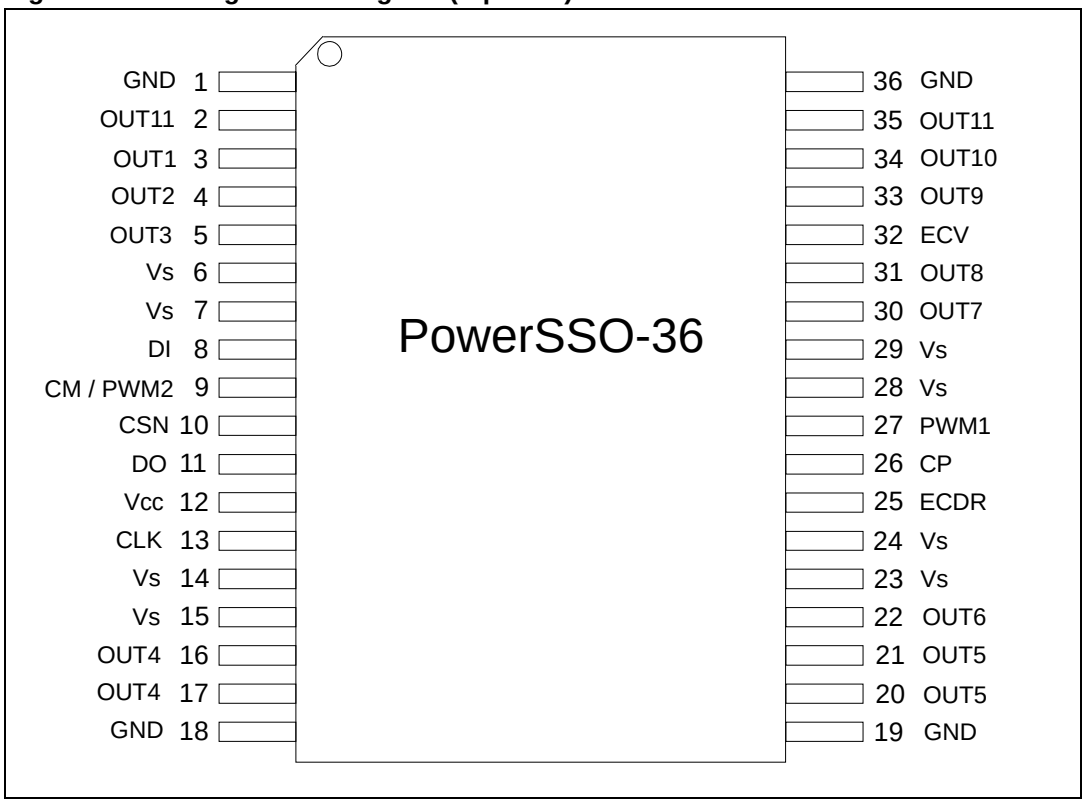
Table 2. Pin definition and functions (continued)

Pin	Symbol	Function
3 4 5	OUT1, OUT2, OUT3	Halfbridge outputs 1,2,3. The output is built by a highside and a lowside switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: highside driver from output to VS, lowside driver from GND to output). This output is over-current protected.
6, 7, 14, 15, 23, 24, 28, 29	V_S	Power supply voltage (external reverse protection required). For this input a ceramic capacitor as close as possible to GND is recommended. *Important:* For the capability of driving the full current at the outputs all pins of VS must be externally connected!
8	DI	Serial data input. The input requires CMOS logic levels and receives serial data from the microcontroller. The data is a 24 bit control word and the most significant bit (MSB, bit 23) is transferred first.
9	CM/ PWM2	Current monitor output/PWM2 input. Depending on the selected multiplexer bits of the control register this output sources an image of the instant current through the corresponding highside driver with a ratio of 1/10.000 or 1/2000. This pin is bidirectional. The microcontroller can overdrive the current monitor signal to provide a second PWM input for the outputs OUT5, OUT8 and OUT10.
10	CSN	Chip Select Not input / Testmode. This input is low active and requires CMOS logic levels. The serial data transfer between L99DZ70 and the microcontroller is enabled by pulling the input CSN to low level.
11	DO	Serial data output. The diagnosis data is available via the SPI and this tristate-output. The output will remain in tristate, if the chip is not selected by the input CSN (CSN = high)
12	VCC	Supply voltage. For this input a ceramic capacitor as close as possible to GND is recommended.
13	CLK	Serial clock input. This input controls the internal shift register of the SPI and requires CMOS logic levels.
16,17 20,21 22	OUT4, OUT5, OUT6	Halfbridge outputs 4,5,6: see OUT1 (pin 3). *Important:* For the capability of driving the full current at the outputs both pins of OUT4 (OUT5, respectively) must be externally connected!
25	ECDR	Electrocromic driver output. If the electrochrome mode is selected this pin is used to control the gate of an external MOSFET, otherwise it remains in high-impedance state. *Note:* It is possible to connect the pin to VS as in L9950/53/54 applications, as long as the electrochome mode is not enabled via SPI.
26	CP	Charge pump output. This output is provided to drive the gate of an external n-channel power MOS used for reverse polarity protection (see *Figure 1.*).

Table 2. Pin definition and functions (continued)

Pin	Symbol	Function
27	PWM1	PWM1 input. This input signal can be used to control the drivers OUT1-4, OUT6-7, OUT9 and OUT11 and ECV by an external PWM signal.
30 31	OUT7, OUT8,	Highside driver outputs 7,8: see OUT9. By selection of one of the 2 power DMOS at same output is it possible to supply a bulb with low on-resistance or a LED with higher on-resistance in a different application.
32	ECV	Electrochrome voltage input and lowside driver output. This input senses voltage in electrocrome mode for charge monitoring. The lowside switch provides a fast discharge of electrocromic mirror and can be used 'stand alone' as lowside switch beside electrocromic mode.
33	OUT9	Highside driver output 9. The output is built by a highside switch and is intended for resistive loads, hence the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present but the energy which can be dissipated is limited. The highside driver is a power DMOS transistor with an internal parasitic reverse diode from the output to VS (bulk-drain-diode). The output is over-current and open load protected.
34	OUT10	Highside driver output 10: see OUT9. *Important:* beside the bit10 in control register 1 this output can be switched on setting bit1 for electrocromic control mode with higher priority.

Figure 2. Configuration diagram (top view)



Note: All pins with the same name must be externally connected.

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
Vs	DC supply voltage	-0.3...28	V
	Single pulse t_{max} < 400 ms	40	V
Vcc	Stabilized supply voltage, logic supply	-0.3 to 5.5	V
V_{DI}, V_{DO}, V_{CLK}, V_{CSN}, V_{PWM}	Digital input / output voltage	-0.3 to V_{CC} + 0.3	V
V_{CM}	Current monitor output	-0.3 to V_{CC} + 0.3	V
V_{CP}	Charge pump output	-25 .. V_S + 11	V
$V_{OUTn, ECDR, ECV}$	Static output voltage (n= 1 to 11)	-0.3 to V_S + 0.3	V
$I_{OUT,2,3,9,10, ECV}$	Output current	±1.25	A
$I_{OUT1,6,7,8,}$	Output current	±5	A
$I_{OUT4,5,11}$	Output current	±10	A

2.2 ESD protection

Table 4. ESD protection

Parameter	Value	Unit
All pins	± 2 (1)	kV
Output pins: OUT1 - OUT6, ECV	± 4 (2)	kV

1. HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114-A.
2. HBM with all unzapped pins grounded.

2.3 Thermal data

Table 5. Operating junction temperature

Symbol	Parameter	Value	Unit
T_j	Operating junction temperature	-40 to 150	°C

Table 6. Temperature warning and thermal shutdown

Symbol	Parameter		Min.	Typ.	Max.	Unit
$T_{jTW\ ON}$	Temperature warning threshold junction temperature	T_j	130		150	°C
$T_{jSD\ ON}$	Thermal shutdown threshold junction temperature	T_j increasing			170	°C
$T_{jSD\ OFF}$	Thermal shutdown threshold junction temperature	T_j decreasing	150			°C
$T_{jSD\ HYS}$	Thermal shutdown hysteresis			5		°K

2.4 Electrical characteristics

V_S = 8 to 16V, V_{CC}= 4.5 to 5.3V, T_j = - 40 to 150°C, unless otherwise specified.

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 7. Supply

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
7.1	VS	Operating voltage range		7		28	V
7.2	I_S	V_S DC supply current	V_S = 16 V, V_{CC} = 5.3 V active mode OUT1 - OUT11, ECV, ECDR floating		7	20	mA
7.3		V_S quiescent supply current	V_S = 16 V, V_{CC} = 0 V standby mode OUT1 - OUT11, ECV, ECDR floating T_{test} = -40°C, 25°C		4	12	µA
7.4(1)			T_{test} = 85°C		6	25	

Table 7. Supply (continued)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
7.5	I_{CC}	V_{CC} DC supply current	V_S = 16 V, V_{CC} = 5.3 V CSN = V_{CC}, active mode OUT1 - OUT11, ECV, ECDR floating		1	3	mA
7.6(2)		V_{CC} quiescent supply current	V_S = 16 V, V_{CC} = 5.3 V_{CSN} = V_{CC} standby mode OUT1 - OUT11, ECV, ECDR floating T_{test} = -40°C, 25°C		3	6	µA
7.7(1)			T_{test} = 85°C		5	10	

1. This parameter is guaranteed by design.
2. CM/ PWM 2 = V_{CC} or 0 V.

Table 8. Overvoltage and under voltage detection

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
8.1	$V_{SUV\ on}$	V_S UV-threshold voltage	V_S increasing	5.6		7.2	V
8.2	$V_{SUV\ off}$	V_S UV-threshold voltage	V_S decreasing	5.2		6.1	V
8.3	$V_{SUV\ hyst}$	V_S UV-hysteresis	$V_{SUV\ ON}$ - $V_{SUV\ OFF}$		0.5		V
8.4	$V_{SOV\ off}$	V_S OV-threshold voltage	V_S increasing	18		24.5	V
8.5	$V_{SOV\ on}$	V_S OV-threshold voltage	V_S decreasing	17.5		23.5	V
8.6	$V_{SOV\ hyst}$	V_S OV-hysteresis	$V_{SOV\ OFF}$ - $V_{SOV\ ON}$		1		V
8.7	$V_{POR\ off}$	Power-on-reset threshold	V_{CC} increasing			2.9	V
8.8	$V_{POR\ on}$	Power-on-reset threshold	V_{CC} decreasing	2.0			V
8.9	$V_{POR\ hyst}$	Power-on-reset hysteresis	$V_{POR\ OFF}$ - $V_{POR\ ON}$		0.11		V

Table 9. Current monitor output CM / PWM 2

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max	Unit
9.1	V_{CM}	Functional voltage range		0		V_{CC}-1V	V
9.2	$I_{CM,r}$	Current monitor output ratio: I_{CM} / $I_{OUT1,4,5,6,11}$ and 7,8 (low on-resistance)	0V <= V_{CM} <= 4V V_{CC}=5V		$\frac{1}{10.000}$		
9.3		I_{CM} / $I_{OUT2,3,9,10}$ and 7,8 (high on-resistance)			$\frac{1}{2000}$		

Table 9. Current monitor output CM / PWM 2 (continued)

Item	Symbol	Parameter	Test condition		Min.	Typ.	Max	Unit
9.4	$I_{CM\ acc}$	Current monitor accuracy $acc I_{CMOUT1,4,5,6,}$ 11and 7, 8 (low on-res.)	V_{CM} <= 3.8V, V_{CC} = 5V	$I_{Out,min}$= 500mA $I_{Out4,5,11max}$= 5.9A $I_{Out1,6\ max}$= 2.9A $I_{Out7,8\ max}$= 1.3A		4% + 1%FS(1)	8% + 2%FS(1)	
9.5		$acc I_{CMOUT2,3,9,10,}$ and 7, 8 (high on-res.)		$I_{Out,min}$= 100 mA $I_{Out2,3\ max}$= 0.6 A $I_{Out9,10max}$= 0.4 A $I_{Out8\ max}$= 0.3 A				

1. FS (full scale)= I_{OUTmax} * $I_{CM,r}$.

Table 10. Charge pump output CP

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max	Unit
10.1	V_{CP}	Charge pump output voltage	V_S = 8V, I_{CP} = -60µA	V_S+6		V_S+13	V
10.2			V_S = 10V, I_{CP} = -80µA	V_S+8		V_S+13	V
10.3			V_S >=12V, I_{CP} = -100µA	V_S+10		V_S+13	V
10.4	I_{CP}	Charge pump output current	V_{CP} = V_S+10V, V_S =13.5V	95	150	300	µA

2.4.1 Outputs OUT1 - OUT11, ECV

Table 11. On-resistance and switching times

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
11.1	$r_{ON\ OUT1,}$ $r_{ON\ OUT6}$	On-resistance to supply or GND	V_S = 13.5 V, T_j = 25 °C, $I_{OUT1,6}$ = ± 1.5 A		300	400	mΩ
11.2			V_S = 13.5 V, T_j = 125 °C, $I_{OUT1,6}$ = ± 1.5 A		450	600	mΩ
11.3	$r_{ON\ OUT2,}$ $r_{ON\ OUT3}$	On-resistance to supply or GND	V_S = 13.5 V, T_j = 25 °C, $I_{OUT2,3}$ = ± 0.4A		1600	2200	mΩ
11.4			V_S = 13.5 V, T_j = 125 °C, $I_{OUT2,3}$ = ± 0.4 A		2500	3400	mΩ

Table 11. On-resistance and switching times (continued)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
11.5	$r_{ON\ OUT4}$, $r_{ON\ OUT5}$	On-resistance to supply or GND	V_S = 13.5 V, T_j = 25 °C, $I_{OUT4,5}$ = ± 3.0 A		150	200	mΩ
11.6			V_S = 13.5 V, T_j = 125 °C, $I_{OUT4,5}$ = ± 3.0 A		225	300	mΩ
11.7	$r_{ON\ OUT9}$, $r_{ON\ OUT10}$	On-resistance to supply	V_S = 13.5 V, T_j = 25 °C, $I_{OUT9,10}$ = -0.4 A		1600	2200	mΩ
11.8			V_S = 13.5 V, T_j = 125 °C, $I_{OUT9,10}$ = -0.4 A		2500	3400	mΩ
11.9	$r_{ON\ OUT11}$	On-resistance to supply	V_S = 13.5 V, T_j = 25 °C, I_{OUT11} = -3.0 A		90	130	mΩ
11.10			V_S = 13.5 V, T_j = 125 °C, I_{OUT11} = -3.0 A		130	180	mΩ
11.11	$r_{ON\ OUT7}$ $r_{ON\ OUT8}$	On-resistance to supply in low mode (control register 1 bits 12 to15: 0101)	V_S = 13.5 V, T_j = 25 °C, $I_{OUT7,8}$ = - 0.8 A		500	700	mΩ
11.12			V_S = 13.5 V, T_j = 125 °C, $I_{OUT7,8}$ = - 0.8 A		700	950	mΩ
11.13		On-resistance to supply in high mode (control register 1 bits 12 to15: 1010)	V_S = 13.5 V, T_j = 25 °C, $I_{OUT7,8}$ = - 0.2 A		1800	2400	mΩ
11.14			V_S = 13.5 V, T_j = 125 °C, $I_{OUT7,8}$ = - 0.2 A		2500	3400	mΩ
11.15	$r_{ON\ ECV}$	On-resistance to GND	V_S = 13.5 V, T_j = 25 °C, I_{OUTECV} = + 0.4 A		1600	2200	mΩ
11.16			V_S = 13.5 V, T_j = 125 °C, I_{OUTECV} = + 0.4 A		2500	3400	mΩ
11.17	I_{QLH}	Switched-off output current highside drivers of OUT1-6, 8-11	V_{OUT}= 0V, standby mode	-5	-2		µA
11.18			V_{OUT}= 0V, active mode	-10	-7		µA

Table 11. On-resistance and switching times (continued)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
11.19	$I_{QLH7,8}$	Switched-off output current highside drivers of OUT7-8	V_{OUT}= 0V, standby mode	-5	-2		µA
11.20			V_{OUT}= 0V, active mode	-15	-10		µA
11.21	I_{QLL}	Switched-off output current lowside drivers of OUT1-6	V_{OUT}= V_S, standby mode		80	120	µA
11.22			V_{OUT}= 0V, active mode	-10	-7		µA
11.23		Switched-off output current lowside drivers of ECV	V_{OUT}= V_S, standby mode	-15		15	µA
11.24			V_{OUT}= V_S, active mode	-10		10	µA
11.25	$t_{d\ ON\ H}$	Output delay time, highside driver on (OUT_X except $OUT_{7,8}$)	V_S = 13.5 V, V_{CC} = 5 V (1)(2)(3)	20	40	80	µs
11.26		Output delay time, highside driver on ($OUT_{7,8}$ in high R_{DSon} mode)		15	35	60	µs
11.27		Output delay time, highside driver on ($OUT_{7,8}$ in low R_{DSon} mode)		10	35	80	µs
11.28	$t_{d\ OFF\ H}$	Output delay time, highside driver off ($OUT_{1, 4, 5, 6, 11}$)	V_S = 13.5 V, V_{CC} = 5 V(1)(2)(3)	60	150	200	µs
11.29		Output delay time, highside driver off ($OUT_{2,3,7}$, high/low $R_{DSon\ ,\ 8}$ high/low $R_{DSon\ ,\ 9,\ 10}$)		40	70	100	µs
11.30	$t_{d\ ON\ L}$	Output delay time, lowside driver On	V_S = 13.5 V, V_{CC} = 5 V, corresponding highside driver is not active(1)(2)(3)	15	30	70	µs
11.31	$t_{d\ OFF\ L\ 1\text{-}6}$	Output delay time, lowside driver OUT 1-6 off	V_S=13.5V, V_{CC}=5V(1)(2)(3)	40	150	300	µs
11.32	$t_{d\ OFF\ L\ ECV}$	Output delay time, lowside driver ECV off		15	45	80	µs

Table 11. On-resistance and switching times (continued)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
11.33	$t_{D\ HL}$	Cross current protection time	$t_{cc\ ONLS_OFFHS}$ - $t_{d\ OFFH}$ (4)	50	200	400	µs
11.34	$t_{D\ LH}$		$t_{cc\ ONHS_OFFLS}$ - $t_{d\ OFFL}$ (4)				
11.35	$dV_{OUT}/dt_{on/off}$	Slew rate of OUTx	V_S = 13.5V, V_{CC} = 5 V (1)(2)(3))	0.1	0.2	0.6	V/µs

1. Rload = 16Ω at OUT1, 6 and 7,8 in low on-resistance mode.
2. Rload = 4Ω at OUT4, 5 and 11.
3. Rload = 64Ω at OUT2, 3, 9, 10, ECV and 7, 8 in high On-resistance mode.
4. t_{cc} is the switch-on delay time if complement in half bridge has to switch-off.

Table 12. Current monitoring

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
12.1	$\|I_{OC1}\|$, $\|I_{OC6}\|$	Over-current threshold to supply or GND	V_S = 13.5V, V_{CC} = 5V, sink and source	3		5	A
12.2	$\|I_{OC2}\|$, $\|I_{OC3}\|$			0.75		1.25	A
12.3	$\|I_{OC4}\|$, $\|I_{OC5}\|$			6		10	A
12.4	$\|I_{OC9}\|$, $\|I_{OC10}\|$	Over-current threshold to supply	V_S = 13.5V, V_{CC} = 5 V, source	0.5		1.0	A
12.5	$\|I_{OC11}\|$			6		10	A
12.6	$\|I_{OC7}\|$, $\|I_{OC8}\|$	Over-current threshold to supply in low on-resistance mode	V_S = 13.5V, V_{CC} = 5V, source, control register 1 bits 12 to 15: 0101	1.5		2.5	A
12.7		Over-current threshold to supply in high on-resistance mode	V_S = 13.5V, V_{CC} = 5V, source, control register 1 bits 12 to 15: 1010	0.35		0.65	A
12.8	$\|I_{OCECV}\|$	Output current limitation to GND	V_S = 13.5V, V_{CC} = 5 V, source	0.75		1.25	A
12.9	t_{FOC}	Filter time of over-current signal	Duration of over-current condition to set the status bit	10	55	100	µs
12.10	f_{rec0}	Recovery frequency for OC recovery duty cycle bit= 0		1		4	kHz
12.11	f_{rec1}	Recovery frequency for OC recovery duty cycle bit= 1		2		6	kHz

Table 12. Current monitoring (continued)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
12.12	$\|I_{OLD1}\|$, $\|I_{OLD6}\|$	Under-current threshold to supply or GND	V_S = 13.5V, V_{CC} = 5V, sink and source	10	30	80	mA
12.13	$\|I_{OLD2}\|$, $\|I_{OLD3}\|$			10	20	30	mA
12.14	$\|I_{OLD4}\|$, $\|I_{OLD5}\|$			60	150	300	mA
12.15	$\|I_{OLD9}\|$, $\|I_{OLD10}\|$	Under-current threshold to supply	V_S = 13.5 V, V_{CC} = 5 V, source	5	10	15	mA
12.16	$\|I_{OLD11}\|$			30	150	300	mA
12.17	$\|I_{OLD7}\|$, $\|I_{OLD8}\|$	Under-current threshold to supply in low on-resistance mode		15	40	60	mA
12.18		Under-current threshold to supply in high on-resistance mode		5	10	15	mA
12.19	$\|I_{OLDECV}\|$	Under-current threshold to GND	V_S = 13.5V, VCC = 5V, sink	10	20	30	mA
12.20	t_{FOL}	Filter time of under-current	Duration of under-current condition to set the status bit	0.5		3	ms

Table 13. Electrochrome control

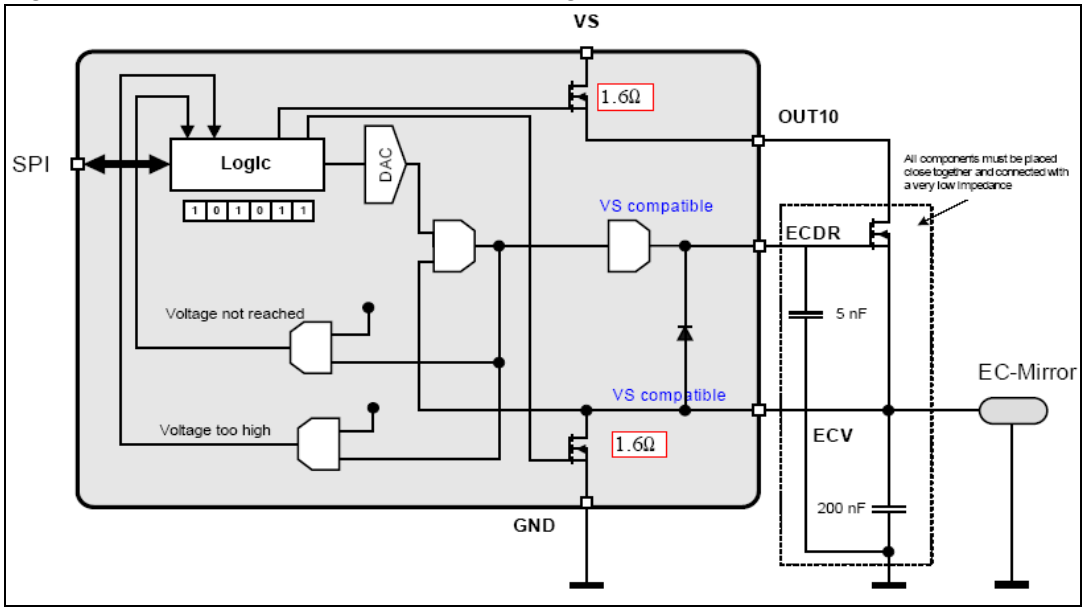
Item	Symbol	Parameter		Test condition		Min.	Typ.	Max.	Unit
13.1	$V_{CTRLmax}$	Maximum EC-control voltage		bit 0= 1 control reg. 2(1)		1.4		1.6	V
13.2				bit 0= 0 control reg. 2(1)		1.12		1.28	V
13.3	DNL	Differential non linearity				-1		1	LSB(2)
13.4	$\|dV_{ECV}\|$	Voltage deviation between target and ECV		$dV_{ECV} = V_{target}$(3)$-V_{ECV}$ $\|I_{ECDR}\| < 1\mu A$		-5% -1 LSB (3)		+5% +1 LSB (3)	mV
13.5	dV_{ECVnr}	Difference voltage between target and ECV sets flag if V_{ECV} is:	Below it	$dV_{ECV} = V_{target} - V_{ECV}$	Toggle bit 1=1 status reg. 2		120		mV
13.6	dV_{ECVhi}		Above it		Toggle bit 0= 1 status reg. 3		-120		mV
13.7	$V_{ECDRmin_high}$	Output voltage range		I_{ECDR} = -10 µA		4.5		5.5	V
13.8	$V_{ECDRmax_low}$			I_{ECDR} = 10 µA		0		0.7	V

Table 13. Electrochrome control (continued)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
13.9	I_{ECDR}	Current into ECDR	$V_{target} > V_{ECV}$ + 500mV, V_{ECDR} = 3.5V	-100		-10	µA
13.10			$V_{target} < V_{ECV}$ - 500mV, V_{ECDR} = 1.0V; V_{target}=1 LSB; V_{ECV}=0.5V	10		100	µA
13.11	$R_{ecdrdis}$	Pulldown resistance at ECDR in fast discharge mode	V_{ECDR} = 0.7V ; Cntrl Reg 1: bit 8 and bit 1 = 1, all other bits = 0			5	kΩ
13.12	I_{QECDR}	Quiescent current	$V_{ECDR} = V_S$; Cntrl. reg 1 bit 1 = 0			1	µA

1. Bit 7 to 2 = '1' control register 1: ECV voltage, where I_{ECDR} can change sign.
2. 1 LSB (Least Significant Bit)= 23.8 mV.
3. V_{target} is set by bit 7 to 2 of control register 1 and bit 0 of control register 2; tested for each individual bit.

Figure 3. Electrochrome control block diagram



2.5 SPI - Electrical characteristics

V_S = 8 to 16V, V_{CC} = 4.5 to 5.5V, T_j = - 40 to 150°C, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 14. Delay time from standby to active mode

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
14.1	t_{set}	Delay time	Switching from standby to active mode. Time until output drivers are enabled after CSN going to high and set bit 0=1 of control register 0.		256	300	µs

Table 15. Inputs: CSN, CLK, PWM1/2 and DI

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
15.1	V_{inL}	Input low level	V_{CC} = 5V			0.3* Vcc	V
15.2	V_{inH}	Input high level	V_{CC} = 5V	0.7* Vcc			V
15.3	$V_{in\ Hyst}$	Input hysteresis	V_{CC} = 5V	500			mV
15.4	$R_{CSN\ in}$	CSN pull up resistor	V_{CC} = 5V 0V<V_{CSN}<0.7V_{CC}	30	120	250	kΩ
15.5	$R_{CLK\ in}$	CLK pull down resistor	V_{CC} = 5V V_{CLK} = 1.5V	30	60	150	kΩ
15.6	$R_{DI\ in}$	DI pull down resistor	V_{CC} = 5V V_{DI} = 1.5V	30	60	150	kΩ
15.7	$R_{PWM1\ in}$	PWM1 pull down resistor	V_{CC} = 5V V_{PWM1}= 1.5V	30	60	150	kΩ
15.8	C_{in} (1)	Input capacitance at input CSN, CLK, DI and PWM1/2	0 V < V_{CC} < 5.3V			10	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 16. SDI timing (1)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
16.1	t_{CLK}	Clock period	V_{CC} = 5V		1000		ns
16.2	t_{CLKH}	Clock high time	V_{CC} = 5V	115			ns
16.3	t_{CLKL}	Clock low time	V_{CC} = 5V	115			ns
16.4	$t_{set\ CSN}$	CSN setup time, CSN low before rising edge of CLK	V_{CC} = 5V	400			ns
16.5	$t_{set\ CLK}$	CLK setup time, CLK high before rising edge of CSN	V_{CC} = 5V	400			ns
16.6	$t_{set\ DI}$	DI setup time	V_{CC} = 5V	200			ns
16.7	$t_{hold\ DI}$	DI hold time	V_{CC} = 5V	200			ns

Table 16. SDI timing (continued)(1)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
16.8	$t_{r\ in}$	Rise time of input signal DI, CLK, CSN	V_{CC} = 5V			100	ns
16.9	$t_{f\ in}$	Fall time of input signal DI, CLK, CSN	V_{CC} = 5V			100	ns

1. DI timing parameters tested in production by a passed / failed test:

Tj= -40°C / +25°C: SPI communication @ 2MHz.

Tj= +125°C SPI communication @ 1.25 MHz.

Table 17. DO

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
17.1	V_{DOL}	Output low level	I_{DO} = -5 mA			0.2V_{CC}	V
17.2	V_{DOH}	Output high level	I_{DO} = 5 mA	0.8 V_{CC}			V
17.3	I_{DOLK}	Tristate leakage current	$V_{CSN} = V_{CC}$, 0V < V_{DO} < V_{CC}	-10		10	µA
17.4	C_{DO} (1)	Tristate input capacitance	$V_{CSN} = V_{CC}$, 0V < V_{CC} < 5.3V			10	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 18. DO timing

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
18.1	$t_{r\ DO}$	DO rise time	C_{DO} = 100 pF		80	140	ns
18.2	$t_{f\ DO}$	DO fall time	C_{DO} = 100 pF		50	100	ns
18.3	$t_{en\ DO\ tri\ L}$	DO enable time from tristate to low level	C_{DO} = 100 pF, I_{load} = 1mA pull-up load to V_{CC}		100	250	ns
18.4	$t_{dis\ DO\ L\ tri}$	DO disable time from low level to tristate	C_{DO} = 100 pF, I_{load} = 4 mA pull-up load to V_{CC}		380	450	ns
18.5	$t_{en\ DO\ tri\ H}$	DO enable time from tristate to high level	C_{DO} =100 pF, I_{load} = -1mA pull-down load to GND		100	250	ns
18.6	$t_{dis\ DO\ H\ tri}$	DO disable time from high level to tristate	C_{DO} = 100 pF, I_{load} = -4mA pull-down load to GND		380	450	ns
18.7	$t_{d\ DO}$	DO delay time	V_{DO} < 0.3 V_{CC}, V_{DO} > 0.7 V_{CC}, C_{DO} = 100 pF		50	250	ns

Table 19. CSN timing

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
19.1	$t_{CSN_HI,stb}$	Mimimum CSN HI time, switching from standby mode	Transfer of SPI-command to input register		20	50	µs
19.2	$t_{CSN_HI,min}$	Minimum CSN HI time, active mode	Transfer of SPI-command to input register		2	4	µs

Figure 4. SPI - Transfer timing diagram

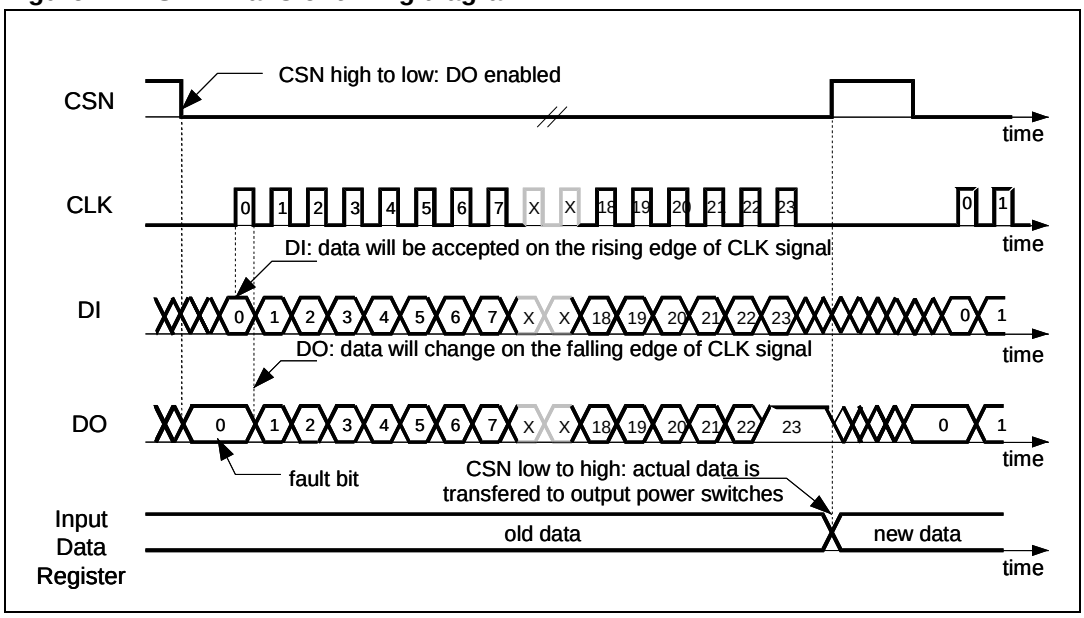


Figure 5. SPI - Input timing

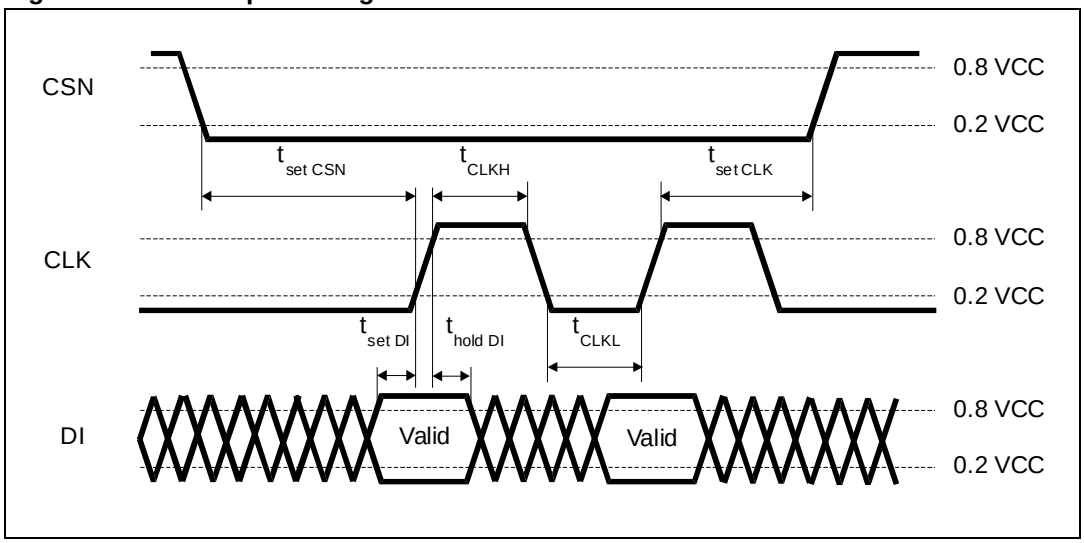


Figure 6. SPI - DO valid data delay time and valid time

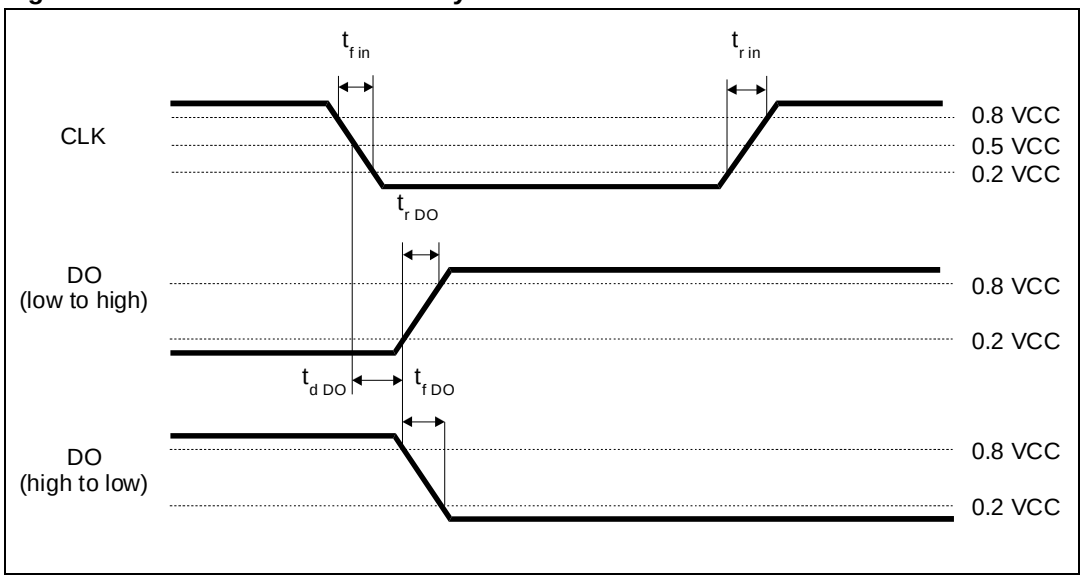


Figure 7. SPI - DO enable and disable time

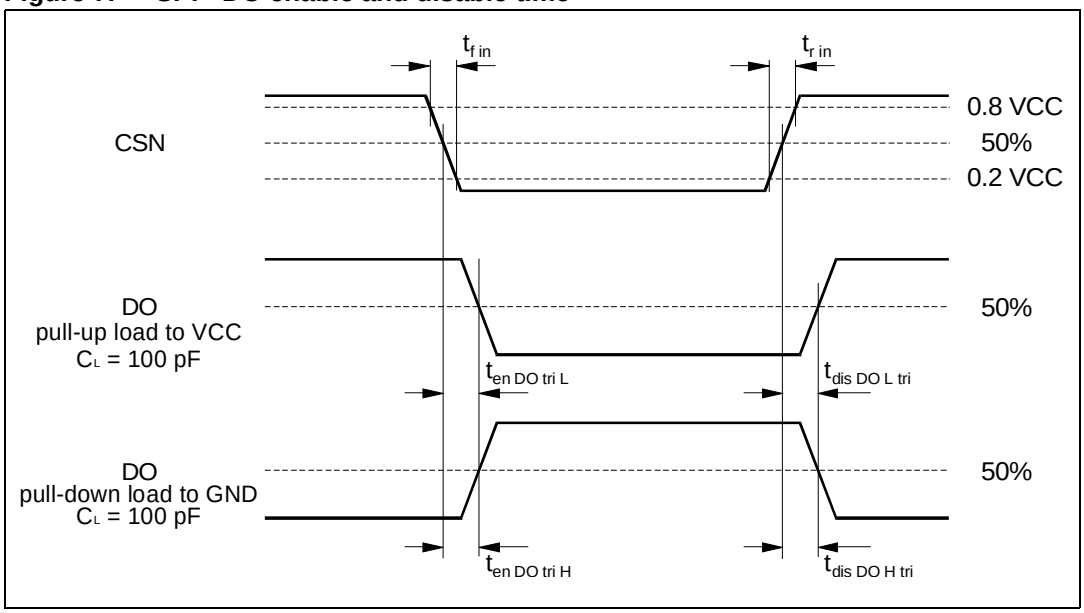
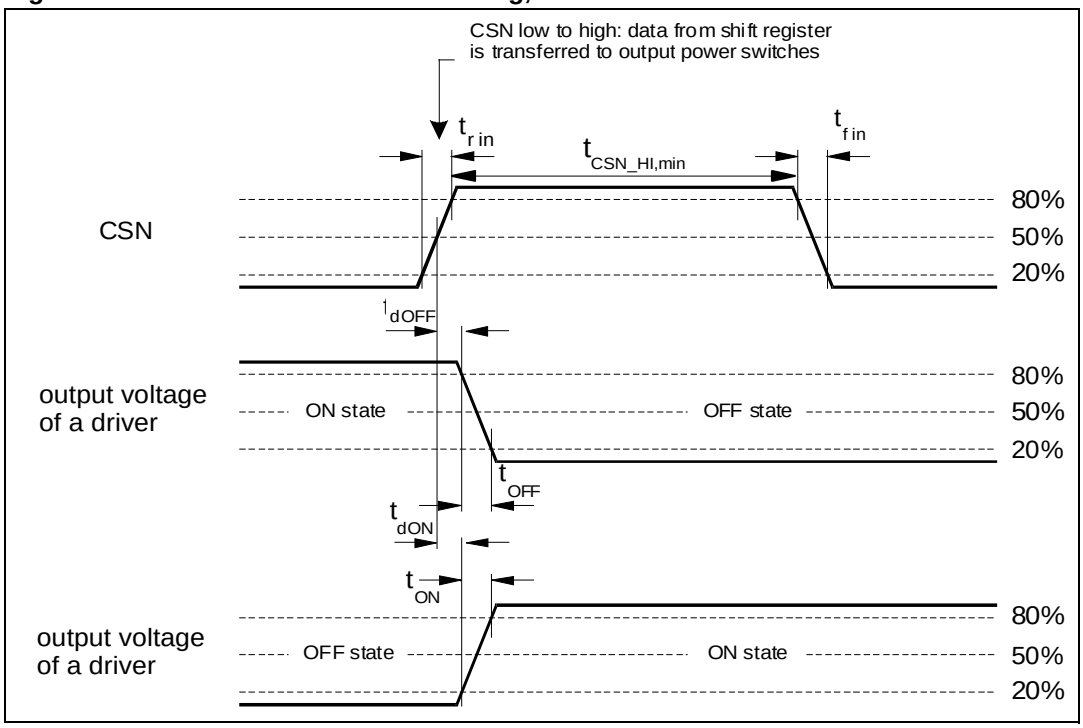


Figure 8. SPI - driver turn on/off timing, minimum CSN HI time



3 Application information

3.1 Dual power supply: V_S and V_{CC}

The power supply voltage V_S supplies the half bridges and the highside drivers. An internal charge-pump is used to drive the highside switches. The logic supply voltage V_{CC} is used for the logic part and the SPI of the device.

Due to the independent logic supply voltage the control and status information will not be lost, if there are temporary spikes or glitches on the power supply voltage.

3.2 Wake up and active mode / standby mode

After power up of VS and Vcc the device operates in standby-mode. Pulling the signal CSN to low level wakes the device up and the analog part will be activated (active mode).

After at least 10µs, the first SPI communication is valid and bit 0 of the Control Register 0 can be used to set the EN-mode. If bit 0 is not set to 1, the device doesn't remain in the active mode. After at least 256µs all latched data will be cleared and the inputs and outputs are switched to high impedance. In standby mode the current at V_S (V_{CC}) is less than 6 µA (5 µA) for CSN = high (DO in tristate).

3.3 Charge pump

In standby mode the chargepump is turned off. After enabling the device by SPI command (bit0=1 Control Register 0) the oscillator starts and the voltage begins to increase. The output drivers are enabled after at least 256 µs after CSN went to high.

3.4 Diagnostic functions

All diagnostic functions (over/under-current, power supply over-/undervoltage, temperature warning and thermal shutdown) are internally filtered. The condition has to be valid for at least 32 µs (open load: 1ms) before the corresponding status bit in the status registers is set.

The filters are used to improve the noise immunity of the device. The under-current and temperature warning functions are intended for information purpose and will not change the state of the output drivers. On contrary, the over-current condition disables the corresponding driver and thermal shutdown disables all drivers. Without setting the over-current recovery bits in the input data register, the microcontroller has to clear the over-current status bits to reactivate the corresponding drivers.

3.5 Overvoltage and undervoltage detection at V_S

If the power supply voltage VS rises above the overvoltage threshold $V_{SOV\ OFF}$ (typical 21 V), the outputs OUT1 to OUT11, ECDR and ECV are switched to high impedance state to protect the load. When the voltage VS drops below the undervoltage threshold $V_{SUV\ OFF}$ (UV-switch-OFF voltage), the output stages are switched to high impedance to avoid the operation of the power devices without sufficient gate driving voltage (increased power dissipation). If the supply voltage V_S recovers (control register 3: bit 4=0) to normal operating voltage then the outputs stages return to the programmed state. If the undervoltage/overvoltage recovery disable bit is set (control register 3: bit 4=1), the automatic turn-on of the drivers is deactivated.

The microcontroller needs to clear the status bits to reactivate the drivers. It is recommended to set bit1 control register 3 to avoid a possible high current oscillation in case of a shorted output to GND and low battery voltage.

3.6 Overvoltage and undervoltage detection at V_{CC}

In case of power-on (VCC increases from undervoltage to $V_{POR\ OFF}$ = 2.9 V) the circuit is initialized by an internally generated power-on-reset (POR). If the voltage VCC decreases below the minimum threshold ($V_{POR\ ON}$ = 2.0 V), the outputs are switched to tristate (high impedance) and the status registers are cleared.

3.7 Temperature warning and thermal shutdown

If the junction temperature rises above $T_{j\ TW}$, a temperature warning flag is set after at least 32 µs and it can be read via the SPI. If the junction temperature increases above the second threshold $T_{j\ SD}$, the thermal shutdown bit is set and the power DMOS transistors of all output stages are switched off to protect the device after at least 32 µs.

The temperature warning and thermal shutdown flags are latched and the bits must be cleared by the microcontroller. This is possible only if the temperature has decreased below trigger temperature. If the thermal shutdown bit has been cleared the output stages are reactivated.

3.8 Inductive loads

Each half bridge is built by internally connected highside and lowside power DMOS transistors. Due to the built-in reverse diodes of the output transistors, inductive loads can be driven at the outputs OUT1 to OUT6 without external free-wheeling diodes. The highside drivers OUT7 to OUT11 are intended to drive resistive loads. Therefore only a limited energy (E<1mJ) can be dissipated by the internal ESD-diodes in freewheeling condition. For inductive loads (L>100µH) an external free-wheeling diode connected between GND and the corresponding output is required.

The low side driver at ECV does not have a freewheel diode built into the device.

3.9 Open load detection

The open load detection monitors the load current in each activated output stage. If the load current is below the open load detection threshold for at least 1 ms (t_{dOL}) the corresponding open load bit is set in the status register. Due to mechanical/electrical inertia of typical loads a short activation of the outputs (e.g. 3 ms) can be used to test the open load status without changing the mechanical/electrical state of the loads.

3.10 Over-load detection

In case of an over-current condition a flag is set in the status register in the same way as during open load detection. If the over-current signal is valid for at least t_{ISC}(typ) = 55 µs, the over-current flag is set and the corresponding driver is switched off to reduce the power dissipation and to protect the integrated circuit. If the over-current recovery bit of the output is zero, the microcontroller has to clear the status bits to reactivate the corresponding driver.

3.11 Current monitor

The current monitor output sources a current image at the current monitor output which has two fixed ratios of the instantaneous current of the selected highside driver. Outputs with a resistance of 500 mΩ and higher have a ratio of 1/2000 and those with a lower resistance of 1/10000. The signal at output CM is blanked after switching on the driver until correct settlement of the circuitry (at least for 64 µs). The bits 0 to 3 of the control register 3 define which of the outputs are multiplexed to the current monitor output CM/PWM2. The current monitor output allows a more precise analysis of the actual state of the load rather than the detection of an open- or overload condition. For example it can be used to detect the motor state (starting, free-running, stalled). Moreover, it is possible to control the power of the defroster more precisely by measuring the load current. The current monitor output is bidirectional (PWM inputs).

3.12 PWM inputs

Each driver has a corresponding PWM enable bit, which can be programmed by the SPI interface. If the PWM enable bit is set in control registers 2 or 3, the output is controlled by the logically AND-combination of the PWM signal and the output control bit in Control Registers 0 and 1. The outputs OUT1-4, 6, 7, 9, OUT11 are controlled by the PWM1 input and the outputs OUT5, 8 and OUT10 are controlled by the bidirectional input CM/PMW2. For example, the two PWM inputs can be used to dim two lamps independently by external PWM signals. In case of switching off a high/low side switch in PWM mode a minimum off time of appr. (256 µs – $td_{on^+}td_{off}$) is predefined by the state machine, to avoid switching on the high/low side again during the negative slope. For a PWM frequency of 100Hz this means the maximum duty cycle is about 98%. Larger duty cycles can be realized by applying pulse skipping.

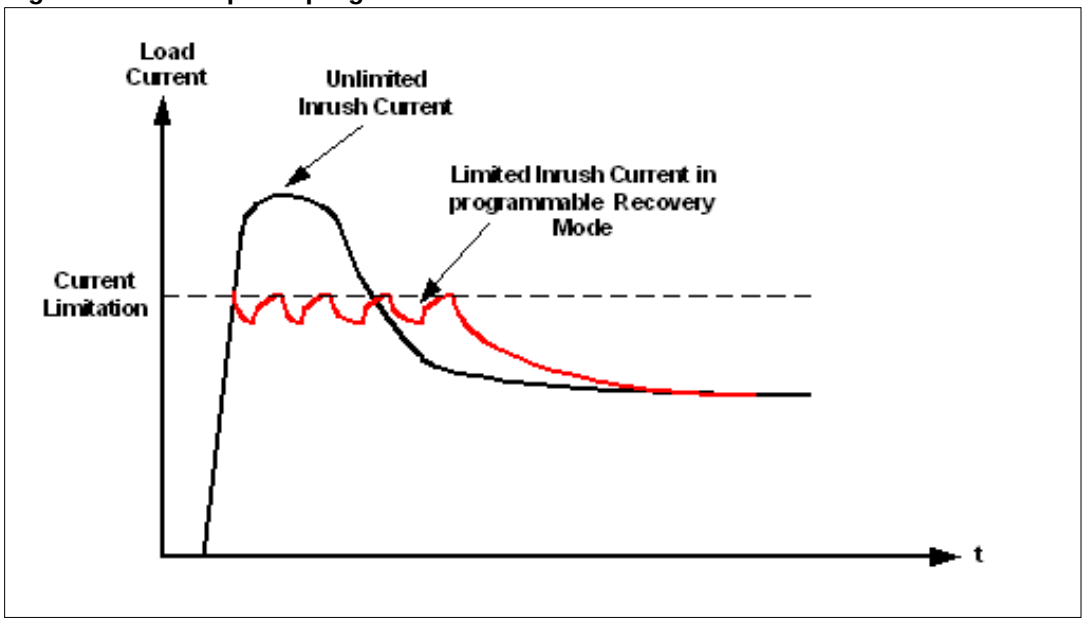
3.13 Cross-current protection

The six half-brides of the device are cross-current protected by an internal delay time. If one driver (LS or HS) is turned off, the activation of the other driver of the same half bridge will be automatically delayed by the cross-current protection time. After the cross-current protection time is expired the slew-rate limited switch-off phase of the driver is changed to a fast turn-off phase and the opposite driver is turned-on with slew-rate limitation. Due to this behaviour it is always guaranteed that the previously activated driver is completely turned off before the opposite driver starts to conduct.

3.14 Programmable soft-start function to drive loads with higher inrush current

Loads with start-up currents higher than the over-current limits (e.g. inrush current of lamps, start current of motors and cold resistance of heaters) can be driven by using the programmable softstart function (i.e. overcurrent recovery mode). Each driver has a corresponding over-current recovery bit. If this bit is set, the device automatically switches the outputs on again after a programmable recovery time. The duty cycle in over-current condition can be programmed by the SPI interface to about 12% or 25%. The PWM modulated current will provide sufficient average current to power up the load (e.g. heat up the bulb) until the load reaches operating condition. The PWM frequency settles at 1.7kHz and 3kHz. The device itself cannot distinguish between a real overload and a non linear load like a light bulb. A real overload condition can only be qualified by time. For over-load detection the microcontroller can switch on the light bulbs by setting the over-current recovery bit for the first e.g. 50ms. After clearing the recovery bit the output will be automatically switched off, if the overload condition remains. This over-load detection procedure has to be followed in order make it possible to switch on the low-side driver of a bridge output, if the associated high-side driver has been used in recovery mode before.

Figure 9. Example of programmable soft-start function for inductive loads



3.15 Controller for electrochromic glass

The voltage of an electrochromic element connected at pin ECV can be controlled to a target value, which is set by the bits 7 down to 2 of control register 1. Setting bit 1 of control register 1 enables this function. An on-chip differential amplifier and an external MOS source follower, with its gate connected to pin ECDR and which drives the electrochrome mirror voltage at pin ECV, form the control loop. The drain of the external MOS transistor is supplied by OUT10. A diode from pin ECV (anode) to pin ECDR (cathode) has been placed on the chip to protect the external MOS source follower. A capacitor of at least 5 nF has to be added to pin ECDR for loop-stability.

The target voltage is binary coded with a full scale range of 1.5V. If Bit 0 of control register 2 is set to '1', the maximum controller output voltage is clamped to 1.2V without changing the resolution of bits 7-2 of control register 1. When setting the target voltage to 0V and programming the ECVLS driver to on-state, the voltage at pin ECV is pulled to ground by a 1.6 Ohm low-side switch (fast discharge).

The status of the voltage control loop is reported via SPI. Bit 0 in the status register 2 is set, if the voltage at pin ECV is higher, whereas Bit 1 in the same status register is set, if the voltage at pin ECV is lower than the target value. Both status bits are valid, if they are stable for at least 150 µs.

Since OUT10 is the output of a high-side driver, it contains the same diagnose functions as the other high-side drivers (e.g. During an over current detection, the control loop is switched off). In electrochrome mode OUT10 cannot be controlled by PWM mode. For EMS reasons the loop capacitor at pin ECDR as well as the capacitor between ECV and GND have to be placed to the respective pins as close as possible.

4 Functional description of the SPI

4.1 General description

Standard ST-SPI Interface Version 3.0.

The SPI communication is based on a Serial Peripheral Interface interface structure using CSN (Chip Select Not), DI (Serial Data In), DO (Serial Data Out/Error) and CLK (Serial Clock) signal lines.

4.1.1 Chip Select Not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) is in high impedance state. A low signal wakes up the device and a serial communication can be started. The state when CSN is going low until the rising edge of CSN will be called a communication frame.

4.1.2 Serial Data In (DI)

The input pin is used to transfer data serially into the device. The data applied to the DI will be sampled at the rising edge of the CLK signal.

4.1.3 Serial Clock (CLK)

This input signal provides the timing of the serial interface. The Data Input (DI) is latched at the rising edge of Serial Clock CLK . The SPI can be driven by a micro controller with its SPI peripheral running in following mode: CPOL = 0 and CPHA = 0. Data on Serial Data Out (DO) is shifted out at the falling edge of the serial clock (CLK). The serial clock CLK must be active only during a frame (CSN low). Any other switching of CLK close to any CSN edge could generate set up/hold violations in the SPI logic of the device.

The clock monitor counts the number of clock pulses during a communication frame (while CSN is low). If the number of CLK pulses does not correspond to the frame width indicated in the <SPI-frame-ID> (ROM address 03H) the frame is ignored and the *<frame error>* bit in the *<Global Status Byte>* is set.

Note: Due to this safety functionality, daisy chaining the SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

4.1.4 Serial Data Out (DO)

The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the global status bit 7 (Global Error Flag). The first rising edge of the CLK input after a high to low transition of the CSN pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out.

4.1.5 SPI communication flow

At the beginning of each communication the master can read the contents of the <*SPI-frame-ID*> register (ROM address 03H) of the slave device. This 8-bit register indicates the SPI frame length (24 bit) and the availability of additional features.

Each communication frame consists of a command byte which is followed by 2 data bytes.

The data returned on DO within the same frame always starts with the <*Global Status*> Byte. It provides general status information about the device. It is followed by 2 data bytes (i. e. '*In-frame-response*').

For Write cycles the <*Global Status*> Byte is followed by the previous content of the addressed register.

Figure 10. Write and read SPI

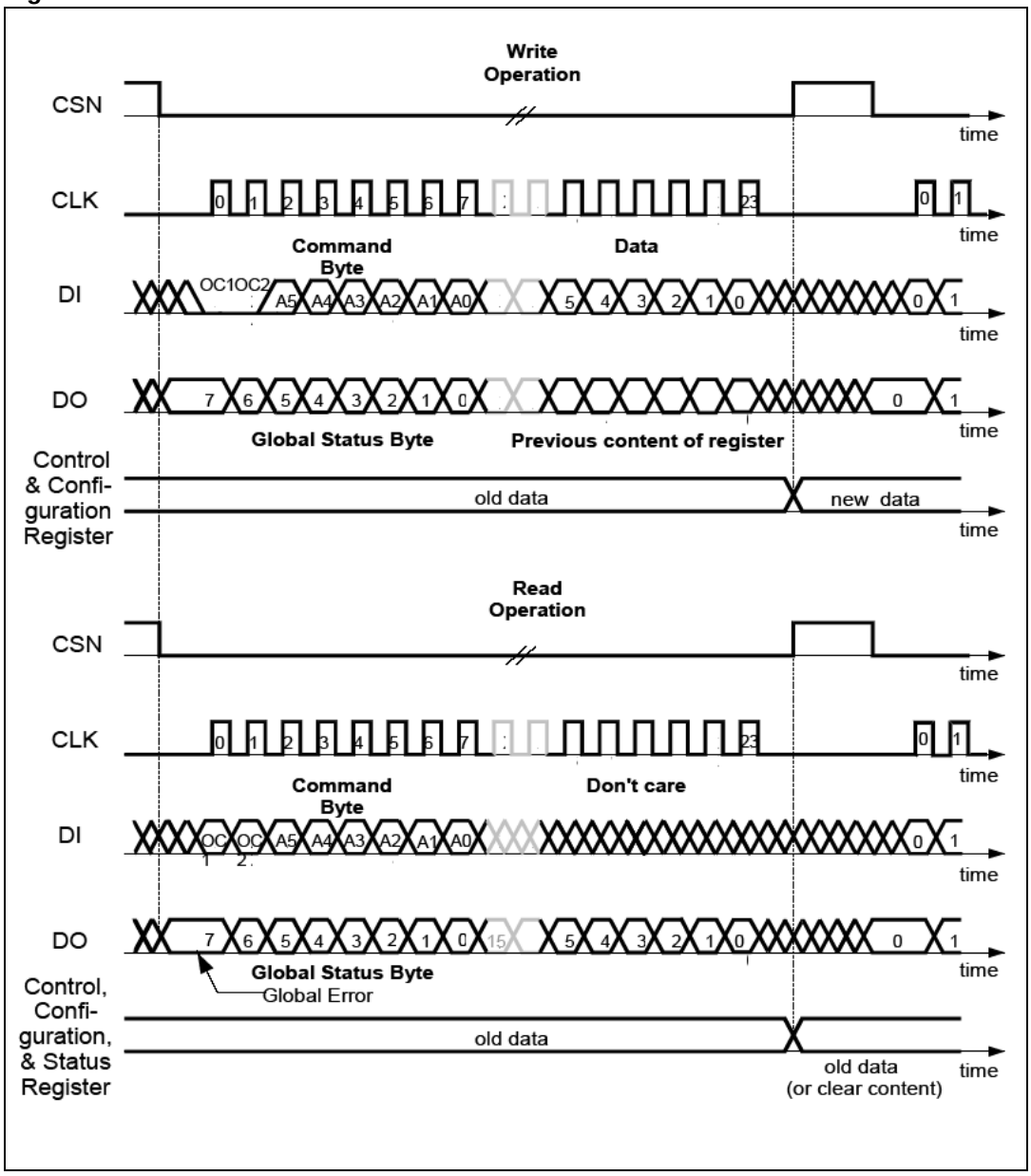


Table 20. SPI frame

	Command Byte								Data Byte								Data Byte							
Bit	23	22	21	29	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OC1	OC0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

Ocx: Operation code

Ax: Address

Dx: Data Bit

4.2 Command byte

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (<*Read*>, <*Write*>, <*Read and Clear*>, <*Read Device Information*>) and a 6 bit address. If less than 6 address bits are required, the remaining bits are unused but are reserved.

4.2.1 Operation code definition

Table 21. Operation code definition

OC1	OC0	Meaning
0	0	<Write Mode>
0	1	<Read Mode>
1	0	<Read and Clear Mode>
1	1	<Read Device Information>

The <Write Mode> and <Read Mode> operations allow access to the RAM of the device.

A <Read and Clear Mode> operation is used to read a status register and subsequently clear its content.

The <Read Device Information> allows access to the ROM area which contains device related information such as <ID-Header>, <Product Code>, <Silicon Version and Category> and <*SPI-frame-ID*>.

4.3 Global status byte

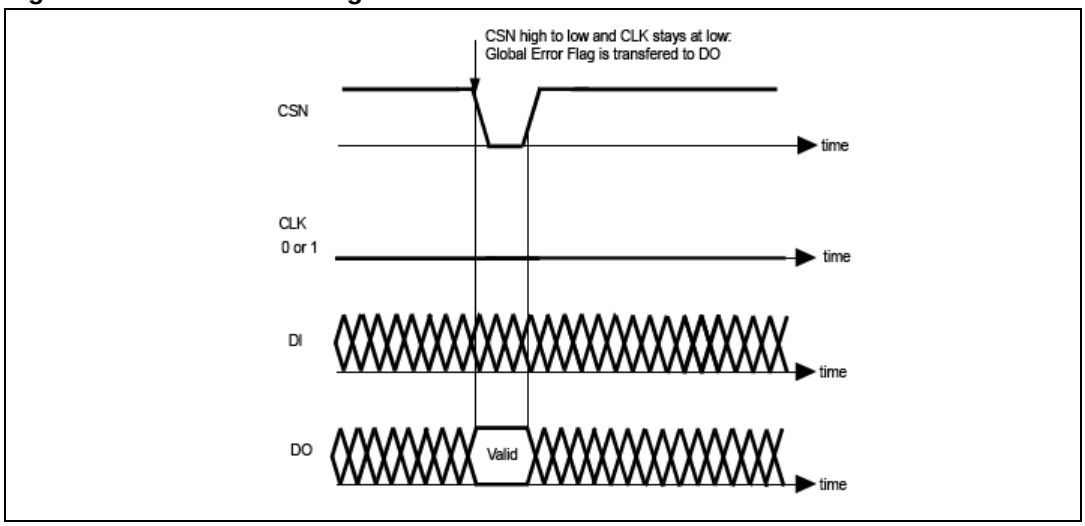
Table 22. Global status byte

Bit	7	6	5	4	3	2	1	0
Name	GL_ER	CO_ER	C_RESET	TSD	TW	UOV_OC	OL	NR
Reset	0	0	1	0	0	0	0	0

Description:

- GL_ER : Global Error Flag. Failures of Bits 0-6 are always linked to the Global Error Flag. This flag is generated by an OR combination of all failure events of the device. It is reflected via the DO pin while CSN is held low and no clock signal is available. The flag will remain as long as CSN is low. This operation does not cause the Communication Error bit in the <Global Status> to be set. The signal TW bit3 and OL bit1can be masked.
- CO_ER : Communication Error. If the number of clock pulses within the previous frame is not 24 the frame is ignored and this bit is set.
- C_RESET : Chip RESET. If a stuck at '1' on input DI during any SPI frame occurs, or if a Power On Reset (VCC monitor) occurs. C_RESET will be reset ('1') with any SPI command. When STK_RESET_Q is active ('0'), the Gate drivers are switched off (resistive path to source).
  After a startup of the circuit the STK_RESET_Q is active because of the POR pulse and the Gate drivers are switched off. The Gate drivers can only be activated after the STK_RESET_Q has been reset with a SPI command.
- TSD : Thermal shutdown due to an internal sensor. All the gate drivers and the charge pump must be switched off (resistive path to source). The TSD bit has to be cleared through a software reset to reactivate the gate drivers and the charge pump.
- TW : Thermal Warning. This bit is maskable by configuration register.
- UOV_OC : Logical OR among the filtered under-/over-voltage signals and over-current signals.
- OL : Open Load. Logical OR among the filtered under-current signals. This bit is maskable by configuration register.
- NR : Not Ready. After switching the device from standby mode to active mode an internal timer is started to allow chargepump to settle before the outputs can be activated. This bit is cleared automatically after start up time has finished.

Figure 11. Global error flag definition



4.4 Address mapping

Table 23. RAM memory map

Address	Name	Access	Content
00h	Control register 0	Read/write	Enable of device and bridge control
01h	Control register 1	Read/write	High/low-side control and Electrocrome block set up
02h	Control register 2	Read/write	Bridge recovery mode and PWM set up and Electrocrome block set up
03h	Control register 3	Read/write	Highside recovery mode and PWM set up and current monitor selection
10h	Status register 0	Read only	Bridge over-current diagnosis
11h	Status register 1	Read only	Bridge open load (under-current) diagnosis
12h	Status register 2	Read only	Open load (under-current) diagnosis, VS and electrocrome diagnosis
3Fh	Configuration register	Read/write	Mask of bits in global status register and for global error bit

Table 24. ROM memory map

Address	Name	Access	Content
00h	ID header	Read only	4300h (ASSP ST_SPI)
01h	Version	Read only	0300h
02h	Product code 1	Read only	4300h (67 ST_SPI)
03h	Product code 2	Read only	4800h (H ST_SPI)
3Eh	SPI-frame ID	Read only	0200h SPI-Frame-ID register (ST_SPI)

5 SPI - control and status registers

5.1 Control register 0

Table 25. Control register 0 (read/write)

Bit	Name	Comment
15	OUT1 – HS on/off	If a bit is set the selected output driver is switched on. If the corresponding PWM enable bit is set the driver is only activated if PWM1 (PWM2) input signal is high. The outputs of OUT1-OUT6 are half bridges. If the bits of HS- and LS-driver of the same half bridge are set, the internal logic prevents that both drivers of this output stage can be switched on simultaneously in order to avoid a high internal current from Vs to GND.
14	OUT1 – LS on/off	
13	OUT2 – HS on/off	
12	OUT2 – LS on/off	
11	OUT3 – HS on/off	
10	OUT3 – LS on/off	
9	OUT4 – HS on/off	
8	OUT4 – LS on/off	
7	OUT5 – HS on/off	
6	OUT5 – LS on/off	
5	OUT6 – HS on/off	
4	OUT6 – LS on/off	
3	0	Reserved (has to be set to '0')
2	0	
1	0	
0	Enable bit	If enable bit is set the device will be switched in active mode. If enable bit is cleared, the device enters standby mode and all bits are cleared.

5.2 Control register 1

Table 26. Control register 1 (read/write)

<table>
<tr><th>Bit</th><th>Name</th><th colspan="5">Comment</th></tr>
<tr><td rowspan="2">15</td><td rowspan="2">OUT7 – HS1 on/off</td><td>OUT 7/8</td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">14</td><td rowspan="2">OUT7 – HS2 on/off</td><td></td><td>HS1</td><td>HS2</td><td>Mode</td><td></td></tr>
<tr><td></td><td>1</td><td>1</td><td>Off</td><td></td></tr>
<tr><td rowspan="2">13</td><td rowspan="2">OUT8 – HS1 on/off</td><td></td><td>1</td><td>0</td><td>Low on-resistance</td><td></td></tr>
<tr><td></td><td>0</td><td>1</td><td>High on-resistance</td><td></td></tr>
<tr><td rowspan="2">12</td><td rowspan="2">OUT8 – HS2 on/off</td><td></td><td>0</td><td>0</td><td>Off</td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>11</td><td>OUT9 – HS on/off</td><td colspan="5" rowspan="4">If a bit is set, the selected output driver is switched on. If the corresponding PWM enable bit is set the driver is only activated if PWM1 (PWM2) input signal is high. The outputs of OUT1-OUT6 are half bridges. If the bits of HS- and LS-driver of the same half bridge are set, the internal logic prevents that both drivers of this output stage can be switched on simultaneously in order to avoid a high internal current from VS to GND.</td></tr>
<tr><td>10</td><td>OUT10 – HS on/off</td></tr>
<tr><td>9</td><td>OUT11 – HS on/off</td></tr>
<tr><td>8</td><td>ECV – LS on/off</td></tr>
<tr><td>7</td><td>EC bit 5</td><td colspan="5" rowspan="6">Reference value for difference voltage amplifier at pin ECV is binary coded. Full scale value is set in control register 2. If all EC bits are set to zero the reference value is 0V. For fast discharge a lowside switch can be activated at pin ECV, if the ECV – LS on/off bit is set to '1'..</td></tr>
<tr><td>6</td><td>EC bit 4</td></tr>
<tr><td>5</td><td>EC bit 3</td></tr>
<tr><td>4</td><td>EC bit 2</td></tr>
<tr><td>3</td><td>EC bit 1</td></tr>
<tr><td>2</td><td>EC bit 0</td></tr>
<tr><td>1</td><td>EC switch</td><td colspan="5">In case this bit is set to 1, the electrochrome control is active and enables the driver at pin ECDR for the external MOS transistor. The bit switches the highside OUT10 directly on, ignoring bit 10 in control register 1. If the drain of the external MOS transistor is connected to OUT10, the current from supply VS to the load at ECV can be monitored.</td></tr>
<tr><td>0</td><td>0</td><td colspan="5">Reserved (has to be set to '0')</td></tr>
</table>

5.3 Control register 2

Table 27. Control register 2 (read/write)

Bit	Name	Comment
15	OUT1 – OCR enable	In case of an over-current event the over-current status bit (Status Register 0) is set and the output is switched off. If the Over-current Recovery Enable bit (OCR) is set, the output will be automatically reactivated after a delay time resulting in a PWM modulated current with a programmable duty cycle (bit 5 of control register 3). Depending on occurrence of over-current event and internal clock phase it is possible that one recovery cycle is executed even if this bit is set to zero. The ECV-OCR enable bit is disabled in electrochrome mode (bit1=1 control register 1).
14	OUT2 – OCR enable	
13	OUT3 – OCR enable	
12	OUT4 – OCR enable	
11	OUT5 – OCR enable	
10	OUT6 – OCR enable	
9	ECV – OCR enable	
8	0	Reserved (has to be set to '0')
7	OUT1 PWM1 enable	If the PWM1/2 Enable bit is set and the output is enabled (control register 0 or 1) the output is switched on if PWM1/2 input is high and switched off if PWM1/2 input is low. OUT5, 8 and OUT10 are controlled by PWM2 input, all other outputs are controlled by PWM1 input.
6	OUT2 PWM1 enable	
5	OUT3 PWM1 enable	
4	OUT4 PWM1 enable	
3	OUT5 PWM2 enable	
2	OUT6 PWM1 enable	
1	ECV PWM1 enable	
0	ECV-low voltage	The maximum ECV voltage in electrochrome mode is 1.5V. It corresponds to the full scale range of the digital to analog converter DAC set by the bits 7 to 2 of control register 1. If the ECV_low voltage bit is set to '0', the maximum voltage is limited to 1.2V without changing the resolution of the DAC. This is the default mode.

5.4 Control register 3

Table 28. Control register 3 (read/write)

<table>
<tr><th>Bit</th><th>Name</th><th>Comment</th></tr>
<tr><td>15</td><td>OUT7-OCR enable</td><td rowspan="5">In case of an over-current event the over-current status bit (Status register 1) is set and the output is switched off. If the Over-current Recovery Enable bit (OCR) is set the output will be automatically reactivated after a delay time resulting in a PWM modulated current with a programmable duty cycle (bit 5). Depending on the occurrence of the over-current event and the internal clock phase it is possible that one recovery cycle is executed even if this bit is set to zero.</td></tr>
<tr><td>14</td><td>OUT8-OCR enable</td></tr>
<tr><td>13</td><td>OUT9-OCR enable</td></tr>
<tr><td>12</td><td>OUT10-OCR enable</td></tr>
<tr><td>11</td><td>OUT11-OCR enable</td></tr>
<tr><td>10</td><td>OUT7 PWM1 enable</td><td rowspan="5">If the PWM1/2 Enable bit is set and the output is enabled (control register 0 or 1) the output is switched on if PWM1/2 input is high and switched off if PWM1/2 input is low. OUT5, 8 and OUT10 are controlled by PWM2 input all other outputs are controlled by PWM1 input.</td></tr>
<tr><td>9</td><td>OUT8 PWM2 enable</td></tr>
<tr><td>8</td><td>OUT9 PWM1 enable</td></tr>
<tr><td>7</td><td>OUT10 PWM2 enable</td></tr>
<tr><td>6</td><td>OUT11 PWM1 enable</td></tr>
<tr><td>5</td><td>OCR frequency
0: 1.7 kHz
1: 3 kHz</td><td>This bit defines in combination with the over-current recovery bit (Input Register 1) the over-current recovery frequency of an activated driver.</td></tr>
<tr><td>4</td><td>OV/UVR disable</td><td>If this bit is set the microcontroller has to clear the status register after undervoltage/overvoltage event to enable the outputs.</td></tr>
<tr><td>3</td><td>CM select bit 3</td><td rowspan="4">Depending on combination of bit 3 to 0 the current image of the selected highside output OUTn will be multiplexed to the CM/PWM2 output (see table below).
Other combinations deactivate the current monitor.

<table>
<tr><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Current image of</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>OUT1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>OUT2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>OUT3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>OUT4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>OUT5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>OUT6</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>OUT7</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>OUT8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>OUT9</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>OUT10</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>OUT11</td></tr>
</table>
</td></tr>
<tr><td>2</td><td>CM select bit 2</td></tr>
<tr><td>1</td><td>CM select bit 1</td></tr>
<tr><td>0</td><td>CM select bit 0</td></tr>
</table>

5.5 Status register 0

Table 29. Status register 0 (read)

Bit	Name	Comment
15	OUT1 – HS OC	In case of an over-current event the corresponding status bit is set and the output driver is disabled. If the over-current Recovery Enable bit is set the output will be automatically reactivated after a delay time resulting in a PWM modulated current with a programmable duty cycle. If the over-current recovery bit is not set, the micro controller has to clear the over-current bit to reactivate the output driver.
14	OUT1 – LS OC	
13	OUT2 – HS OC	
12	OUT2 – LS OC	
11	OUT3 – HS OC	
10	OUT3 – LS OC	
9	OUT4 – HS OC	
8	OUT4 – LS OC	
7	OUT5 – HS OC	
6	OUT5 – LS OC	
5	OUT6 – HS OC	
4	OUT6 – LS OC	
3	0	Reserved
2	0	
1	0	
0	0	

5.6 Status register 1

Table 30. Status register 1 (read)

Bit	Name	Comment
15	OUT1 – HS UC	Maskable by the configuration register
14	OUT1 – LS UC	
13	OUT2 – HS UC	The open load detection monitors the load current in each activated output stage. If the load current is below the under-current detection threshold for at least 1 ms (t_{dOL}) , the corresponding under-current bit UC is set. Due to mechanical/electrical inertia of typical loads a short activation of the outputs (e.g. 3ms) can be used to test the open load status without changing the mechanical/electrical state of the loads.
12	OUT2 – LS UC	
11	OUT3 – HS UC	
10	OUT3 – LS UC	
9	OUT4 – HS UC	
8	OUT4 – LS UC	
7	OUT5 – HS UC	
6	OUT5 – LS UC	
5	OUT6 – HS UC	
4	OUT6 – LS UC	
3	0	Reserved
2	0	
1	0	
0	0	

5.7 Status register 2

Table 31. Status register 2 (read)

Bit	Name	Comment
15	OUT7 – OC	In case of an over-current event the corresponding status bit OC is set and the output driver is disabled. If the over-current recovery enable bit is set the output will be automatically reactivated after a delay time resulting in a PWM modulated current with a programmable duty cycle. If the over-current recovery bit is not set the micro controller has to clear the over-current bit to reactivate the output driver. The open load detection monitors the load current in each activated output stage. If the load current is below the under-current detection threshold for at least 1 ms (t_{dOL}) the corresponding under-current bit UC is set. Due to mechanical/electrical inertia of typical loads a short activation of the outputs (e.g. 3ms) can be used to test the open load status without changing the mechanical/electrical state of the loads.
14	OUT7 – UC	
13	OUT8 – OC	
12	OUT8 – UC	
11	OUT9 – OC	
10	OUT9 – UC	
9	OUT10 – OC	
8	OUT10 – UC	
7	OUT11 – OC	
6	OUT11 – UC	
5	ECV – OC	
4	ECV – UC	
3	VS under-voltage	In case of an over-voltage or under-voltage event the corresponding bit is set and the outputs are deactivated. If VS voltage recovers to normal operating conditions outputs are reactivated automatically (if bit 4 of control register 3 is not set).
2	VS over-voltage	
1	ECV voltage not reached	Two comparators monitor the voltage at pin ECV in electrocrome mode. If this voltage is below / above the programmed target these bits signal the difference after at least 32 µs. The bits are not latched and may toggle after at least 32 µs, if the ECV voltage has not yet reached the target. They are not assigned to the Global Error Flag.
0	ECV voltage too high	

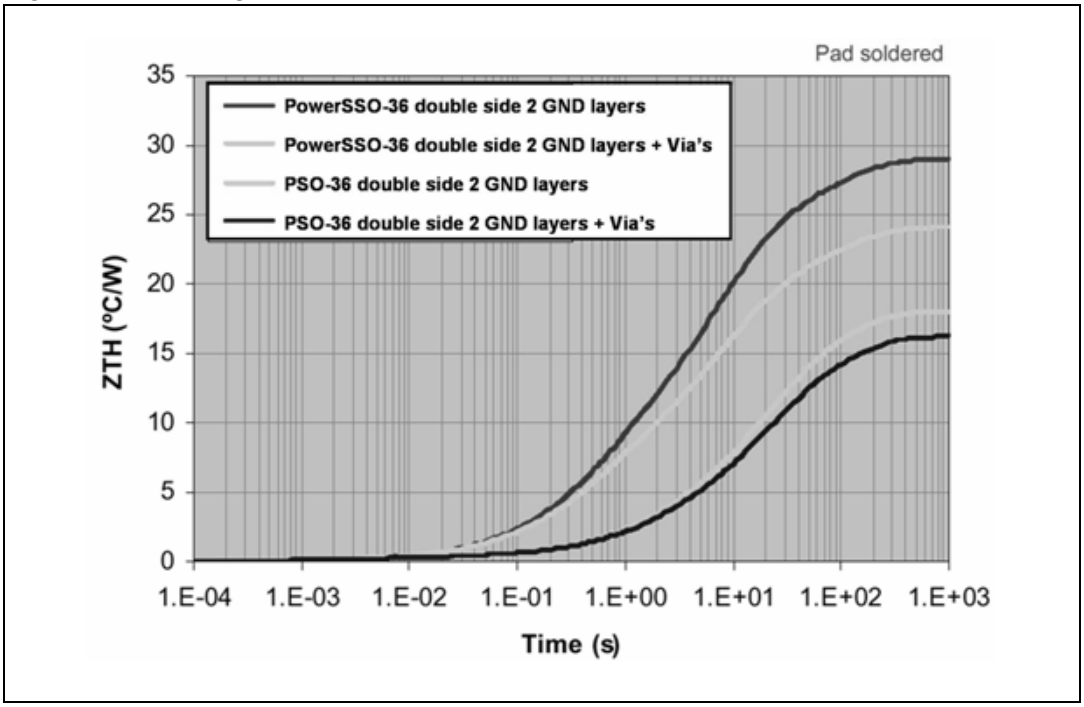
5.8 Configuration register

Table 32. Configuration register (read/write)

Bit	Name	Comment
15	0	Reserved (has to be set to '0')
14	0	
13	0	
12	0	
11	0	
10	0	
9	0	
8	0	
7	0	
6	0	
5	Mask for bit 15 of status reg. 1	Openload event (under-current status bit of OUT1 HS) is not considered in openload bit 1 of global status register.
4	Mask for bit 14 of status reg. 1	Openload event (under-current status bit of OUT1 LS) is not considered in openload bit 1 of global status register.
3	Mask for bit 3 of global status reg.	Temperature warning event is not considered in the 'Global Error Flag'.
2	0	Reserved (has to be set to '0')
1	Mask for bit 1 of global status reg.	Openload event (under-current status bit of OUTn) is not considered in the 'Global Error Flag'.
0	0	Reserved (has to be set to '0')

6 Packages thermal data

Figure 12. Packages thermal data



7 Package and packing information

7.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

7.2 PowerSSO-36 package information

Figure 13. PowerSSO-36 package dimensions

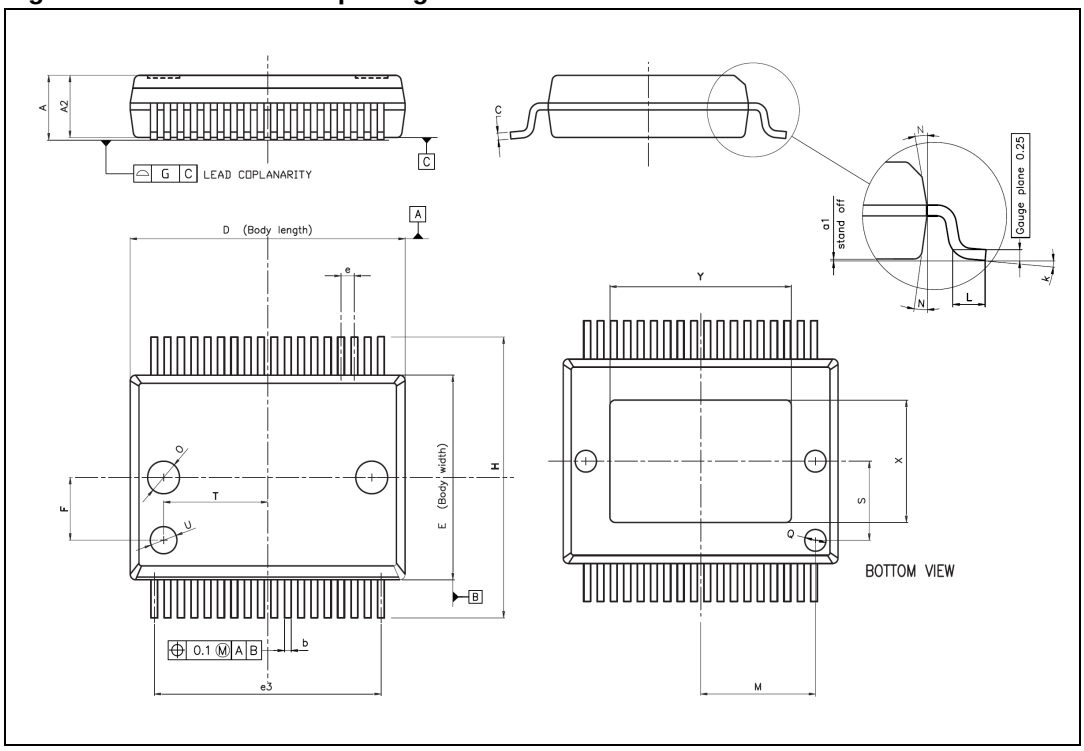


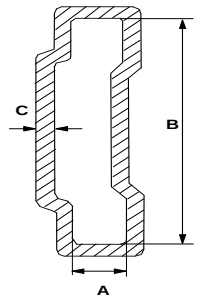
Table 33. PowerSSO-36 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	-	-	2.45
A2	2.15	-	2.35
a1	0	-	0.1
b	0.18	-	0.36
c	0.23	-	0.32
D(1)	10.10	-	10.50
E	7.4	-	7.6
e	-	0.5	-
e3	-	8.5	-
F	-	2.3	-
G	-	-	0.1
G1	-	-	0.06
H	10.1	-	10.5
h	-	-	0.4
k	0°	-	8°
L	0.55	-	0.85
M	-	4.3	-
N	-	-	10°
O	-	1.2	-
Q	-	0.8	-
S	-	2.9	-
T	-	3.65	-
U	-	1	-
X	4.3	-	5.2
Y	6.9	-	7.5

1. “D” and “E” do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side (0.006”).

7.3 PowerSSO-36 packing information

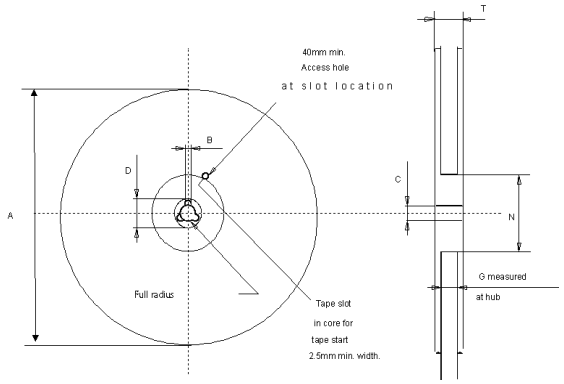
Figure 14. PowerSSO-36 tube shipment (no suffix)



Base Qty	49
Bulk Qty	1225
Tube length (±0.5)	532
A	3.5
B	13.8
C (±0.1)	0.6

All dimensions are in mm.

Figure 15. PowerSSO-36 tape and reel shipment (suffix "TR")



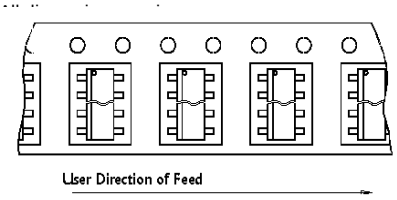
Reel dimensions

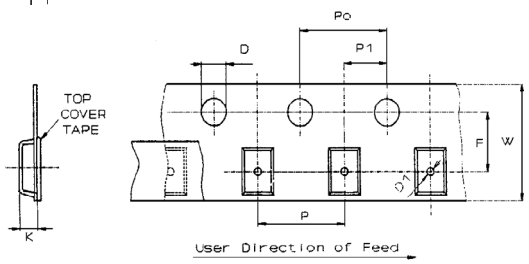
Base Qty	1000
Bulk Qty	1000
A (max)	330
B (min)	1.5
C (±0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

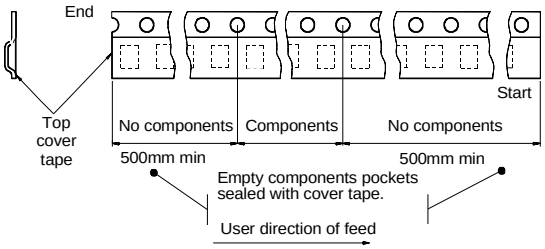
Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (±0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (±0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (±0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (±0.1)**	2







8 Revision history

Table 34. Document revision history

Date	Revision	Description of changes
12-Nov-2008	1	Initial release.
02-Jul-2009	2	*Table 33: PowerSSO-36 mechanical data*: – Deleted A (min) value – Changed A (max) value from 2.50 to 2.45 – Changed A2 (max) value from 2.40 to 2.35 – Changed L (max) value from 0.90 to 0.85
19-Nov-2010	3	Updated *Figure 1: Block diagram*
22-Sep-2013	4	Updated Disclaimer.

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