Mixed-Signal Dual-Core Control Processor with ARM Cortex-M4/M0 and 16-bit ADCs

Preliminary Technical Data

ADSP-CM411F/412F/413F/416F/417F/418F/419F

SYSTEM FEATURES

- Up to 240 MHz ARM Cortex-M4 with floating-point unit with up to 160K Byte zero-wait-state ECC SRAM
- Safety based dual independent- core concept
- Up to 1M Byte high performance ECC FLASH that can execute instructions at near SRAM speed
- Highest precision, low latency 31-channel analog front end
- 100 MHz ARM Cortex-M0 supervisor core with 32K Byte zero wait state ECC SRAM
- Single 3.3 V power supply
- Static memory controller (SMC) with asynchronous memory interface that supports 8-bit and 16-bit memories
- Heightened, 24-channel precision pulse PWM unit
- Four 3rd or 4th order SINC filters for glueless connection of sigma-delta modulators
- Hardware based harmonic analysis engine (HAE)
- Logic block array (LBA)
- FFT signal spectrum monitor
- MATH accelerator and FSAT blocks
- Two CAN 2.0B interfaces and up to five UARTs
- Two serial peripheral interface (SPI compatible) ports
- Four encoder interfaces, two with frequency division
- Package options:
  - 176-lead (24 mm × 24 mm) LQFP_EP package
  - 210-ball (15 mm × 15 mm) CSP_BGA package

ANALOG FRONT END

- 16-bit A/D converter with 24 multiplexed inputs, supporting 6-way simultaneous sampling and 6-channel conversion in 1.4µ seconds
- Independent 14-bit, 7-channel auxiliary ADC with seven inputs
- ADC controllers (ADCC0/ADCC1) and DAC controller (DACC0)
- 12-bit D/A converter
- Up to three 2.5 V precision voltage reference outputs
- (For details, see ADC/DAC/Voltage Reference/Comparator Specifications.)

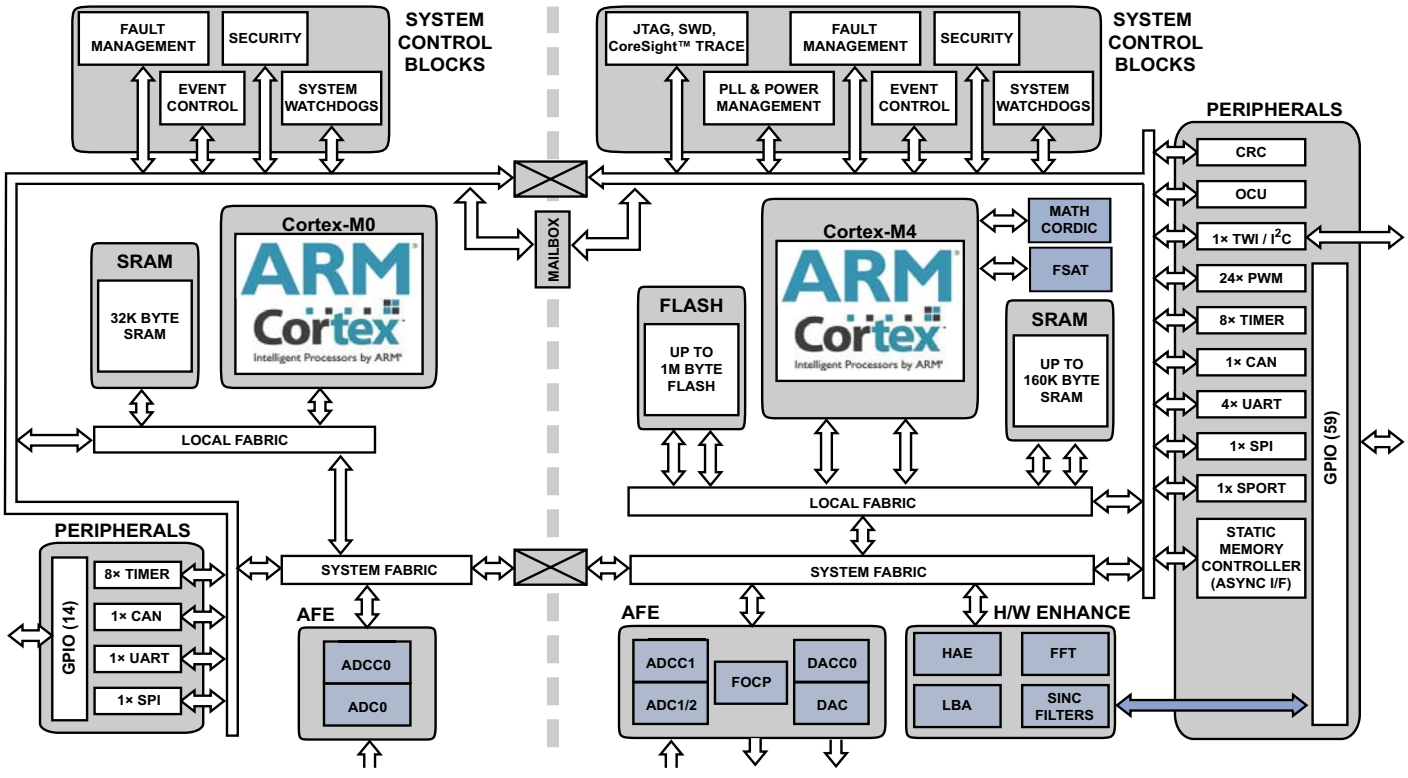

Figure 1. ADSP-CM41xF Block Diagram

Rev. PrC Document Feedback

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3/2018—Rev. PrB to Rev. PrC

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GENERAL DESCRIPTION

The ADSP-CM41xF family of mixed-signal control processors is based on the ARM® Cortex®-M4 processor core with floating-point unit operating at frequencies up to 240 MHz and the ARM® Cortex®-M0 processor core operating at frequencies up to 100 MHz. The processors integrate up to 192K Bytes of SRAM memory with ECC, up to 1M Byte of flash memory with ECC, accelerators and peripherals optimized for motor control and photo-voltaic (PV) inverter control, and an analog module consisting of up to two 16-bit SAR-type ADCs, one 14-bit ADC, and one 12-bit DAC. The ADSP-CM41xF family operates from a single voltage supply, generating its own internal voltage supplies using internal voltage regulators and a simple external transistor circuit.

By integrating a rich set of industry leading system functions and memory (shown in Table 1), the ADSP-CM41xF mixed-signal control processors are the platform of choice for next generation applications that require RISC (reduced instruction set computing) programmability and leading edge signal processing in one integrated package. These applications span a wide array of markets in power conversion and include solar PV inverters, motor/power control, and battery charging/control.

Table 1 provides the product features shown by generic model.

Table 1. Product Features

Generic	ADSP-CM411F		ADSP-CM412F		ADSP-CM413F		ADSP-CM416F		ADSP-CM417F		ADSP-CM418F		ADSP-CM419F	
Package Type	210-Ball BGA		176-Lead LQFP								210-Ball BGA			
Processor														
Processor Type	**SINGLE CORE:** ARM Cortex-M4						**DUAL CORE:** ARM Cortex-M4, ARM Cortex-M0							
M4 Processor Feature Code	A	B	A	B	B	C	B	C	C	D	B	C	C	D
M4 L1 SRAM (KB)[1]	128	128	128	128	128	160	128	160	160	160	128	160	160	160
M0 L1 SRAM (KB)[2, 3]	32	32	32	32	32	32	32	32	32	32	32	32	32	32
M4 L1 Flash (KB)	256	256	256	256	256	512	256	512	512	1024	256	512	512	1024
M4 Core Clock (MHz)	180	240	180	240	240	240	240	240	240	240	240	240	240	240
M0 Core Clock (MHz)[4]	N/A	N/A	N/A	N/A	N/A	N/A	100	100	100	100	100	100	100	100
Analog Functions														
16-bit ADC Simultaneous Sampling	3-Way at 2.2 Msps										6-Way at 4.4 Msps			
16-bit ADC Inputs	24		24		24		24		24		24		24	
16-bit ADC ENOB	11+		11+		13+		11+		13+		11+		13+	
14-bit ADC Inputs	7		7		7		7		7		7		7	
DAC Outputs	1		1		1		1		1		1		1	
FOCP (Fast Overcurrent Protection)	3		3		3		3		3		3		3	
Digital Functions														
GPIO (General-Purpose I/O)	73		73		73		73		73		73		73	
PWM (Pulse Width Modulator Out)	24		24		24		24		24		24		24	
HAE (Harmonics Analysis Engine)	0		0		1		1		1		1		1	
CORDIC	1		1		1		1		1		1		1	
FFT Arcing Detection	0		0		0		1		1		1		1	
SINC3 or SINC4 Filter Inputs	4		4		4		4		4		4		4	
CAN	2		2		2		2		2		2		2	
UART	3		3		5		5		5		5		5	
SPI	2		2		2		2		2		2		2	
I^2C	1		1		1		1		1		1		1	
GP Timers (General Purpose)	8		8		8		16		16		16		16	
SPORTs (Serial Ports)	1		1		1		1		1		1		1	
16-Bit EBIU	1		1		1		1		1		1		1	

[1] M4 L1 SRAM memory blocks are accessible from the M0 core as an L2 memory space. Memory protection features are available to regulate access.
[2] M0 L1 SRAM memory block is available on all models and variants.
[3] M0 L1 SRAM memory block is accessible from the M4 core as an L2 memory space.
[4] N/A means not applicable.

ANALOG FRONT END

The processors contain one ADC attached to the ARM Cortex-M0 core and two ADCs plus one DAC attached to the ARM Cortex-M4 core. Control of these data converters is simplified by two powerful on-chip analog-to-digital conversion controllers (ADCC) and a digital-to-analog conversion controller (DACC). The ADCC and DACC are integrated seamlessly into the software programming model, and they efficiently manage the configuration and real-time operation of the ADCs and DACs.

For technical details, see ADC/DAC/Voltage Reference/Comparator Specifications.

The ADCC of the ARM Cortex-M4 core provides the mechanism to control timing and execution of analog sampling events on the ADCs. The ADCC supports up to 6-channel simultaneous sampling (3x each on ADC1, ADC2) and can deliver 6 channels of consecutively and simultaneously sampled ADC data to memory in 1.4µs, or 16 channels sampled consecutively in simultaneous pairs to memory in 3.0µs. Conversion data from the ADCs may be either routed via DMA to memory, or to a destination register read by the processor, or written directly to any destination register without processor intervention (for example to the FFT). The ADCC can be configured so that the two ADCs sample and convert both sets of analog inputs simultaneously or at different times and may be operated in asynchronous or synchronous modes. Full time-matching performance can be achieved in synchronous mode.

Likewise, the DACC interfaces to one externally connected DAC and two internally connected threshold DACs, and has the purpose of managing those DACs. Conversion data to the DACs may be either routed from memory through DMA, or from a source register via the processor.

Functional operation and programming for the ADCC and DACC are described in detail in the ADSP-CM41x Mixed-Signal Control Processor with ARM Cortex-M4/ARM Cortex-M0 and 16-bit ADCs Hardware Reference.

ADC and DAC features and performance specifications differ by processor model. Simplified block diagrams of the ADCC, DACC and the ADCs and DACs are shown in Figure 2, Figure 3, and Figure 4.

Considerations for Best Converter Performance

As with any high performance analog/digital circuit, to achieve best performance, good circuit design and board layout practices should be followed. The power supply and its noise bypass (decoupling), ground return paths and pin connections, and analog/digital routing channel paths and signal shielding, are all of first-order consideration. For application hints of design best practice, see Figure 5 and Figure 6 and the ADSP-CM41x Mixed-Signal Control Processor with ARM Cortex-M4/ARM Cortex-M0 and 16-bit ADCs Hardware Reference. For more information about the VREG circuit, see Figure 18, Internal Voltage Regulator Circuit.

Fast Over Current Protection (FOCP)

The fast over current protection (FOCP) block is required to overcome the sampling rate requirement for certain inputs. There are three comparators available. The input of each comparator is connected internally to inputs A0, B0, and C0. The comparators have a common upper threshold (LIMIT_U) and a common lower threshold (LIMIT_L), which is set by the internal 8-bit DACs. COMP_OUT_A/B/C outputs are user accessible. If one or more comparators are signaling LIMT (availability of COMP_OUT_A/B/C), the AFE asserts an interrupt to the processor.

Analog Front End (AFE) Module

The ADC module contains two primary ADCs (ADC1 and ADC2), each with three multiplexed track and hold (T/H) units, which can each sample up to 8 analog inputs per T/H. In addition, the ADC module also contains a fully independent monitor ADC (ADC0) preceded by a 7-input channel multiplexer. See ADC Specifications –ADC0, ADC1, ADC2 for detailed performance specifications.

The voltage input range requirement for analog inputs is 0 V to 3.0 V. All analog inputs are of the same single-ended design. As with all single-ended inputs, signals from high impedance sources are the most difficult to control, and depending on the electrical environment, may require an external buffer circuit for signal conditioning (see Figure 7). Precharge buffers are included to assist the external buffers in charging the 25pF input capacitor. The precharge feature may be disabled in software.

DAC Module

The DAC is a 12-bit, low power, string DAC design. The output of the DAC is buffered, and can drive an R/C load to either ground or V_{DD_ANA}. See DAC Specifications for detailed performance specifications.

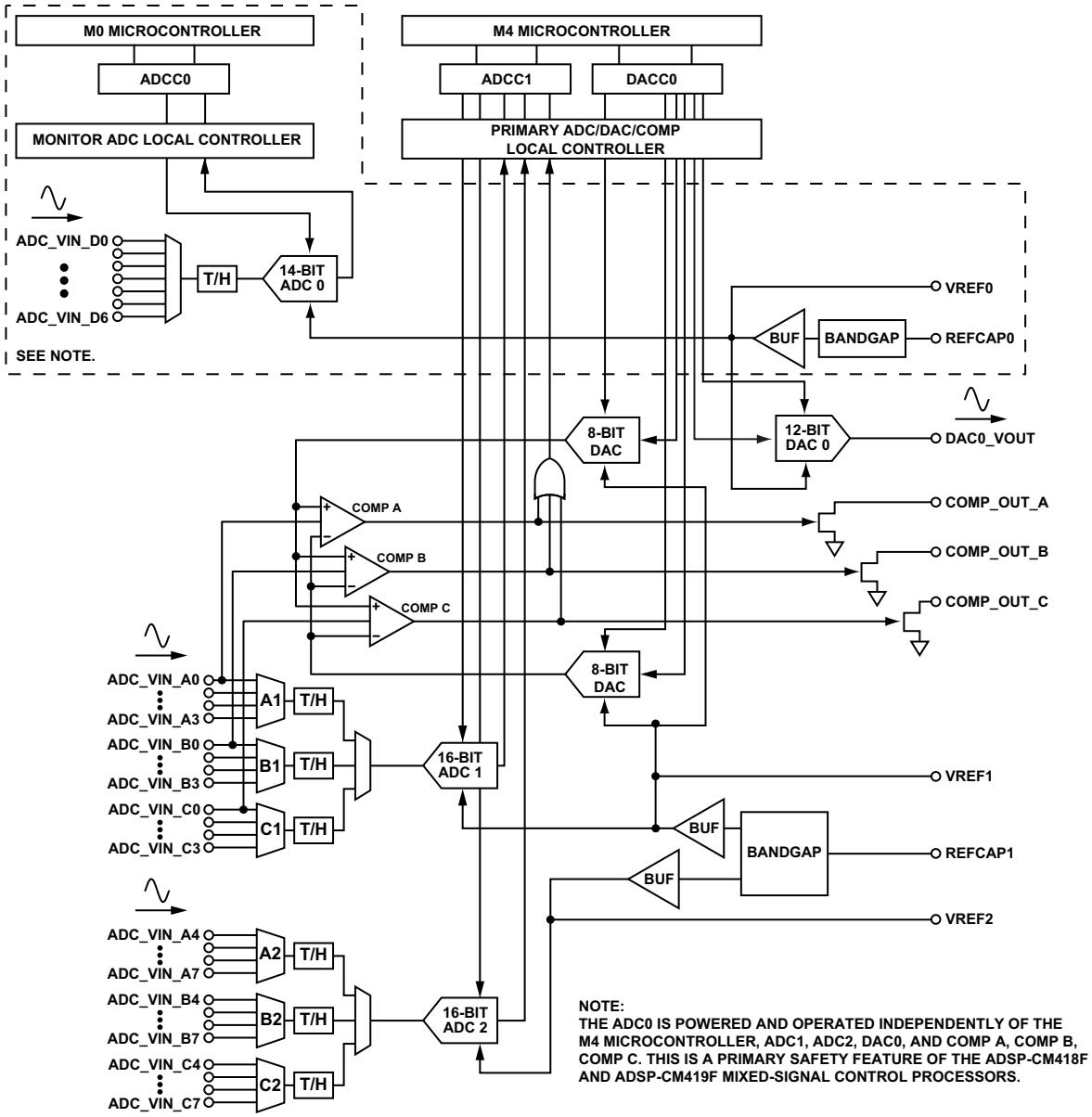


Figure 2. Analog Front End Block Diagram ADSP-CM418F/CM419F Dual-Core, 6-Way Sampling

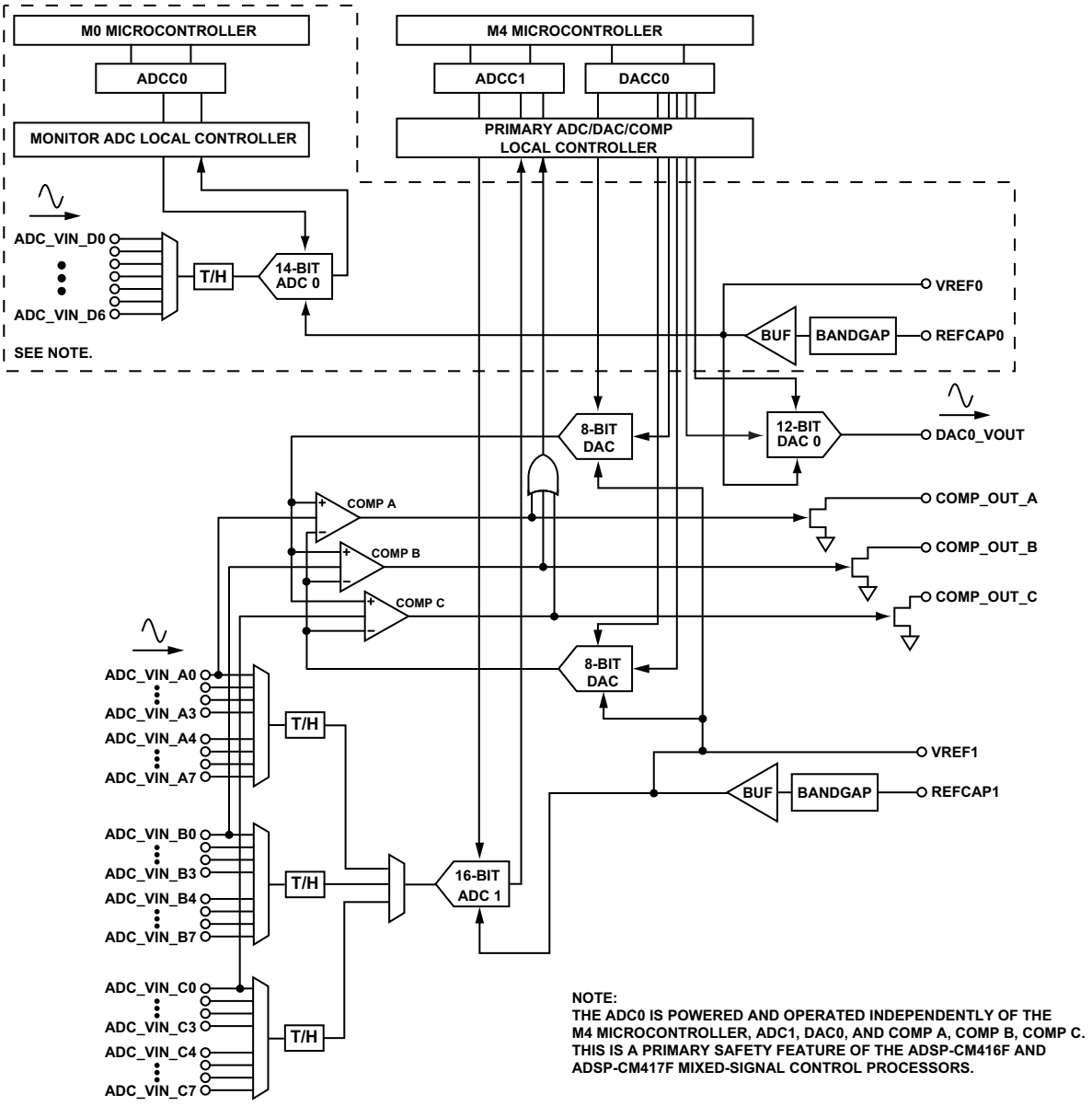


Figure 3. Analog Front End Block Diagram ADSP-CM416F/CM417F Dual-Core, 3-Way Sampling

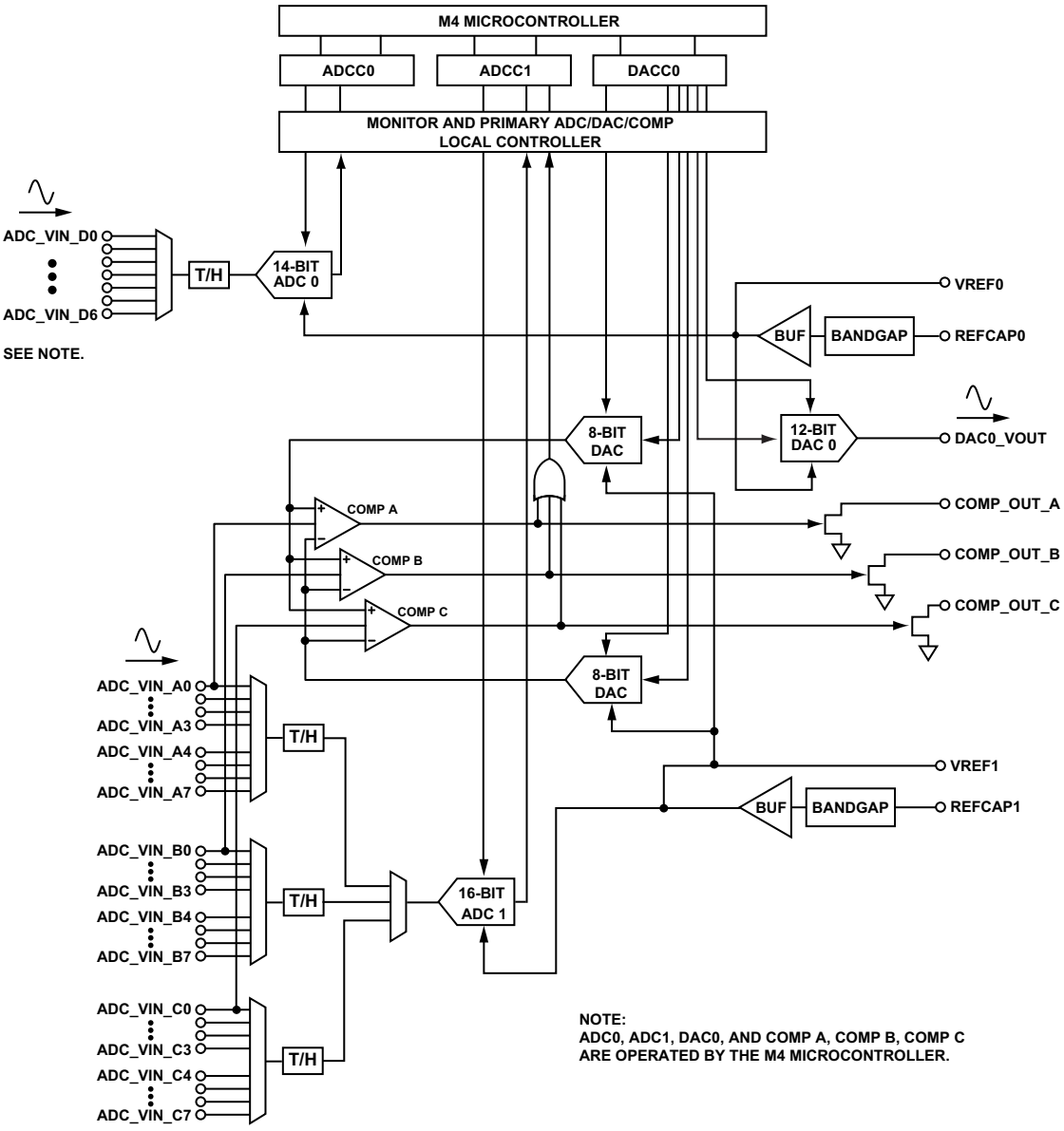


Figure 4. Analog Front End Block Diagram ADSP-CM411F/CM412F/CM413F Single Core, 3-Way Sampling

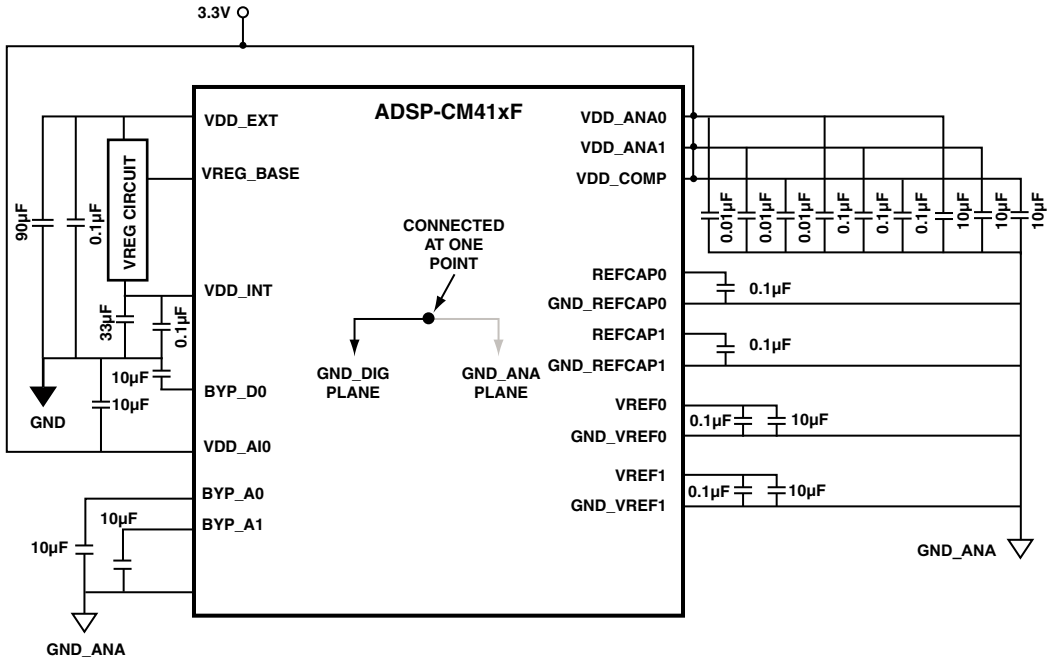


Figure 5. Typical Power Supply Configuration ADSP-CM411F, ADSP-CM412F, ADSP-CM413F, ADSP-CM416F, ADSP-CM417F

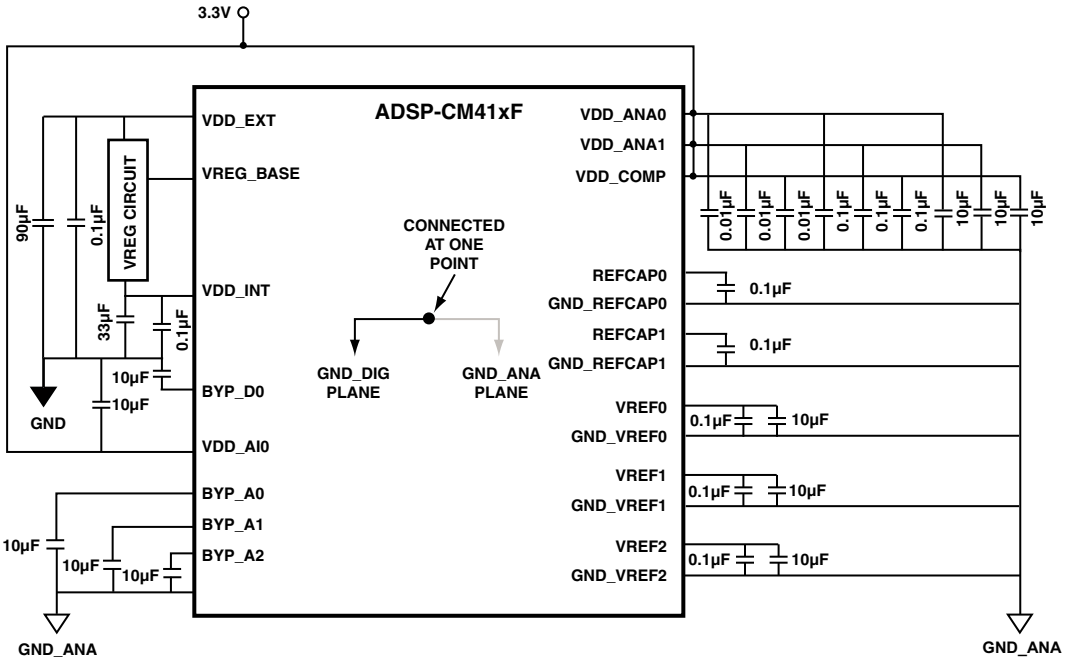


Figure 6. Typical Power Supply Configuration ADSP-CM418F, ADSP-CM419F

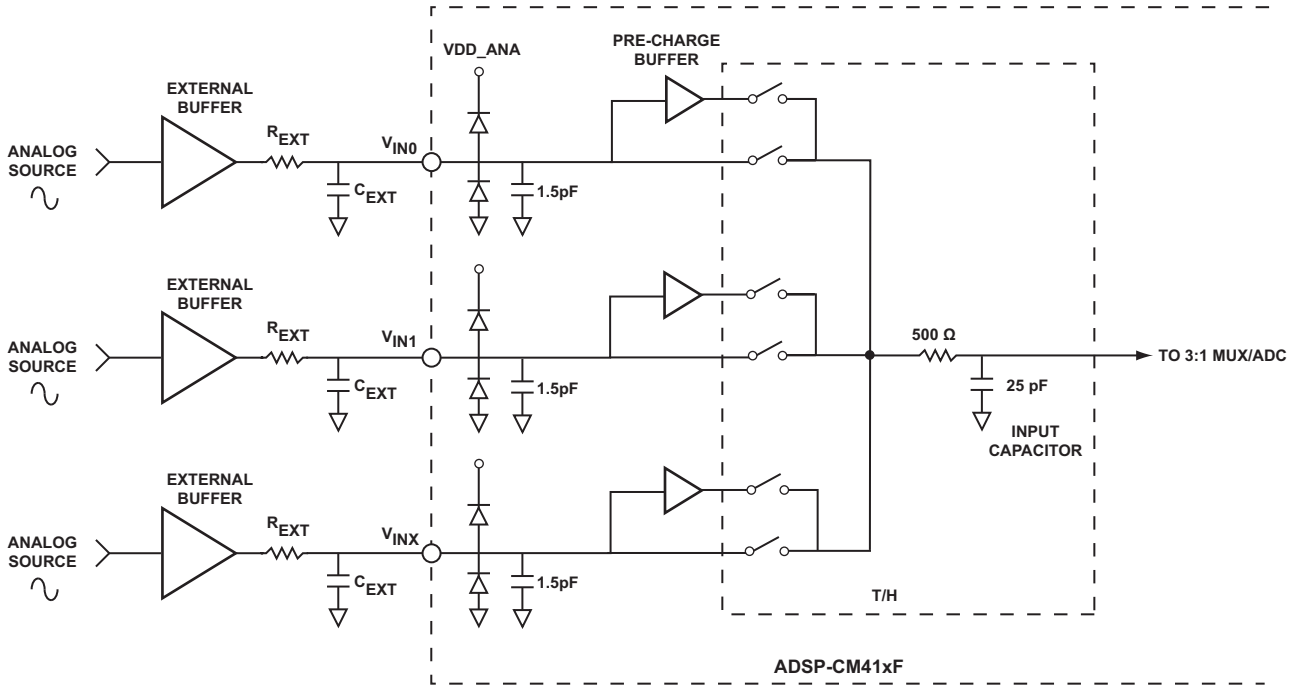


Figure 7. Equivalent Single-Ended Input (Simplified)

DUAL-CORE SYSTEM ARCHITECTURE

ADSP-CM41xF products may contain one ARM Cortex-M4 core, or may contain two ARM Cortex cores, an ARM Cortex-M4 and an ARM Cortex-M0. In dual-core products, the system architecture is functionally partitioned to allow each core reliable, independent operation (see Figure 8). Using system protection resources (SPUs and SMPUs), the programmer can partition control of the system resources arbitrarily among the two processors, down to the level of individual peripherals and to memory regions. Access to DMA slaves may be similarly regulated. Programmable bus timeout protection guarantees deterministic access completion time between core domains even in the presence of hardware faults in one domain.

Each processor is equipped with its own essential infrastructure: local SRAM, a set of communications peripherals (each has at least one universal asynchronous receiver/transmitter (UART), CAN, and SPI,) a trigger routing unit (TRU), a watchdog timer (WDT), a system event controller (SEC), an ADC controller (ADCC) and independent ADCs on the AFE, and a local APB and AXI bus fabric. The mailbox memory provides a shared memory bridge between the two subsystems for semaphores and messages. A number of general-purpose interrupts and triggers cross between subsystems to allow selected communication.

The main system AXI fabric provides universal memory interconnect between the two subsystems, displaying a unified memory map to both processors containing all system resources (except those internal to or tightly coupled to the ARM cores).

ARM Cortex-M0 Core

The ARM Cortex-M0 is a 32-bit ultra low gate count reduced instruction set computer (RISC). It uses 32-bit buses for instruction and data. The length of the data can be eight bits, 16 bits, or 32 bits. The length of the instruction word is 16 or 32 bits.

The M0 subsystem (see Figure 9) consists of the ARM Cortex-M0 core (see Figure 10), its local M0P platform SRAM, and its own communications peripherals (SPI, UART, CAN), instrumentation (ADCC), and infrastructure (SEC, TRU, WDT). The M0 subsystem operates in its own SCLK0 clock domain at speeds up to 100 MHz.The local AXI fabric supports DMA between the local peripherals and the M0P SRAM, independently from the connection of the M0 processor to the SRAM via the tightly coupled memory AHB bus matrix. The M0P SRAM is protected by SEC_DED ECC in hardware. The multibank striped construction of the SRAM supports concurrent core and DMA access when no bank conflict occurs. The APB and AXI fabrics of the M0 subsystems are connected to the ADSP-CM41x system, supporting incoming APB and DMA transactions (as DMA slave), as well as outgoing DMA transactions (as DMA master). DMA access latency is bounded by a fixed delay priority shift mechanism. A number of general-purpose trigger and interrupt signals also cross the boundary in both directions

The ARM Cortex-M0 controller features are described in the sections found on Page 12.

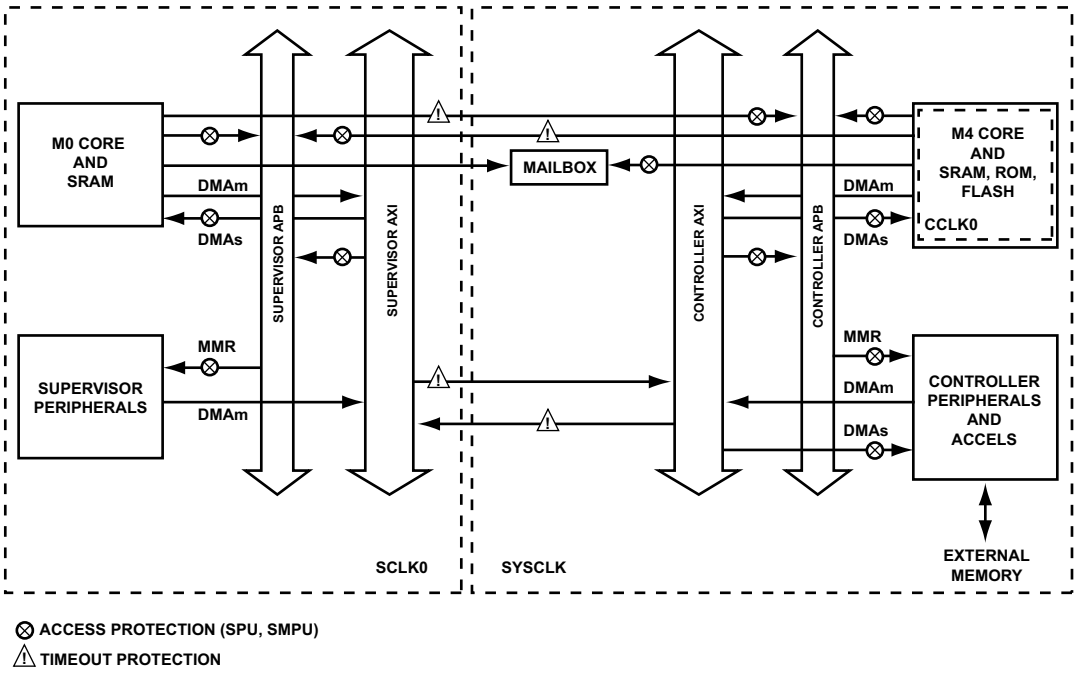


Figure 8. ADSP-CM41xF Dual-Core ARM Architecture

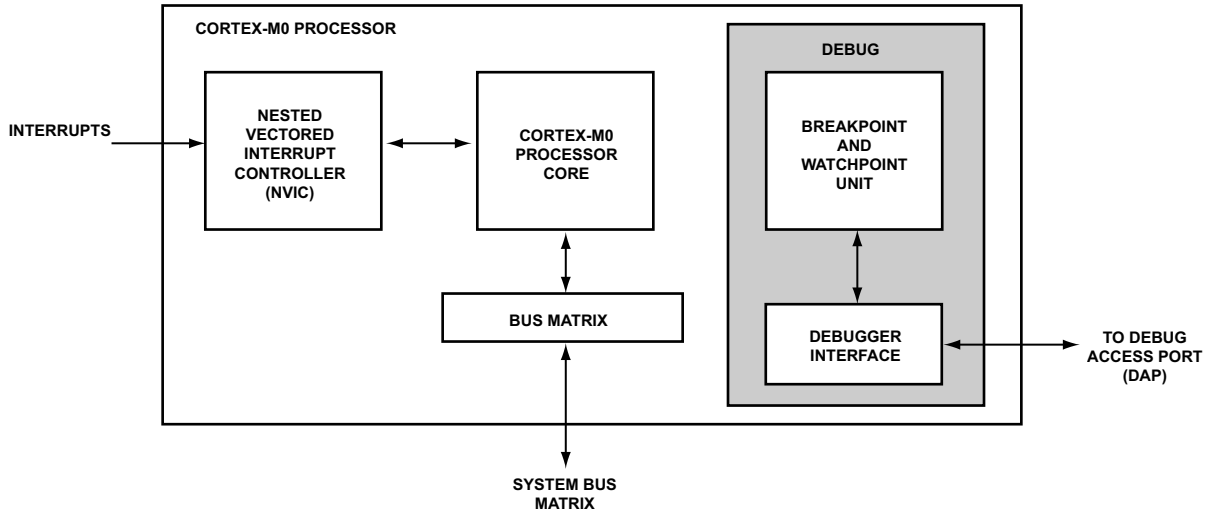


Figure 9. ARM Cortex-M0 Core

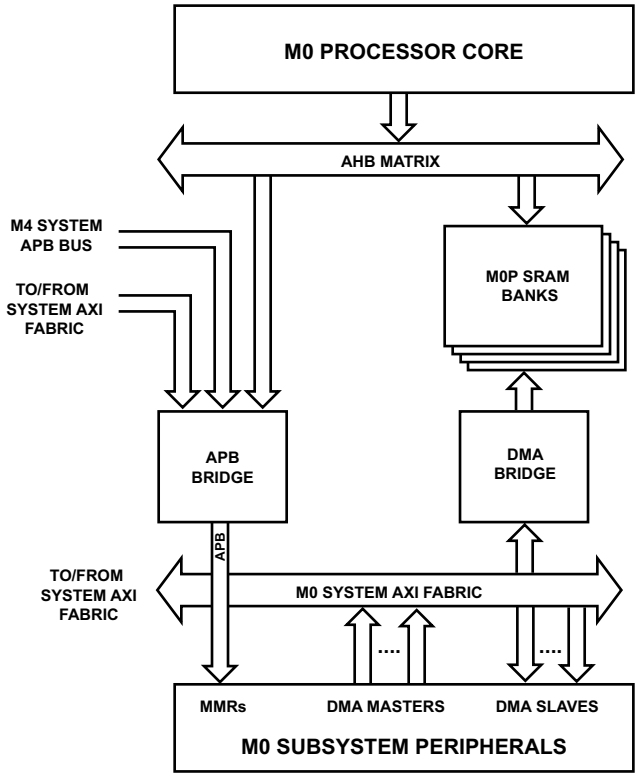


Figure 10. ADSP-CM41xF ARM Cortex-M0 Core Memory Subsystem (SCLK0 Clock Domain)

ARM Cortex-M0 Architecture

- Thumb-2 ISA technology
- Upward compatibility to the rest of the Cortex family
- 32-cycle multiplier, in designs optimized for low area
- NVIC interrupt controller (32 interrupts and 4 priority levels) supporting 75 interrupt sources with auxiliary multiplexing
- CoreSight™ debug, breakpoints, watchpoints, and cross-triggers

Microarchitecture

- 3-stage pipeline with branch speculation
- Low latency interrupt processing
- Von Neumann architecture

ARM Cortex-M4 Core

The ARM Cortex-M4 core (Figure 11) is a 32-bit reduced instruction set computer (RISC). It uses 32-bit buses for instruction and data. The length of the data can be 8 bits, 16 bits, or 32 bits. The length of the instruction word is 16 or 32 bits.

The M4F core memory subsystem (Figure 12) consists of the M4 core (Figure 11), the main memory group, the MATH/CORDIC co-processor, and the M4P subsystem control/status registers. The M4F subsystem operates in its own CCLK0 clock domain at speeds up to 240 MHz. The main memory group consists of the ECC-protected, 20-way-banked main SRAM, the boot ROM and the dual-banked, ECC-protected flash memory. The main memories support concurrent accesses by any of the three AHB buses of the M4 (ICODE, DCODE, and SYS) and by DMA slave accesses from the system AXI fabric, unless bank access conflicts occur. (System DMA cannot access the boot ROM, however.) DMA access latency is bounded by a programmable priority-shift mechanism. The M4F subsystem also features a MATH/CORDIC co-processor which accelerates IEEE single-precision floating-point transcendental functions. The subsystem connects to the ADSP-CM41x system peripherals and infrastructure by an APB bus bridge for memory-mapped register (MMR) access, and an AXI bus bridge for accesses to the ADSP-CM41x slave memory spaces (SMC, FFT, HAE, and the M0P).

The ARM Cortex-M4 controller features are described in the following sections.

ARM Cortex-M4 Architecture

- Thumb-2 ISA technology
- DSP and SIMD extensions
- Single cycle MAC (Up to 32 × 32 + 64 → 64)
- Hardware divide instructions
- Single precision FPU
- NVIC interrupt controller (129 interrupts and 16 priorities)
- Memory protection unit (MPU)
- Full CoreSight debug, trace, breakpoints, watchpoints, and cross triggers

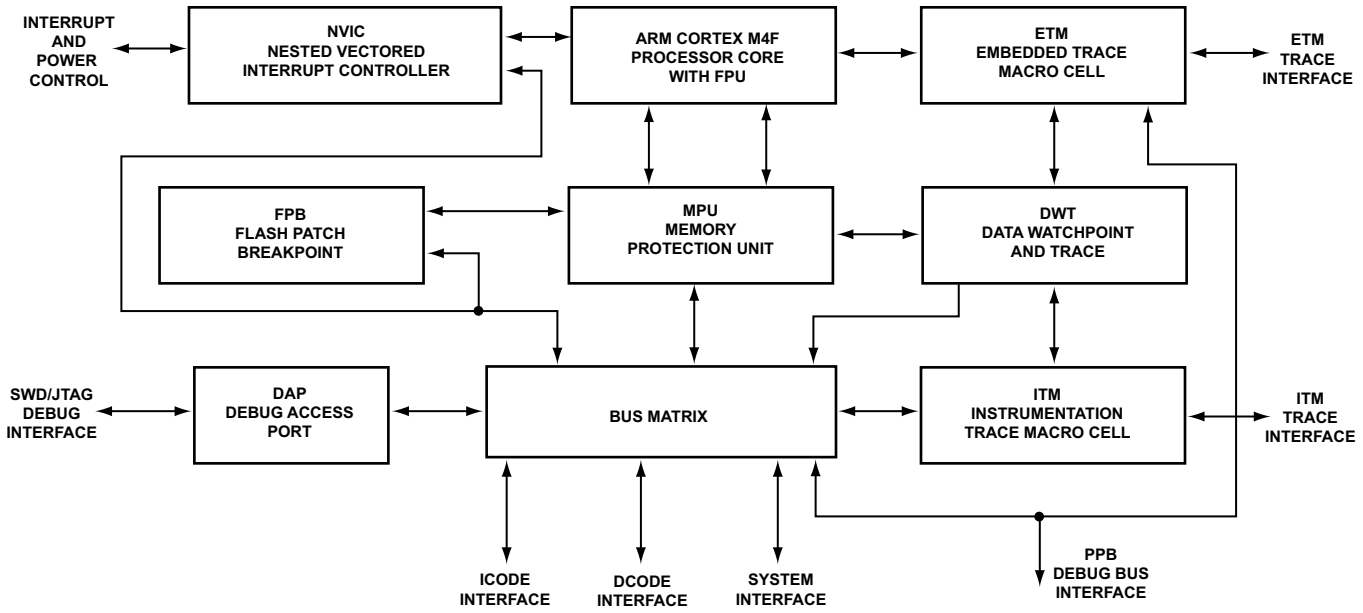


Figure 11. ARM Cortex-M4 Core

Microarchitecture

- 3 stage pipeline with branch speculation
- Low latency interrupt processing with tail chaining

Configurable For Ultra Low Power

- Deep sleep mode, dynamic power management
- Programmable clock generator unit

EmbeddedICE

EmbeddedICE® provides integrated on-chip support for the core. The EmbeddedICE module contains the breakpoint and watchpoint registers that allow code to be halted for debugging purposes. These registers are controlled through the JTAG and SWD test ports.

When a breakpoint or watchpoint is encountered, the processor halts and enters debug state. Once in a debug state, the processor registers can be inspected as well as the flash/EE, SRAM, and memory-mapped registers.

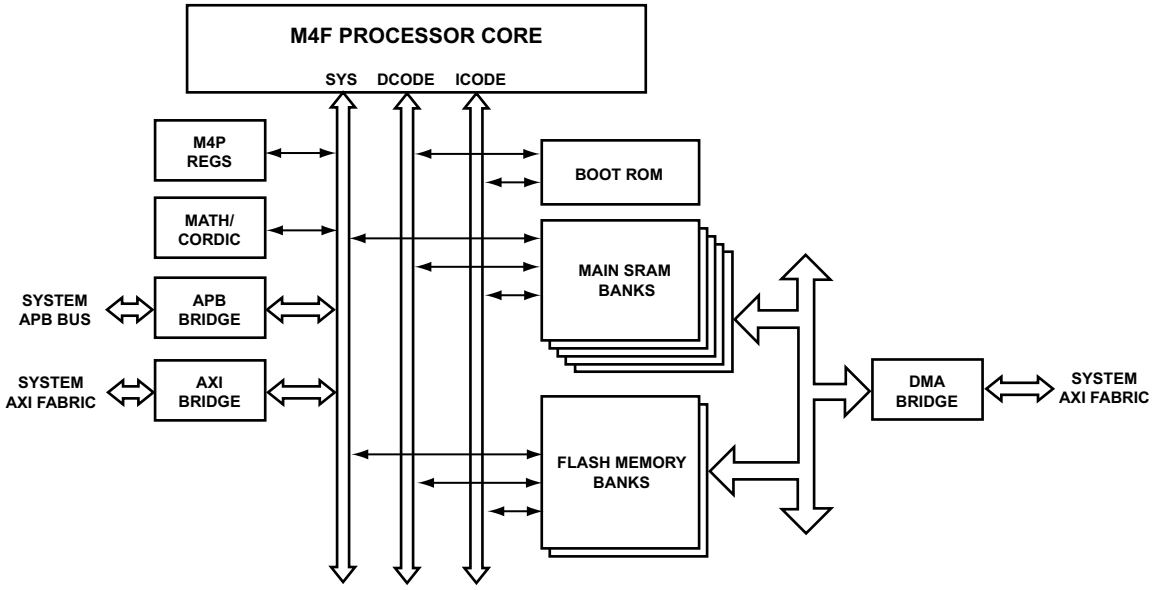


Figure 12. ADSP-CM41xF ARM Cortex-M4 Core Memory Subsystem (CCLK0 Clock Domain)

PROCESSOR INFRASTRUCTURE

The ADSP-CM41xF processor infrastructure supports two types of DMA connections: general-purpose DMA and optimized DMA. The following sections provide information on the primary infrastructure components of the ADSP-CM41xF processors.

General-Purpose DMA Controllers (DDEs)

The processor contains 12 peripheral DMA channels using one DDE engine each, plus one memory-to-memory (MDMA) stream with two DDE controllers plus CRC. DDE channels 0-3 (Figure 13) are for peripheral DMA within the M0 subsystem; channels 4-11 are for peripheral DMA within the M4 subsystem, and DDE channels 12-13 are for MDMA (Figure 14).

The DMA infrastructure supports concurrent access by DMA masters (peripherals, cores) to slave memory spaces (main and M0 SRAM, off-chip SMC SDRAM, and accelerator embedded memories), in a fully matrixed fashion (Figure 13, Figure 14). The DMA fabrics concurrently support one access per slave memory space per system clock cycle without conflict.

Each of the 14 DDE engines contains an independent data FIFO. In peripheral DDEs, one end of each FIFO is connected directly to the peripheral, while the other connects independently to the system fabric. This maximizes real-time peripheral performance, as the peripheral-to-FIFO connection does not consume system bus bandwidth to accept or deliver data to the peripheral.

A CRC engine is connected to the MDMA DDEs for validating the contents of data buffers, either during transport or in place (for example, for validating flash memory.)

To reflect the peripheral pin multiplexing selections of the user, individual DDEs are similarly multiplexed among up to three peripherals (Figure 14). This allows efficiently supporting a larger number of peripheral DMA endpoints with a smaller number of DDEs, while guaranteeing that for any set of peripherals connected to pins through the pin mux, there are always DDEs available to support them.

All ADSP-CM41xF processor DDEs support a powerful set of addressing and control options:

- 32-bit addressing with 32-bit increments
- 1-D or 2-D addressing with independent X, Y counts and offsets
- Selectable interrupts on completion of X_row or XY-array transfer
- Descriptor (scatter-gather) DMA mode controlled by arrays or linked lists of descriptors in system memory
- Autobuffer mode which continuously transfers data without processor intervention once started
- Trigger slave modes which start DMA based on an arbitrary hardware or software TRU event
- Trigger master modes which emit TRU triggers upon completion of X-row or XY-array

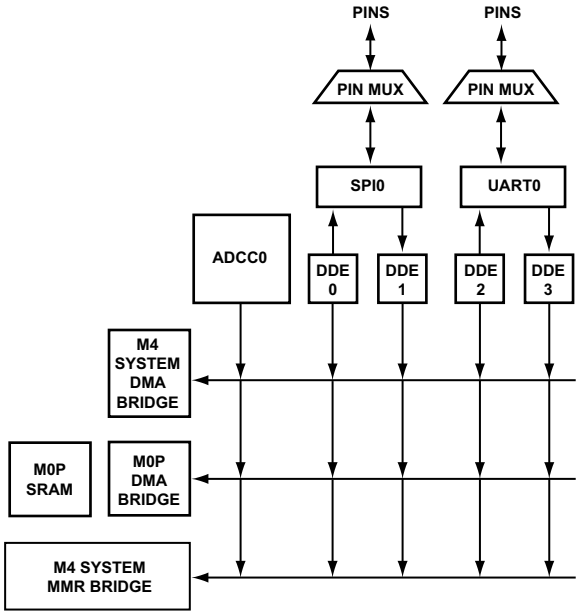


Figure 13. ADSP-CM41xF ARM Cortex-M0 DMA

Optimized DMA Controllers

High performance system peripherals and accelerators have different memory handling needs which cannot be met by a centralized, one-size-fits-all DMA controller. In the ADSP-CM41xF processor, the following system elements have integrated DMA capability which is tailored to the specific function of the unit:

- **ADCC**: The ADC controller writes data structures to memory for each timer's multi-sample frame, with an arbitrary layout of samples within the frame as designed by the user. Two or more sample frames can be arranged in a circular buffer, with an interrupt every N frames, or an unconstrained output buffer array of sample frames may be generated, followed by an interrupt upon completion.
- **SINC**: Similarly, the SINC unit writes data structures to memory for each timer, each containing filter output samples for one to four sigma-delta input streams. These frames may be arranged in a circular or linear fashion, with interrupts on each data frame.
- **FFT**: The FFT accelerator not only accepts input time-domain data from any memory master in the system (including the ADCC), but also outputs spectrum data to M4, M0, or SMC memory as each accelerator operation is completed.
- **DACC**: The DAC controller contains a DMA controller for reading output data from memory with 16- or 32-bit stride, in a linear or circular buffer fashion. Interrupts on each data sample may be enabled.

DMA Concurrency

In the processor architectures, the M4 and M0 memories and system fabrics are designed for ensuring high concurrency operation. The SRAM memories are divided into up to 20 independent array banks, with a combination of 4-way LSB-address and up to 5-way MSB-address striping methods. This means that up to four accesses to the SRAMs may all happen concurrently without any stall penalty, including one by system DMA and three by the AHB buses of the M4, provided no two accesses simultaneously contend for the same physical array bank. MSB-striping means that accesses to different 32 KB

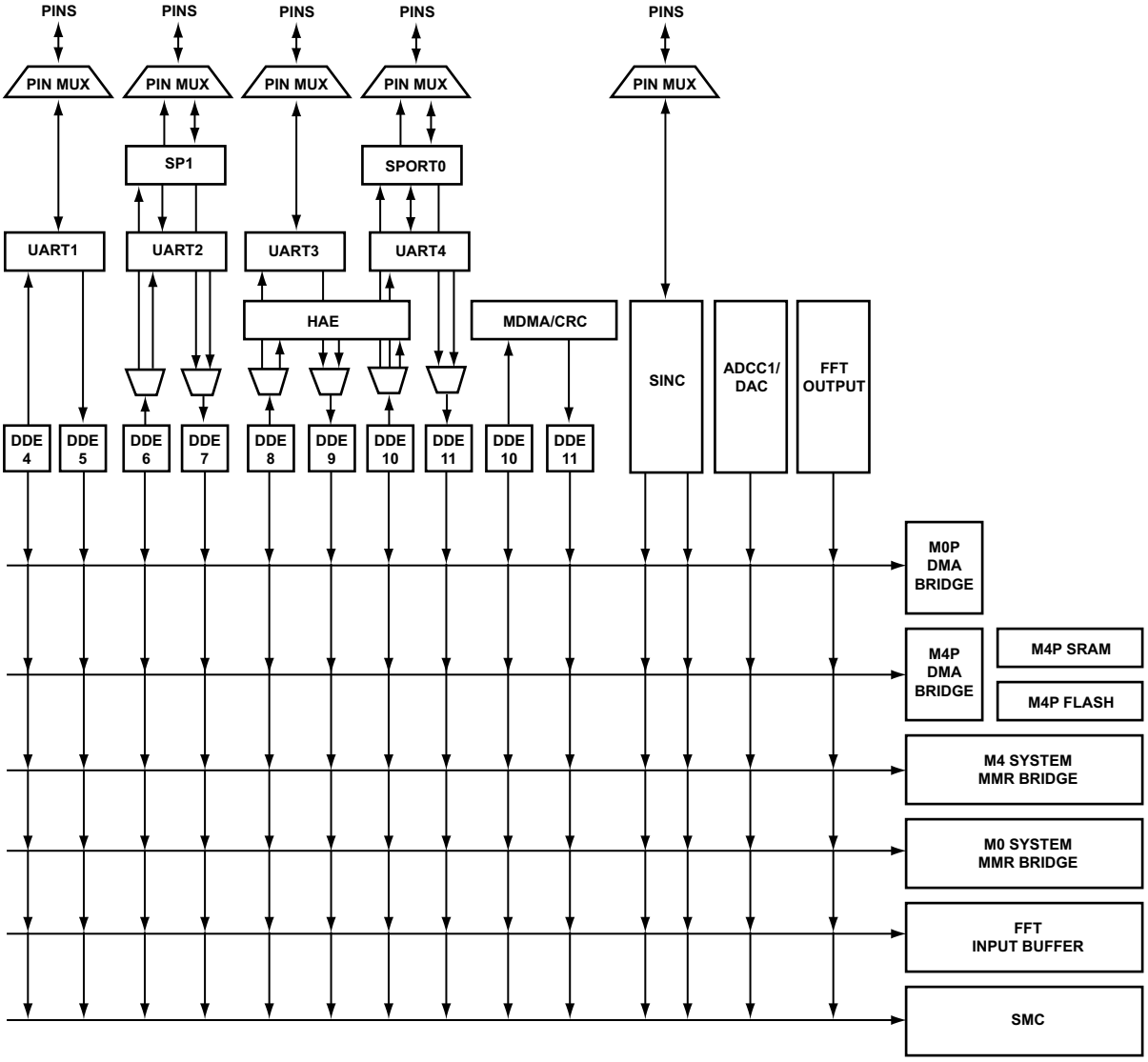


Figure 14. ADSP-CM41xF ARM Cortex-M4 DMA

ranges never cause stalls. LSB-striping means that concurrent accesses within such ranges only rarely conflict with one another (for example, ICODE vs. DCODE accesses.)

Further, DMA usually defers to core activity even if a banking access conflict occurs, but in a time-bounded manner. In almost all ARM-Mx code applications, DMA completes within a cycle or two of request without ever causing a processor stall, due to the memory bank partitioning. DMA will stall the processor, however, should a rare Mx application's access pattern impede DMA for longer than a programmable threshold, so that the real-time maximum latency of DMA within the system can be definitively bounded.

System Event Controller (SEC)

The system event controller (SEC) manages the enabling and routing of system fault sources through its integrated fault management unit.

There is a separate SEC for each processor core (SEC0 for M0, SEC1 for M4), allowing each core to maintain autonomous hardware monitors for all relevant interrupt and fault sources.

The SECs allow each core to enable and prioritize the notification of each fault source, to identify the highest priority active fault, and to coherently mark the end of handling of each event by the core. Non handled events may, after a programmable delay, be selected to cause the assertion of the $\overline{\text{SYS\_FAULT}}$ output, and/or to notify the other core through a TRU trigger that a failure of event processing has occurred.

The fault/event handling mechanism may be extended to off-chip sources as well, by using the bidirectional, open-drain SYS_FAULT pin. If so enabled, when this pin is externally pulled down, either or both cores can be notified.

Trigger Routing Unit (TRU)

The trigger routing unit (TRU) provides system-level sequence control without core intervention. The TRU maps trigger masters (generators of triggers) to trigger slaves (receivers of triggers). Slave endpoints can be configured to respond to triggers in various ways. Trigger events can also be routed from one TRU to another as general-purpose trigger pulses (GTPs). Common applications enabled by the TRU include,

- Initiating the ADC sampling periodically in each pulse width modulation (PWM) period or based on external events
- Controlling functional safety mechanisms
- Automatically triggering the start of a DMA sequence after a sequence from another DMA channel completes
- Software triggering
- Synchronization of concurrent activities

Trigger Timing Unit (TTU)

The trigger timing unit (TTU) provides a flexible mechanism for splitting, delaying, and generating periodic patterns of TRU triggers. Eight TRU outputs can be associated with any of four trigger groups, whose operation is initiated by TRU trigger inputs. A trigger group can be configured as a single-shot pattern, with each assigned trigger output delayed by an independent delay with SYSCLK resolution. Alternatively, any trigger group can be configured for periodic operation, where each assigned trigger output has an independent positive or negative delay which may lead or lag the reference timer.

A typical use of the TTU is to precisely control the relative time of the activity of several peripherals. For example, the TTU can be used to synchronize the periodic operation of multiple PWM units with the acquisition of ADC samples at a precise time offset.

Pin Interrupts (PINT)

Every port pin on the processors can request interrupts in either an edge sensitive or a level sensitive manner with programmable polarity. Interrupt functionality is decoupled from GPIO operation. Six system-level interrupt channels (PINT0–PINT5) are reserved for this purpose. Each of these interrupt channels can manage up to 32 interrupt pins. The assignment from pin to interrupt is not performed on a pin by pin basis. Rather, groups of eight pins (half ports) can be flexibly assigned to interrupt channels.

Every pin interrupt channel features a special set of 32-bit memory-mapped registers that enable half-port assignment and interrupt management. This includes masking, identification, and clearing of requests. These registers also enable access to the respective pin states and use of the interrupt latches, regardless of whether the interrupt is masked or not. Most control registers feature multiple MMR address entries to write-one-to-set or write-one-to-clear them individually.

General-Purpose I/O (GPIO)

Each general-purpose port pin can be individually controlled by manipulating the port control, status, and interrupt registers:

- GPIO direction control register specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers have a write one to modify mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins.
- GPIO interrupt mask registers allow each individual GPIO pin to function as an interrupt to the processors. GPIO pins defined as inputs can be configured to generate hardware interrupts, while output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers specify whether individual pins are level or edge sensitive and specify, if edge sensitive, whether the rising edge or both the rising and falling edges of the signal are significant.
- GPIO pull-up enable registers enable weak, pull-ups on individual pins.

PWM Pin Programmable Drive Strength

GPIOs configured as PWM pins support a programmable, two-level drive strength capability to support glueless drive of opto-isolated interface devices.

Pin Multiplexing

The processors support a flexible multiplexing scheme that multiplexes the GPIO pins with various peripherals. A maximum of five peripherals plus GPIO functionality is shared by each GPIO pin. All GPIO pins have a bypass path feature—that is, when the output enable and the input enable of a GPIO pin are both active, the data signal before the pad driver is looped back to the receive path for the same GPIO pin.

For more information, see:

- GPIO Multiplexing for 210-Ball CSP_BGA Package
- GPIO Multiplexing for 176-Lead LQFP_EP Package

GPIO Pin Safe State Sequence

Each ADSP-CM41xF GPIO supports a fault-safety mechanism by which, upon detection of a serious fault, the pin can be programmed to drive a preselected safe state of 0, 1, or Z. This safe state event can further be programmed to be immediate or delayed in a global delay programmed in approximately 1 µs units timed by an on-board RC oscillator. This allows a fault response comprising a two-step sequence of arbitrary pin states, separated by 1 to 15 µs. The fault response is completely independent of the processor, the processor clocks (PLL and crystal), and even of the VDDINT supply, and only requires the presence of the 3V VDDEXT supply.

The serious faults which can be selected to trigger a pin safe state response include:

- VMU-detected power supply faults on VDDINT or VDDEXT
- OSCWDOG-detected major faults of the system SYS_CLKIN0 input (missing or wrong harmonic mode)
- OCU-detected fine-grained faults of the system clocks or faults of the PLL
- Arbitrary hardware-detected faults or software-initiated events routed by the trigger routing unit.

As these types of faults may prevent the proper operation of one or both processor cores, these are called unrecoverable faults, and can only be cleared by the assertion of the SYS_HWRST hard reset pin.

MEMORY ARCHITECTURE

The internal and external memory of the ADSP-CM41xF processor is shown in Figure 15 and described in the following sections.

ARM Cortex-M4 Memory Subsystem

The memory map of the ADSP-CM41xF family is based on the Cortex-M4 model from ARM. By retaining the standardized memory mapping, it becomes easier to port applications across M4 platforms. Only the physical implementation of memories inside the model differs from other vendors.

ADSP-CM41xF application development is typically based on memory blocks across CODE/SRAM and external memory regions. Sufficient internal memory is available via internal SRAM and internal flash. Additional external memory devices may be interfaced via the SMC asynchronous memory port, as well as through the SPI0 serial memory interface.

Code Region

Accesses in this region (0x0000_0000 to 0x1FFF_FFFF) are performed by the core on its ICODE and DCODE interfaces, and they target the memory resources within the Cortex-M4F platform integration component.

- **Boot ROM.** An 8K byte boot ROM executed at system reset. This space supports read-only access by the M4F core only. Note that ROM memory contents cannot be modified by the user.
- **Internal SRAM Code Region.** This memory space contains the application instructions and literal (constant) data which must be executed in real time. It supports read/write access by the M4F core and read/write DMA access by system devices. Internal SRAM can be partitioned between code and data (SRAM region in M4 space) in 32K byte blocks. Access to this region occurs at core clock speed, with no wait states.
- **Integrated Flash.** This memory space includes up to 1M byte of flash memory which holds the user program and constant data. The initial vector table and reset boot vector are located at the base of flash memory.

  Read access to this region occurs at up to core clock speed, optimized by a powerful flash prefetch unit.

  The flash memory also includes up to two 4K byte blocks called info blocks. Predefined locations in the info blocks can contain user's security keys for locking debug access to the device as well as controls for boot-time initialization of the device

  Flash memory can be erased in 4 KB page units, or in mass erase operations. The memory is ECC-protected, supporting writes in 64-bit (8-byte) units.

SRAM Region

Accesses in this region (0x2000_0000 to 0x3FFF_FFFF) are performed by the ARM Cortex-M4F core on its SYS interface. The SRAM region of the core can otherwise act as a data region for an application.

- **Internal SRAM Data Region.** This space can contain read/write data. Internal SRAM can be partitioned between code and data (SRAM region in M4 space) in 32K byte blocks. Access to this region occurs at core clock speed, with no wait states. It supports read/write access by the M4F core and read/write DMA access by system devices. It supports exclusive memory accesses via the global exclusive access monitor within the Cortex-M4F platform. Bit-banding support is also available.

System Memory Spaces

- **System MMRs.** Various system MMRs reside in this region. Bit-banding support is available for MMRs.

External Asynchronous Parallel Flash/RAM

- **L2 Asynchronous Memory.** Up to 32M byte × 4 banks of external memory can be optionally connected to the asynchronous memory port (SMC). Direct read/write data access is also possible.

System Region

Accesses in this region (0xE000_0000 to 0xF7FF_FFFF) are performed by the ARM Cortex-M4F core on its SYS interface and are handled within the Cortex-M4F platform. The MPU may be programmed to limit access to this space to privileged mode only.

- **CoreSight ROM.** The ROM table entries point to the debug components of the processor.
- **ARM PPB Peripherals.** This space is defined by ARM and occupies the bottom 256K byte of the SYS region (0xE000_0000 to 0xE004_0000). The space supports read/write access by the M4F core to the internal peripherals of the ARM core (MPU, ITM, DWT, FPB, SCS, TPIU, ETM) and the CoreSight ROM. It is not accessible by system DMA.
- **Platform Control Registers.** This space has registers within the Cortex-M4F platform integration component that control the ARM core, its memory, and the flash memory controllers. It is accessible by the M4F core via its SYS port (but is not accessible by system DMA).

Static Memory Controller (SMC)

The static memory controller (SMC) is programmed to control up to four blocks of external memories or memory-mapped devices, with flexible timing parameters. Each block occupies a 32 Mb segment regardless of the size of the device used.

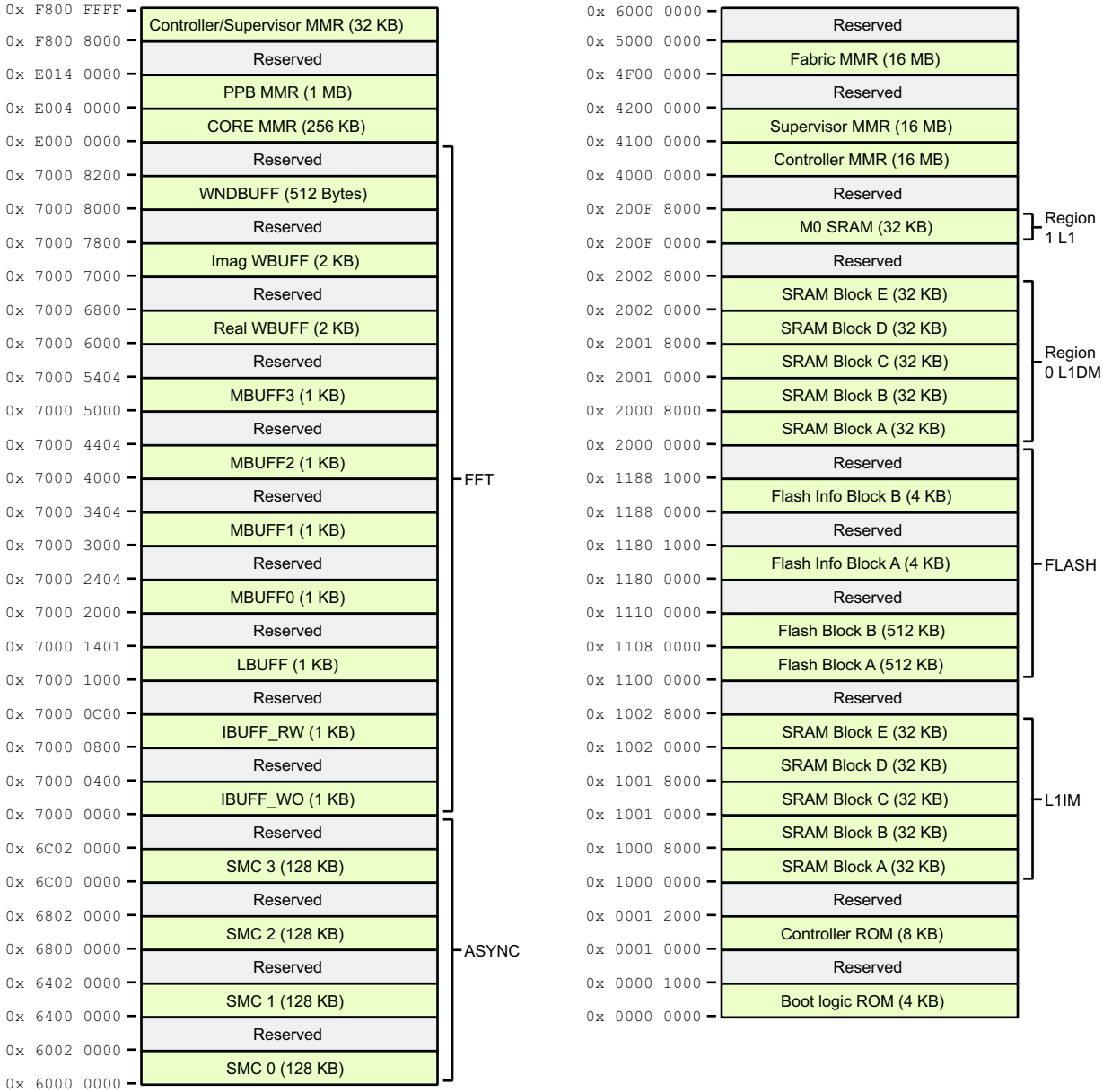


Figure 15. ADSP-CM41xF ARM Cortex-M4 Memory Map

Booting

The processors have two mechanisms for automatically loading internal and external memory after a reset. The boot mode is defined by the SYS_BMODE[0] input pins. There are two boot modes: boot from flash memory, or load flash from a UART serial port.

Because the M0 subsystem does not have a ROM, the M4 must load an M0 application into M0 SRAM before starting the M0. The M0 application can be conveniently stored in flash memory, or it can be loaded from any desired source or communications interface in the ADSP-CM41x system.

The boot modes are shown in Table 2. These modes are implemented by the SYS_BMODE[0] bits of the reset configuration register and are sampled during power-on resets and software initiated resets.

Table 2. Boot Modes

SYS_BMODE[0] Setting	Description
0	Direct code execution from integrated flash memory
1	UART based flash firmware upgrade

SYSTEM ACCELERATION

The following sections describe the system acceleration blocks of the ADSP-CM41xF processors.

Harmonic Analysis Engine (HAE)

The harmonic analysis engine (HAE) block receives 8 kHz input samples from two source signals whose frequencies are between 45 Hz and 65 Hz. The HAE processes the input samples and produces output results. The output results consist of power quality measurements of the fundamental and up to 12 additional harmonics.

FFTB Signal Spectrum Monitor

The FFTB signal spectrum monitor accelerator provides background input signal spectrum analysis, with built-in data conversion for various sensor input formats, spectrum averaging, square magnitude computation, and band power limit detection. The FFTB unit provides up to 512-point 16-bit FFT on the input signal data provided by memory or by DMA, with optional input format conversion, Comb filtering, windowing, programmable FFT size, squared-magnitude computation, spectrum averaging, and spectrum limit checking.

The FFTB unit can be configured to accept data directly from a signal source stream such as an ADC or SINC filter, without processor intervention, and without DMA into/out of SRAM. The FFT can write its results directly to any memory space, including SRAM on either the M0 or M4.

Sinus Cardinalis (SINC) Filter

The sinus cardinalis (SINC) filter module processes four bit streams using a pair of configurable SINC filters for each bit stream. The purpose of the primary SINC filter of each pair is to produce the filtered and decimated output for the pair. The output can decimate any integer rate between 8 and 256 times lower than the input rate. Greater decimation allows greater removal of noise, and, therefore, greater effective number of bits (ENOB).

Optional additional filtering outside the SINC module can further increase ENOB. The primary SINC filter output is accessible through transfer to processor memory, or to another peripheral, via DMA.

Each of the four channels is also provided with a low latency secondary filter with programmable positive and negative overrange detection comparators. These limit detection events can interrupt the core, generate a trigger, or signal a system fault.

SECURITY FEATURES

The processor provides a combination of hardware and software protection mechanisms that lock out access to the device in secure mode, but grant access in open mode. These mechanisms include password-protected UART flash loader, as well as password-protected JTAG/SWD debug interfaces.

CAUTION
This product includes security features that can be used to protect embedded nonvolatile memory contents and prevent execution of unauthorized code. When security is enabled on this device (either by the ordering party or the subsequent receiving parties), the ability of Analog Devices to conduct failure analysis on returned devices is limited. Contact Analog Devices for details on the failure analysis limitations for this device.

SECURITY FEATURES DISCLAIMER

To our knowledge, the Security Features, when used in accordance with the data sheet and hardware reference manual specifications, provide a secure method of implementing code and data safeguards. However, Analog Devices does not guarantee that this technology provides absolute security. ACCORDINGLY, ANALOG DEVICES HEREBY DISCLAIMS ANY AND ALL EXPRESS AND IMPLIED WARRANTIES THAT THE SECURITY FEATURES CANNOT BE BREACHED, COMPROMISED, OR OTHERWISE CIRCUMVENTED AND IN NO EVENT SHALL ANALOG DEVICES BE LIABLE FOR ANY LOSS, DAMAGE, DESTRUCTION, OR RELEASE OF DATA, INFORMATION, PHYSICAL PROPERTY, OR INTELLECTUAL PROPERTY.

SAFETY FEATURES

The ADSP-CM41xF processors are designed to support functional safety applications. While the level of safety is mainly dominated by the system concept, the following primitives are provided by the processors to build a robust safety concept.

Voltage Monitoring Unit (VMU)

The voltage monitoring unit (VMU) is an on-chip integrated power supply supervisory block for detecting under voltage and over voltage on both VDD_EXT and VDD_INT power supplies. The VMU is responsible for controlling the GPIO pin safe state mechanism and its sequence timing. The VMU is also responsible for putting flash into a safe state upon detecting a supply fault. Note, the internal voltage regulator must be used when using the VMU.

Oscillator Comparator Unit (OCU)

The processors contain an oscillator comparator unit (OCU) for detecting faults in the SYSCLK clock line. The OCU uses an external auxiliary clock or crystal input SYS_CLKIN1 to detect various conditions such as clock dead and clock frequency limit violations. The OCU can generate several events to inform the processor about the violations. A clock not good signal (CLKNG) can be configured to put the chip into a reset state when detecting a fault event. It can also initiate the GPIO pin safe state mechanism.

Error Correcting Codes (ECC) Protected L1 Memories

The M4 and M0 processor L1 SRAMs, flash memory, and mailbox memory are all protected with zero-wait-state SEC-DED ECC, natively protecting 32-bit memory elements. Writes of 8- and 16-bit data, where applicable, cause automatic background read-modify-write ECC updates, typically with no observable processor stalls. Refresh assist hardware enables periodic scrubbing of single-bit errors. Multi-bit error detections optionally can signal interrupts and/or faults.

Cyclic Redundancy Check (CRC)

The cyclic redundancy check (CRC) is a hardware block used to compute the CRC of the block of data. This is based on a CRC32 engine which computes the CRC value of 32-bit data words presented to it. For data words of < 32 b its in size, it is the responsibility of the core/external source to pack the data into 32-bit data units.

In particular, the CRC unit is used to validate the contents of flash memory and constant blocks of data (text or code) in SRAM. The main features of the CRC peripheral are:

- Memory scan mode
- Memory transfer mode
- Data verify mode
- Data fill mode
- 32-bit CRC polynomial (programmable polynomials)
- Bit/byte mirroring option
- Fault/error interrupt mechanisms

Cortex-M4 Memory Protection Unit (MPU)

The MPU divides the memory map into a number of regions and allows the system programmer to define the location, size, access permissions, and memory attributes of each region. It supports independent attribute settings for each region, overlapping regions, and export of memory attributes to the system.

For more information, refer to the ARM Infocenter web page.

System Protection Unit (SPU)

All system resources and L2 memory banks are controlled by either a processor core, memory-to-memory DMA, or the debug unit. A system protection unit (SPU) enables write accesses to specific resources that are locked to a given master.

Two SPU units are provided to manage peripheral groups and their associated APB bus. SPU0 manages the local peripherals of M0, and SPU1 manages the M4 system peripherals.

Three system memory protection units (SMPU) are provided for each memory space—M4 SRAM, M0 SRAM, and off-chip L2.

SPUs and SPMUs can be programmed to detect access timeouts and to return control to the initiating master. This protects the system against indefinite stall faults.

System protection is enabled in greater granularity for some modules through a global lock concept, available on the most system critical blocks. After a set of peripherals is initialized, each desired peripheral can be marked for protection by writing its Lock bit. Then, when the global lock is set in the SPU, the entire configuration is protected. Peripherals whose Lock bit was previously set are protected against any writes until the global SPU lock is once again unlocked.

Watchpoint Protection

The primary purpose of watchpoints and hardware breakpoints is to serve emulator needs. When enabled, they signal an emulator event whenever user-defined system resources are accessed or a core executes from user-defined addresses. Watchdog events can be configured such that they signal the events to the core or to the SEC.

Watchdog Timer (WDOG)

Each core is associated with a 32-bit timer, which may be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processors to a known state, via a general-purpose interrupt, or a fault, if the timer expires before being reset by software.

The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts down to zero from the programmed value, protecting the system from remaining in an unknown state where software that normally resets the timer stops running due to an external noise condition or software error. Optionally, the fault management unit (FMU) can directly initiate the processor reset upon the watchdog expiry event.

Signal Watchdogs

The eight general-purpose timers feature two modes to monitor off-chip signals. The watchdog period mode monitors whether external signals toggle with a period within an expected range. The watchdog width mode monitors whether the pulse widths of external signals are within an expected range. Both modes help to detect undesired toggling or lack of toggling of system level signals.

Oscillator Watchdog

The oscillator watchdog monitors the external clock oscillator and can detect the absence of clock as well as incorrect harmonic oscillation. The oscillator watchdog detection signal is routed to the fault management portion of the SEC and to the GPIO pin safe state mechanism.

Low Latency Sinc Filter Over Range Detection

The SINC filter units provide a low latency secondary filter with programmable positive and negative limit detectors for each input channel. These may be used to monitor an isolation ADC bitstream for over or under range conditions with a filter group delay as low as 0.7 µs on a 10 MHz bit stream. The secondary SINC filter events can be used to interrupt the core, to trigger other events directly in hardware using the TRU, or to signal the FMU of a system fault.

Up/Down Count Mismatch Detection

The GP counter monitors external signal pairs, such as request/grant strobes. If the edge count mismatch exceeds the expected range, the up/down counter flags this to the processor or to the SEC.

Fault Management Unit (FMU)

The fault management unit (FMU) is part of the SEC. Most system events can be defined as faults. If defined as such, the SEC forwards the event to its FMU which may automatically reset the entire device for reboot, or simply toggle the $\overline{\text{SYS\_FAULT}}$ output pin to signal off-chip hardware. Optionally, the FMU can delay the action taken via a keyed sequence to provide a final chance for the core to resolve the crisis and to prevent the fault action from being taken.

PROCESSOR PERIPHERALS

The ADSP-CM41xF processors contain a rich set of peripherals, which serve to connect the external system to the processor to provide real-time sensing (ADCs, GPIOs, CNTs), control (timers, LBA, MATH, MBOX), actuation (PWMs, GPIOs), and communication with external devices (CANs, SPIs, SPORT, UARTs, and TWI). These peripherals are connected to the core via several concurrent high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see Figure 1).

The infrastructure of the processor features high speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

Timers

The processors include several timers which are described in the following sections.

General-Purpose (GP) Timers

The ADSP-CM41xF processors provide two sets of eight general-purpose (GP) timers, one set primarily associated with each processor core. Each timer has an external pin that can be configured either as a PWM or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input on the TM0_ACLKx pins, an external TM0_CLK input pin, or to the internal SCLK0.

These timer units can be used in conjunction with the UARTs and the CAN controller to measure the width of the pulses in the data stream to provide a software autobaud detect function for the respective serial channels.

The GP timers can generate interrupts to the processor core, providing periodic events for synchronization to either the system clock or to external signals. Timer events can also trigger other peripherals via the TRU (for instance, to signal a fault). Each timer can also be started and/or stopped by any TRU master without core intervention.

Pulse Width Modulator Units (PWM)

The pulse width modulator (PWM) units provide duty cycle and phase control capabilities to a resolution of one system clock cycle (SCLK). The processors provide 24 PWM outputs, grouped into three PWM units which each feature four PWM output pairs.

The heightened precision PWM (HPPWM) modules provide increased performance to each PWM unit by increasing its resolution by several bits, resulting in enhanced precision levels. Additional features include:

- 16-bit center-based PWM generation unit
- Programmable PWM pulse width
- Single and double update modes
- Programmable dead time and switching frequency
- Twos complement implementation which permits smooth transition to full on and full off states
- Dedicated asynchronous PWM shutdown signal

Each PWM block integrates a flexible and programmable 3-phase PWM waveform generator that can be programmed to generate the required switching patterns to drive a 3-phase voltage source inverter for ac induction motor (ACIM) or permanent magnet synchronous motor (PMSM) control. In addition, the PWM block contains special functions that considerably simplify the generation of the required PWM switching patterns for control of the electronically commutated motor (ECM) or brushless dc motor (BDCM). Software can enable a special mode for switched reluctance motors (SRM).

The eight PWM output signals (per PWM unit) consist of four high side drive signals and four low side drive signals. The polarity of a generated PWM signal can be set with software, so that either active HI or active LO PWM patterns can be produced.

The PWM units can be immediately shut down by several PWM trip mechanisms. A synchronous software trip register allows simultaneous shutdown of any combination of PWM outputs. A synchronous TRU trigger mechanism allows any on-chip TRU master to cause shutdown of selected PWM outputs in a programmable sequential manner to support multilevel inverter topologies. Three asynchronous general-purpose $\overline{\text{PWM\_TRIP}}$ inputs (active low) can be routed to any combination of the three PWM blocks to immediately cause PWM shutdown to any

selected PWM output. Similarly, the three FOCP analog comparators can be connected to any combination of the PWM_TRIP inputs.

Finally, a set of internal asynchronous monitors can also cause PWM output shutdown using the GPIO pin safe state mechanism, including clock or power fault detections by the voltage monitoring unit, the oscillator watchdog, and the oscillator comparator units.

Debounce Unit

Selected GPIO signals and asynchronous inter-die signals from the AFE are connected to independent channels of a programmable debounce unit. This eliminates external hardware and supports filtering of unwanted high frequency glitches from critical signals. The signals connected to debounce channels include the three PWM_TRIP signals, the FOCP comparator detection signal, and the AFE_OK status signal.

Serial Port (SPORT)

The synchronous serial port provides an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. These devices include Analog Devices audio codecs, analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The serial port is made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. For full-duplex operation, two half SPORTs can work in conjunction with clock and frame sync signals shared internally through the SPMUX block. In some operation modes, SPORT supports gated clock.

Serial ports operate in the following six modes:

- Standard DSP serial mode
- Multichannel time division multiplexing (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left justified mode
- Right justified mode

General-Purpose Counters (CNT)

A 32-bit counter (CNT) is provided that can operate in general-purpose up/down count modes and can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumbwheels. Count direction is either controlled by a level-sensitive input pin or by two edge detectors.

A third counter input can provide flexible zero marker support and can input the push button signal of thumbwheel devices. All three CNT0 pins have a programmable debouncing circuit.

The GP counter can also support a programmable M/N frequency scaling of the CNT_CUD and CNT_CDG pins onto output pins in quadrature encoding mode.

Internal signals forwarded to a GP timer enable this timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmed count values are exceeded.

Serial Peripheral Interface (SPI) Ports

The processors have two industry-standard SPI-compatible ports (one associated with each processor) that allow the processors to communicate with multiple SPI-compatible devices.

In its simplest mode, the SPI interface uses three pins for transferring data: two data pins master output-slave input and master input-slave output (SPI_MOSI and SPI_MISO) and a clock pin, SPI_CLK. A SPI chip select input pin (SPI_SS) lets other SPI devices select the processor, and three SPI chip select output pins (SPI_SELn) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI provides a full-duplex, synchronous serial interface, which supports both master and slave modes and multimaster environments.

In a multimaster or multi-slave SPI system, the MOSI and MISO data output pins can be configured to behave as open drain outputs (using the ODM bit) to prevent contention and possible damage to pin drivers. An external pull-up resistor is required on both the MOSI and MISO pins when this option is selected.

When ODM is set, and the SPI is configured as a master, the MOSI pin is three-stated when the data driven out on MOSI is a logic high. The MOSI pin is not three-stated when the driven data is a logic low. Similarly, when ODM is set and the SPI is configured as a slave, the MISO pin is three-stated if the data driven out on MISO is a logic high.

The baud rate and clock phase/polarities of the SPI port are programmable. The port has integrated DMA channels for both transmit and receive data streams.

Universal Asynchronous Receiver/Transmitter (UART) Ports

The processors provide five full-duplex universal asynchronous receiver/transmitter (UART) ports, four associated with the M4 and one associated with the M0. These UARTs are fully compatible with PC standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits as well as no parity, even parity, or odd parity.

Optionally, an additional address bit can be transferred to interrupt only addressed nodes in multidrop bus (MDB) systems. A frame is terminated by configurable number of stop bits.

The UART ports support automatic hardware flow control through the clear to send (CTS) input and request to send (RTS) output with programmable assertion first in, first out (FIFO) levels.

To help support the Local Interconnect Network (LIN) protocols, a special command causes the transmitter to queue a break command of programmable bit length into the transmit buffer. Similarly, the number of stop bits can be extended by a programmable interframe space.

The capabilities of the UARTs are further extended with support for the infrared data association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

2-Wire Controller Interface (TWI)

The processors include a 2-wire interface (TWI) module that provides a simple exchange method of control data between multiple devices. The TWI module is compatible with the widely used I^2C bus standard. The TWI module offers the capabilities of simultaneous master and slave operation and support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (TWI_SCL) and data (TWI_SDA) and supports the protocol at speeds up to 400 kb/sec. The TWI interface pins are compatible with 5 V logic levels.

Additionally, the TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

Controller Area Network (CAN)

There are two controller area network (CAN) modules, one associated with the M4 and the other with the M0. A CAN controller implements the CAN 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well suited for control applications due to its capability to communicate reliably over a network. This is because the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The CAN controller offers the following features:

- 32 mailboxes (8 receive only, 8 transmit only, 16 configurable for receive or transmit)
- Dedicated acceptance masks for each mailbox
- Additional data filtering on first two bytes
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats
- Support for remote frames
- Active or passive network support
- Interrupts, including transmit and receive complete, error, and global

An additional crystal is not required to supply the CAN clock because it is derived from a system clock through a programmable divider.

Logic Block Array (LBA)

The logic block array (LBA) contains a number of logic blocks which can be programmed to perform logical or arithmetic functions. The logical or arithmetic function can be defined in either look-up-table (LUT) mode or product term array (PTA) mode. Each logic block generates one output as a function of up to 8 or 16 inputs, depending upon the chosen mode. The exact function is defined by programming eight 32-bit function registers which are mapped into the processor register space. A total of eight individual logic blocks form the logic block array. The LBA has the following features.

- Configurable per output in either LUT or PTA modes
- LUT mode allows any 8-input combinational logic function
- PTA mode allows eight product terms with up to 16 inputs
- Scalable with up to eight independent outputs
- System inputs can be connected to system-specific signals (for example, timer outputs and TRU slaves)
- System outputs can be connected to system-specific signals (for example, TRU masters and core interrupts)

MATH Unit

The math function unit is an accelerator that performs highly accurate single-precision floating-point computations of common transcendental functions via a single MMR interface. These functions include trigonometric, inverse trigonometric, hyperbolic, exponential, logarithm, square roots, and reciprocals.

The math unit supports both functions with single operands and two operand conversions between rectangular and polar coordinate functions. The functions are accurate to within 23.50 bit error of the IEEE-754 single-precision format. Most operations by this tightly coupled accelerator complete within a defined number of core clock cycles for each function, which is more competitive than those provided by software libraries for the Cortex-M4.

Floating-Point Saturation (FSAT) Unit

The floating-point saturation unit (FSAT) saturates a 32-bit floating-point number within a programmable maximum and minimum value. The unit returns the minimum value if the number is below minimum; the function returns the maximum value if the number is above the maximum. Otherwise, the function returns the input number. The FSAT acts as a co-processor to the ARM core to implement an accelerated saturate function in hardware.

Mailbox (MBOX)

The mailbox (MBOX) block is a shared system resource used to establish communication between Cortex-M4 and Cortex-M0 processor domains. The MBOX block has two access ports. Each access port is connected to a master block in the system. The size of the MBOX memory is 4 KB. To assist implementation of interprocessor semaphores, the MBOX memory supports exclusive memory operations natively from the M4 port, and emulates exclusive operations from the M0. Bit-banding operations by the M4 are also supported to the MBOX memory.The MBOX contains decode logic to alternate between the two processors. Access ports are in the same clock domain.

In ADSP-CM41xF processors, the intended use of the MBOX is as follows:

- PORT1 is connected to Cortex-M4
- PORT0 is connected to Cortex-M0

There are two register blocks. The register block for PORT1 contains:

- Control registers for PORT1, auto-refresh logic, and ECC test logic
- Status registers for PORT1 and auto-refresh logic

The register block for PORT0 contains:

- Control fields for PORT0
- Status registers for PORT0

Each port can access only its own register block.

CLOCK AND POWER MANAGEMENT

The processors provide three operating modes, each with a different performance/power profile. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 3 for a summary of the power settings for each mode.

Table 3. Power Settings

Mode	CGU PLL	CGU PLL Bypassed	f_{CCLK}	f_{SCLK}	Core Power
Full On	Enabled	No	Enabled	Enabled	On
Active	Enabled	Yes	Enabled	Enabled	On
	Disabled	Yes	Enabled	Enabled	On
Deep Sleep[1]	Disabled	N/A	Disabled	Disabled	On

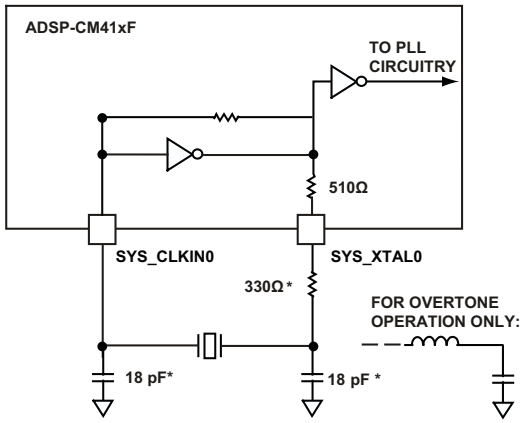
[1] N/A means not applicable.

Crystal Oscillators (SYS_XTAL0/1)

The processors can be clocked by an external crystal (see Figure 16), a sine wave input, or a buffered, shaped clock derived from an external clock oscillator. If using an external clock, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation.This signal is connected to the SYS_CLKINx pin of the processor. When using an external clock, the SYS_XTALx pin must be left unconnected. Alternatively, because the processor includes an on-chip oscillator circuit, an external crystal can be used.

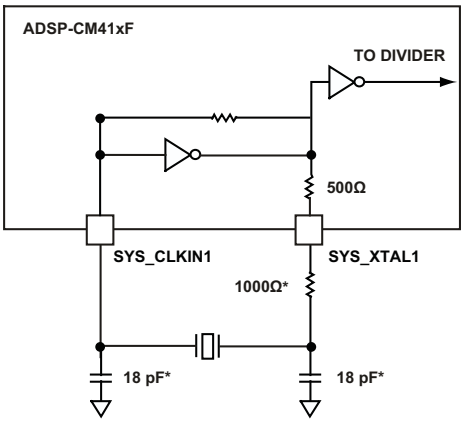
For functional safety purposes, an auxiliary clock input (Figure 17) can be connected to SYS_CLKIN1 and SYS_XTAL1. Its frequency can be used to monitor the main SYS_CLKIN0 frequency by the OCU unit. If not used, SYS_CLKIN1 must be grounded and SYS_XTAL1 must be left unconnected.

For fundamental frequency operation, use the circuit shown in Figure 16 for each connected crystal. A parallel resonant, fundamental frequency, microprocessor grade crystal is connected across the SYS_CLKINx pin and the SYS_XTALx pin. The on-chip resistance between SYS_CLKINx pin and the SYS_XTALx pin is in the 500 kΩ range. Further parallel resistors are typically not recommended.



NOTE: VALUES MARKED WITH * MUST BE CUSTOMIZED, DEPENDING ON THE CRYSTAL AND LAYOUT. ANALYZE CAREFULLY. FOR FREQUENCIES ABOVE 33 MHz, THE SUGGESTED CAPACITOR VALUE OF 18pF SHOULD BE TREATED AS A MAXIMUM, AND THE SUGGESTED RESISTOR VALUE SHOULD BE REDUCED TO 0 Ω.

Figure 16. External Crystal Connection for CLKIN0



NOTE: VALUES MARKED WITH * MUST BE CUSTOMIZED, DEPENDING ON THE CRYSTAL AND LAYOUT. FOR FREQUENCIES ABOVE 22 MHz, THE SUGGESTED RESISTOR VALUE SHOULD BE REDUCED (~450 Ω).

Figure 17. External Crystal Connection for CLKIN1

The two capacitors and the series resistor shown, in Figure 16, fine tune phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 16 are typical values only. The capacitor values are dependent upon the load capacitance recommendations of the crystal manufacturer and the physical layout of the printed circuit board (PCB). The resistor value depends on the drive level specified by the crystal manufacturer. The user must verify the customized values based on careful investigations on multiple devices over the required temperature range.

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit,

shown in Figure 16. A design procedure for the third overtone operation is discussed in detail in "Using Third Overtone Crystals with the ADSP-218x DSP" (EE-168).

Oscillator Watchdog

A programmable oscillator watchdog unit is provided to allow verification of proper startup and harmonic mode of the external crystal. This allows the user to specify the expected frequency of oscillation, and to enable detection of non oscillation and improper oscillation faults. These events can be routed to the SYS_FAULT output pin and/or to cause a reset of the part.

Clock Generation Unit (CGU)

The clock generation unit (CGU) generates all on-chip clocks and synchronization signals. Multiplication factors are programmed to the PLLs to define the PLLCLK frequency.

Programmable values divide the PLLCLK frequency to generate the core clock (CCLK), the system clocks (SCLK) and the output clock (OCLK). This is illustrated in Figure 19.

Writing to the CGU control registers does not affect the behavior of the PLL immediately. Registers are first programmed with a new value and the PLL logic executes the changes so it transitions smoothly from the current conditions to the new conditions.

SYS_CLKIN oscillations start when power is applied to the VDD_EXT pins. The rising edge of SYS_HWRST can be applied as soon as all voltage supplies are within specifications (see Operating Conditions) and SYS_CLKIN oscillations are stable.

Clock Out/External Clock

A SYS_CLKOUT output pin has programmable options to output divided-down versions of the on-chip clocks. The SYS_CLKOUT pin can be programmed to drive a buffered version of the SYS_CLKIN input, or any of a set of available clocks in the ADSP-CM41x system. By default, the SYS_CLKOUT pin is driven low. Clock generation faults (for example, PLL unlock) can trigger a reset by hardware.

SYS_CLKOUT can be used to output one of several clocks used on the processor. The clocks shown in Table 4 can be outputs from SYS_CLKOUT.

Table 4. SYS_CLKOUT Source and Divider Options

Clock Source	Divider
GND	Logic low
CLKBUF0	Buffered SYS_CLKIN0
CLKBUF1	Buffered SYS_CLKIN1
CCLK0	M4 controller clock, divided by 4
SCLK0	M0 supervisor clock, divided by 2
SYSCLK	System clock, divided by 2
DCLK	CGU DCLK output used for generating the AFE FOCP clock, prior to the FOCP_DIV divider

Table 4. SYS_CLKOUT Source and Divider Options

Clock Source	Divider
FOCP_CLK	The AFE FOCP clock, after the FOCP_DIV divider
OUTCLK	Programmable
M0RST	Buffered M0 supervisor reset
SYSRST	Buffered system reset from RCU

Power Management

As shown in Table 5 and Figure 5, the processor supports three different power domains, VDD_INT, VDD_EXT and VDD_ANA. By isolating the internal logic of the processor into its own power domain (separate from other I/O), the processor can take advantage of dynamic power management without affecting the other I/O devices. All domains must be powered according to the appropriate specifications (see the Specifications section for processor operating conditions). If the feature or the peripheral is not used, refer to Table 21.

The dynamic power management feature of the processor allows the core clock frequency (f_{CCLK}) of the processor to be dynamically controlled.

Table 5. Power Domains

Power Domain	V_{DD} Range
All Internal Logic	V_{DD_INT}
Digital I/O	V_{DD_EXT}
Analog	V_{DD_ANA}

The power dissipated by a processor is largely a function of the clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation. For more information on power pins, see Operating Conditions.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

For more information about PLL controls, see the "Dynamic Power Management" chapter in the ADSP-CM41x Mixed-Signal Control Processor with ARM Cortex-M4/ARM Cortex-M0 and 16-bit ADCs Hardware Reference.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core and to all synchronous peripherals. Asynchronous peripherals may still be running but cannot access internal resources or external memory. GPIO pin and JTAG interface events can be configured to wake the device from the deep sleep mode.

Voltage Regulation for VDD_INT

The internal voltage VDD_INT to the ADSP-CM41xF processors is generated either by using an on-chip voltage regulator or by an external voltage regulator.

The VDD_INT supply is generated using the external I/O supply VDD_EXT. Figure 18 shows the external components required to complete the power management system for proper operation. For more details regarding component selection, refer to "ADSP-CM41x Power Supply Transistor Selection Guidelines" (EE-390).

The internal voltage regulator can be bypassed and VDD_INT can be supplied using an external regulator. When an external regulator is used, VREG_BASE must be tied to ground for minimal current consumption.

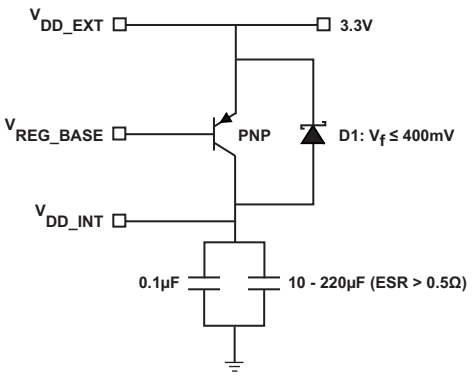


Figure 18. Internal Voltage Regulator Circuit

Reset Control Unit (RCU)

Reset is the initial state of the whole processor, or the core, and is the result of a hardware or software triggered event. In this state, all control registers are set to default values and functional units are idle. Exiting a full system reset starts with the core ready to boot.

The reset control unit (RCU) controls how all the functional units enter and exit reset. Differences in functional requirements and clocking constraints define how reset signals are generated. Programs must guarantee that none of the reset functions put the system into an undefined state or causes resources to stall. This is particularly important when the core resets (programs must ensure that there is no pending system activity involving the core when it is reset).

From a system perspective, reset is defined by both the reset target and the reset source.

The reset target is defined as the following:

- System reset—all functional units except the RCU are set to default states.
- Hardware reset—all functional units are set to default states without exception. History is lost.
- Core only reset— affects the core only. When in reset state, the core is not accessed by any bus master.

The reset source is defined as the following:

- System reset—can be triggered by software (writing to the RCU_CTL register) or by another functional unit such as the dynamic power management (DPM) unit or any of the SEC, TRU, or emulator inputs.
- Hardware reset—the $\overline{\text{SYS\_HWRST}}$ input signal asserts active (pulled down).
- Core only reset—affects only the core. The core is not accessed by any bus master when in reset state.
- Trigger request (peripheral).

SYSTEM DEBUG

The processors include various features that allow easy system debug. These are described in the following sections.

JTAG Debug and Serial Wire Debug Port (SWJ-DP)

SWJ-DP is a combined JTAG-DP and SW-DP that enables either a serial wire debug (SWD) or JTAG probe to be connected to a target. SWD signals share the same pins as JTAG. There is an auto detect mechanism that switches between JTAG-DP and SW-DP depending on which special data sequence is used the emulator pod transmits to the JTAG pins.The SWJ-DP behaves as a JTAG target if normal JTAG sequences are sent to it and as a single wire target if the SW_DP sequence is transmitted.

Embedded Trace Macrocell (ETM) and Instrumentation Trace Macrocell (ITM)

The ADSP-CM41xF processors support both embedded trace macrocell (ETM) and instrumentation trace macrocell (ITM). These both offer an optional debug component that enables logging of real-time instruction and data flow within the CPU core. This data is stored and read through special debugger pods that have the trace feature capability. The ITM is a single-data pin feature and the ETM is a 4-data pin feature.

System Watchpoint Unit (SWU)

The system watchpoint unit (SWU) is a single module that connects to a single system bus and provides transaction monitoring. One SWU is attached to the bus going to each system slave. The SWU provides ports for all system bus address channel signals. Each SWU contains four match groups of registers with associated hardware. These four SWU match groups operate independently, but share common event (for example, interrupt and trigger) outputs.

Flash Patch and Breakpoint Unit (FPB)

The flash patch and breakpoint unit (FPB) implements hardware breakpoints, and implements patching of code and data by redirecting specified code or literal addresses to locations in read/write system memory. The ADSP-CM41xF processors implement a full FPB with eight comparators (six code/breakpoint and two literal data.)

DEVELOPMENT TOOLS

The ADSP-CM41xF processor is supported with a set of highly sophisticated and easy to use development tools for embedded applications. For more information, see the Analog Devices website.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-CM41xF architecture and functionality. It also describes the ARM Cortex-M4 and ARM Cortex-M0 core and memory architecture used on the ADSP-CM41xF processors. The data sheet does not provide detailed programming information for the ARM processor. For more information about programming the ARM processor, visit the ARM Infocenter web page.

RELATED SIGNAL CHAINS

A signal chain is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (www.analog.com\circuits) provides the following:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

ADSP-CM41xF DETAILED SIGNAL DESCRIPTIONS

Table 6 provides a detailed description of each pin.

Table 6. ADSP-CM41xF Detailed Signal Descriptions

Signal Name	Direction	Description
ADC_VIN_A[n]	InOut	**Channel n Single-Ended Analog Input for ADC.**
ADC_VIN_B[n]	InOut	**Channel n Single-Ended Analog Input for ADC.**
ADC_VIN_C[n]	InOut	**Channel n Single-Ended Analog Input for ADC.**
ADC_VIN_D[n]	InOut	**Channel n Single-Ended Analog Input for ADC.**
BYP_A2	InOut	**On-chip Analog Power Regulation Bypass Filter Node for ADC.**
BYP_A[n]	InOut	**On-chip Analog Power Regulation Bypass Filter Node for ADC.**
BYP_D0	InOut	**On-chip Analog Power Regulation Bypass Filter Node for DAC.**
CAN_RX	Input	**Receive.** Typically an external CAN transceiver RX output.
CAN_TX	Output	**Transmit.** Typically an external CAN transceiver TX input.
CNT_DG	Input	**Count Down and Gate.** Depending on the mode of operation this input acts either as a count down signal or a gate signal. Count down—this input causes the GP counter to decrement. Gate—stops the GP counter from incrementing or decrementing.
CNT_OUTA	InOut	**Output Divider A.**
CNT_OUTB	InOut	**Output Divider B.**
CNT_UD	Input	**Count Up and Direction.** Depending on the mode of operation this input acts either as a count up signal or a direction signal. Count up—this input causes the GP counter to increment. Direction—selects whether the GP counter is incrementing or decrementing.
CNT_ZM	Input	**Count Zero Marker.** Input that connects to the zero marker output of a rotary device or detects the pressing of a pushbutton.
COMP_OUT_A	InOut	**Fast Over-Current Protection Comparator A Output.**
COMP_OUT_B	InOut	**Fast Over-Current Protection Comparator B Output.**
COMP_OUT_C	InOut	**Fast Over-Current Protection Comparator C Output**.
CPTMR_IN[n]	Input	**Input.**
DAC0_VOUT	InOut	**Analog Voltage Output 0.**
GND_ANA4_COMP	InOut	**Analog Ground for Comparators.**
GND_ANA5_DAC	InOut	**Analog Ground for DAC.**
GND_ANA[n]	InOut	**Analog Ground Return for VDD_ANA[n].**
GND_REFCAP0	InOut	**Ground Return for REF_INOUT0.**
GND_REFCAP1	InOut	**VREF Bypass Capacitor.**
GND_VREF2	InOut	**Analog VREF Ground.**
JTG_TCK/SWCLK	Input	**JTAG Clock/Serial Wire Clock.**
JTG_TDI	Input	**JTAG Serial Data In.**
JTG_TDO/SWO	Output	**JTAG Serial Data Out/Serial Wire Trace Output.**
JTG_TMS/SWDIO	InOut	**JTAG Mode Select/Serial Wire Debug Data I/O.**
$\overline{\text{JTG\_TRST}}$	Input	**JTAG Reset.** JTAG test access port reset.
LBA_PIN[n]	InOut	**LBA Data Input or the Logic Output.**
PWM_AH	Output	**Channel A High Side.** High side drive signal.
PWM_AL	Output	**Channel A Low Side.** Low side drive signal.
PWM_BH	Output	**Channel B High Side.** High side drive signal.
PWM_BL	Output	**Channel B Low Side.** Low side drive signal.
PWM_CH	Output	**Channel C High Side.** High side drive signal.
PWM_CL	Output	**Channel C Low Side.** Low side drive signal.

Table 6. ADSP-CM41xF Detailed Signal Descriptions (Continued)

Signal Name	Direction	Description
PWM_DH	Output	**Channel D High Side.** High side drive signal.
PWM_DL	Output	**Channel D Low Side.** Low side drive signal.
PWM_SYNC	InOut	**PWMTMR Grouped.** This input is for an externally generated sync signal. If the sync signal is internally generated, no connection is necessary.
$\overline{\text{PWM\_TRIPA}}$	Input	**Muxed PWM Trip A Interrupt**
$\overline{\text{PWM\_TRIPB}}$	Input	**Muxed PWM Trip B Interrupt**
$\overline{\text{PWM\_TRIPC}}$	Input	**Muxed PWM Trip C Interrupt**
P_[nn]	InOut	**Position n.** General purpose input/output. See the GP Ports chapter of the ADSP-CM41x Mixed-Signal Control Processor with ARM Cortex-M4/ARM Cortex-M0 and 16-bit ADCs Hardware Reference for more details.
REFCAP0	InOut	**Output of BandGap Generator Filter Node.**
REFCAP1	InOut	**Output of BandGap Generator Filter Node.**
REF_BUFOUT[n]	InOut	**Voltage Reference Buffered Output**.
SINC_CLK0	InOut	**Clock 0.**
SINC_D0	InOut	**Data 0.**
SINC_D1	InOut	**Data 1.**
SINC_D2	InOut	**Data 2.**
SINC_D3	InOut	**Data 3.**
$\overline{\text{SMC\_ABE[n]}}$	Output	**Byte Enable n.** Indicates whether the lower or upper byte of a memory is being accessed. When an asynchronous write is made to the upper byte of a 16-bit memory, $\overline{\text{SMC\_ABE1}}$ = 0 and $\overline{\text{SMC\_ABE0}}$ = 1. When an asynchronous write is made to the lower byte of a 16-bit memory, $\overline{\text{SMC\_ABE1}}$ = 1 and $\overline{\text{SMC\_ABE0}}$ = 0.
$\overline{\text{SMC\_AMS[n]}}$	Output	**Memory Select n.** Typically connects to the chip select of a memory device.
$\overline{\text{SMC\_AOE}}$	Output	**Output Enable.** Asserts at the beginning of the setup period of a read access.
SMC_ARDY	Input	**Asynchronous Ready.** Flow control signal used by memory devices to indicate to the SMC when further transactions may proceed.
$\overline{\text{SMC\_ARE}}$	Output	**Read Enable.** Asserts at the beginning of a read access.
$\overline{\text{SMC\_AWE}}$	Output	**Write Enable.** Asserts for the duration of a write access period.
SMC_A[nn]	Output	**Address n.** Address bus.
SMC_D[nn]	InOut	**Data n.** Bidirectional data bus.
SPI_CLK	InOut	**Clock.** Input in slave mode, output in master mode.
SPI_D2	InOut	**Data 2.** Transfers serial data in quad mode. Open-drain when ODM mode is enabled.
SPI_D3	InOut	**Data 3.** Transfers serial data in quad mode. Open-drain when ODM mode is enabled.
SPI_MISO	InOut	**Master In, Slave Out.** Transfers serial data. Operates in the same direction as SPI_MOSI in dual and quad modes. Open-drain when ODM mode is enabled.
SPI_MOSI	InOut	**Master Out, Slave In.** Transfers serial data. Operates in the same direction as SPI_MISO in dual and quad modes. Open-drain when ODM mode is enabled.
SPI_RDY	InOut	**Ready.** Optional flow signal. Output in slave mode, input in master mode.
$\overline{\text{SPI\_SEL[n]}}$	Output	**Slave Select Output n.** Used in master mode to enable the desired slave.
$\overline{\text{SPI\_SS}}$	Input	**Slave Select Input.** Slave mode—acts as the slave select input. Master mode—optionally serves as an error detection input for the SPI when there are multiple masters.
SPT_ACLK	InOut	**Channel A Clock.** Data and frame sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_AD0	InOut	**Channel A Data 0.** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_AD1	InOut	**Channel A Data 1.** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.

Table 6. ADSP-CM41xF Detailed Signal Descriptions (Continued)

Signal Name	Direction	Description
SPT_AFS	InOut	**Channel A Frame Sync.** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_ATDV	Output	**Channel A Transmit Data Valid.** This signal is optional and only active when SPORT is configured in multichannel transmit mode. It is asserted during enabled slots.
SPT_BCLK	InOut	**Channel B Clock.** Data and frame sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_BD0	InOut	**Channel B Data 0.** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_BD1	InOut	**Channel B Data 1.** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_BFS	InOut	**Channel B Frame Sync.** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_BTDV	Output	**Channel B Transmit Data Valid.** This signal is optional and only active when SPORT is configured in multichannel transmit mode. It is asserted during enabled slots.
SYS_BMODE0	Input	**Boot Mode Control n.** Selects the boot mode of the processor.
$\overline{\text{SYS\_CLKIN0}}$	Input	**Clock/Crystal Input.**
$\overline{\text{SYS\_CLKIN1}}$	Input	**Clock/Crystal Input.**
SYS_CLKOUT	Output	**Processor Clock Output.** Outputs internal clocks. Clocks may be divided down. See the CGU chapter of the ADSP-CM41x Mixed-Signal Control Processor with ARM Cortex-M4/ARM Cortex-M0 and 16-bit ADCs Hardware Reference for more details.
SYS_DSWAKE[n]	InOut	**Deep Sleep Wakeup n.**
$\overline{\text{SYS\_FAULT}}$	InOut	**Active-High Fault Output.** Indicates indicates internal faults or senses external faults depending on the operating mode.
$\overline{\text{SYS\_HWRST}}$	Input	**Processor Hardware Reset Control.** Resets the device when asserted.
$\overline{\text{SYS\_NMI}}$	Input	**Non-maskable Interrupt.** See the ADSP-CM41x Mixed-Signal Control Processor with ARM Cortex-M4/ARM Cortex-M0 and 16-bit ADCs Hardware Reference for more details.
$\overline{\text{SYS\_RESOUT}}$	Output	**Reset Output.** Indicates the device is in the reset state.
$\overline{\text{SYS\_XTAL0}}$	Output	**Crystal Output.**
$\overline{\text{SYS\_XTAL1}}$	Output	**Crystal Output.**
TM_ACI[n]	Input	**Alternate Capture Input n.** Provides an additional input for WIDCAP, WATCHDOG, and PININT modes.
TM_ACLK[n]	Input	**Alternate Clock n.** Provides an additional time base for use by an individual timer.
TM_CLK	Input	**Clock.** Provides an additional global time base for all GP timers.
TM_TMR[n]	InOut	**Timer n.** The main input/output signal for each timer.
TRACE_CLK	Output	**Trace Clock.** Clock output.
TRACE_D[nn]	Output	**Trace Data n.** Unidirectional data bus.
TWI_SCL	InOut	**Serial Clock.** Clock output when master, clock input when slave.
TWI_SDA	InOut	**Serial Data.** Receives or transmits data.
$\overline{\text{UART\_CTS}}$	Input	**Clear to Send.** Flow control signal.
$\overline{\text{UART\_RTS}}$	Output	**Request to Send.** Flow control signal.
UART_RX	Input	**Receive.** Receives input. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
UART_TX	Output	**Transmit**. Transmits output. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
VDD_ANA[n]	InOut	**Analog Power Supply Voltage.**
VDD_COMP	InOut	**Power Supply for Over Current Comparator.**
VDD_EXT	InOut	**External Voltage Domain.**

176-LEAD LQFP_EP SIGNAL DESCRIPTIONS

The processor pin definitions are shown in Table 7 for the 176-lead LQFP_EP package. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The description column provides a descriptive name for each signal.
- The port column shows whether or not a signal is multiplexed with other signals on a general-purpose I/O port pin.
- The pin name column identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).

Table 7. ADSP-CM412F/CM413F/CM416F/CM417F 176-Lead LQFP_EP Signal Descriptions

Signal Name	Description	Port	Pin Name
ADC_VIN_A0	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_A0
ADC_VIN_A1	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_A1
ADC_VIN_A2	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_A2
ADC_VIN_A3	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_A3
ADC_VIN_A4	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_A4
ADC_VIN_A5	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_A5
ADC_VIN_A6	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_A6
ADC_VIN_A7	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_A7
ADC_VIN_B0	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_B0
ADC_VIN_B1	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_B1
ADC_VIN_B2	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_B2
ADC_VIN_B3	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_B3
ADC_VIN_B4	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_B4
ADC_VIN_B5	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_B5
ADC_VIN_B6	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_B6
ADC_VIN_B7	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_B7
ADC_VIN_C0	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_C0
ADC_VIN_C1	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_C1
ADC_VIN_C2	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_C2
ADC_VIN_C3	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_C3
ADC_VIN_C4	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_C4
ADC_VIN_C5	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_C5
ADC_VIN_C6	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_C6
ADC_VIN_C7	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_C7
ADC_VIN_D0	Channel n Single-Ended Analog Input for ADC0	Not Muxed	ADC_VIN_D0
ADC_VIN_D1	Channel n Single-Ended Analog Input for ADC0	Not Muxed	ADC_VIN_D1
ADC_VIN_D2	Channel n Single-Ended Analog Input for ADC0	Not Muxed	ADC_VIN_D2
ADC_VIN_D3	Channel n Single-Ended Analog Input for ADC0	Not Muxed	ADC_VIN_D3
ADC_VIN_D4	Channel n Single-Ended Analog Input for ADC0	Not Muxed	ADC_VIN_D4
ADC_VIN_D5	Channel n Single-Ended Analog Input for ADC0	Not Muxed	ADC_VIN_D5
ADC_VIN_D6	Channel n Single-Ended Analog Input for ADC0	Not Muxed	ADC_VIN_D6
BYP_A0	On-chip Analog Power Regulation Bypass Filter Node for ADC	Not Muxed	BYP_A0
BYP_A1	On-chip Analog Power Regulation Bypass Filter Node for ADC	Not Muxed	BYP_A1
BYP_D0	On-chip Analog Power Regulation Bypass Filter Node for DAC	Not Muxed	BYP_D0
CAN0_RX	CAN0 Receive	A	PA_06
CAN0_TX	CAN0 Transmit	A	PA_07

Table 7. ADSP-CM412F/CM413F/CM416F/CM417F 176-Lead LQFP_EP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
CAN1_RX	CAN1 Receive	E	PE_12
CAN1_TX	CAN1 Transmit	E	PE_13
CNT0_DG	CNT0 Count Down and Gate	C	PC_13
CNT0_OUTA	CNT0 Output Divider A	B	PB_08
CNT0_OUTB	CNT0 Output Divider B	B	PB_10
CNT0_UD	CNT0 Count Up and Direction	B	PB_09
CNT0_ZM	CNT0 Count Zero Marker	C	PC_14
COMP_OUT_A	Fast over-current protection comparator A output	Not Muxed	COMP_OUT_A
COMP_OUT_B	Fast over-current protection comparator B output	Not Muxed	COMP_OUT_B
COMP_OUT_C	Fast over-current protection comparator C output	Not Muxed	COMP_OUT_C
CPTMR0_IN0	CPTMR0 Input	E	PE_02
CPTMR0_IN1	CPTMR0 Input	E	PE_04
CPTMR0_IN2	CPTMR0 Input	F	PF_06
DAC0_VOUT	Analog Voltage Output 0	Not Muxed	DAC0_VOUT
GND_ANA0	Analog Ground return for VDD_ANA0	Not Muxed	GND_ANA0
GND_ANA1	Analog Ground return for VDD_ANA1	Not Muxed	GND_ANA1
GND_ANA2	Analog Ground return for VDD_ANA2	Not Muxed	GND_ANA2
GND_ANA3	Analog Ground return for VDD_ANA3	Not Muxed	GND_ANA3
GND_ANA4_COMP	AFE_GND_COMP_ANA4	Not Muxed	GND_ANA4_COMP
GND_ANA5_DAC	AFE_GND_DAC_ANA5	Not Muxed	GND_ANA5_DAC
GND_REFCAP0	Ground return for REF_INOUT0	Not Muxed	GND_REFCAP0
GND_REFCAP1	GND_REFCAP1	Not Muxed	GND_REFCAP1
GND_VREF0	Ground return for REF_BUFOUT[0]	Not Muxed	GND_VREF0
GND_VREF1	Ground return for REF_BUFOUT[1]	Not Muxed	GND_VREF1
JTG_TCK/SWCLK	JTAG Clock/Serial Wire Clock	Not Muxed	JTG_TCK/SWCLK
JTG_TDI	JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO/SWO	JTAG Serial Data Out/Serial Wire Trace Output	Not Muxed	JTG_TDO/SWO
JTG_TMS/SWDIO	JTAG Mode Select/Serial Wire Debut Data I/O	Not Muxed	JTG_TMS/SWDIO
$\overline{\text{JTG\_TRST}}$	JTAG Reset	Not Muxed	$\overline{\text{JTG\_TRST}}$
LBA0_PIN0	LBA0 LBA data input or the logic output	F	PF_03
LBA0_PIN1	LBA0 LBA data input or the logic output	F	PF_04
LBA0_PIN2	LBA0 LBA data input or the logic output	F	PF_05
LBA0_PIN3	LBA0 LBA data input or the logic output	F	PF_06
LBA0_PIN4	LBA0 LBA data input or the logic output	F	PF_07
LBA0_PIN5	LBA0 LBA data input or the logic output	F	PF_08
LBA0_PIN6	LBA0 LBA data input or the logic output	C	PC_02
LBA0_PIN7	LBA0 LBA data input or the logic output	C	PC_04
PWM0_AH	PWM0 Channel A High Side	B	PB_00
PWM0_AL	PWM0 Channel A Low Side	B	PB_01
PWM0_BH	PWM0 Channel B High Side	B	PB_02
PWM0_BL	PWM0 Channel B Low Side	B	PB_03
PWM0_CH	PWM0 Channel C High Side	B	PB_04
PWM0_CL	PWM0 Channel C Low Side	B	PB_05
PWM0_DH	PWM0 Channel D High Side	B	PB_06
PWM0_DL	PWM0 Channel D Low Side	B	PB_07
PWM0_SYNC	PWM0 PWMTMR Grouped	D	PD_00

Table 7. ADSP-CM412F/CM413F/CM416F/CM417F 176-Lead LQFP_EP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PWM1_AH	PWM1 Channel A High Side	B	PB_08
PWM1_AL	PWM1 Channel A Low Side	B	PB_09
PWM1_BH	PWM1 Channel B High Side	B	PB_10
PWM1_BL	PWM1 Channel B Low Side	B	PB_11
PWM1_CH	PWM1 Channel C High Side	B	PB_12
PWM1_CL	PWM1 Channel C Low Side	B	PB_13
PWM1_DH	PWM1 Channel D High Side	B	PB_14
PWM1_DL	PWM1 Channel D Low Side	B	PB_15
PWM1_SYNC	PWM1 PWMTMR Grouped	E	PE_09
PWM2_AH	PWM2 Channel A High Side	E	PE_00
PWM2_AL	PWM2 Channel A Low Side	E	PE_01
PWM2_BH	PWM2 Channel B High Side	E	PE_02
PWM2_BL	PWM2 Channel B Low Side	E	PE_03
PWM2_CH	PWM2 Channel C High Side	E	PE_04
PWM2_CL	PWM2 Channel C Low Side	E	PE_05
PWM2_DH	PWM2 Channel D High Side	E	PE_06
PWM2_DL	PWM2 Channel D Low Side	E	PE_07
PWM2_SYNC	PWM2 PWMTMR Grouped	E	PE_08
$\overline{\text{PWM\_TRIPA}}$	Muxed PWM Trip A signal	D	PD_01
$\overline{\text{PWM\_TRIPB}}$	Muxed PWM Trip B signal	E	PE_10
$\overline{\text{PWM\_TRIPC}}$	Muxed PWM Trip C signal	E	PE_11
REFCAP0	Output of BandGap Generator Filter Node	Not Muxed	REFCAP0
REFCAP1	Output of BandGap Generator Filter Node	Not Muxed	REFCAP1
REF_BUFOUT0	Voltage reference ADC0 and DAC0	Not Muxed	VREF0
REF_BUFOUT1	Voltage reference ADC1 and Over Current Comparator DACs	Not Muxed	VREF1
SINC0_CLK0	SINC0 Clock 0	C	PC_15
SINC0_D0	SINC0 Data 0	C	PC_05
SINC0_D1	SINC0 Data 1	C	PC_06
SINC0_D2	SINC0 Data 2	F	PF_00
SINC0_D3	SINC0 Data 3	F	PF_01
SMC0_A01	SMC0 Address 1	B	PB_13
SMC0_A02	SMC0 Address 2	B	PB_15
SMC0_A03	SMC0 Address 3	D	PD_00
SMC0_A04	SMC0 Address 4	D	PD_01
SMC0_A05	SMC0 Address 5	E	PE_14
SMC0_A06	SMC0 Address 6	F	PF_00
SMC0_A07	SMC0 Address 7	F	PF_01
SMC0_A08	SMC0 Address 8	F	PF_02
SMC0_A09	SMC0 Address 9	F	PF_03
SMC0_A10	SMC0 Address 10	E	PE_15
SMC0_A11	SMC0 Address 11	E	PE_06
SMC0_A12	SMC0 Address 12	E	PE_07
SMC0_A13	SMC0 Address 13	F	PF_04
SMC0_A14	SMC0 Address 14	E	PE_05
SMC0_A15	SMC0 Address 15	E	PE_03
SMC0_A16	SMC0 Address 16	E	PE_11

Table 7. ADSP-CM412F/CM413F/CM416F/CM417F 176-Lead LQFP_EP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_ABE0	SMC0 Byte Enable 0	E	PE_13
SMC0_ABE1	SMC0 Byte Enable 1	E	PE_12
SMC0_AMS0	SMC0 Memory Select0	B	PB_04
SMC0_AMS1	SMC0 Memory Select 1	E	PE_01
SMC0_AMS2	SMC0 Memory Select 2	E	PE_02
SMC0_AMS3	SMC0 Memory Select 3	E	PE_08
SMC0_AOE	SMC0 Output Enable	B	PB_02
SMC0_ARDY	SMC0 Asynchronous Ready	B	PB_00
SMC0_ARE	SMC0 Read Enable	B	PB_03
SMC0_AWE	SMC0 Write Enable	B	PB_01
SMC0_D00	SMC0 Data 0	B	PB_05
SMC0_D01	SMC0 Data 1	B	PB_06
SMC0_D02	SMC0 Data 2	B	PB_07
SMC0_D03	SMC0 Data 3	B	PB_08
SMC0_D04	SMC0 Data 4	B	PB_09
SMC0_D05	SMC0 Data 5	B	PB_10
SMC0_D06	SMC0 Data 6	B	PB_11
SMC0_D07	SMC0 Data 7	B	PB_12
SMC0_D08	SMC0 Data 8	C	PC_09
SMC0_D09	SMC0 Data 9	C	PC_10
SMC0_D10	SMC0 Data 10	C	PC_11
SMC0_D11	SMC0 Data 11	C	PC_12
SMC0_D12	SMC0 Data 12	C	PC_13
SMC0_D13	SMC0 Data 13	C	PC_14
SMC0_D14	SMC0 Data 14	C	PC_05
SMC0_D15	SMC0 Data 15	C	PC_06
SPI0_CLK	SPI0 Clock	A	PA_08
SPI0_D2	SPI0 Data 2	A	PA_02
SPI0_D3	SPI0 Data 3	A	PA_03
SPI0_MISO	SPI0 Master In, Slave Out	A	PA_10
SPI0_MOSI	SPI0 Master Out, Slave In	A	PA_09
SPI0_RDY	SPI0 Ready	A	PA_01
SPI0_SEL1	SPI0 Slave Select Output 1	A	PA_11
SPI0_SEL2	SPI0 Slave Select Output 2	A	PA_00
SPI0_SEL3	SPI0 Slave Select Output 3	A	PA_01
SPI0_SEL4	SPI0 Slave Select Output 4	A	PA_06
SPI0_SEL5	SPI0 Slave Select Output 5	A	PA_07
SPI0_SEL6	SPI0 Slave Select Output 6	A	PA_02
SPI0_SEL7	SPI0 Slave Select Output 7	A	PA_03
SPI0_SS	SPI0 Slave Select Input	A	PA_00
SPI1_CLK	SPI1 Clock	C	PC_09
SPI1_D2	SPI1 Data 2	F	PF_06
SPI1_D3	SPI1 Data 3	F	PF_07
SPI1_MISO	SPI1 Master In, Slave Out	C	PC_10
SPI1_MOSI	SPI1 Master Out, Slave In	C	PC_11
SPI1_RDY	SPI1 Ready	C	PC_14

Table 7. ADSP-CM412F/CM413F/CM416F/CM417F 176-Lead LQFP_EP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SPI1_SEL1	SPI1 Slave Select Output 1	C	PC_12
SPI1_SEL2	SPI1 Slave Select Output 2	C	PC_13
SPI1_SEL3	SPI1 Slave Select Output 3	C	PC_14
SPI1_SEL4	SPI1 Slave Select Output 4	F	PF_02
SPI1_SEL5	SPI1 Slave Select Output 5	F	PF_05
SPI1_SEL6	SPI1 Slave Select Output 6	F	PF_03
SPI1_SEL7	SPI1 Slave Select Output 7	F	PF_08
SPI1_SS	SPI1 Slave Select Input	C	PC_12
SPT0_ACLK	SPORT0 Channel A Clock	C	PC_09
SPT0_AD0	SPORT0 Channel A Data 0	B	PB_09
SPT0_AD1	SPORT0 Channel A Data 1	C	PC_06
SPT0_AFS	SPORT0 Channel A Frame Sync	C	PC_11
SPT0_ATDV	SPORT0 Channel A Transmit Data Valid	C	PC_15
SPT0_BCLK	SPORT0 Channel B Clock	C	PC_12
SPT0_BD0	SPORT0 Channel B Data 0	C	PC_14
SPT0_BD1	SPORT0 Channel B Data 1	C	PC_10
SPT0_BFS	SPORT0 Channel B Frame Sync	C	PC_13
SPT0_BTDV	SPORT0 Channel B Transmit Data Valid	C	PC_05
SYS_BMODE0	Boot Mode Control 0	Not Muxed	SYS_BMODE0
SYS_CLKIN0	Clock/Crystal Input	Not Muxed	SYS_CLKIN0
SYS_CLKIN1	Clock/Crystal Input	Not Muxed	SYS_CLKIN1
SYS_CLKOUT	Processor Clock Output	Not Muxed	SYS_CLKOUT
SYS_DSWAKE0	Deep Sleep Wakeup 0	C	PC_05
SYS_DSWAKE1	Deep Sleep Wakeup 1	D	PD_00
SYS_DSWAKE2	Deep Sleep Wakeup 2	F	PF_08
SYS_DSWAKE3	Deep Sleep Wakeup 3	A	PA_11
SYS_FAULT	Fault Output	Not Muxed	SYS_FAULT
SYS_HWRST	Processor Hardware Reset Control	Not Muxed	SYS_HWRST
SYS_NMI	Non-maskable Interrupt	Not Muxed	SYS_NMI
SYS_RESOUT	Reset Output	Not Muxed	SYS_RESOUT
SYS_XTAL0	Crystal Output	Not Muxed	SYS_XTAL0
SYS_XTAL1	Crystal Output	Not Muxed	SYS_XTAL1
TM0_ACI0	TIMER0 Alternate Capture Input 0	A	PA_04
TM0_ACI1	TIMER0 Alternate Capture Input 1	A	PA_06
TM0_ACI2	TIMER0 Alternate Capture Input 2	A	PA_01
TM0_ACI3	TIMER0 Alternate Capture Input 3	A	PA_02
TM0_ACI4	TIMER0 Alternate Capture Input 4	A	PA_03
TM0_ACLK0	TIMER0 Alternate Clock 0	A	PA_09
TM0_ACLK1	TIMER0 Alternate Clock 1	A	PA_10
TM0_ACLK2	TIMER0 Alternate Clock 2	A	PA_07
TM0_ACLK3	TIMER0 Alternate Clock 3	A	PA_08
TM0_ACLK4	TIMER0 Alternate Clock 4	A	PA_05
TM0_CLK	TIMER0 Clock	A	PA_00
TM0_TMR0	TIMER0 Timer 0	A	PA_12
TM0_TMR1	TIMER0 Timer 1	A	PA_13
TM1_ACI0	TIMER1 Alternate Capture Input 0	E	PE_12

Table 7. ADSP-CM412F/CM413F/CM416F/CM417F 176-Lead LQFP_EP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
TM1_ACI2	TIMER1 Alternate Capture Input 2	C	PC_08
TM1_ACI4	TIMER1 Alternate Capture Input 4	C	PC_09
TM1_ACI5	TIMER1 Alternate Capture Input 5	E	PE_09
TM1_ACI6	TIMER1 Alternate Capture Input 6	F	PF_05
TM1_ACLK3	TIMER1 Alternate Clock 3	C	PC_15
TM1_ACLK4	TIMER1 Alternate Clock 4	C	PC_00
TM1_ACLK5	TIMER1 Alternate Clock 5	E	PE_08
TM1_CLK	TIMER1 Clock	C	PC_06
TM1_TMR0	TIMER1 Timer 0	E	PE_14
TM1_TMR0	TIMER1 Timer 0	B	PB_14
TM1_TMR1	TIMER1 Timer 1	B	PB_15
TM1_TMR1	TIMER1 Timer 1	E	PE_15
TM1_TMR2	TIMER1 Timer 2	B	PB_13
TM1_TMR3	TIMER1 Timer 3	C	PC_10
TM1_TMR4	TIMER1 Timer 4	E	PE_04
TM1_TMR5	TIMER1 Timer 5	F	PF_06
TM1_TMR6	TIMER1 Timer 6	E	PE_02
TM1_TMR7	TIMER1 Timer 7	C	PC_12
TRACE0_CLK	TRACE0 Trace Clock	C	PC_00
TRACE0_D00	TRACE0 Trace Data 0	C	PC_03
TRACE0_D01	TRACE0 Trace Data 1	C	PC_01
TRACE0_D02	TRACE0 Trace Data 2	C	PC_04
TRACE0_D03	TRACE0 Trace Data 3	C	PC_02
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
$\overline{\text{UART0\_CTS}}$	UART0 Clear to Send	A	PA_03
$\overline{\text{UART0\_RTS}}$	UART0 Request to Send	A	PA_02
UART0_RX	UART0 Receive	A	PA_04
UART0_TX	UART0 Transmit	A	PA_05
$\overline{\text{UART1\_CTS}}$	UART1 Clear to Send	C	PC_05
$\overline{\text{UART1\_RTS}}$	UART1 Request to Send	C	PC_15
UART1_RX	UART1 Receive	E	PE_09
UART1_TX	UART1 Transmit	E	PE_10
$\overline{\text{UART2\_CTS}}$	UART2 Clear to Send	C	PC_06
$\overline{\text{UART2\_RTS}}$	UART2 Request to Send	B	PB_09
UART2_RX	UART2 Receive	C	PC_09
UART2_TX	UART2 Transmit	C	PC_11
$\overline{\text{UART3\_CTS}}$	UART3 Clear to Send	B	PB_07
$\overline{\text{UART3\_RTS}}$	UART3 Request to Send	E	PE_08
UART3_RX	UART3 Receive	C	PC_08
UART3_TX	UART3 Transmit	C	PC_07
$\overline{\text{UART4\_CTS}}$	UART4 Clear to Send	E	PE_03
$\overline{\text{UART4\_RTS}}$	UART4 Request to Send	E	PE_01
UART4_RX	UART4 Receive	F	PF_05
UART4_TX	UART4 Transmit	F	PF_04
VDD_ANA0	Analog Power Supply Voltage	Not Muxed	VDD_ANA0

Table 7. ADSP-CM412F/CM413F/CM416F/CM417F 176-Lead LQFP_EP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
VDD_ANA1	Analog Power Supply Voltage	Not Muxed	VDD_ANA1
VDD_COMP	Power supply for over current comparator	Not Muxed	VDD_COMP
VDD_EXT	External Voltage Domain	Not Muxed	VDD_EXT

GPIO MULTIPLEXING FOR 176-LEAD LQFP_EP PACKAGE

Table 8 through Table 13 identify the pin functions that are multiplexed on the general-purpose I/O pins of the 176-lead LQFP_EP package.

Table 8. Signal Multiplexing for Port A

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function InputTap
PA_00	SPI0_SEL2	TM0_CLK			SPI0_SS
PA_01	SPI0_SEL3	SPI0_RDY			TM0_ACI2
PA_02	SPI0_D2	UART0_RTS	SPI0_SEL6		TM0_ACI3
PA_03	SPI0_D3	UART0_CTS	SPI0_SEL7		TM0_ACI4
PA_04	UART0_RX				TM0_ACI0
PA_05	UART0_TX				TM0_ACLK4
PA_06	CAN0_RX	SPI0_SEL4			TM0_ACI1
PA_07	CAN0_TX	SPI0_SEL5			TM0_ACLK2
PA_08	SPI0_CLK				TM0_ACLK3
PA_09	SPI0_MOSI				TM0_ACLK0
PA_10	SPI0_MISO				TM0_ACLK1
PA_11	SPI0_SEL1				SYS_DSWAKE3
PA_12	TM0_TMR0				
PA_13	TM0_TMR1				

Table 9. Signal Multiplexing for Port B

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function InputTap
PB_00	PWM0_AH		SMC0_ARDY		
PB_01	PWM0_AL		SMC0_AWE		
PB_02	PWM0_BH		SMC0_AOE		
PB_03	PWM0_BL		SMC0_ARE		
PB_04	PWM0_CH		SMC0_AMS0		
PB_05	PWM0_CL		SMC0_D00		
PB_06	PWM0_DH		SMC0_D01		
PB_07	PWM0_DL	UART3_CTS	SMC0_D02		
PB_08	PWM1_AH	CNT0_OUTA	SMC0_D03		
PB_09	PWM1_AL	UART2_RTS	SMC0_D04	SPT0_AD0	CNT0_UD
PB_10	PWM1_BH	CNT0_OUTB	SMC0_D05		
PB_11	PWM1_BL		SMC0_D06		
PB_12	PWM1_CH		SMC0_D07		
PB_13	PWM1_CL	TM1_TMR2	SMC0_A01		
PB_14	PWM1_DH			TM1_TMR0	
PB_15	PWM1_DL		SMC0_A02	TM1_TMR1	

Table 10. Signal Multiplexing for Port C

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function InputTap
PC_00	TRACE0_CLK				TM1_ACLK4
PC_01	TRACE0_D01				
PC_02	TRACE0_D03			LBA0_PIN6	
PC_03	TRACE0_D00				
PC_04	TRACE0_D02			LBA0_PIN7	
PC_05	SINC0_D0	UART1_CTS	SMC0_D14	SPT0_BTDV	SYS_DSWAKE0
PC_06	SINC0_D1	UART2_CTS	SMC0_D15	SPT0_AD1	TM1_CLK
PC_07	UART3_TX				
PC_08	UART3_RX				TM1_ACI2
PC_09	SPI1_CLK	UART2_RX	SMC0_D08	SPT0_ACLK	TM1_ACI4
PC_10	SPI1_MISO	TM1_TMR3	SMC0_D09	SPT0_BD1	
PC_11	SPI1_MOSI	UART2_TX	SMC0_D10	SPT0_AFS	
PC_12	SPI1_SEL1	TM1_TMR7	SMC0_D11	SPT0_BCLK	SPI1_SS
PC_13	SPI1_SEL2		SMC0_D12	SPT0_BFS	CNT0_DG
PC_14	SPI1_SEL3	SPI1_RDY	SMC0_D13	SPT0_BD0	CNT0_ZM
PC_15	SINC0_CLK0	UART1_RTS		SPT0_ATDV	TM1_ACLK3

Table 11. Signal Multiplexing for Port D

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function InputTap
PD_00	PWM0_SYNC		SMC0_A03		SYS_DSWAKE1
PD_01	PWM_TRIPA		SMC0_A04		

Table 12. Signal Multiplexing for Port E

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function InputTap
PE_00	PWM2_AH				
PE_01	PWM2_AL	UART4_RTS	SMC0_AMS1		
PE_02	PWM2_BH	TM1_TMR6	SMC0_AMS2		CPTMR0_IN0
PE_03	PWM2_BL	UART4_CTS	SMC0_A15		
PE_04	PWM2_CH	TM1_TMR4			CPTMR0_IN1
PE_05	PWM2_CL		SMC0_A14		
PE_06	PWM2_DH		SMC0_A11		
PE_07	PWM2_DL		SMC0_A12		
PE_08	PWM2_SYNC	UART3_RTS	SMC0_AMS3		TM1_ACLK5
PE_09	PWM1_SYNC	UART1_RX			TM1_ACI5
PE_10	PWM_TRIPB	UART1_TX			
PE_11	PWM_TRIPC		SMC0_A16		
PE_12	CAN1_RX		SMC0_ABE1		TM1_ACI0
PE_13	CAN1_TX		SMC0_ABE0		
PE_14	TM1_TMR0		SMC0_A05		
PE_15	TM1_TMR1		SMC0_A10		

Table 13. Signal Multiplexing for Port F

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function InputTap
PF_00	SINC0_D2		SMC0_A06		
PF_01	SINC0_D3		SMC0_A07		
PF_02	SPI1_SEL4		SMC0_A08		
PF_03	SPI1_SEL6		SMC0_A09	LBA0_PIN0	
PF_04	UART4_TX		SMC0_A13	LBA0_PIN1	
PF_05	UART4_RX	SPI1_SEL5		LBA0_PIN2	TM1_ACI6
PF_06	SPI1_D2	TM1_TMR5		LBA0_PIN3	CPTMR0_IN2
PF_07	SPI1_D3			LBA0_PIN4	
PF_08	SPI1_SEL7			LBA0_PIN5	SYS_DSWAKE2

210-BALL CSP_BGA SIGNAL DESCRIPTIONS

The processor pin definitions are shown in Table 14 for the 210-ball CSP_BGA package. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The description column provides a descriptive name for each signal.
- The port column shows whether or not a signal is multiplexed with other signals on a general-purpose I/O port pin.
- The pin name column identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).

Table 14. ADSP-CM411F/CM418F/CM419F 210-Ball CSP_BGA Signal Descriptions

Signal Name	Description	Port	Pin Name
ADC_VIN_A0	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_A0
ADC_VIN_A1	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_A1
ADC_VIN_A2	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_A2
ADC_VIN_A3	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_A3
ADC_VIN_A4	Channel n Single-Ended Analog Input for ADC2[1]	Not Muxed	ADC_VIN_A4
ADC_VIN_A5	Channel n Single-Ended Analog Input for ADC2[1]	Not Muxed	ADC_VIN_A5
ADC_VIN_A6	Channel n Single-Ended Analog Input for ADC2[1]	Not Muxed	ADC_VIN_A6
ADC_VIN_A7	Channel n Single-Ended Analog Input for ADC2[1]	Not Muxed	ADC_VIN_A7
ADC_VIN_B0	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_B0
ADC_VIN_B1	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_B1
ADC_VIN_B2	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_B2
ADC_VIN_B3	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_B3
ADC_VIN_B4	Channel n Single-Ended Analog Input for ADC2[1]	Not Muxed	ADC_VIN_B4
ADC_VIN_B5	Channel n Single-Ended Analog Input for ADC2[1]	Not Muxed	ADC_VIN_B5
ADC_VIN_B6	Channel n Single-Ended Analog Input for ADC2[1]	Not Muxed	ADC_VIN_B6
ADC_VIN_B7	Channel n Single-Ended Analog Input for ADC2[1]	Not Muxed	ADC_VIN_B7
ADC_VIN_C0	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_C0
ADC_VIN_C1	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_C1
ADC_VIN_C2	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_C2
ADC_VIN_C3	Channel n Single-Ended Analog Input for ADC1	Not Muxed	ADC_VIN_C3
ADC_VIN_C4	Channel n Single-Ended Analog Input for ADC2[1]	Not Muxed	ADC_VIN_C4
ADC_VIN_C5	Channel n Single-Ended Analog Input for ADC2[1]	Not Muxed	ADC_VIN_C5
ADC_VIN_C6	Channel n Single-Ended Analog Input for ADC2[1]	Not Muxed	ADC_VIN_C6
ADC_VIN_C7	Channel n Single-Ended Analog Input for ADC2[1]	Not Muxed	ADC_VIN_C7
ADC_VIN_D0	Channel n Single-Ended Analog Input for ADC0	Not Muxed	ADC_VIN_D0
ADC_VIN_D1	Channel n Single-Ended Analog Input for ADC0	Not Muxed	ADC_VIN_D1
ADC_VIN_D2	Channel n Single-Ended Analog Input for ADC0	Not Muxed	ADC_VIN_D2
ADC_VIN_D3	Channel n Single-Ended Analog Input for ADC0	Not Muxed	ADC_VIN_D3
ADC_VIN_D4	Channel n Single-Ended Analog Input for ADC0	Not Muxed	ADC_VIN_D4
ADC_VIN_D5	Channel n Single-Ended Analog Input for ADC0	Not Muxed	ADC_VIN_D5
ADC_VIN_D6	Channel n Single-Ended Analog Input for ADC0	Not Muxed	ADC_VIN_D6
BYP_A0	On-chip Analog Power Regulation Bypass Filter Node for ADC	Not Muxed	BYP_A0
BYP_A1	On-chip Analog Power Regulation Bypass Filter Node for ADC	Not Muxed	BYP_A1
BYP_A2	On-chip Analog Power Regulation Bypass Filter Node for ADC	Not Muxed	BYP_A2
BYP_D0	On-chip Analog Power Regulation Bypass Filter Node for DAC	Not Muxed	BYP_D0
CAN0_RX	CAN0 Receive	A	PA_06
CAN0_TX	CAN0 Transmit	A	PA_07

Table 14. ADSP-CM411F/CM418F/CM419F 210-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
CAN1_RX	CAN1 Receive	E	PE_12
CAN1_TX	CAN1 Transmit	E	PE_13
CNT0_DG	CNT0 Count Down and Gate	C	PC_13
CNT0_OUTA	CNT0 Output Divider A	B	PB_08
CNT0_OUTB	CNT0 Output Divider B	B	PB_10
CNT0_UD	CNT0 Count Up and Direction	B	PB_09
CNT0_ZM	CNT0 Count Zero Marker	C	PC_14
COMP_OUT_A	Fast over-current protection comparator A output	Not Muxed	COMP_OUT_A
COMP_OUT_B	Fast over-current protection comparator B output	Not Muxed	COMP_OUT_B
COMP_OUT_C	Fast over-current protection comparator C output	Not Muxed	COMP_OUT_C
CPTMR0_IN0	CPTMR0 Input	E	PE_02
CPTMR0_IN1	CPTMR0 Input	E	PE_04
CPTMR0_IN2	CPTMR0 Input	F	PF_06
DAC0_VOUT	Analog Voltage Output n	Not Muxed	DAC0_VOUT
GND_REFCAP0	Ground return for REF_INOUT0	Not Muxed	GND_REFCAP0
GND_REFCAP1	GND_REFCAP1	Not Muxed	GND_REFCAP1
GND_VREF0	Ground return for REF_BUFOUT[0]	Not Muxed	GND_VREF0
GND_VREF1	Ground return for REF_BUFOUT[1]	Not Muxed	GND_VREF1
GND_VREF2	GND_VREF2	Not Muxed	GND_VREF2
JTG_TCK/SWCLK	JTAG Clock/Serial Wire Clock	Not Muxed	JTG_TCK/SWCLK
JTG_TDI	JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO/SWO	JTAG Serial Data Out/Serial Wire Trace Output	Not Muxed	JTG_TDO/SWO
JTG_TMS/SWDIO	JTAG Mode Select/Serial Wire Debug Data I/O	Not Muxed	JTG_TMS/SWDIO
$\overline{\text{JTG\_TRST}}$	JTAG Reset	Not Muxed	$\overline{\text{JTG\_TRST}}$
LBA0_PIN0	LBA0 LBA data input or the logic output	F	PF_03
LBA0_PIN1	LBA0 LBA data input or the logic output	F	PF_04
LBA0_PIN2	LBA0 LBA data input or the logic output	F	PF_05
LBA0_PIN3	LBA0 LBA data input or the logic output	F	PF_06
LBA0_PIN4	LBA0 LBA data input or the logic output	F	PF_07
LBA0_PIN5	LBA0 LBA data input or the logic output	F	PF_08
LBA0_PIN6	LBA0 LBA data input or the logic output	C	PC_02
LBA0_PIN7	LBA0 LBA data input or the logic output	C	PC_04
PWM0_AH	PWM0 Channel A High Side	B	PB_00
PWM0_AL	PWM0 Channel A Low Side	B	PB_01
PWM0_BH	PWM0 Channel B High Side	B	PB_02
PWM0_BL	PWM0 Channel B Low Side	B	PB_03
PWM0_CH	PWM0 Channel C High Side	B	PB_04
PWM0_CL	PWM0 Channel C Low Side	B	PB_05
PWM0_DH	PWM0 Channel D High Side	B	PB_06
PWM0_DL	PWM0 Channel D Low Side	B	PB_07
PWM0_SYNC	PWM0 PWMTMR Grouped	D	PD_00
PWM1_AH	PWM1 Channel A High Side	B	PB_08
PWM1_AL	PWM1 Channel A Low Side	B	PB_09
PWM1_BH	PWM1 Channel B High Side	B	PB_10
PWM1_BL	PWM1 Channel B Low Side	B	PB_11
PWM1_CH	PWM1 Channel C High Side	B	PB_12
PWM1_CL	PWM1 Channel C Low Side	B	PB_13

Table 14. ADSP-CM411F/CM418F/CM419F 210-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PWM1_DH	PWM1 Channel D High Side	B	PB_14
PWM1_DL	PWM1 Channel D Low Side	B	PB_15
PWM1_SYNC	PWM1 PWMTMR Grouped	E	PE_09
PWM2_AH	PWM2 Channel A High Side	E	PE_00
PWM2_AL	PWM2 Channel A Low Side	E	PE_01
PWM2_BH	PWM2 Channel B High Side	E	PE_02
PWM2_BL	PWM2 Channel B Low Side	E	PE_03
PWM2_CH	PWM2 Channel C High Side	E	PE_04
PWM2_CL	PWM2 Channel C Low Side	E	PE_05
PWM2_DH	PWM2 Channel D High Side	E	PE_06
PWM2_DL	PWM2 Channel D Low Side	E	PE_07
PWM2_SYNC	PWM2 PWMTMR Grouped	E	PE_08
$\overline{\text{PWM\_TRIPA}}$	Muxed PWM Trip A signal	D	PD_01
$\overline{\text{PWM\_TRIPB}}$	Muxed PWM Trip B signal	E	PE_10
$\overline{\text{PWM\_TRIPC}}$	Muxed PWM Trip C signal	E	PE_11
REFCAP0	Output of BandGap Generator Filter Node	Not Muxed	REFCAP0
REFCAP1	Output of BandGap Generator Filter Node	Not Muxed	REFCAP1
REF_BUFOUT0	Voltage reference ADC0 and DAC0	Not Muxed	VREF0
REF_BUFOUT1	Voltage reference ADC1 and Over Current Comparator DACs	Not Muxed	VREF1
SINC0_CLK0	SINC0 Clock 0	C	PC_15
SINC0_D0	SINC0 Data 0	C	PC_05
SINC0_D1	SINC0 Data 1	C	PC_06
SINC0_D2	SINC0 Data 2	F	PF_00
SINC0_D3	SINC0 Data 3	F	PF_01
SMC0_A01	SMC0 Address 1	B	PB_13
SMC0_A02	SMC0 Address 2	B	PB_15
SMC0_A03	SMC0 Address 3	D	PD_00
SMC0_A04	SMC0 Address 4	D	PD_01
SMC0_A05	SMC0 Address 5	E	PE_14
SMC0_A06	SMC0 Address 6	F	PF_00
SMC0_A07	SMC0 Address 7	F	PF_01
SMC0_A08	SMC0 Address 8	F	PF_02
SMC0_A09	SMC0 Address 9	F	PF_03
SMC0_A10	SMC0 Address 10	E	PE_15
SMC0_A11	SMC0 Address 11	E	PE_06
SMC0_A12	SMC0 Address 12	E	PE_07
SMC0_A13	SMC0 Address 13	F	PF_04
SMC0_A14	SMC0 Address 14	E	PE_05
SMC0_A15	SMC0 Address 15	E	PE_03
SMC0_A16	SMC0 Address 16	E	PE_11
$\overline{\text{SMC0\_ABE0}}$	SMC0 Byte Enable 0	E	PE_13
$\overline{\text{SMC0\_ABE1}}$	SMC0 Byte Enable 1	E	PE_12
$\overline{\text{SMC0\_AMS0}}$	SMC0 Memory Select 0	B	PB_04
$\overline{\text{SMC0\_AMS1}}$	SMC0 Memory Select 1	E	PE_01
$\overline{\text{SMC0\_AMS2}}$	SMC0 Memory Select 2	E	PE_02
$\overline{\text{SMC0\_AMS3}}$	SMC0 Memory Select 3	E	PE_08
$\overline{\text{SMC0\_AOE}}$	SMC0 Output Enable	B	PB_02

Table 14. ADSP-CM411F/CM418F/CM419F 210-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_ARDY	SMC0 Asynchronous Ready	B	PB_00
$\overline{\text{SMC0\_ARE}}$	SMC0 Read Enable	B	PB_03
$\overline{\text{SMC0\_AWE}}$	SMC0 Write Enable	B	PB_01
SMC0_D00	SMC0 Data 0	B	PB_05
SMC0_D01	SMC0 Data 1	B	PB_06
SMC0_D02	SMC0 Data 2	B	PB_07
SMC0_D03	SMC0 Data 3	B	PB_08
SMC0_D04	SMC0 Data 4	B	PB_09
SMC0_D05	SMC0 Data 5	B	PB_10
SMC0_D06	SMC0 Data 6	B	PB_11
SMC0_D07	SMC0 Data 7	B	PB_12
SMC0_D08	SMC0 Data 8	C	PC_09
SMC0_D09	SMC0 Data 9	C	PC_10
SMC0_D10	SMC0 Data 10	C	PC_11
SMC0_D11	SMC0 Data 11	C	PC_12
SMC0_D12	SMC0 Data 12	C	PC_13
SMC0_D13	SMC0 Data 13	C	PC_14
SMC0_D14	SMC0 Data 14	C	PC_05
SMC0_D15	SMC0 Data 15	C	PC_06
SPI0_CLK	SPI0 Clock	A	PA_08
SPI0_D2	SPI0 Data 2	A	PA_02
SPI0_D3	SPI0 Data 3	A	PA_03
SPI0_MISO	SPI0 Master In, Slave Out	A	PA_10
SPI0_MOSI	SPI0 Master Out, Slave In	A	PA_09
SPI0_RDY	SPI0 Ready	A	PA_01
$\overline{\text{SPI0\_SEL1}}$	SPI0 Slave Select Output 1	A	PA_11
$\overline{\text{SPI0\_SEL2}}$	SPI0 Slave Select Output 2	A	PA_00
$\overline{\text{SPI0\_SEL3}}$	SPI0 Slave Select Output 3	A	PA_01
$\overline{\text{SPI0\_SEL4}}$	SPI0 Slave Select Output 4	A	PA_06
$\overline{\text{SPI0\_SEL5}}$	SPI0 Slave Select Output 5	A	PA_07
$\overline{\text{SPI0\_SEL6}}$	SPI0 Slave Select Output 6	A	PA_02
$\overline{\text{SPI0\_SEL7}}$	SPI0 Slave Select Output 7	A	PA_03
$\overline{\text{SPI0\_SS}}$	SPI0 Slave Select Input	A	PA_00
SPI1_CLK	SPI1 Clock	C	PC_09
SPI1_D2	SPI1 Data 2	F	PF_06
SPI1_D3	SPI1 Data 3	F	PF_07
SPI1_MISO	SPI1 Master In, Slave Out	C	PC_10
SPI1_MOSI	SPI1 Master Out, Slave In	C	PC_11
SPI1_RDY	SPI1 Ready	C	PC_14
$\overline{\text{SPI1\_SEL1}}$	SPI1 Slave Select Output 1	C	PC_12
$\overline{\text{SPI1\_SEL2}}$	SPI1 Slave Select Output 2	C	PC_13
$\overline{\text{SPI1\_SEL3}}$	SPI1 Slave Select Output 3	C	PC_14
$\overline{\text{SPI1\_SEL4}}$	SPI1 Slave Select Output 4	F	PF_02
$\overline{\text{SPI1\_SEL5}}$	SPI1 Slave Select Output 5	F	PF_05
$\overline{\text{SPI1\_SEL6}}$	SPI1 Slave Select Output 6	F	PF_03
$\overline{\text{SPI1\_SEL7}}$	SPI1 Slave Select Output 7	F	PF_08
$\overline{\text{SPI1\_SS}}$	SPI1 Slave Select Input	C	PC_12

Table 14. ADSP-CM411F/CM418F/CM419F 210-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SPT0_ACLK	SPORT0 Channel A Clock	C	PC_09
SPT0_AD0	SPORT0 Channel A Data 0	B	PB_09
SPT0_AD1	SPORT0 Channel A Data 1	C	PC_06
SPT0_AFS	SPORT0 Channel A Frame Sync	C	PC_11
SPT0_ATDV	SPORT0 Channel A Transmit Data Valid	C	PC_15
SPT0_BCLK	SPORT0 Channel B Clock	C	PC_12
SPT0_BD0	SPORT0 Channel B Data 0	C	PC_14
SPT0_BD1	SPORT0 Channel B Data 1	C	PC_10
SPT0_BFS	SPORT0 Channel B Frame Sync	C	PC_13
SPT0_BTDV	SPORT0 Channel B Transmit Data Valid	C	PC_05
SYS_BMODE0	Boot Mode Control 0	Not Muxed	SYS_BMODE0
$\overline{\text{SYS\_CLKIN0}}$	Clock/Crystal Input	Not Muxed	SYS_CLKIN0
$\overline{\text{SYS\_CLKIN1}}$	Clock/Crystal Input	Not Muxed	SYS_CLKIN1
SYS_CLKOUT	Processor Clock Output	Not Muxed	SYS_CLKOUT
SYS_DSWAKE0	Deep Sleep Wakeup 0	C	PC_05
SYS_DSWAKE1	Deep Sleep Wakeup 1	D	PD_00
SYS_DSWAKE2	Deep Sleep Wakeup 2	F	PF_08
SYS_DSWAKE3	Deep Sleep Wakeup 3	A	PA_11
$\overline{\text{SYS\_FAULT}}$	Fault Output	Not Muxed	$\overline{\text{SYS\_FAULT}}$
$\overline{\text{SYS\_HWRST}}$	Processor Hardware Reset Control	Not Muxed	$\overline{\text{SYS\_HWRST}}$
$\overline{\text{SYS\_NMI}}$	Non-maskable Interrupt	Not Muxed	$\overline{\text{SYS\_NMI}}$
$\overline{\text{SYS\_RESOUT}}$	Reset Output	Not Muxed	$\overline{\text{SYS\_RESOUT}}$
$\overline{\text{SYS\_XTAL0}}$	Crystal Output	Not Muxed	SYS_XTAL0
$\overline{\text{SYS\_XTAL1}}$	Crystal Output	Not Muxed	SYS_XTAL1
TM0_ACI0	TIMER0 Alternate Capture Input 0	A	PA_04
TM0_ACI1	TIMER0 Alternate Capture Input 1	A	PA_06
TM0_ACI2	TIMER0 Alternate Capture Input 2	A	PA_01
TM0_ACI3	TIMER0 Alternate Capture Input 3	A	PA_02
TM0_ACI4	TIMER0 Alternate Capture Input 4	A	PA_03
TM0_ACLK0	TIMER0 Alternate Clock 0	A	PA_09
TM0_ACLK1	TIMER0 Alternate Clock 1	A	PA_10
TM0_ACLK2	TIMER0 Alternate Clock 2	A	PA_07
TM0_ACLK3	TIMER0 Alternate Clock 3	A	PA_08
TM0_ACLK4	TIMER0 Alternate Clock 4	A	PA_05
TM0_CLK	TIMER0 Clock	A	PA_00
TM0_TMR0	TIMER0 Timer 0	A	PA_12
TM0_TMR1	TIMER0 Timer 1	A	PA_13
TM1_ACI0	TIMER1 Alternate Capture Input 0	E	PE_12
TM1_ACI2	TIMER1 Alternate Capture Input 2	C	PC_08
TM1_ACI4	TIMER1 Alternate Capture Input 4	C	PC_09
TM1_ACI5	TIMER1 Alternate Capture Input 5	E	PE_09
TM1_ACI6	TIMER1 Alternate Capture Input 6	F	PF_05
TM1_ACLK3	TIMER1 Alternate Clock 3	C	PC_15
TM1_ACLK4	TIMER1 Alternate Clock 4	C	PC_00
TM1_ACLK5	TIMER1 Alternate Clock 5	E	PE_08
TM1_CLK	TIMER1 Clock	C	PC_06
TM1_TMR0	TIMER1 Timer 0	E	PE_14

Table 14. ADSP-CM411F/CM418F/CM419F 210-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
TM1_TMR0	TIMER1 Timer 0	B	PB_14
TM1_TMR1	TIMER1 Timer 1	B	PB_15
TM1_TMR1	TIMER1 Timer 1	E	PE_15
TM1_TMR2	TIMER1 Timer 2	B	PB_13
TM1_TMR3	TIMER1 Timer 3	C	PC_10
TM1_TMR4	TIMER1 Timer 4	E	PE_04
TM1_TMR5	TIMER1 Timer 5	F	PF_06
TM1_TMR6	TIMER1 Timer 6	E	PE_02
TM1_TMR7	TIMER1 Timer 7	C	PC_12
TRACE0_CLK	TRACE0 Trace Clock	C	PC_00
TRACE0_D00	TRACE0 Trace Data 0	C	PC_03
TRACE0_D01	TRACE0 Trace Data 1	C	PC_01
TRACE0_D02	TRACE0 Trace Data 2	C	PC_04
TRACE0_D03	TRACE0 Trace Data 3	C	PC_02
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
$\overline{\text{UART0\_CTS}}$	UART0 Clear to Send	A	PA_03
$\overline{\text{UART0\_RTS}}$	UART0 Request to Send	A	PA_02
UART0_RX	UART0 Receive	A	PA_04
UART0_TX	UART0 Transmit	A	PA_05
$\overline{\text{UART1\_CTS}}$	UART1 Clear to Send	C	PC_05
$\overline{\text{UART1\_RTS}}$	UART1 Request to Send	C	PC_15
UART1_RX	UART1 Receive	E	PE_09
UART1_TX	UART1 Transmit	E	PE_10
$\overline{\text{UART2\_CTS}}$	UART2 Clear to Send	C	PC_06
$\overline{\text{UART2\_RTS}}$	UART2 Request to Send	B	PB_09
UART2_RX	UART2 Receive	C	PC_09
UART2_TX	UART2 Transmit	C	PC_11
$\overline{\text{UART3\_CTS}}$	UART3 Clear to Send	B	PB_07
$\overline{\text{UART3\_RTS}}$	UART3 Request to Send	E	PE_08
UART3_RX	UART3 Receive	C	PC_08
UART3_TX	UART3 Transmit	C	PC_07
$\overline{\text{UART4\_CTS}}$	UART4 Clear to Send	E	PE_03
$\overline{\text{UART4\_RTS}}$	UART4 Request to Send	E	PE_01
UART4_RX	UART4 Receive	F	PF_05
UART4_TX	UART4 Transmit	F	PF_04
VDD_ANA0	Analog Power Supply Voltage	Not Muxed	VDD_ANA0
VDD_ANA1	Analog Power Supply Voltage	Not Muxed	VDD_ANA1
VDD_COMP	Power supply for over current comparator	Not Muxed	VDD_COMP
VDD_EXT	External Voltage Domain	Not Muxed	VDD_EXT
VREF2	Voltage reference ADC2	Not Muxed	VREF2

[1] For the ADSP-CM411F model, all analog inputs go to ADC1 (see Figure 4).

GPIO MULTIPLEXING FOR 210-BALL CSP_BGA PACKAGE

Table 15 through Table 20 identify the pin functions that are multiplexed on the general-purpose I/O pins of the 210-ball CSP_BGA package.

Table 15. Signal Multiplexing for Port A

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function InputTap
PA_00	$\overline{\text{SPI0\_SEL2}}$	TM0_CLK			$\overline{\text{SPI0\_SS}}$
PA_01	$\overline{\text{SPI0\_SEL3}}$	SPI0_RDY			TM0_ACI2
PA_02	SPI0_D2	$\overline{\text{UART0\_RTS}}$	$\overline{\text{SPI0\_SEL6}}$		TM0_ACI3
PA_03	SPI0_D3	$\overline{\text{UART0\_CTS}}$	$\overline{\text{SPI0\_SEL7}}$		TM0_ACI4
PA_04	UART0_RX				TM0_ACI0
PA_05	UART0_TX				TM0_ACLK4
PA_06	CAN0_RX	$\overline{\text{SPI0\_SEL4}}$			TM0_ACI1
PA_07	CAN0_TX	$\overline{\text{SPI0\_SEL5}}$			TM0_ACLK2
PA_08	SPI0_CLK				TM0_ACLK3
PA_09	SPI0_MOSI				TM0_ACLK0
PA_10	SPI0_MISO				TM0_ACLK1
PA_11	$\overline{\text{SPI0\_SEL1}}$				SYS_DSWAKE3
PA_12	TM0_TMR0				
PA_13	TM0_TMR1				

Table 16. Signal Multiplexing for Port B

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function InputTap
PB_00	PWM0_AH		SMC0_ARDY		
PB_01	PWM0_AL		$\overline{\text{SMC0\_AWE}}$		
PB_02	PWM0_BH		$\overline{\text{SMC0\_AOE}}$		
PB_03	PWM0_BL		$\overline{\text{SMC0\_ARE}}$		
PB_04	PWM0_CH		$\overline{\text{SMC0\_AMS0}}$		
PB_05	PWM0_CL		SMC0_D00		
PB_06	PWM0_DH		SMC0_D01		
PB_07	PWM0_DL	$\overline{\text{UART3\_CTS}}$	SMC0_D02		
PB_08	PWM1_AH	CNT0_OUTA	SMC0_D03		
PB_09	PWM1_AL	$\overline{\text{UART2\_RTS}}$	SMC0_D04	SPT0_AD0	CNT0_UD
PB_10	PWM1_BH	CNT0_OUTB	SMC0_D05		
PB_11	PWM1_BL		SMC0_D06		
PB_12	PWM1_CH		SMC0_D07		
PB_13	PWM1_CL	TM1_TMR2	SMC0_A01		
PB_14	PWM1_DH			TM1_TMR0	
PB_15	PWM1_DL		SMC0_A02	TM1_TMR1	

Table 17. Signal Multiplexing for Port C

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function InputTap
PC_00	TRACE0_CLK				TM1_ACLK4
PC_01	TRACE0_D01				
PC_02	TRACE0_D03			LBA0_PIN6	
PC_03	TRACE0_D00				
PC_04	TRACE0_D02			LBA0_PIN7	
PC_05	SINC0_D0	UART1_CTS	SMC0_D14	SPT0_BTDV	SYS_DSWAKE0
PC_06	SINC0_D1	UART2_CTS	SMC0_D15	SPT0_AD1	TM1_CLK
PC_07	UART3_TX				
PC_08	UART3_RX				TM1_ACI2
PC_09	SPI1_CLK	UART2_RX	SMC0_D08	SPT0_ACLK	TM1_ACI4
PC_10	SPI1_MISO	TM1_TMR3	SMC0_D09	SPT0_BD1	
PC_11	SPI1_MOSI	UART2_TX	SMC0_D10	SPT0_AFS	
PC_12	SPI1_SEL1	TM1_TMR7	SMC0_D11	SPT0_BCLK	SPI1_SS
PC_13	SPI1_SEL2		SMC0_D12	SPT0_BFS	CNT0_DG
PC_14	SPI1_SEL3	SPI1_RDY	SMC0_D13	SPT0_BD0	CNT0_ZM
PC_15	SINC0_CLK0	UART1_RTS		SPT0_ATDV	TM1_ACLK3

Table 18. Signal Multiplexing for Port D

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function InputTap
PD_00	PWM0_SYNC		SMC0_A03		SYS_DSWAKE1
PD_01	PWM_TRIPA		SMC0_A04		

Table 19. Signal Multiplexing for Port E

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function InputTap
PE_00	PWM2_AH				
PE_01	PWM2_AL	UART4_RTS	SMC0_AMS1		
PE_02	PWM2_BH	TM1_TMR6	SMC0_AMS2		CPTMR0_IN0
PE_03	PWM2_BL	UART4_CTS	SMC0_A15		
PE_04	PWM2_CH	TM1_TMR4			CPTMR0_IN1
PE_05	PWM2_CL		SMC0_A14		
PE_06	PWM2_DH		SMC0_A11		
PE_07	PWM2_DL		SMC0_A12		
PE_08	PWM2_SYNC	UART3_RTS	SMC0_AMS3		TM1_ACLK5
PE_09	PWM1_SYNC	UART1_RX			TM1_ACI5
PE_10	PWM_TRIPB	UART1_TX			
PE_11	PWM_TRIPC		SMC0_A16		
PE_12	CAN1_RX		SMC0_ABE1		TM1_ACI0
PE_13	CAN1_TX		SMC0_ABE0		
PE_14	TM1_TMR0		SMC0_A05		
PE_15	TM1_TMR1		SMC0_A10		

Table 20. Signal Multiplexing for Port F

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function InputTap
PF_00	SINC0_D2		SMC0_A06		
PF_01	SINC0_D3		SMC0_A07		
PF_02	$\overline{\text{SPI1\_SEL4}}$		SMC0_A08		
PF_03	$\overline{\text{SPI1\_SEL6}}$		SMC0_A09	LBA0_PIN0	
PF_04	UART4_TX		SMC0_A13	LBA0_PIN1	
PF_05	UART4_RX	$\overline{\text{SPI1\_SEL5}}$		LBA0_PIN2	TM1_ACI6
PF_06	SPI1_D2	TM1_TMR5		LBA0_PIN3	CPTMR0_IN2
PF_07	SPI1_D3			LBA0_PIN4	
PF_08	$\overline{\text{SPI1\_SEL7}}$			LBA0_PIN5	SYS_DSWAKE2

ADSP-CM41xF DESIGNER QUICK REFERENCE

Table 21 provides a quick reference summary of pin related information for circuit board design. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The type column identifies the I/O type or supply type of the pin. The abbreviations used in this column are a (analog), s (supply), g (ground) and Input, Output, and InOut.
- The driver type column identifies the driver type used by the corresponding pin. The driver types are defined in the Output Drive Currents section of this data sheet.
- The int term column specifies the termination present when the processor is not in the reset state.
- The reset term column specifies the termination present when the processor is in the reset state.
- The reset drive column specifies the active drive on the signal when the processor is in the reset state.
- The power domain column specifies the power supply domain in which the signal resides.
- The description and notes column identifies any special requirements or characteristics for a signal. These recommendations apply whether or not the hardware block associated with the signal is featured on the product. If no special requirements are listed, the signal can be left unconnected if it is not used. For multiplexed general-purpose I/O pins, this column identifies the functions available on the pin.

Table 21. ADSP-CM41xF Designer Quick Reference

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
ADC_VIN_A0	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1 Notes: No notes
ADC_VIN_A1	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1 Notes: No notes
ADC_VIN_A2	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1 Notes: No notes
ADC_VIN_A3	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1 Notes: No notes
ADC_VIN_A4	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1[1] Notes: No notes
ADC_VIN_A5	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1[1] Notes: No notes
ADC_VIN_A6	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1[1] Notes: No notes
ADC_VIN_A7	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1[1] Notes: No notes
ADC_VIN_B0	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1 Notes: No notes
ADC_VIN_B1	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1 Notes: No notes
ADC_VIN_B2	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1 Notes: No notes
ADC_VIN_B3	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1 Notes: No notes
ADC_VIN_B4	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1[1] Notes: No notes
ADC_VIN_B5	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1[1] Notes: No notes
ADC_VIN_B6	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1[1] Notes: No notes

Table 21. ADSP-CM41xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
ADC_VIN_B7	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1[1] Notes: No notes
ADC_VIN_C0	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1 Notes: No notes
ADC_VIN_C1	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1 Notes: No notes
ADC_VIN_C2	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1 Notes: No notes
ADC_VIN_C3	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1 Notes: No notes
ADC_VIN_C4	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1[1] Notes: No notes
ADC_VIN_C5	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1[1] Notes: No notes
ADC_VIN_C6	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1[1] Notes: No notes
ADC_VIN_C7	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC1[1] Notes: No notes
ADC_VIN_D0	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC0 Notes: No notes
ADC_VIN_D1	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC0 Notes: No notes
ADC_VIN_D2	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC0 Notes: No notes
ADC_VIN_D3	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC0 Notes: No notes
ADC_VIN_D4	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC0 Notes: No notes
ADC_VIN_D5	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC0 Notes: No notes
ADC_VIN_D6	a	na	none	none	none	VDD_ANA	Desc: Channel n Single-Ended Analog Input for ADC0 Notes: No notes
BYP_A0	a	na	none	none	none	VDD_ANA	Desc: On-chip Analog Power Regulation Bypass Filter Node for ADC Notes: No notes
BYP_A1	a	na	none	none	none	VDD_ANA	Desc: On-chip Analog Power Regulation Bypass Filter Node for ADC Notes: No notes
BYP_A2	a	na	none	none	none	VDD_ANA	Desc: On-chip Analog Power Regulation Bypass Filter Node for ADC Notes: No notes
BYP_D0	a	na	none	none	none	VDD_EXT	Desc: On-chip Analog Power Regulation Bypass Filter Node for DAC Notes: No notes
COMP_OUT_A	a	OUT	none	none	none	VDD_ANA	Desc: Fast over-current protection comparator A output Notes: No notes
COMP_OUT_B	a	OUT	none	none	none	VDD_ANA	Desc: Fast over-current protection comparator B output Notes: No notes

Table 21. ADSP-CM41xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
COMP_OUT_C	a	OUT	none	none	none	VDD_ANA	Desc: Fast over-current protection comparator C output Notes: No notes
DAC0_VOUT	a	na	none	none	none	VDD_ANA	Desc: Analog Voltage Output 0 Notes: No notes
DNC	InOut	na	none	none	none		Desc: Do Not Connect Notes: No notes
DNC	InOut	na	none	none	none		Desc: Do Not Connect Notes: No notes
DNC	InOut	na	none	none	none		Desc: Do Not Connect Notes: No notes
DNC	InOut	na	none	none	none		Desc: Do Not Connect Notes: No notes
DNC	InOut	na	none	none	none		Desc: Do Not Connect Notes: No notes
DNC	InOut	na	none	none	none		Desc: Do Not Connect Notes: No notes
DNC	InOut	na	none	none	none		Desc: Do Not Connect Notes: No notes
DNC	InOut	na	none	none	none		Desc: Do Not Connect Notes: No notes
GND	g	na	none	none	none	VDD_EXT	Desc: Digital Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes

Table 21. ADSP-CM41xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground Notes: No notes
GND_ANA0	g	na	none	none	none	VDD_ANA	Desc: Analog Ground return for VDD_ANA0 Notes: No notes
GND_ANA1	g	na	none	none	none	VDD_ANA	Desc: Analog Ground return for VDD_ANA1 Notes: No notes
GND_ANA2	g	na	none	none	none	VDD_ANA	Desc: Analog Ground return for VDD_ANA2 Notes: No notes
GND_ANA3	g	na	none	none	none	VDD_ANA	Desc: Analog Ground return for VDD_ANA3 Notes: No notes
GND_ANA4_COMP	g	na	none	none	none	VDD_ANA	Desc: GND_COMP_ANA4 Notes: No notes
GND_ANA5_DAC	g	na	none	none	none	VDD_ANA	Desc: GND_DAC_ANA5 Notes: No notes
GND_REFCAP0	g	na	none	none	none	VDD_ANA	Desc: Ground return for REF_INOUT0 Notes: No notes
GND_REFCAP1	g	na	none	none	none	VDD_ANA	Desc: REFCAP1 Notes: No notes
GND_VREF0	g	na	none	none	none	VDD_ANA	Desc: Ground return for REF_BUFOUT[0] Notes: No notes
GND_VREF1	g	na	none	none	none	VDD_ANA	Desc: Ground return for REF_BUFOUT[1] Notes: No notes
GND_VREF2	g	na	none	none	none	VDD_ANA	Desc: GND_VREF2 Notes: No notes
JTG_TCK/SWCLK	Input	IN	pd	pd	none	VDD_EXT	Desc: JTAG Clock/Serial Wire Clock Notes: No notes
JTG_TDI	Input	IN	pu	pu	none	VDD_EXT	Desc: JTAG Serial Data In Notes: No notes
JTG_TDO/SWO	Output	OUT	pu	pu	none	VDD_EXT	Desc: JTAG Serial Data Out Notes: No notes
JTG_TMS/SWDIO	InOut	IO	pu	pu	none	VDD_EXT	Desc: JTAG Mode Select/Serial Wire Debug Data I/O Notes: No notes
$\overline{\text{JTG\_TRST}}$	Input	IN	pu	pu	none	VDD_EXT	Desc: JTAG Reset Notes: No notes

Table 21. ADSP-CM41xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PA_00	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTA Position 0 | SPI0 Slave Select Output 2 | TIMER0 Clock | SPI0 Slave Select Input Notes: No notes
PA_01	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTA Position 1 | SPI0 Ready | SPI0 Slave Select Output 3 | TIMER0 Alternate Capture Input 2 Notes: No notes
PA_02	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTA Position 2 | SPI0 Data 2 | SPI0 Slave Select Output 6 | UART0 Request to Send | TIMER0 Alternate Capture Input 3 Notes: No notes
PA_03	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTA Position 3 | SPI0 Data 3 | SPI0 Slave Select Output 7 | UART0 Clear to Send | TIMER0 Alternate Capture Input 4 Notes: No notes
PA_04	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTA Position 4 | UART0 Receive | TIMER0 Alternate Capture Input 0 Notes: No notes
PA_05	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTA Position 5 | UART0 Transmit | TIMER0 Alternate Clock 4 Notes: No notes
PA_06	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTA Position 6 | CAN0 Receive | SPI0 Slave Select Output 4 | TIMER0 Alternate Capture Input 1 Notes: No notes
PA_07	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTA Position 7 | CAN0 Transmit | SPI0 Slave Select Output 5 | TIMER0 Alternate Clock 2 Notes: No notes
PA_08	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTA Position 8 | SPI0 Clock | TIMER0 Alternate Clock 3 Notes: No notes
PA_09	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTA Position 9 | SPI0 Master Out, Slave In | TIMER0 Alternate Clock 0 Notes: No notes
PA_10	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTA Position 10 | SPI0 Master In, Slave Out | TIMER0 Alternate Clock 1 Notes: No notes
PA_11	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTA Position 11 | SPI0 Slave Select Output 1 | Deep Sleep Wakeup 3 Notes: No notes
PA_12	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTA Position 12 | TIMER0 Timer 0 Notes: No notes
PA_13	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTA Position13 | TIMER0 Timer 1 Notes: No notes
PB_00	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTB Position 0 | PWM0 Channel A High Side | SMC0 Asynchronous Ready Notes: No notes
PB_01	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTB Position 0 | PWM0 Channel A Low Side | SMC0 Write Enable Notes: No notes

Table 21. ADSP-CM41xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PB_02	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTB Position 2 | PWM0 Channel B High Side | SMC0 Output Enable Notes: No notes
PB_03	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTB Position 3 | PWM0 Channel B Low Side | SMC0 Read Enable Notes: No notes
PB_04	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTB Position 4 | PWM0 Channel C High Side | SMC0 Memory Select 0 Notes: No notes
PB_05	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTB Position 5 | PWM0 Channel C Low Side | SMC0 Data 0 Notes: No notes
PB_06	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTB Position 6 | PWM0 Channel D High Side | SMC0 Data 1 Notes: No notes
PB_07	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTB Position 7 | PWM0 Channel D Low Side | SMC0 Data 2 | UART3 Clear to Send Notes: No notes
PB_08	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTB Position 8 | CNT0 Output Divider A | PWM1 Channel A High Side | SMC0 Data 3 Notes: No notes
PB_09	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTB Position 9 | PWM1 Channel A Low Side | SMC0 Data 4 | SPORT0 Channel A Data 0 | UART2 Request to Send | CNT0 Count Up and Direction Notes: No notes
PB_10	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTB Position 10 | CNT0 Output Divider B | PWM1 Channel B High Side | SMC0 Data 5 Notes: No notes
PB_11	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTB Position 11 | PWM1 Channel B Low Side | SMC0 Data 6 Notes: No notes
PB_12	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTB Position 12 | PWM1 Channel C High Side | SMC0 Data 7 Notes: No notes
PB_13	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTB Position 13 | PWM1 Channel C Low Side | SMC0 Address 1 | TIMER1 Timer 2 Notes: No notes
PB_14	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTB Position 14 | PWM1 Channel D High Side | TIMER1 Timer 0 Notes: No notes
PB_15	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTB Position 15 | PWM1 Channel D Low Side | SMC0 Address 2 | TIMER1 Timer 1 Notes: No notes
PC_00	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTC Position 0 | TRACE0 Trace Clock | TIMER1 Alternate Clock 4 Notes: No notes
PC_01	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTC Position 1 | TRACE0 Trace Data 1 Notes: No notes

Table 21. ADSP-CM41xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PC_02	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTC Position 2 | LBA LBA data input or the logic output | TRACE0 Trace Data 3 Notes: No notes
PC_03	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTC Position 3 | TRACE0 Trace Data 0 Notes: No notes
PC_04	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTC Position 4 | LBA LBA data input or the logic output | TRACE0 Trace Data 2 Notes: No notes
PC_05	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTC Position 5 | SINC0 Data 0 | SMC0 Data 14 | SPORT0 Channel B Transmit Data Valid | UART1 Clear to Send | Deep Sleep Wakeup 0 Notes: No notes
PC_06	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTC Position 6 | SINC0 Data 1 | SMC0 Data 15 | SPORT0 Channel A Data 1 | UART2 Clear to Send | TIMER1 Clock Notes: No notes
PC_07	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTC Position 7 | UART3 Transmit Notes: No notes
PC_08	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTC Position 8 | UART3 Receive | TIMER1 Alternate Capture Input 2 Notes: No notes
PC_09	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTC Position 9 | SMC0 Data 8 | SPI1 Clock | SPORT0 Channel A Clock | UART2 Receive | TIMER1 Alternate Capture Input 4 Notes: No notes
PC_10	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTC Position 10 | SMC0 Data 9 | SPI1 Master In, Slave Out | SPORT0 Channel B Data 1 | TIMER1 Timer 3 Notes: No notes
PC_11	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTC Position 11 | SMC0 Data 10 | SPI1 Master Out, Slave In | SPORT0 Channel A Frame Sync | UART2 Transmit Notes: No notes
PC_12	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTC Position 12 | SMC0 Data 11 | SPI1 Slave Select Output 1 | SPORT0 Channel B Clock | TIMER1 Timer 7 | SPI1 Slave Select Input Notes: No notes
PC_13	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTC Position 13 | SMC0 Data 12 | SPI1 Slave Select Output 2 | SPORT0 Channel B Frame Sync | CNT0 Count Down and Gate Notes: No notes
PC_14	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTC Position 14 | SMC0 Data 13 | SPI1 Ready | SPI1 Slave Select Output 3 | SPORT0 Channel B Data 0 | CNT0 Count Zero Marker Notes: No notes
PC_15	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTC Position 15 | SINC0 Clock 0 | SPORT0 Channel A Transmit Data Valid | UART1 Request to Send | TIMER1 Alternate Clock 3 Notes: No notes
PD_00	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTD Position 0 | PWM0 PWMTMR Grouped | SMC0 Address 3 | Deep Sleep Wakeup 1 Notes: No notes

Table 21. ADSP-CM41xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PD_01	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTD Position 1 | SMC0 Address 4 | Muxed PWM Trip A signal Notes: No notes
PE_00	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTE Position 0 | PWM2 Channel A High Side Notes: No notes
PE_01	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTE Position 1 | PWM2 Channel A Low Side | SMC0 Memory Select 1 | UART4 Request to Send Notes: No notes
PE_02	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTE Position 2 | PWM2 Channel B High Side | SMC0 Memory Select 2 | TIMER1 Timer 6 | CPTMR0 Input Notes: No notes
PE_03	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTE Position 3 | PWM2 Channel B Low Side | SMC0 Address 15 | UART4 Clear to Send Notes: No notes
PE_04	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTE Position 4 | PWM2 Channel C High Side | TIMER1 Timer 4 | CPTMR0 Input Notes: No notes
PE_05	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTE Position 5 | PWM2 Channel C Low Side | SMC0 Address 14 Notes: No notes
PE_06	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTE Position 6 | PWM2 Channel D High Side | SMC0 Address 11 Notes: No notes
PE_07	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTE Position 7 | PWM2 Channel D Low Side | SMC0 Address 12 Notes: No notes
PE_08	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTE Position 8 | PWM2 PWMTMR Grouped | SMC0 Memory Select 3 | UART3 Request to Send | TIMER1 Alternate Clock 5 Notes: No notes
PE_09	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTE Position 9 | PWM1 PWMTMR Grouped | UART1 Receive | TIMER1 Alternate Capture Input 5 Notes: No notes
PE_10	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTE Position 10 | Muxed PWM Trip B signal | UART1 Transmit Notes: No notes
PE_11	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTE Position 11 | SMC0 Address 16 | Muxed PWM Trip C signal Notes: No notes
PE_12	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTE Position 12 | CAN1 Receive | SMC0 Byte Enable 1 | TIMER1 Alternate Capture Input 0 Notes: No notes
PE_13	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTE Position 13 | CAN1 Transmit | SMC0 Byte Enable 0 Notes: No notes
PE_14	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTE Position 14 | SMC0 Address 5 | TIMER1 Timer 0 Notes: No notes
PE_15	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTE Position 15 | SMC0 Address 10 | TIMER1 Timer 1 Notes: No notes

Table 21. ADSP-CM41xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PF_00	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTF Position 0 | SINC0 Data 2 | SMC0 Address 6 Notes: No notes
PF_01	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTF Position 1 | SINC0 Data 3 | SMC0 Address 7 Notes: No notes
PF_02	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTF Position 2 | SMC0 Address 8 | SPI1 Slave Select Output 4 Notes: No notes
PF_03	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTF Position 3 | LBA LBA data input or the logic output | SMC0 Address 9 | SPI1 Slave Select Output 6 Notes: No notes
PF_04	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTF Position 4 | LBA LBA data input or the logic output | SMC0 Address 13 | UART4 Transmit Notes: No notes
PF_05	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTF Position 5 | LBA LBA data input or the logic output | SPI1 Slave Select Output 5 | UART4 Receive | TIMER1 Alternate Capture Input 6 Notes: No notes
PF_06	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTF Position 6 | LBA LBA data input or the logic output | SPI1 Data 2 | TIMER1 Timer 5 | CPTMR0 Input Notes: No notes
PF_07	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTF Position 7 | LBA LBA data input or the logic output | SPI1 Data 3 Notes: No notes
PF_08	InOut	GPIO	pu or none	pu	none	VDD_EXT	Desc: PORTF Position 8 | LBA LBA data input or the logic output | SPI1 Slave Select Output 7 | Deep Sleep Wakeup 2 Notes: No notes
REFCAP0	a	na	none	none	none	VDD_ANA	Desc: Output of BandGap Generator Filter Node Notes: No notes
REFCAP1	a	na	none	none	none	VDD_ANA	Desc: Output of BandGap Generator Filter Node Notes: No notes
SYS_BMODE0	Input	IN	none	none	none	VDD_EXT	Desc: Boot Mode Control 0 Notes: No notes
SYS_CLKIN0	Input	AIN	none	none	none	VDD_EXT	Desc: Clock/Crystal Input Notes: No notes
SYS_CLKIN1	Input	AIN	none	none	none	VDD_EXT	Desc: Clock/Crystal Input Notes: No notes
SYS_CLKOUT	Output	OUT	none	none	L	VDD_EXT	Desc: Processor Clock Output Notes: No notes
$\overline{\text{SYS\_FAULT}}$	Output	IO	none	none	none	VDD_EXT	Desc: Fault Output Notes: No notes
$\overline{\text{SYS\_HWRST}}$	Input	IN	none	none	none	VDD_EXT	Desc: Processor Hardware Reset Control Notes: No notes
$\overline{\text{SYS\_NMI}}$	Input	IN	none	none	none	VDD_EXT	Desc: Non-maskable Interrupt Notes: No notes
$\overline{\text{SYS\_RESOUT}}$	Output	IO	none	none	L	VDD_EXT	Desc: Reset Output Notes: No notes
SYS_XTAL0	Input	AOUT	none	none	none	VDD_EXT	Desc: Crystal Output Notes: No notes

Table 21. ADSP-CM41xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
SYS_XTAL1	Input	AOUT	none	none	none	VDD_EXT	Desc: Crystal Output Notes: No notes
TWI0_SCL	InOut	TWI	none	none	none	VDD_EXT	Desc: TWI0 Serial Clock Notes: No notes
TWI0_SDA	InOut	TWI	none	none	none	VDD_EXT	Desc: TWI0 Serial Data Notes: No notes
VDD_ANA0	a	na	none	none	none	na	Desc: Analog Power Supply Voltage Notes: No notes
VDD_ANA1	a	na	none	none	none	na	Desc: Analog Power Supply Voltage Notes: No notes
VDD_COMP	a	na	none	none	none	na	Desc: Power supply for over current comparator Notes: No notes
VDD_EXT	s	na	none	none	none	na	Desc: External Voltage Domain Notes: No notes
VDD_INT	s	na	none	none	none	na	Desc: Internal Voltage Domain Notes: No notes
VREF0	s	na	none	none	none	na	Desc: Voltage reference ADC0 and DAC0 Notes: No notes
VREF1	s	na	none	none	none	na	Desc: Voltage reference ADC1 and Over Current Comparator DACs Notes: No notes
VREF2	s	na	none	none	none	na	Desc: Voltage reference ADC2 Notes: No notes
VREG_BASE	s	na	none	none	none	na	Desc: Voltage Regulator Base Node Notes: No notes

[1] For the ADSP-CM418F and ADSP-CM419F models, this analog input goes to ADC2 (see Figure 2).

SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DD_INT}[1]	Digital Internal Supply Voltage	$f_{CCLK} \le 240$ MHz	1.17	1.21	1.24	V
V_{DD_INT}[2]	Digital Internal Supply Voltage	$f_{CCLK} \le 240$ MHz	1.14	1.20	1.26	V
V_{DD_EXT}[3]	Digital External Supply Voltage		3.13	3.3	3.47	V
V_{DD_ANA0}, V_{DD_ANA1}, V_{DD_COMP}[3]	Analog Supply Voltage		3.13	3.3	3.47	V
V_{IH}[4]	High Level Input Voltage	V_{DD_EXT} = Maximum V	TBD			V
V_{IH_CLKIN}[5]	High Level Input Voltage	V_{DD_EXT} = Maximum V	TBD			V
V_{IHTWI}[6, 7]	High Level Input Voltage	V_{DD_EXT} = Maximum V	TBD		V_{BUSTWI}	V
V_{IL}[4]	Low Level Input Voltage	V_{DD_EXT} = Minimum V			TBD	V
V_{ILTWI}[6, 7]	Low Level Input Voltage	V_{DD_EXT} = Minimum V			TBD	V
T_J	Junction Temperature	$T_{AMBIENT}$ = TBD°C to TBD°C	–40		+125	°C

[1] When using the internal regulator.
[2] When using an external regulator.
[3] Must remain powered (even if the associated function is not used).
[4] Parameter values apply to all input and bidirectional signals except SYS_CLKIN1 and TWI signals.
[5] Parameter applies to SYS_CLKIN0 signal.
[6] Parameter applies to TWI_SDA and TWI_SCL.
[7] TWI signals are pulled up to V_{BUSTWI}. See Table 22.

Table 22. TWI_VSEL Selections and V_{DD_EXT}/V_{BUSTWI}

		V_{BUSTWI}			
TWI_VSEL Selections	V_{DD_EXT} Nominal	Min	Nominal	Max	Unit
TWI000[1]	3.30	3.13	3.30	3.47	V
TWI100	3.30	4.75	5.00	5.25	V

[1] Designs must comply with the V_{DD_EXT} and V_{BUSTWI} voltages specified for the default TWI_DT setting for correct JTAG boundary scan operation during reset.

Clock Related Operating Conditions

Table 23 describes the core clock, system clock, and peripheral clock timing requirements. The data presented in the tables applies to all speed grades found in the Pre Release Products except where expressly noted. Figure 19 provides a graphical representation of the various clocks and their available multiplier or divider values.

Table 23. Clock Related Operating Conditions

Parameter		Restriction	Min	Typ	Max	Unit
f_{PLLCLK}	PLL Clock Frequency		250		880	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$			240	MHz
f_{SYSCLK}	System Clock Frequency				100	MHz
f_{SCLK}	M0 Subsystem Clock Frequency				100	MHz
f_{OCLK}	Output Clock Frequency				50	MHz
f_{TCK}	JTG_TCK Frequency	$f_{TCK} \leq f_{SYSCLK}/2$			50	MHz
$f_{FOCPCLK}$	Fast Overcurrent Protection Clock		TBD	10	TBD	MHz
$f_{ADCC0\_ADC0\_CLK\_PROG}$	Programmed ADCC0 ADC0 Clock				50	MHz
$f_{ADCC1\_ADC1\_CLK\_PROG}$	Programmed ADCC1 ADC1 Clock				50	MHz
$f_{ADCC1\_ADC2\_CLK\_PROG}$	Programmed ADCC1 ADC2 Clock				50	MHz
$f_{DACC0\_DAC0\_CLK\_PROG}$	Programmed DACC0 DAC0 Clock				50	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Transmitting Data and Frame Sync				50	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Receiving Data and Frame Sync				50	MHz
$f_{SPTCLKEXT}$	External SPT Clock When Transmitting Data and Frame Sync[1, 2]	$f_{SPTCLKEXT} \leq f_{SYSCLK}$			50	MHz
$f_{SPTCLKEXT}$	External SPT Clock When Receiving Data and Frame Sync[1, 2]	$f_{SPTCLKEXT} \leq f_{SYSCLK}$			50	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Transmitting Data[1, 2]				50	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Receiving Data				50	MHz
$f_{SPICLKEXT}$	External SPI Clock When Transmitting Data[1, 2]	$f_{SPICLKEXT} \leq f_{SYSCLK}$			50	MHz
$f_{SPICLKEXT}$	External SPI Clock When Receiving Data[1, 2]	$f_{SPICLKEXT} \leq f_{SYSCLK}$			50	MHz
$f_{TMRCLKEXT}$	External TMR Clock	$f_{TMRCLKEXT} \leq f_{SYSCLK}/4$			25	MHz
$f_{SINCLKPROG}$	Programmed SINC Clock	$f_{SINCLKPROG} \leq f_{SYSCLK}/4$			20	MHz

[1] The maximum achievable frequency for any peripheral in external clock mode is dependent on being able to meet the setup and hold times in the AC timing specifications for that peripheral.

[2] The peripheral external clock frequency must also be less than or equal to f_{SYSCLK} that clocks the peripheral.

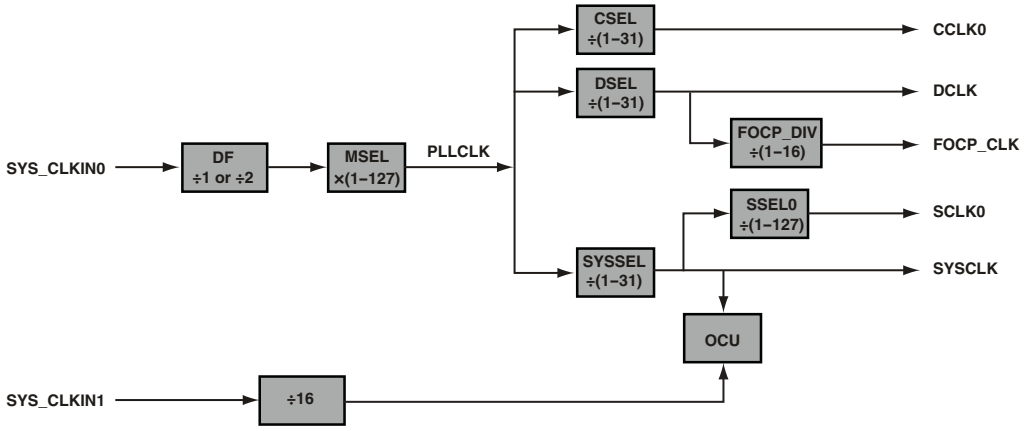


Figure 19. Clock Relationships and Divider Values

ELECTRICAL CHARACTERISTICS

Parameter		Conditions	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage	V_{DD_EXT} = minimum, I_{OH} = –0.5 mA	TBD			V
V_{OL}	Low Level Output Voltage	V_{DD_EXT} = minimum, I_{OL} = 2.0 mA			TBD	V
V_{OH_PWM}[1]	High Level Output Voltage	V_{DD_EXT} = minimum, I_{OH} = 10 mA			TBD	V
V_{OL_PWM}[1]	Low Level Output Voltage	V_{DD_EXT} = minimum, I_{OL} = 10 mA			TBD	V
V_{OLTWI}[2]	Low Level Output Voltage	V_{DD_EXT} = minimum, I_{OL} = 2.0 mA			TBD	V
V_{HVDEXT}	High Voltage Detection Threshold on V_{DD_EXT}	TBD	3.54	3.58	3.64	V
V_{HVDINT}	High Voltage Detection Threshold on V_{DD_INT}	Must use on-chip VREG	1.256	1.27	1.32	V
V_{LVDEXT_0}	Low Voltage Detection Threshold on V_{DD_EXT}	Ref Comparator Bit = 0	2.90	2.95	3.02	V
V_{LVDEXT_1}	Low Voltage Detection Threshold on V_{DD_EXT}	Ref Comparator Bit = 1	2.85	2.92	2.99	V
V_{LVDINT_0}[3]	Low Voltage Detection Threshold on V_{DD_INT}	Ref Comparator Bit = 0	1.09	1.11	1.154	V
V_{LVDINT_1}[3]	Low Voltage Detection Threshold on V_{DD_INT}	Ref Comparator Bit = 1	1.08	1.10	1.14	V
V_{LVREXT}	Low Voltage Reset Threshold on V_{DD_EXT}	TBD	TBD	2.5	TBD	V
V_{LVRINT}	Low Voltage Reset Threshold on V_{DD_INT}	TBD			1.05	V
I_{IH}[4]	High Level Input Current	V_{DD_EXT} = maximum, V_{IN} = V_{DD_EXT} V			TBD	µA
I_{IL}[4]	Low Level Input Current	V_{DD_EXT} = maximum, V_{IN} = 0 V			TBD	µA
I_{IH_PD}[5]	High Level Input Current	V_{DD_EXT} = maximum, V_{IN} = V_{DD_EXT} V			TBD	µA
I_{IL_PU}[6]	Low Level Input Current	V_{DD_EXT} = maximum, V_{IN} = 0 V			TBD	µA
I_{OZH}[7]	Three-State Leakage Current	V_{DD_EXT} = maximum, V_{IN} = V_{DD_EXT} V			TBD	µA
I_{OZHTWI}[2]	Three-State Leakage Current	V_{DD_EXT} = maximum, V_{IN} = $V_{BUSTWI(MAX)}$			TBD	µA
I_{OZL}[7]	Three-State Leakage Current	V_{DD_EXT} = maximum, V_{IN} = 0 V			TBD	µA
C_{IN}[8]	Input Capacitance	T_J = 25°C		TBD	TBD	pF
C_{IN_TWI}[9]	Input Capacitance	T_J = 25°C		TBD	TBD	pF
$I_{DD\_DEEPSLEEP}$[10]	V_{DD_INT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz f_{SCLK} = 0 MHz		TBD		mA
I_{DD_IDLE}	V_{DD_INT} Current in Idle	TBD		TBD		mA
I_{DD_TYP}	V_{DD_INT} Current	TBD		TBD		mA
I_{DD_INT}	V_{DD_INT} Current	f_{CCLK} > 0 MHz $f_{SCLK} \geq$ 0 MHz			TBD	mA
I_{DD_EXT}	V_{DD_EXT} Current				TBD	mA
I_{DD_ANA0}	V_{DD_ANA0} Current	TBD		TBD	TBD	mA
I_{VDD_ANA1}	V_{DD_ANA1} Current, 6-Way Sampling	TBD		TBD	TBD	mA
I_{VDD_ANA1}	V_{DD_ANA1} Current, 3-Way Sampling	TBD		TBD	TBD	mA
I_{VDD_COMP}	V_{DD_COMP} Current	TBD		TBD	TBD	mA

[1] Applies to PWM output pins only.
[2] Applies to bidirectional pins TWI_SCL and TWI_SDA.
[3] Must use on-chip VREG.
[4] Applies to input pins.
[5] Applies to signal JTG_TCK.
[6] Applies to signals JTG_TMS, $\overline{\text{JTG\_TRST}}$, and JTAG_TDI.
[7] Applies to three-statable pins.
[8] Applies to all signal except TWI signals.
[9] Applies to all TWI signals.
[10] See the ADSP-CM41x Mixed-Signal Control Processor with ARM Cortex-M4/ARM Cortex-M0 and 16-bit ADCs Hardware Reference for definition of deep sleep operating mode.

Total Power Dissipation (PD)

Total power dissipation is the sum of power dissipation for each V_{DD} domain, shown in the following equation.

$P_D = P_{D\_INT} + P_{D\_ANA} + P_{D\_EXT}$

where:

$P_{D\_INT} = V_{DD\_INT} \times I_{DD\_INT}$ —Internal voltage domain power dissipation

$P_{D\_ANA} = V_{DD\_ANA} \times I_{DD\_ANA}$—Analog 3.3 V voltage domain power dissipation

$P_{D\_EXT} = V_{DD\_EXT} \times I_{DD\_EXT}$ —Digital 3.3 V voltage domain power dissipation

Total External Power Dissipation (IDD_EXT)

There are three different items that contribute to the digital 3.3 V supply power dissipation: I/O switching, flash subsystem, and analog subsystem (digital portion), shown in the following equation.

$I_{DDEXT\_TOT} = I_{DDEXT\_IO} + I_{DDEXT\_FLASH} + I_{DDEXT\_ANA}$

where:

$I_{DDEXT\_IO/ANA}$ (mA) = Σ {$V_{DDEXT} \times C_L f/2 \times (O \times TR) \times U$}– *IO switching current*

The I/O switching current is the sum of the switching current for all of the enabled peripherals. For each peripheral the capacitive load of each pin in Farads (C_L), operating frequency in MHz (f), number of output pins (O), toggle ratio for each pin (TR), and peripheral utilization (U) are considered.

I_{DDEXT_FLASH} (mA) = *TBD*

Total Internal Power Dissipation (IDD_INT)

Total internal power dissipation for the processor subsystem has two components:

1. Static, including leakage current
2. Dynamic, due to transistors switching characteristics for each clock domain

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. The following equation describes the internal current consumption.

$$I_{DD\_INT\_TOT} = I_{DD\_INT\_CCLK\_DYN} + I_{DD\_INT\_SCLK\_DYN} + I_{DD\_INT\_DMA\_DR\_DYN} + I_{DD\_INT\_STATIC}$$

$I_{DD\_INT\_STATIC}$ is the sole contributor to the static power dissipation component and is specified as a function of voltage (V_{DD_INT}) and junction temperature (T_J) in Figure 20.

There are four different items that contribute to the dynamic power dissipation. These components fall into three broad categories: application dependent currents, clock currents, and data transmission currents.

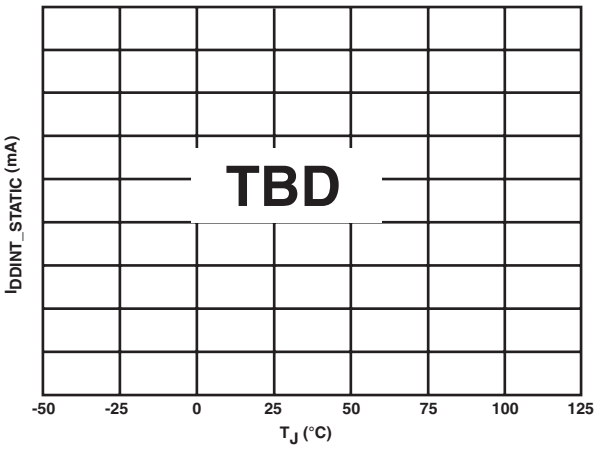


Figure 20. Static Current – $I_{DD\_DEEPSLEEP}$ (mA)

Application Dependent Current

The application dependent current includes the dynamic current in the core clock domain.

Core clock (CCLK) use is subject to an activity scaling factor (ASF) that represents application code running on the processor core and L1 memory (see Table 24). The ASF is combined with the CCLK frequency to calculate this portion.

$I_{DD\_INT\_CCLK\_DYN}$ (mA) = TBD × f_{CCLK} (MHz) × *ASF*

Table 24. Activity Scaling Factors (ASF)

I_{DD_INT} Power Vector	ASF
$I_{DD\text{-}PEAK}$	TBD
$I_{DD\text{-}COREMARK}$ (typical)	TBD
$I_{DD\text{-}IDLE}$	TBD

Clock Current

The dynamic clock currents provide the total power dissipated by all transistors switching in the clock paths. The power dissipated by each clock domain is dependent on voltage (V_{DD_INT}), operating frequency, and a unique scaling factor.

$I_{DD\_INT\_SCLK\_DYN}$ (mA) = TBD × f_{SCLK} (MHz)

Data Transmission Current

The data transmission current represents the power dissipated when moving data throughout the system via direct memory access (DMA). This current is proportional to the data rate. The calculation is performed by adding the data rate (MB/s) of each DMA and core driven access to peripherals and L2/external memory. This number is then multiplied by a coefficient. The following equation provides an estimate of all data transmission current.

$I_{DD\_INT\_DMA\_DR\_DYN}$ (mA) = TBD × *data rate* (MB/s) × V_{DD_INT} (V)

ADC/DAC/VOLTAGE REFERENCE/COMPARATOR SPECIFICATIONS

ADC Specifications –ADC0, ADC1, ADC2

Typical values assume V_{DD_ANA0}, V_{DD_ANA1}, V_{DD_COMP} = 3.3 V, V_{REF} = 2.5 V, T_J = 25°C.

Parameter	Min	Typ	Max	Unit	Conditions
ANALOG INPUT					ADC_VIN_XX (7 + 24 analog inputs)
Requirement					
Single-Ended Input Voltage Range	0		3.0	V	
Characteristic					
DC Leakage Current		±0.01	±1	µA	
Input Resistance		100 K		ohms	
Input Capacitance		TBD		pF	Condition 1 = track
		TBD		pF	Condition 2 = hold

ADC Specifications –ADC1, ADC2

Typical values assume V_{DD_ANA0}, V_{DD_ANA1}, V_{DD_COMP} = 3.3 V, V_{REF} = 2.5 V, T_J = 25°C.

Parameter	Min	Typ	Max	Unit	Conditions
DYNAMIC PERFORMANCE					ADC1, ADC2 – ADC_VIN_AX, BX, CX (24 analog inputs
Throughput Rate			6/2.72	Samples/µs	3-way sampling
Throughput Rate			6/1.36	Samples/µs	6-way sampling
AC ACCURACY					ADC1, ADC2 – ADC_VIN_AX, BX, CX (24 analog inputs
Characteristic					
Signal-to-Noise Ratio (SNR)		81		dB	
Signal-to-(Noise + Distortion) Ratio (SINAD)		80.5		dB	
Total Harmonic Distortion (THD)		–94		dB	
Spurious-Free Dynamic Range (SFDR)		TBD		dB	
Dynamic Range		81		dB	
Effective Number of Bits (ENOB)		13		Bits	
Channel-to-Channel Isolation		–95		dB	Any channel pair referenced on same ADC. Selected channel = 1 kHz, Unselected channel = 10 kHz
Intermodulation Distortion					f_{IN1} = 1 kHz, f_{IN2} = 10 kHz
Second Order Terms		TBD		dB	
Third Order Terms		TBD		dB	
STATIC PERFORMANCE					
DC ACCURACY					ADC1, ADC2 – ADC_VIN_AX, BX, CX (24 analog inputs)
Characteristic					
Resolution		16		Bits	No missing codes, natural binary coding
Differential Non-Linearity (DNL)	–0.99		+1.0	LSB	
Integral Non-Linearity (INL)		±4		LSB	
Offset Error		TBD		LSB	
Offset Error Match		TBD		LSB	
Offset Temperature Drift		TBD		ppm/°C	

Parameter	Min	Typ	Max	Unit	Conditions
Gain Error		TBD		LSB	
Gain Error Match		TBD		LSB	
Gain Temperature Drift		TBD		ppm/°C	

ADC Specifications –ADC0

Typical values assume V_{DD_ANA0}, V_{DD_ANA1}, V_{DD_COMP} = 3.3 V, V_{REF} = 2.5 V, T_J = 25°C.

Parameter	Min	Typ	Max	Unit	Conditions
DYNAMIC PERFORMANCE					ADC0 – ADC_VIN_DX (7 analog inputs)
Throughput					
Conversion Rate			2	MSPS	
AC ACCURACY					ADC0 – ADC_VIN_DX (7 analog inputs)
Characteristic					
Signal-to-Noise Ratio (SNR)		69		dB	
Signal-to-(Noise + Distortion) Ratio (SINAD)		68.5		dB	
Total Harmonic Distortion (THD)		–82		dB	
Spurious-Free Dynamic Range (SFDR)		83		dB	
Dynamic Range		TBD		dB	$V_{IN} = V_{REF}/2$ (DC)
Effective Number of Bits (ENOB)		9.8		Bits	
Channel-to-Channel Isolation		–95		dB	Any channel pair referenced on same ADC. Selected channel = 1 kHz, Unselected channel = 10 kHz
Intermodulation Distortion					f_{IN1} = 1 kHz, f_{IN2} = 10 kHz
Second Order Terms		TBD		dB	
Third Order Terms		TBD		dB	
STATIC PERFORMANCE					
DC ACCURACY					ADC0 – ADC_VIN_DX (7 analog inputs)
Characteristic					
Resolution		14		Bits	No missing codes, natural binary coding
Differential Non-Linearity (DNL)	–0.99		+1.0	LSB	
Integral Non-Linearity (INL)		TBD		LSB	
Offset Error		TBD		LSB	
Offset Error Match		TBD		LSB	Channel-to-channel, within one ADC
Offset Temperature Drift		TBD		ppm/°C	
Gain Error		TBD		LSB	
Gain Error Match		TBD		LSB	
Gain Temperature Drift		TBD		ppm/°C	

DAC Specifications

Typical values assume V_{DD_ANA0}, V_{DD_ANA1}, V_{DD_COMP} = 3.3 V, V_{REF} = 2.5 V, T_J = 25°C.

Parameter	Min	Typ	Max	Unit	Conditions
ANALOG OUTPUT					DAC0_VOUT
Characteristic					
Output Voltage Range		0 to 3.0		V	
Output Impedance		TBD		ohms	Normal operation
		TBD		ohms	DAC at full scale
		TBD		ohms	DAC at zero scale
Update Rate			TBD	kHz	
Short Circuit Current to GND		30		mA	DAC at full scale
Short Circuit Current to V_{DD}		30		mA	DAC at zero scale
STATIC PERFORMANCE					
DC ACCURACY					RL = 500 ohms, CL = 100 pF
Characteristic					
Resolution		12		Bits	
Differential Non-Linearity (DNL)		±0.99		LSB	Guaranteed monotonic
Integral Non-Linearity (INL)		±2		LSB	
Offset Error		TBD		mV	Measured at code TBD
Offset Error Match		TBD		% FSR	% of full scale, measured at code 0xFFF

Voltage Reference Specifications

Typical values assume V_{DD_ANA0}, V_{DD_ANA1}, V_{DD_COMP} = 3.3 V, V_{REF} = 2.5 V, T_J = 25°C.

Parameter	Min	Typ	Max	Unit	Conditions
VOLTAGE REFERENCE (OUTPUT MODE)					V_{REF0}, V_{REF1}, V_{REF2}
Characteristic					
Output Voltage		2.5		V	
Output Impedance		0.5	1.0	ohms	
Temperature Coefficient		15		ppm/°C	$T_{JUNCTION}$ = –40°C to +125°C

Comparator Specifications

Typical values assume V_{DD_ANA0}, V_{DD_ANA1}, V_{DD_COMP} = 3.3 V, V_{REF} = 2.5 V, T_J = 25°C.

Parameter	Min	Typ	Max	Unit	Conditions
COMPARATOR INPUT					ADC_VIN_A0, ADC_VIN_B0, ADC_VIN_C0
Requirement					
Input Range	0		3	V	Signals below 0.075 V are considered always above lowest threshold; signals above 2.925 V are considered always below highest threshold. This feature allows for selectively disabling the comparator by programming the thresholds to 0 V or 3 V respectively.
Characteristic					
Propagation Delay			200	ns	
Voltage Output Low			0.4	V	I_{OL} = 5 ma (OPEN DRAIN)
Comparator to Comparator Matching			14	mV	COMP_OUT_A, COMP_OUT_B, COMP_OUT_C
Hysteresis		0.3%		%	
Offset			TBD	mV	

ADC Typical Performance Characteristics

V_{DD_ANA} = 3.3 V, V_{REF} = 2.5 V, $T_{JUNCTION}$ = 25°C unless otherwise noted.1

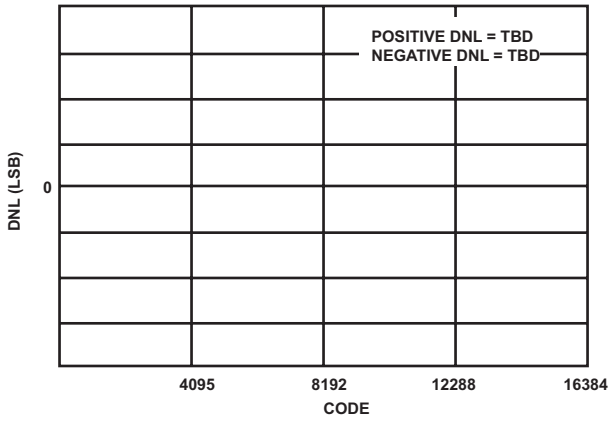


Figure 21. DNL vs. Code

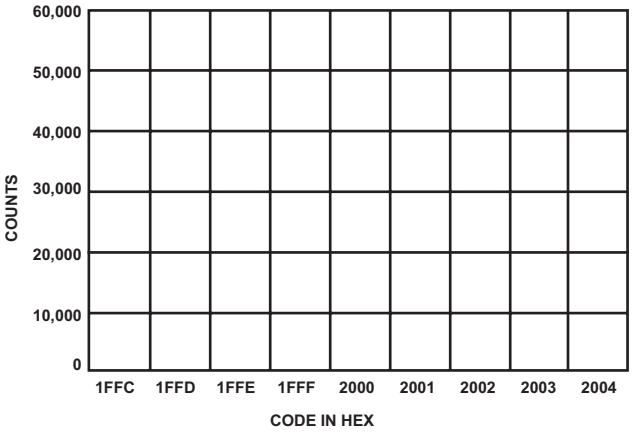


Figure 22. Histogram of DC Input at Code Center (Internal Reference)

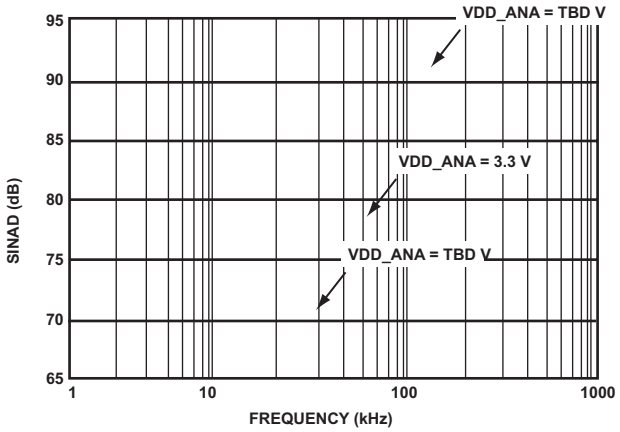


Figure 23. SINAD vs. Frequency, 0 to 3.0 V

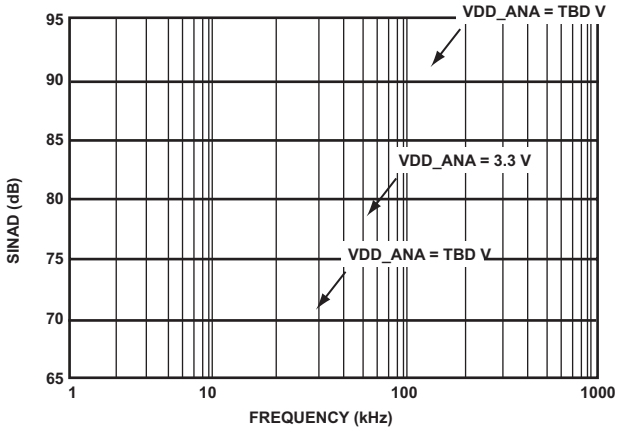


Figure 24. SINAD vs. Frequency, 0 to 1.5 V

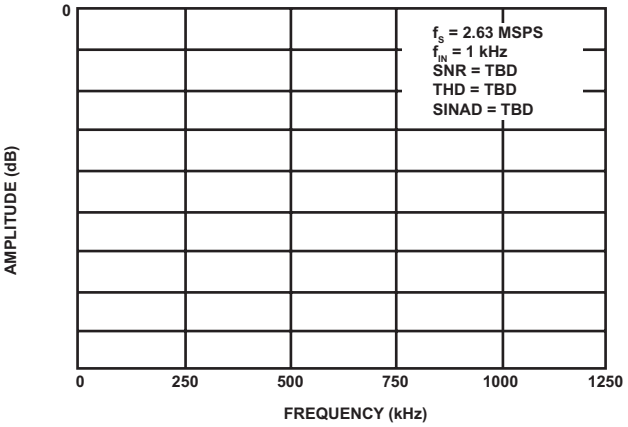


Figure 25. FFT Plot (Internal Reference)

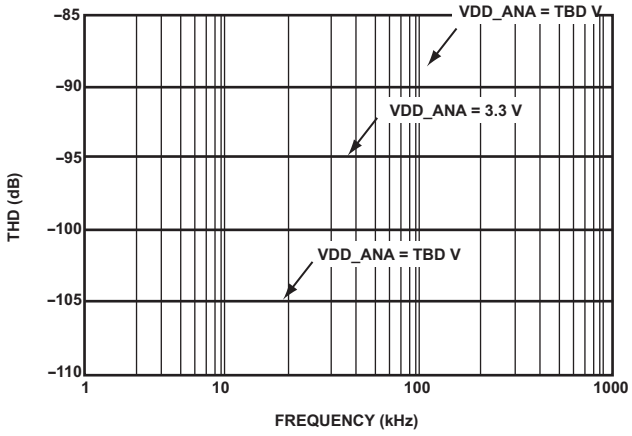


Figure 26. THD vs. Frequency, 0 to 2.5 V

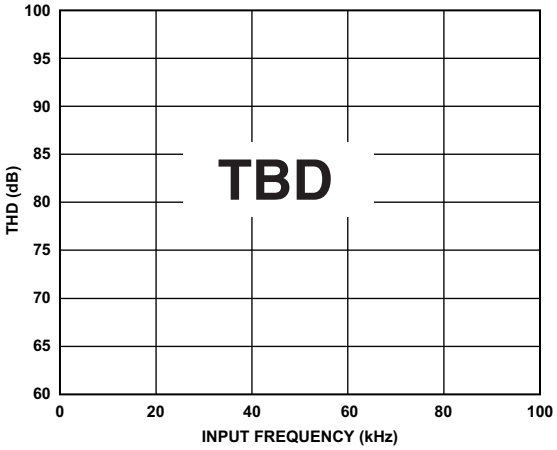


Figure 27. THD vs. Frequency, 0 to 1.25 V

DAC Typical Performance Characteristics

V_{DD_ANA} = 3.3 V, V_{REF} = 2.5 V, $T_{JUNCTION}$ = 25°C unless otherwise noted.

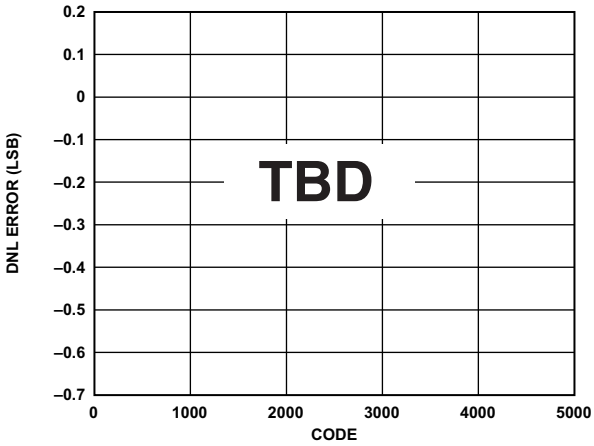


Figure 28. DAC DNL Error vs. Code

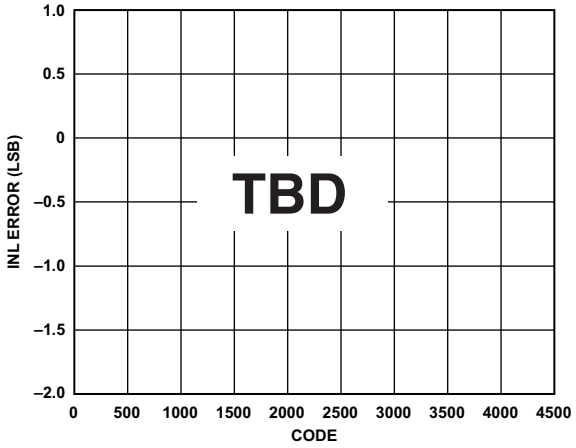


Figure 29. DAC INL Error vs. Code

FLASH SPECIFICATIONS

Parameter	Min	Typ	Max	Unit	Conditions
Endurance[1]	10,000			cycles	
Erase Time	100	112	130	ms	
Program Time	10	12	20	µs	
Data Retention[2]	10			years	Tj = 85°C

[1] Endurance is qualified to 10,000 program/erase cycles as per AEC-Q100-005 at -40°C, 25°C, and 125°C.
[2] Retention lifetime equivalent at junction temperature = 85°C as per JESD22-A117. Retention lifetime derates with junction temperature.

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 25 may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 25. Absolute Maximum Ratings

Parameter	Rating
Internal Supply Voltage (V_{DD_INT})	–0.33 V to +1.32 V
External (I/O) Supply Voltage (V_{DD_EXT})[1]	–0.33 V to +3.63 V
External (I/O) Supply Voltage (V_{DD_EXT})[2]	V_{DD_INT} – 0.5 V to +3.63 V
Analog Supply Voltage (V_{DD_ANA0}, V_{DD_ANA1}, V_{DD_COMP})	–0.33 V to +3.63 V
Digital Input Voltage[3]	–0.33 V to +3.63 V
TWI Digital Input Voltage[3,4]	–0.33 V to +5.50 V
Digital Output Voltage Swing	–0.33 V to V_{DD_EXT} + 0.5 V
Analog Input Voltage[5]	–0.33 V to +3.63 V
I_{OH}/I_{OL} Current per Signal [6]	TBD
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	+125° C

[1] Applies when V_{DD_INT} = 0 V.
[2] Applies when V_{DD_INT} is > 0 V.
[3] Applies only when V_{DD_EXT} is within specifications. When V_{DD_EXT} is outside specifications, the range is V_{DD_EXT} ± 0.2 V.
[4] Applies to TWI_SCL and TWI_SDA.
[5] Applies only when V_{DD_ANA} is within specification. When V_{DD_ANA} is outside specifications, the range is V_{DD_ANA} ± 0.2 V.
[6] Limit applies to constant current loads only. Transient switching currents are allowed to exceed this value.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 30 and Table 26 provides details about package branding for the processors. For a complete listing of product availability, see Pre Release Products.

Figure 30. Product Information on Package[1]

[1] Exact brand may differ, depending on package type.

Table 26. Package Brand Information

Brand Key	Field Description
ADSP-CM41xF	Product name
t	Temperature range
pp	Package type
Z	RoHS compliant designation
cc	See Ordering Guide section
vvvvvv.x	Assembly lot code
n	Product revision
yyww	Date code

TIMING SPECIFICATIONS

Specifications are subject to change without notice.

Clock and Reset Timing

Table 27, Table 28, and Figure 31 describe clock and reset operations related to the clock generation unit (CGU) and reset control unit (RCU). Per the CCLK, SCLK, and OCLK timing specifications in Table 23, combinations of SYS_CLKIN and clock multipliers must not select clock rates in excess of the maximum instruction rate of the processor.

Table 27. Clock and Reset Timing (SYS_CLKIN0)

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
f_{CKIN0}	SYS_CLKIN0 Frequency (Using a Crystal)[1, 2, 3]	20	50	MHz
f_{CKIN0}	SYS_CLKIN0 Frequency (Using a Crystal Oscillator)[1, 2, 3]	20	60	MHz
t_{CKINL0}	SYS_CLKIN0 Low Pulse[1]	TBD		ns
t_{CKINH0}	SYS_CLKIN0 High Pulse[1]	TBD		ns
t_{WRST}	$\overline{\text{SYS\_HWRST}}$ Asserted Pulse Width Low and SYS_CLKIN0 is Stable and Within Specification[4]	11		µs

[1] Applies to PLL bypass mode and PLL non bypass mode.
[2] The t_{CKIN0} period equals $1/f_{CKIN0}$ (see Figure 31).
[3] If the CGU_CTL.DF bit is set, the minimum f_{CKIN0} specification is 40 MHz.
[4] Applies after power-up sequence is complete. See Table 29 and Figure 32 for power-up reset timing.

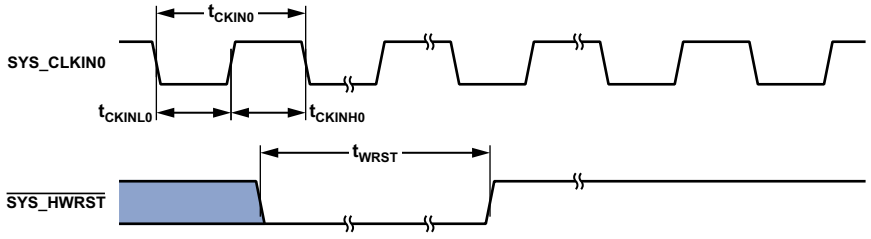


Figure 31. Clock and Reset Timing

Table 28. Clock and Reset Timing (SYS_CLKIN1)

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirement				
f_{CKIN1}	SYS_CLKIN1 Frequency (Using a Crystal)	12	30	MHz

Power-Up Reset Timing

Table 29 and Figure 32 show the relationship between power supply startup and processor reset timing, related to the CGU and the RCU. In Figure 32, $V_{DD\_SUPPLIES}$ are V_{DD_INT}, V_{DD_EXT}, V_{DD_ANA0}, and V_{DD_ANA1}.

Table 29. Power-Up Reset Timing

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{SYS\_HWRST}$ and $\overline{JTG\_TRST}$ Deasserted after V_{DD_INT}, V_{DD_EXT}, V_{DD_ANA0}, V_{DD_ANA1}, and SYS_CLKIN are Stable and within Specification	11		µs

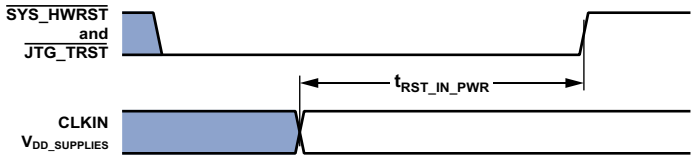


Figure 32. Power-Up Reset Timing

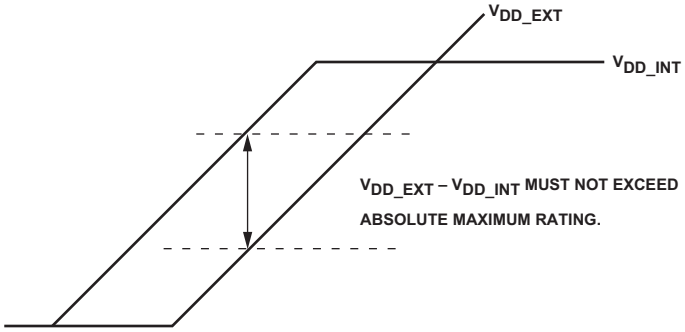


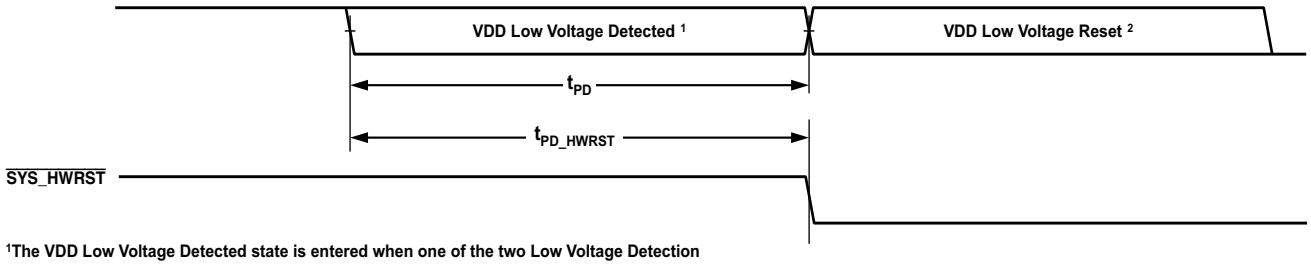
Figure 33. Power-Up Timing

Power-Down Timing

The power-down timing requirement ensures proper shutdown of the flash banks. The voltage monitoring unit (VMU) starts the flash shutdown when the low voltage detection threshold is reached on V_{DD_EXT} or V_{DD_INT}. Once the low voltage detection has been triggered, both the V_{DD_EXT} and V_{DD_INT} supplies must remain above the low voltage reset threshold for the specified time in order for the flash to complete its shutdown process.

Table 30. Power-Down Reset Timing

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{PD}	Power-Down Time Between Low Voltage Detect and Low Voltage Reset	22		µs
t_{PD_HWRST}	Power-Down Time Between Low Voltage Detect and $\overline{SYS\_HWRST}$ Assertion	22		µs



[1]The VDD Low Voltage Detected state is entered when one of the two Low Voltage Detection thresholds is triggered: (a) if VDD_EXT drops below VLVDEXT or (b) if VDD_INT drops below VLVDINT.
[2]The VDD Low Voltage Reset state is entered when one of the two Low Voltage Reset thresholds is triggered: (a) if VDD_EXT drops below VLVREXT or (b) if VDD_INT drops below VLVRINT.

Figure 34. Power-Down Timing

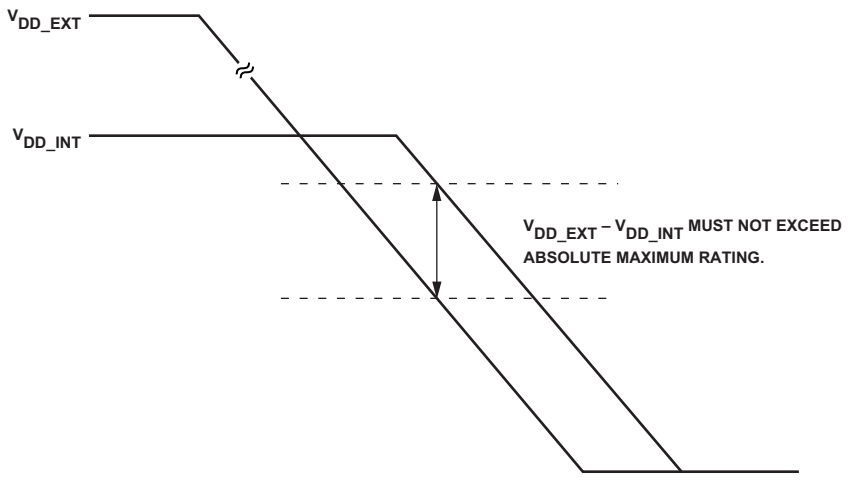


Figure 35. Power-Down V_{DD_EXT} and V_{DD_INT} Relationship

Asynchronous Read

Table 31 and Figure 36 show asynchronous memory read timing, related to the SMC.

Table 31. Asynchronous Read (BxMODE = b#00)

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
$t_{SDATARE}$	DATA in Setup Before $\overline{SMC0\_ARE}$ High	10.8		ns
$t_{HDATARE}$	DATA in Hold After $\overline{SMC0\_ARE}$ High	0		ns
$t_{DARDYARE}$	SMC0_ARDY Valid After $\overline{SMC0\_ARE}$ Low[1, 2]		(RAT – 2.5) × t_{SCLK} – 17.5	ns
Switching Characteristics				
$t_{ADDRARE}$	SMC0_Ax/$\overline{SMC0\_AMSx}$ Assertion Before $\overline{SMC0\_ARE}$ Low[3]	(PREST + RST + PREAT) × t_{SCLK} – 3		ns
t_{AOEARE}	$\overline{SMC0\_AOE}$ Assertion Before $\overline{SMC0\_ARE}$ Low	(RST + PREAT) × t_{SCLK} – 3		ns
t_{HARE}	Output[4] Hold After $\overline{SMC0\_ARE}$ High[5]	RHT × t_{SCLK} –2		ns
t_{WARE}	$\overline{SMC0\_ARE}$ Active Low Width[6]	RAT × t_{SCLK} – 2		ns
$t_{DAREARDY}$	$\overline{SMC0\_ARE}$ High Delay After SMC0_ARDY Assertion[1]	2.5 × t_{SCLK}	3.5 × t_{SCLK} + 17.5	ns

[1] SMC0_BxCTL.ARDYEN bit = 1.
[2] RAT value set using the SMC_BxTIM.RAT bits.
[3] PREST, RST, and PREAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.RST bits, and the SMC_BxETIM.PREAT bits.
[4] Output signals are SMC0_Ax, $\overline{SMC0\_AMS}$, $\overline{SMC0\_AOE}$.
[5] RHT value set using the SMC_BxTIM.RHT bits.
[6] SMC0_BxCTL.ARDYEN bit = 0.

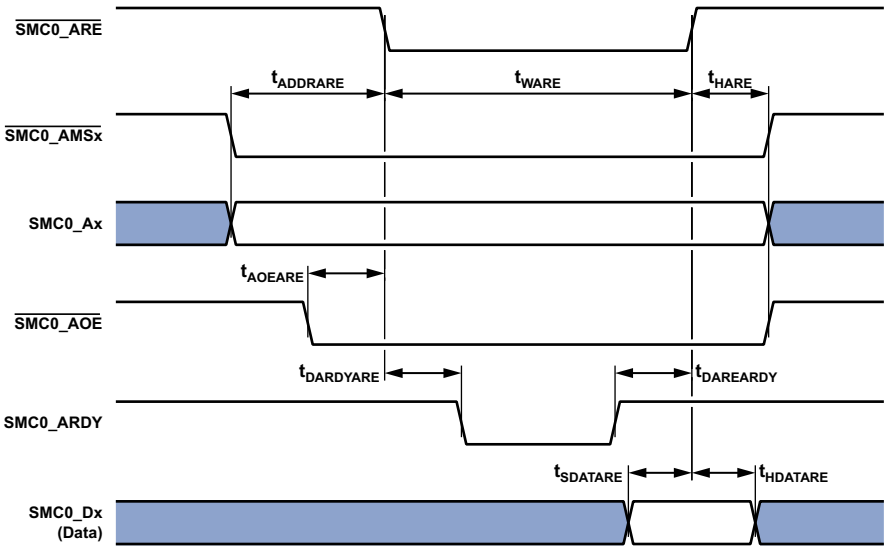


Figure 36. Asynchronous Read

Asynchronous Flash Read

Table 32 and Figure 37 show asynchronous flash memory read timing, related to the SMC.

Table 32. Asynchronous Flash Read

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
t_{AMSADV}	SMC0_Ax (Address)/$\overline{\text{SMC0\_AMSx}}$ Assertion Before $\overline{\text{SMC0\_AOE}}$ Low[1]	PREST × t_{SCLK} – 2		ns
t_{WADV}	$\overline{\text{SMC0\_AOE}}$ Active Low Width[2]	RST × t_{SCLK} – 3		ns
$t_{DADVARE}$	$\overline{\text{SMC0\_ARE}}$ Low Delay From $\overline{\text{SMC0\_AOE}}$ High[3]	PREAT × t_{SCLK} – 3		ns
t_{HARE}	Output[4] Hold After $\overline{\text{SMC0\_ARE}}$ High[5]	RHT × t_{SCLK} – 2		ns
t_{WARE}[6]	$\overline{\text{SMC0\_ARE}}$ Active Low Width[7]	RAT × t_{SCLK} – 2		ns

[1] PREST value set using the SMC_BxETIM.PREST bits.
[2] RST value set using the SMC_BxTIM.RST bits.
[3] PREAT value set using the SMC_BxETIM.PREAT bits.
[4] Output signals are SMC0_Ax, $\overline{\text{SMC0\_AMS}}$.
[5] RHT value set using the SMC_BxTIM.RHT bits.
[6] SMC0_BxCTL.ARDYEN bit = 0.
[7] RAT value set using the SMC_BxTIM.RAT bits.

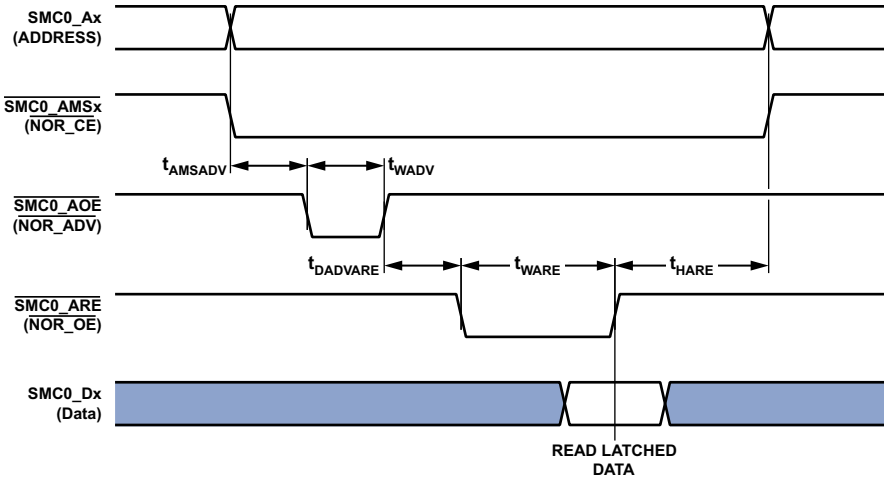


Figure 37. Asynchronous Flash Read

Asynchronous Page Mode Read

Table 33 and Figure 38 show asynchronous memory page mode read timing, related to the SMC.

Table 33. Asynchronous Page Mode Read

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
t_{AV}	SMC0_Ax (Address) Valid for First Address Minimum Width[1]	(PREST + RST + PREAT + RAT) × t_{SCLK} – 2		ns
t_{AV1}	SMC0_Ax (Address) Valid for Subsequent SMC0_Ax (Address) Minimum Width	PGWS × t_{SCLK} – 2		ns
t_{WADV}	$\overline{\text{SMC0\_AOE}}$ Active Low Width[2]	RST × t_{SCLK} – 3		ns
t_{HARE}	Output[3] Hold After $\overline{\text{SMC0\_ARE}}$ High[4]	RHT × t_{SCLK} – 2		ns
t_{WARE}[5]	$\overline{\text{SMC0\_ARE}}$ Active Low Width[6]	RAT × t_{SCLK} – 2		ns

[1] PREST, RST, PREAT and RAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.RST bits, SMC_BxETIM.PREAT bits, and the SMC_BxTIM.RAT bits.
[2] RST value set using the SMC_BxTIM.RST bits.
[3] Output signals are SMC0_Ax, $\overline{\text{SMC0\_AMSx}}$.
[4] RHT value set using the SMC_BxTIM.RHT bits.
[5] SMC_BxCTL.ARDYEN bit = 0.
[6] RAT value set using the SMC_BxTIM.RAT bits.

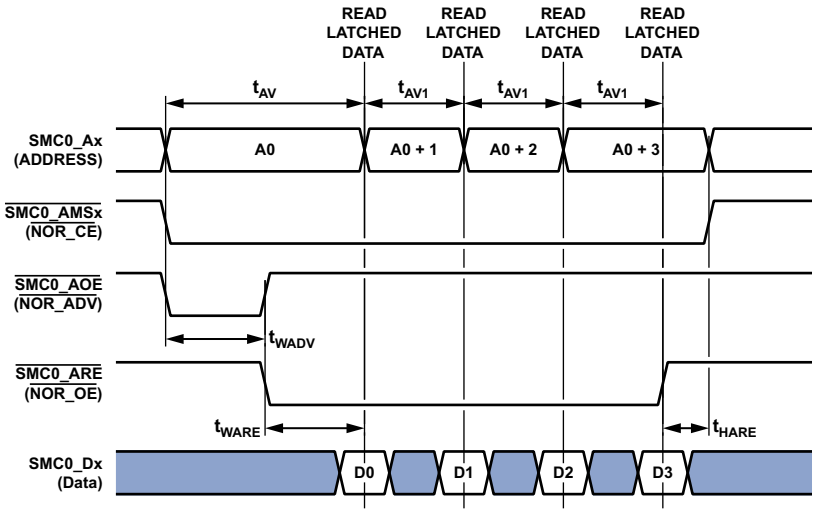


Figure 38. Asynchronous Page Mode Read

Asynchronous Write

Table 34 and Figure 39 show asynchronous memory write timing, related to the SMC.

Table 34. Asynchronous Memory Write (BxMODE = b#00)

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirement				
$t_{DARDYAWE}$[1]	SMC0_ARDY Valid After $\overline{\text{SMC0\_AWE}}$ Low[2]		(WAT – 2.5) × t_{SCLK} – 17.5	ns
Switching Characteristics				
t_{ENDAT}	DATA Enable After $\overline{\text{SMC0\_AMSx}}$ Assertion	–3		ns
t_{DDAT}	DATA Disable After $\overline{\text{SMC0\_AMSx}}$ Deassertion		4	ns
t_{AMSAWE}	SMC0_Ax/$\overline{\text{SMC0\_AMSx}}$ Assertion Before $\overline{\text{SMC0\_AWE}}$ Low[3]	(PREST + WST + PREAT) × t_{SCLK} – 6.4		ns
t_{HAWE}	Output[4] Hold After $\overline{\text{SMC0\_AWE}}$ High[5]	WHT × t_{SCLK} – 2		ns
t_{WAWE}[6]	$\overline{\text{SMC0\_AWE}}$ Active Low Width[2]	WAT × t_{SCLK} – 2		ns
$t_{DAWEARDY}$[1]	$\overline{\text{SMC0\_AWE}}$ High Delay After SMC0_ARDY Assertion	2.5 × t_{SCLK}	3.5 × t_{SCLK} + 17.5	ns

[1] SMC_BxCTL.ARDYEN bit = 1.
[2] WAT value set using the SMC_BxTIM.WAT bits.
[3] PREST, WST, PREAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.WST bits, SMC_BxETIM.PREAT bits, and the SMC_BxTIM.RAT bits.
[4] Output signals are DATA, SMC0_Ax, $\overline{\text{SMC0\_AMSx}}$, $\overline{\text{SMC0\_ABEx}}$.
[5] WHT value set using the SMC_BxTIM.WHT bits.
[6] SMC_BxCTL.ARDYEN bit = 0.

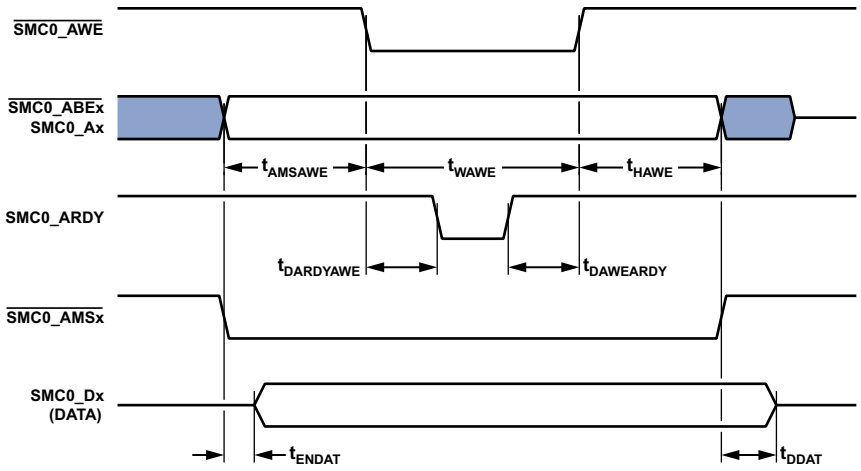


Figure 39. Asynchronous Write

Asynchronous Flash Write

Table 35 and Figure 40 show asynchronous flash memory write timing, related to the SMC.

Table 35. Asynchronous Flash Write

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
t_{AMSADV}	SMC0_Ax/$\overline{\text{SMC0\_AMSx}}$ Assertion Before $\overline{\text{SMC0\_AOE}}$ Low[1]		PREST × t_{SCLK} – 2	ns
$t_{DADVAWE}$	$\overline{\text{SMC0\_AWE}}$ Low Delay From $\overline{\text{SMC0\_AOE}}$ High[2]		PREAT × t_{SCLK} – 6.2	ns
t_{WADV}	$\overline{\text{SMC0\_AOE}}$ Active Low Width[3]		WST × t_{SCLK} – 3	ns
t_{HAWE}	Output[4] Hold After $\overline{\text{SMC0\_AWE}}$ High[5]		WHT × t_{SCLK} – 2	ns
t_{WAWE}[6]	$\overline{\text{SMC0\_AWE}}$ Active Low Width[7]		WAT × t_{SCLK} – 2	ns

[1] PREST value set using the SMC_BxETIM.PREST bits.
[2] PREAT value set using the SMC_BxETIM.PREAT bits.
[3] WST value set using the SMC_BxTIM.WST bits.
[4] Output signals are DATA, SMC0_Ax, $\overline{\text{SMC0\_AMSx}}$.
[5] WHT value set using the SMC_BxTIM.WHT bits.
[6] SMC_BxCTL.ARDYEN bit = 0.
[7] WAT value set using the SMC_BxTIM.WAT bits.

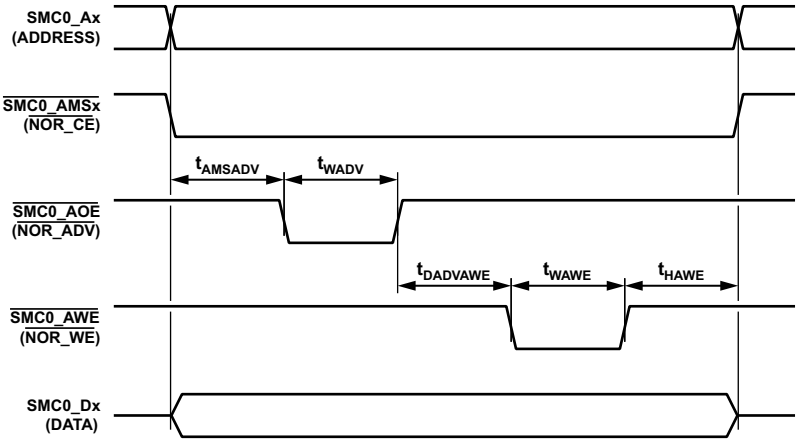


Figure 40. Asynchronous Flash Write

All Accesses

Table 36 describes timing that applies to all memory accesses, related to the SMC.

Table 36. All Accesses

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Switching Characteristic				
t_{TURN}	$\overline{\text{SMC0\_AMSx}}$ Inactive Width		(IT + TT) × t_{SCLK} – 2	ns

Serial Ports (SPORT)

To determine whether a device is compatible with the SPORT at clock speed n, the following specifications must be confirmed: frame sync delay and frame sync setup and hold; data delay and data setup and hold; and serial clock (SPTx_CLK) width. In Figure 43 through Figure 44, either the rising edge or the falling edge of SPTx_CLK (external or internal) can be used as the active sampling edge.

When externally generated, the SPORT clock is called $f_{SPTCLKEXT}$:

$$t_{SPTCLKEXT} = \frac{1}{f_{SPTCLKEXT}}$$

When internally generated, the programmed SPORT clock ($f_{SPTCLKPROG}$) frequency in MHz is set by the following equation where CLKDIV is a field in the SPORT_DIV register that can be set from 0 to 65535:

$$f_{SPTCLKPROG} = \frac{f_{SCLK1}}{(CLKDIV + 1)}$$

$$t_{SPTCLKPROG} = \frac{1}{f_{SPTCLKPROG}}$$

Table 37. Serial Ports—External Clock

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{SFSE}	Frame Sync Setup Before SPT_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[1]	2		ns
t_{HFSE}	Frame Sync Hold After SPT_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[1]	2.7		ns
t_{SDRE}	Receive Data Setup Before Receive SPT_CLK[1]	2		ns
t_{HDRE}	Receive Data Hold After SPT_CLK[1]	2.7		ns
t_{SCLKW}	SPT_CLK Width[2]	$0.5 \times t_{SPTCLKEXT} - 1$		ns
t_{SPTCLK}	SPT_CLK Period[2]	$t_{SPTCLKEXT} - 1$		ns
Switching Characteristics				
t_{DFSE}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in either Transmit or Receive Mode)[3]		14.5	ns
t_{HOFSE}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in either Transmit or Receive Mode)[3]	2		ns
t_{DDTE}	Transmit Data Delay After Transmit SPT_CLK[3]		15	ns
t_{HDTE}	Transmit Data Hold After Transmit SPT_CLK[3]	2		ns

[1] Referenced to sample edge.

[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPT_CLK. For the external SPT_CLK maximum frequency, see the $f_{SPTCLKEXT}$ specification in Table 23.

[3] Referenced to drive edge.

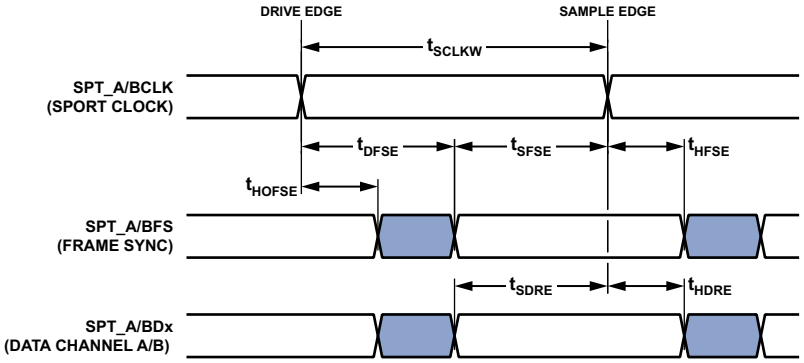


Figure 41. Serial Ports—Data Receive/External Clock

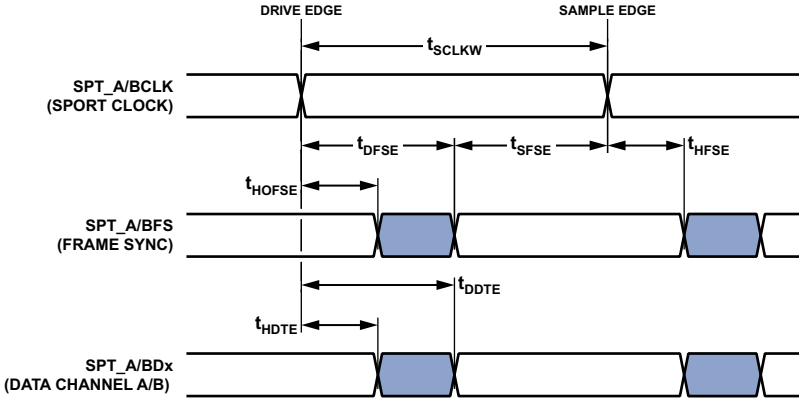


Figure 42. Serial Ports—Data Transmit/External Clock

Table 38. Serial Ports—Internal Clock

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{SFSI}	Frame Sync Setup Before SPT_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[1]	14		ns
t_{HFSI}	Frame Sync Hold After SPT_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[1]	–0.5		ns
t_{SDRI}	Receive Data Setup Before SPT_CLK[1]	4		ns
t_{HDRI}	Receive Data Hold After SPT_CLK[1]	1.5		ns
Switching Characteristics				
t_{DFSI}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2]		3.5	ns
t_{HOFSI}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2]	–1.5		ns
t_{DDTI}	Transmit Data Delay After SPT_CLK[2]		3.5	ns
t_{HDTI}	Transmit Data Hold After SPT_CLK[2]	–1.5		ns
t_{SCLKIW}	SPT_CLK Width[3]	$0.5 \times t_{SPTCLKPROG} - 1$		ns
t_{SPTCLK}	SPT_CLK Period[3]	$t_{SPTCLKPROG} - 1$		ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.
[3] See Table 23 for details on the minimum period that can be programmed for $f_{SPTCLKPROG}$.

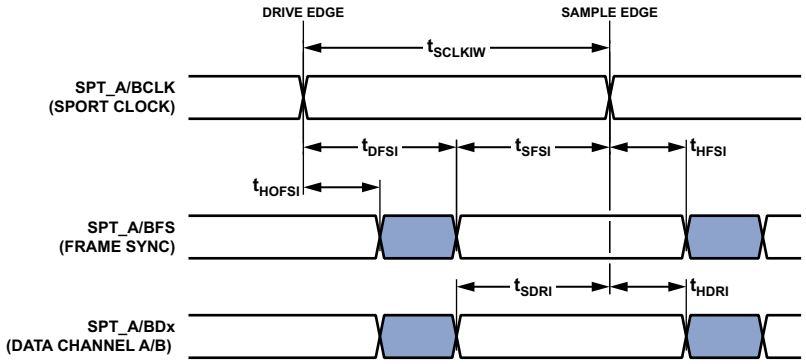


Figure 43. Serial Ports—Data Receive/Internal Clock

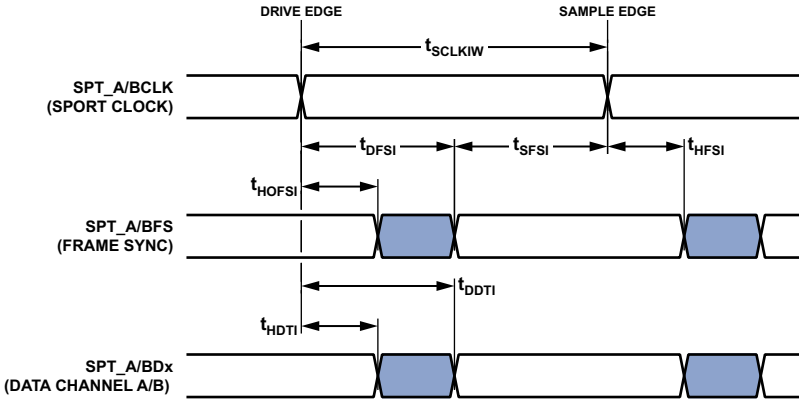


Figure 44. Serial Ports—Data Transmit/Internal Clock

Table 39. Serial Ports—Enable and Three-State

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
t_{DDTEN}	Data Enable from External Transmit SPT_CLK[1]	1		ns
t_{DDTTE}	Data Disable from External Transmit SPT_CLK[1]		14	ns
t_{DDTIN}	Data Enable from Internal Transmit SPT_CLK[1]	–1		ns
t_{DDTTI}	Data Disable from Internal Transmit SPT_CLK[1]		2.8	ns

[1] Referenced to drive edge.

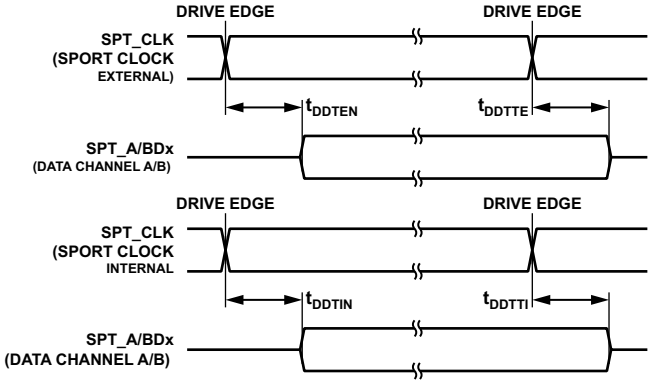


Figure 45. Serial Ports—Enable and Three-State

The SPT_TDV output signal becomes active in SPORT multichannel mode. During transmit slots (enabled with active channel selection registers) the SPT_TDV is asserted for communication with external devices.

Table 40. Serial Ports—TDV (Transmit Data Valid)

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
t_{DRDVEN}	Data Valid Enable Delay from Drive Edge of External Clock[1]	1		ns
t_{DFDVEN}	Data Valid Disable Delay from Drive Edge of External Clock[1]		14	ns
t_{DRDVIN}	Data Valid Enable Delay from Drive Edge of Internal Clock[1]	–1		ns
t_{DFDVIN}	Data Valid Disable Delay from Drive Edge of Internal Clock[1]		3.5	ns

[1] Referenced to drive edge.

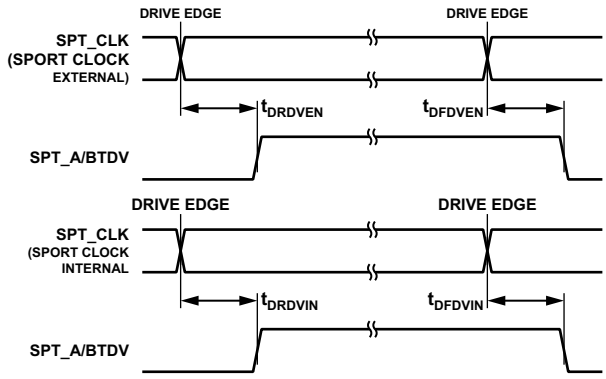


Figure 46. Serial Ports—Transmit Data Valid Internal and External Clock

Table 41. Serial Ports—External Late Frame Sync

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
$t_{DDTLFSE}$	Data and Data Valid Enable Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0[1]		15	ns
$t_{DDTENFS}$	Data Enable for MCE = 1, MFD = 0[1]	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified as well as standard serial mode, and MCE = 1, MFD = 0.

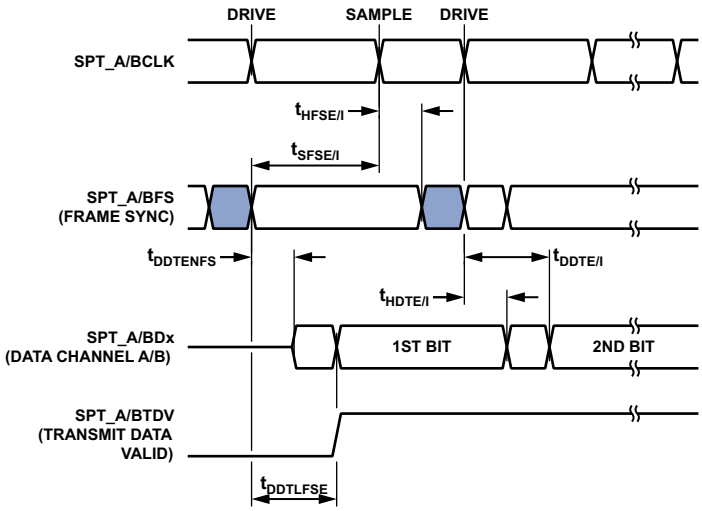


Figure 47. External Late Frame Sync

SPI Port—Master Timing

Table 42 and Figure 48 describe SPI port master operations.

When internally generated, the programmed SPI clock ($f_{SPICLKPROG}$) frequency in MHz is set by the following equation where BAUD is a field in the SPI_CLK register that can be set from 0 to 65535:

$$f_{SPICLKPROG} = \frac{f_{SCLK}}{(BAUD + 1)}$$

$$t_{SPICLKPROG} = \frac{1}{f_{SPICLKPROG}}$$

Note that

- In dual-mode data transmit, the SPI_MISO signal is also an output.
- In quad-mode data transmit, the SPI_MISO, SPI_D2, and SPI_D3 signals are also outputs.
- In dual-mode data receive, the SPI_MOSI signal is also an input.
- In quad-mode data receive, the SPI_MOSI, SPI_D2, and SPI_D3 signals are also inputs.

Table 42. SPI Port—Master Timing

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SPI_CLK Edge (Data Input Setup)	3.75		ns
t_{HSPIDM}	SPI_CLK Sampling Edge to Data Input Invalid	1.3		ns
Switching Characteristics				
t_{SDSCIM}	$\overline{\text{SPI\_SEL}}$ low to First SPI_CLK Edge for CPHA = 1[1]	[t_{SCLK} – 2] or [18]		ns
	$\overline{\text{SPI\_SEL}}$ low to First SPI_CLK Edge for CPHA = 0[1]	[1.5 × t_{SCLK} – 2] or [13]		ns
t_{SPICHM}	SPI_CLK High Period [2]	0.5 × $t_{SPICLKPROG}$ – 1.5		ns
t_{SPICLM}	SPI_CLK Low Period [2]	0.5 × $t_{SPICLKPROG}$ – 1.5		ns
t_{SPICLK}	SPI_CLK Period[2]	$t_{SPICLKPROG}$ – 1.5		ns
t_{HDSM}	Last SPI_CLK Edge to $\overline{\text{SPI\_SEL}}$ High for CPHA = 1[1]	[1.5 × t_{SCLK} –2] or [13]		ns
	Last SPI_CLK Edge to $\overline{\text{SPI\_SEL}}$ High for CPHA = 0[1]	[t_{SCLK} –2] or [18]		ns
t_{SPITDM}	Sequential Transfer Delay[1, 3]	[t_{SCLK} – 1] or [19]		ns
$t_{DDSPIDM}$	SPI_CLK Edge to Data Out Valid (Data Out Delay)		2.6	ns
$t_{HDSPIDM}$	SPI_CLK Edge to Data Out Invalid (Data Out Hold)	–1.5		ns

[1] Whichever is greater.
[2] See Table 23 for details on the minimum period that may be programmed for $t_{SPICLKPROG}$.
[3] Applies to sequential mode with STOP ≥ 1.

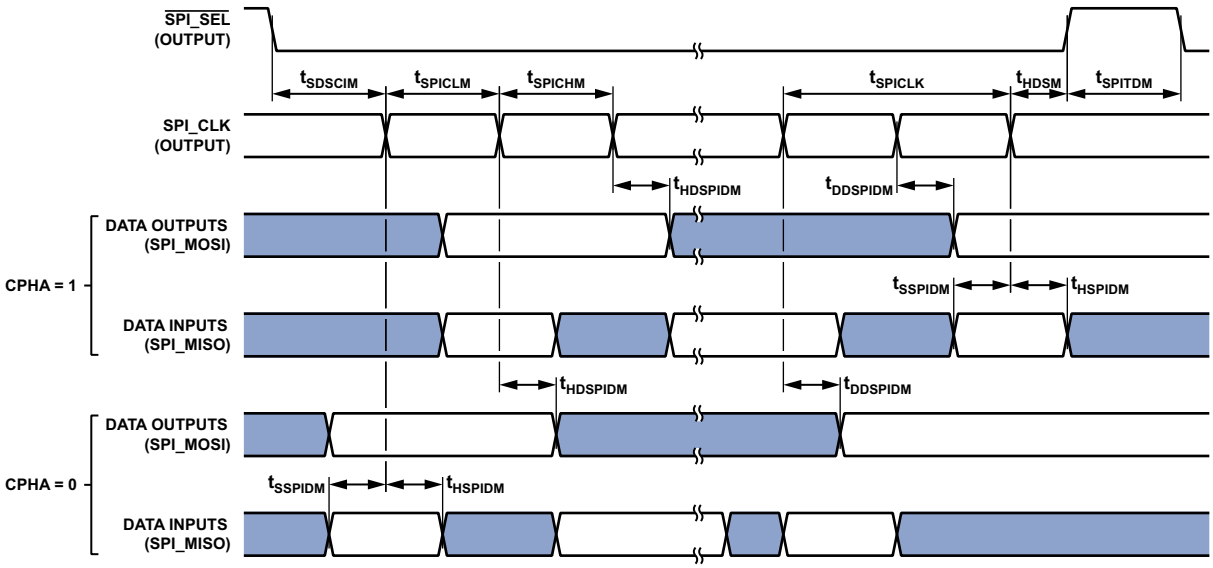


Figure 48. SPI Port—Master Timing

SPI Port—Slave Timing

Table 43 and Figure 49 describe SPI port slave operations. Note that

- In dual-mode data transmit, the SPI_MOSI signal is also an output.
- In quad-mode data transmit, the SPI_MOSI, SPI_D2, and SPI_D3 signals are also outputs.
- In dual-mode data receive, the SPI_MISO signal is also an input.
- In quad-mode data receive, the SPI_MISO, SPI_D2, and SPI_D3 signals are also inputs.
- In SPI slave mode, the SPI clock is supplied externally and is called $f_{SPICLKEXT}$:

$$t_{SPICLKEXT} = \frac{1}{f_{SPICLKEXT}}$$

Table 43. SPI Port—Slave Timing

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{SPICHS}	SPI_CLK High Period [1]	$0.5 \times t_{SPICLKEXT} - 1$		ns
t_{SPICLS}	SPI_CLK Low Period [1]	$0.5 \times t_{SPICLKEXT} - 1$		ns
t_{SPICLK}	SPI_CLK Period[1]	$t_{SPICLKEXT} - 1$		ns
t_{HDS}	Last SPI_CLK Edge to $\overline{\text{SPI\_SS}}$ Not Asserted	5		ns
t_{SPITDS}	Sequential Transfer Delay	$t_{SPICLK} - 1$		ns
t_{SDSCI}	$\overline{\text{SPI\_SS}}$ Assertion to First SPI_CLK Edge	10.5		ns
t_{SSPID}	Data Input Valid to SPI_CLK Edge (Data Input Setup)	2		ns
t_{HSPID}	SPI_CLK Sampling Edge to Data Input Invalid	2		ns
Switching Characteristics				
t_{DSOE}	$\overline{\text{SPI\_SS}}$ Assertion to Data Out Active	0	14	ns
t_{DSDHI}	$\overline{\text{SPI\_SS}}$ Deassertion to Data High Impedance	0	12.5	ns
t_{DDSPID}	SPI_CLK Edge to Data Out Valid (Data Out Delay)		14	ns
t_{HDSPID}	SPI_CLK Edge to Data Out Invalid (Data Out Hold)	0		ns

[1] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPI_CLK. For the external SPI_CLK ideal maximum frequency see the $t_{SPICLKEXT}$ specification in Table 23.

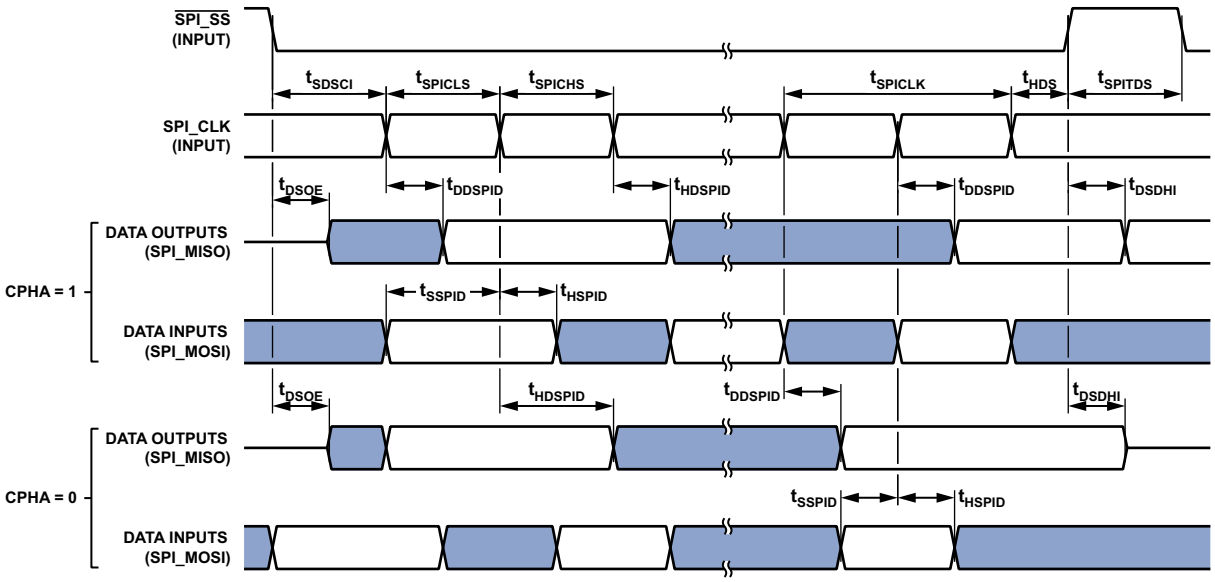


Figure 49. SPI Port—Slave Timing

SPI Port—SPI_RDY Slave Timing

Table 44. SPI Port—SPI_RDY Slave Timing

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
$t_{DSPISCKRDYSR}$	SPI_RDY Deassertion from Last Input SPI_CLK Edge in Slave Mode Receive	$3 \times t_{SCLK}$	$4 \times t_{SCLK} + 10$	ns
$t_{DSPISCKRDYST}$	SPI_RDY Deassertion from Last Input SPI_CLK Edge in Slave Mode Transmit	$4 \times t_{SCLK}$	$5 \times t_{SCLK} + 10$	ns

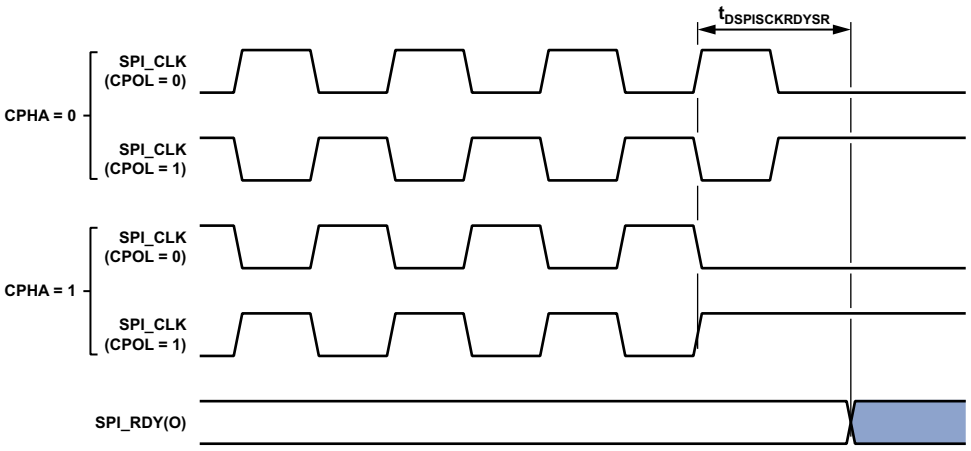


Figure 50. SPI_RDY Deassertion from Valid Input SPI_CLK Edge in Slave Mode Receive (FCCH = 0)

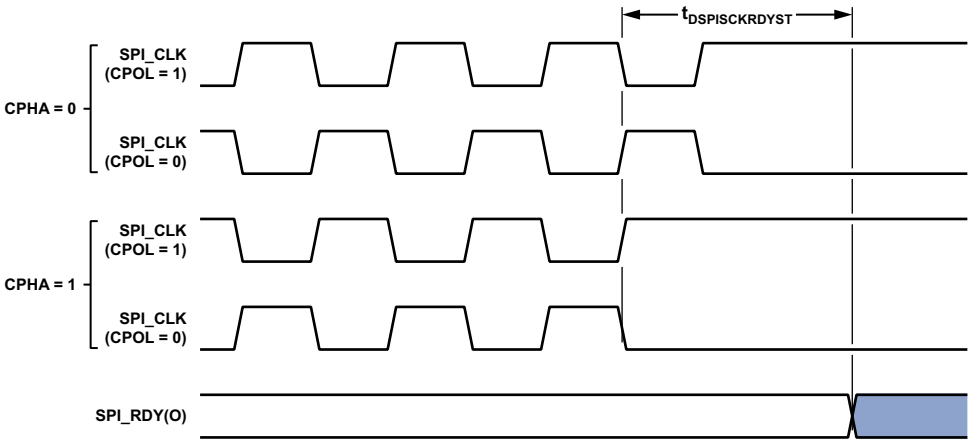


Figure 51. SPI_RDY Deassertion from Valid Input SPI_CLK Edge in Slave Mode Transmit (FCCH = 1)

SPI Port—Open Drain Mode (ODM) Timing

In Figure 52 and Figure 53, the outputs can be SPI_MOSI SPI_MISO, SPI_D2, and/or SPI_D3 depending on the mode of operation.

Table 45. SPI Port ODM Master Mode

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
$t_{HDSPIODMM}$	SPI_CLK Edge to High Impedance from Data Out Valid	–3		ns
$t_{DDSPIODMM}$	SPI_CLK Edge to Data Out Valid from High Impedance		6	ns

Table 46. SPI Port—ODM Slave Mode

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
$t_{HDSPIODMS}$	SPI_CLK Edge to High Impedance from Data Out Valid	0		ns
$t_{DDSPIODMS}$	SPI_CLK Edge to Data Out Valid from High Impedance		11	ns

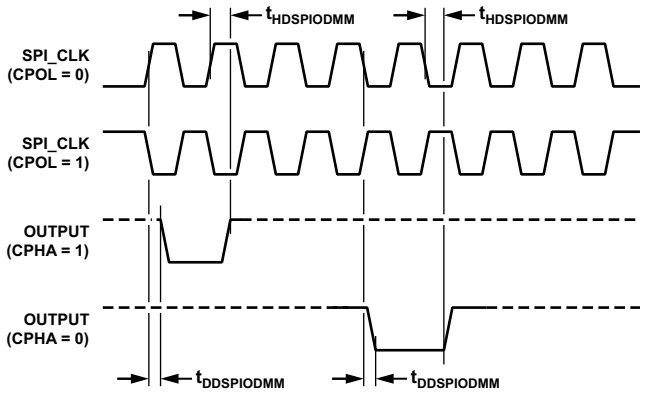


Figure 52. ODM Master Mode

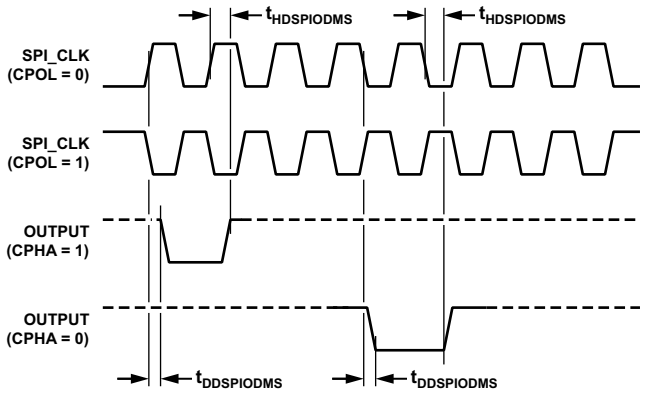


Figure 53. ODM Slave Mode

SPI Port—SPI_RDY Master Timing

SPI_RDY is used to provide flow control. CPOL and CPHA are configuration bits in the SPIx_CTL register, while LEADX, LAGX, and STOP are configuration bits in the SPIx_DLY register.

Table 47. SPI Port—SPI_RDY Master Timing

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
$t_{SRDYSCKM0}$	Minimum Setup Time for SPI_RDY De-assertion in Master Mode Before Last Valid SPI_CLK Edge of Valid Data Transfer to Block Subsequent Transfer with CPHA = 0	$(2 + 2 \times BAUD^{1}) \times t_{SCLK} + 10$		ns
$t_{SRDYSCKM1}$	Minimum Setup Time for SPI_RDY De-assertion in Master Mode Before Last Valid SPI_CLK Edge of Valid Data Transfer to Block Subsequent Transfer with CPHA = 1	$(2 + 2 \times BAUD^{1}) \times t_{SCLK} + 10$		ns
Switching Characteristics				
$t_{SRDYSCKM}$	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA/CPOL = 0 and BAUD = 0 (STOP, LEAD, LAG = 0)	$4.5 \times t_{SCLK}$	$5.5 \times t_{SCLK} + 10$	ns
	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA/CPOL = 1 and BAUD = 0 (STOP, LEAD, LAG = 0)	$4 \times t_{SCLK}$	$5 \times t_{SCLK} + 10$	ns
	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA/CPOL = 0 and BAUD ≥ 1 (STOP, LEAD, LAG = 0)	$(1 + 1.5 \times BAUD^{1}) \times t_{SCLK}$	$(2 + 2.5 \times BAUD^{1}) \times t_{SCLK} + 10$	ns
	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA/CPOL = 1 and BAUD ≥ 1 (STOP, LEAD, LAG = 0)	$(1 + 1 \times BAUD^{1}) \times t_{SCLK}$	$(2 + 2 \times BAUD^{1}) \times t_{SCLK} + 10$	ns

[1] BAUD value set using the SPI_CLK.BAUD bits. BAUD value = SPI_CLK.BAUD bits + 1.

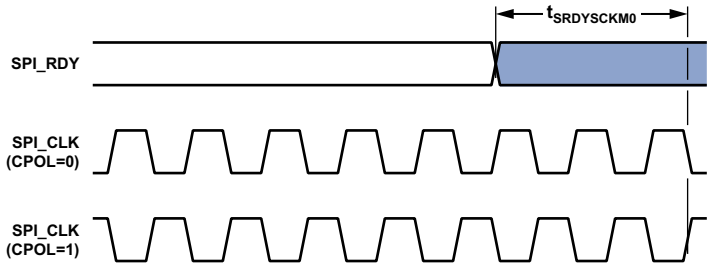


Figure 54. SPI_RDY Setup Before SPI_CLK with CPHA = 0

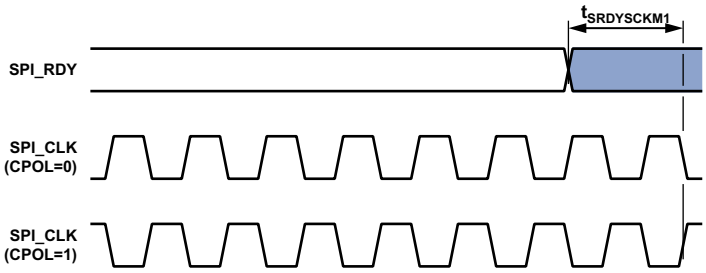


Figure 55. SPI_RDY Setup Before SPI_CLK with CPHA = 1

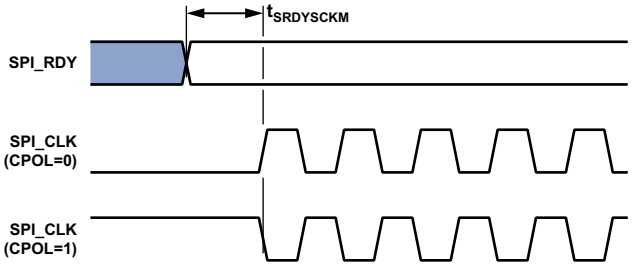


Figure 56. SPI_CLK Switching Diagram after SPI_RDY Assertion, CPHA = x

General-Purpose I/O Port Timing

Table 48 and Figure 57 describe I/O timing, related to the general-purpose ports (PORT).

Table 48. General-Purpose Port Timing

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirement				
t_{WFI}	General-Purpose I/O Port Pin Input Pulse Width	$2 \times t_{SCLK}$		ns

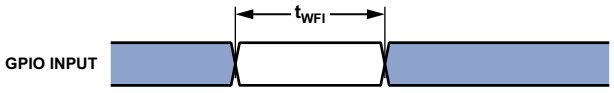


Figure 57. General-Purpose Port Timing

GPIO Timer Cycle Timing

Table 49, Table 50, and Figure 58 describe timer expired operations related to the general-purpose timer (TIMER). The input signal is asynchronous in Width Capture Mode and External Clock Mode and has an absolute maximum input frequency of $f_{SCLK}/4$ MHz. The Width Value value is the timer period assigned in the TMx_TMRn_WIDTH register and can range from 1 to $2^{32} - 1$. When externally generated, the TMx_CLK clock is called $f_{TMRCLKEXT}$:

$$t_{TMRCLKEXT} = \frac{1}{f_{TMRCLKEXT}}$$

Table 49. Timer Cycle Timing (Internal Mode)

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{WL}	Timer Pulse Width Input Low (Measured In SCLK Cycles)[1]	$2 \times t_{SCLK}$		ns
t_{WH}	Timer Pulse Width Input High (Measured In SCLK Cycles)[1]	$2 \times t_{SCLK}$		ns
Switching Characteristic				
t_{HTO}	Timer Pulse Width Output (Measured In SCLK Cycles)[2]	$t_{SCLK} \times$ WIDTH – 1.5	$t_{SCLK} \times$ WIDTH + 1.5	ns

[1] The minimum pulse width applies for timer signals in width capture and external clock modes.
[2] WIDTH refers to the value in the TMRx_WIDTH register (it can vary from 1 to $2^{32} - 1$).

Table 50. Timer Cycle Timing (External Mode)

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{WL}	Timer Pulse Width Input Low (Measured In EXT_CLK Cycles)[1]	$2 \times t_{EXT\_CLK}$		ns
t_{WH}	Timer Pulse Width Input High (Measured In EXT_CLK Cycles)[1]	$2 \times t_{EXT\_CLK}$		ns
t_{EXT_CLK}	Timer External Clock Period[2]	$t_{TMRCLKEXT}$		ns
Switching Characteristic				
t_{HTO}	Timer Pulse Width Output (Measured In EXT_CLK Cycles)[3]	$t_{EXT\_CLK} \times$ WIDTH – 1.5	$t_{EXT\_CLK} \times$ WIDTH + 1.5	ns

[1] The minimum pulse width applies for timer signals in width capture and external clock modes.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external TMR_CLK. For the external TMR_CLK maximum frequency see the $f_{TMRCLKEXT}$ specification in Table 23.
[3] WIDTH refers to the value in the TMRx_WIDTH register (it can vary from 1 to 2^{32} – 1).

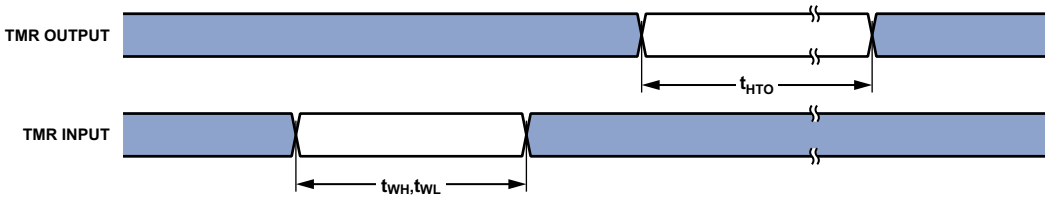


Figure 58. Timer Cycle Timing

Logic Block Array (LBA)

The LBA contains a number of logic blocks which are programmed to perform a variety of logical or arithmetic functions.

Table 51. Logic Block Array Timing

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirement				
t_{WLBAI} (t Width LBA In)	LBA Input Pulse Width	TBD (will be at least $2 \times t_{SCLK}$)		ns
Switching Characteristic				
t_{DLBAR} (t Delay LBA Registered Mode)	Output Delay After Input Transition	TBD	TBD	ns

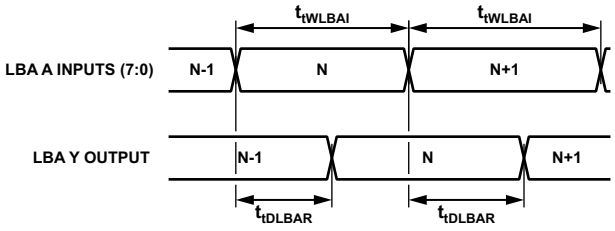


Figure 59. LBA Register Output Mode

Up/Down Counter/Rotary Encoder Timing

Table 52 and Figure 60 describe timing, related to the general-purpose counter (CNT).

Table 52. Up/Down Counter/Rotary Encoder Timing

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirement				
t_{WCOUNT}	Up/Down Counter/Rotary Encoder Input Pulse Width	$2 \times t_{SCLK}$		ns

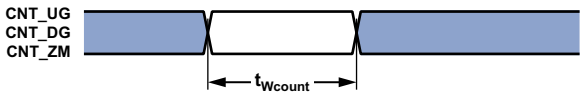


Figure 60. Up/Down Counter/Rotary Encoder Timing

Pulse Width Modulator (PWM) Timing

Table 53 and Figure 61 describe timing, related to the PWM.

Table 53. PWM Timing

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirement				
t_{ES}	External Sync Pulse Width	$2 \times t_{SCLK}$		ns
Switching Characteristics				
t_{DODIS}	Output Inactive (Off) After Trip Input[1]		17	ns
t_{DOE}	Output Delay After External Sync[1, 2]	$2 \times t_{SCLK} + 5.5$	$5 \times t_{SCLK} + 14$	ns

[1] PWM outputs are PWMx_AH, PWMx_AL, PWMx_BH, PWMx_BL, PWMx_CH, PWMx_DH, PWMx_DL, and PWMx_CL.

[2] When the external sync signal is synchronous to the peripheral clock, it takes fewer clock cycles for the output to appear compared to when the external sync signal is asynchronous to the peripheral clock.

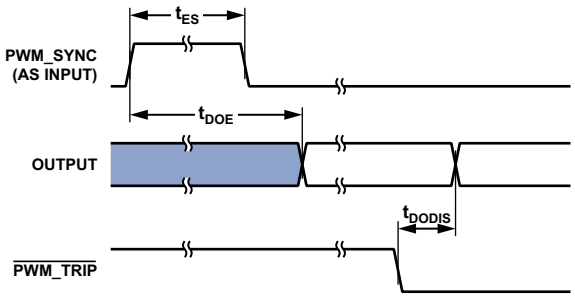


Figure 61. PWM Timing

PWM— Heightened Precision (HP) Mode Timing

Table 54 through Table 56 and Figure 62 through Figure 66 describe heightened precision (HP) PWM operations.

Table 54. PWM—HP Mode, Output Pulse

All specifications are based on simulation data and are subject to change without notice.			
Parameter	**Min**	**Max**	**Unit**
Switching Characteristic			
t_{HPWMW} HP PWM Output Pulse Width[1, 2]	TBD	TBD	ns

[1] N is the DUTY bit field (coarse duty) from the duty register. m is the ENHDIV (Enhanced Precision Divider bits) value from the HP duty register.
[2] Applies to individual PWM channel with 50% duty cycle. Other PWM channels within the same unit are toggling at the same time. No other GPIO pins toggle.

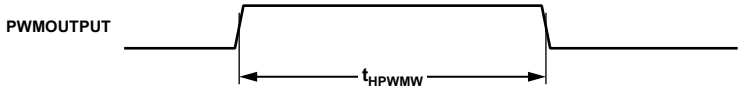


Figure 62. PWM HP Mode Timing, Output Pulse

Table 55. PWM—HP Mode, Output Pulse Width Accuracy

All specifications are based on simulation data and are subject to change without notice.					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
HPPWM Pulse Width Accuracy					
Resolution[1]	Maximum allowed heightened precision divider bits for fractional duty cycles within system clock period			4	Bits
Differential Non-Linearity (DNL)[2]	Guaranteed monotonic	– 0.99		0.99	LSB
Integral Non-Linearity (INL)[3]		TBD		TBD	LSB
RMS Jitter	RMS jitter of any given pulse width code step		TBD		ps

[1] See Figure 63 for an example of 4-bit resolution of fractional duty cycle edge placement.
[2] DNL definition. See Figure 64 for an example of DNL calculation. For each heightened precision duty register value n:

$$DNL(n) = \frac{PW(n) - PW(n-1)}{IdealLSBStepWidth} - 1$$

[3] INL definition. See Figure 65 for an example of INL calculation. For each heightened precision duty register value n:

$$INL(n) = \left| \frac{PW(n) - PW(0)}{IdealLSBPulseWidth} - n \right|$$

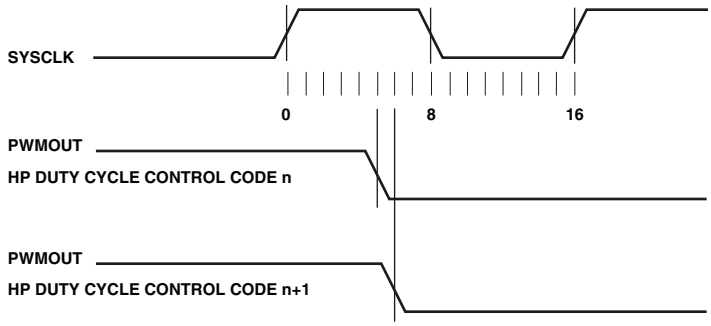


Figure 63. Fractional Duty Cycle Edge Placement (4-Bit Resolution)

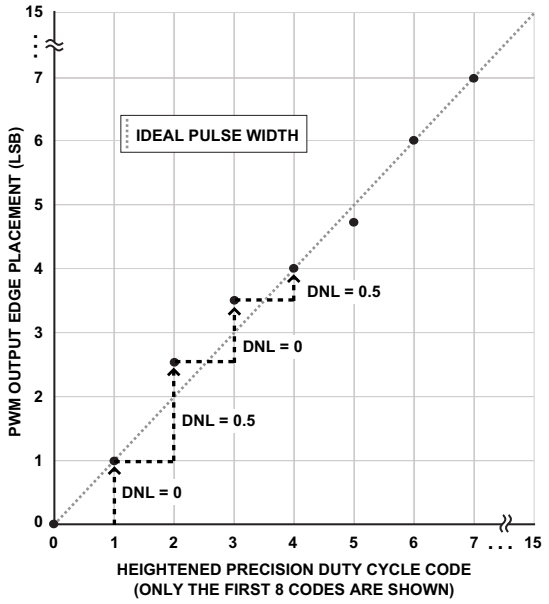


Figure 64. HPPWM Pulse Width Accuracy: DNL Calculation

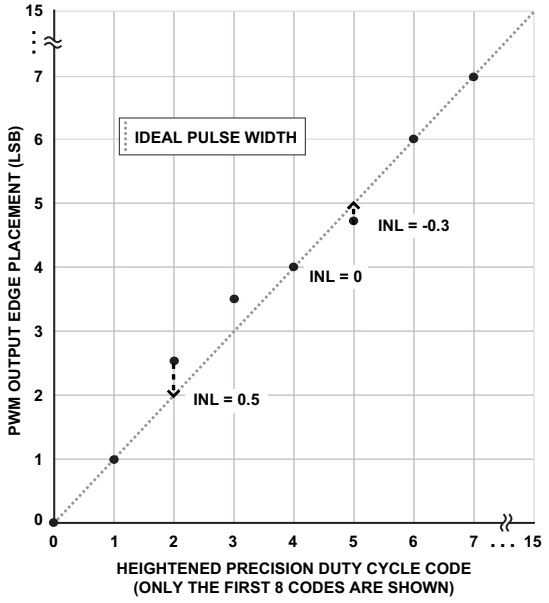


Figure 65. HPPWM Pulse Width Accuracy: INL Calculation

Table 56. PWM—HP Mode, Output Skew

All specifications are based on simulation data and are subject to change without notice.			
Parameter	**Min**	**Max**	**Unit**
Switching Characteristic			
t_{HPWMS} HP-PWM Output Skew [1]		TBD	ns

[1] Output edge difference between any two PWM channels (AH, AL, BH, BL, CH, CL, DH, and DL) in the same PWM unit (a unit is PWMx where x = 0, 1, 2), with the same HP edge placement.

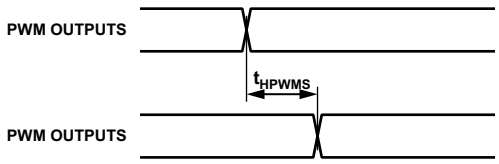


Figure 66. PWM HP Mode Timing, Output Skew

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The UART ports receive and transmit operations are described in the ADSP-CM41x Mixed-Signal Control Processor with ARM Cortex-M4/ARM Cortex-M0 and 16-bit ADCs Hardware Reference.

Controller Area Network (CAN) Interface

The CAN interface timing is described in the ADSP-CM41x Mixed-Signal Control Processor with ARM Cortex-M4/ARM Cortex-M0 and 16-bit ADCs Hardware Reference

Sinus Cardinalis (SINC) Filter Timing

The programmed SINC filter clock ($f_{SINCLKPROG}$) frequency in MHz is set by the following equation where MDIV is a field in the CLK control register that can be set from 4 to 63:

$$f_{SINCLKPROG} = \frac{f_{SCLK}}{MDIV}$$

$$t_{SINCLKPROG} = \frac{1}{f_{SINCLKPROG}}$$

Table 57. SINC Timing

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{SSINC}	SINC0_Dx Setup Before SINC0_CLKx Rise	10		ns
t_{HSINC}	SINC0_Dx Hold After SINC0_CLKx Rise	0		ns
Switching Characteristics				
t_{SINCLK}	SINC0_CLKx Period[1]	$t_{SINCLKPROG} - 2.5$		ns
$t_{SINCLKW}$	SINC0_CLKx Width[1]	$0.5 \times t_{SINCLKPROG} - 2.5$		ns

[1] See Table 23 for details on the minimum period that may be programmed for $t_{SINCLKPROG}$.

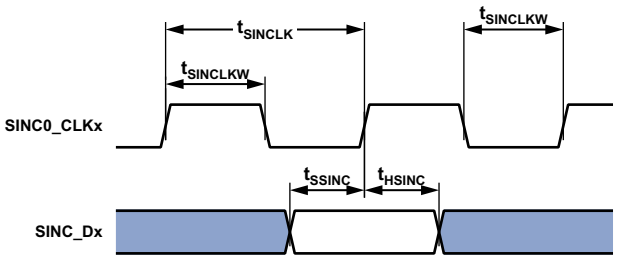


Figure 67. SINC Filter Timing

Trace Timing

Table 58. Trace Timing

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
$t_{DDTRACE}$	Data Delay After TRACE_CLK		$0.5 \times t_{SCLK} + 2$	ns
$t_{HDTRACE}$	Data Hold After TRACE_CLK	$0.5 \times t_{SCLK} - 2$		ns

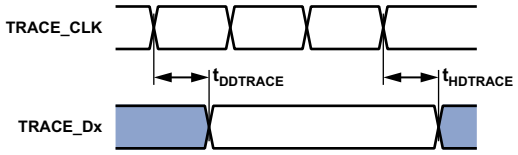


Figure 68. Trace Timing

Serial Wire Debug (SWD) Timing

Table 59 and Figure 69 describe the serial wire debug (SWD) operations.

Table 59. SWD Timing

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{SWCLK}	SWCLK Period	20		ns
t_{SSWDIO}	SWDIO Setup Before SWCLK High	6		ns
t_{HSWDIO}	SWDIO Hold After SWCLK High	4		ns
Switching Characteristics				
t_{DSWDIO}	SWDIO Delay After SWCLK High		12.5	ns
$t_{HOSWDIO}$	SWDIO Hold After SWCLK High	3.5		ns

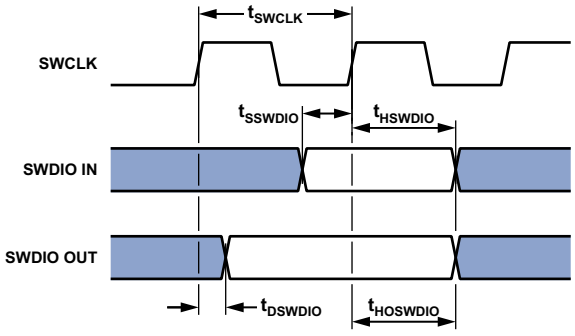


Figure 69. SWD Timing

Debug Interface (JTAG Emulation Port) Timing

Table 60 and Figure 70 provide I/O timing, related to the debug interface (JTAG Emulator Port).

Table 60. JTAG Emulation Port Timing

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{TCK}	JTG_TCK Period	20		ns
t_{STAP}	JTG_TDI, JTG_TMS Setup Before JTG_TCK High	6		ns
t_{HTAP}	JTG_TDI, JTG_TMS Hold After JTG_TCK High	4		ns
t_{SSYS}	System Inputs Setup Before JTG_TCK High[1]	12		ns
t_{HSYS}	System Inputs Hold After JTG_TCK High[1]	5		ns
t_{TRSTW}	$\overline{\text{JTG\_TRST}}$ Pulse Width (Measured in JTG_TCK cycles)[2]	4		t_{TCK}
Switching Characteristics				
t_{DTDO}	JTG_TDO Delay From JTG_TCK Low		14.0	ns
t_{DSYS}	System Outputs Delay After JTG_TCK Low[3]		14.0	ns

[1] System inputs = PA_xx, PB_xx, PC_xx, PD_xx, PE_xx, PF_xx, SYS_BMODEx, $\overline{\text{SYS\_HWRST}}$, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_NMI}}$, TWI0_SCL, TWI0_SDA.
[2] 50 MHz maximum.
[3] System outputs = PA_xx, PB_xx, PC_xx, PD_xx, PE_xx, PF_xx, $\overline{\text{SMC0\_AMS0}}$, $\overline{\text{SMC0\_ARE}}$, $\overline{\text{SMC0\_AWE}}$, SYS_CLKOUT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_RESOUT}}$.

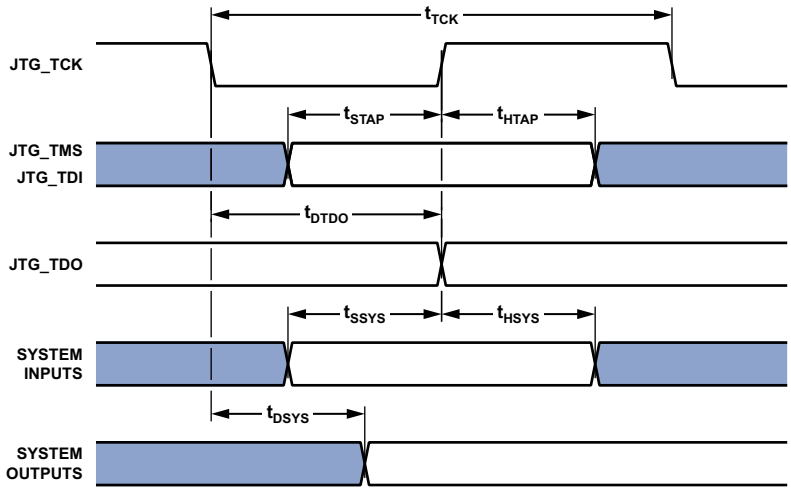


Figure 70. JTAG Port Timing

ADC Timing

Table 61 and Figure 71 describe ADC timing.

Table 61. ADC Timing

All specifications are based on simulation data and are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{CSP}	Total Period of ADCC_xCS ADC Conversion Start for ADC0	500		ns
	Total Period of ADCC_xCS ADC Conversion Start for ADC1 and ADC2	340		ns
t_{CS_ACTIVE}	Active Duration of ADCC_xCS ADC Conversion Start for ADC0	180		ns
	Active Duration of ADCC_xCS ADC Conversion Start for ADC1 and ADC2	180		ns
NCK	Number of ADCC_xCLK Clock Cycles Given in Each CS Active Pulse for ADC0	8	8	
	Number of ADCC_xCLK Clock Cycles Given in Each CS Active Pulse for ADC1 and ADC2	8	8	
t_{CK}	Period of the ADCC_xCLK, ADC Clock for ADC0	See Table 23, $f_{ADCC0\_ADC0\_CLK\_PROG}$		
	Period of the ADCC_xCLK, ADC Clock for ADC1	See Table 23, $f_{ADCC1\_ADC1\_CLK\_PROG}$		
	Period of the ADCC_xCLK, ADC Clock for ADC2	See Table 23, $f_{ADCC1\_ADC2\_CLK\_PROG}$		
t_{CSCK}	Time-CS-to-CK-Setup Time Between the Assertion Edge of ADCC_xCS to the First Falling Edge of the ADCC_xCLK ADC Clock for ADC0	20		ns
	Time-CS-to-CK-Setup Time Between the Assertion Edge of ADCC_xCS to the First Falling Edge of the ADCC_xCLK ADC Clock for ADC1 and ADC2	20		ns
t_{CKCS}	Time-CK-to-CS-Hold Time Between the End of the Last Full Cycle of the ADC Clock and the De-assertion Edge of the CS Signal for ADC0	0		ns
	Time-CK-to-CS-Hold Time Between the End of the Last Full Cycle of the ADC Clock and the De-assertion Edge of the CS Signal for ADC1 and ADC2	0		ns

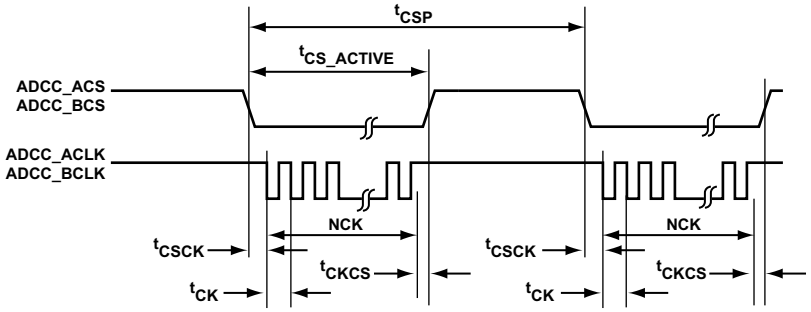


Figure 71. ADC Timing

PROCESSOR TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 72 shows the measurement point for ac measurements (except output enable/disable). The measurement point V_{MEAS} is $V_{DD\_EXT}/2$ for V_{DD_EXT} (nominal) = 3.3 V.

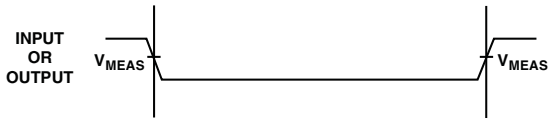


Figure 72. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time, t_{ENA}, is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 73. If multiple pins are enabled, the measurement value is that of the first pin to start driving.

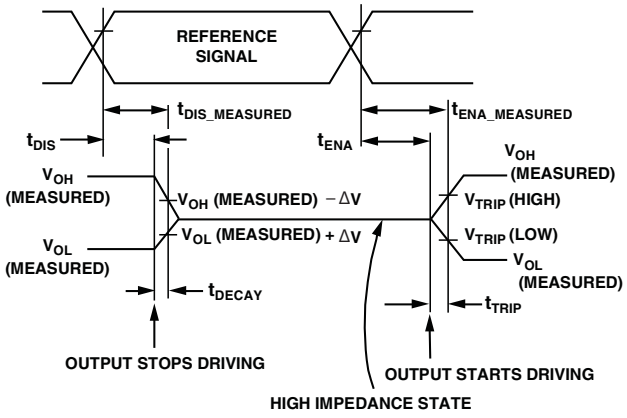


Figure 73. Output Enable/Disable

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time, t_{DIS}, is the interval from when a reference signal reaches a high or low voltage level to the point when the output stops driving as shown on the left side of Figure 73.

OUTPUT DRIVE CURRENTS

Figure 74 and Figure 75 show typical current voltage characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

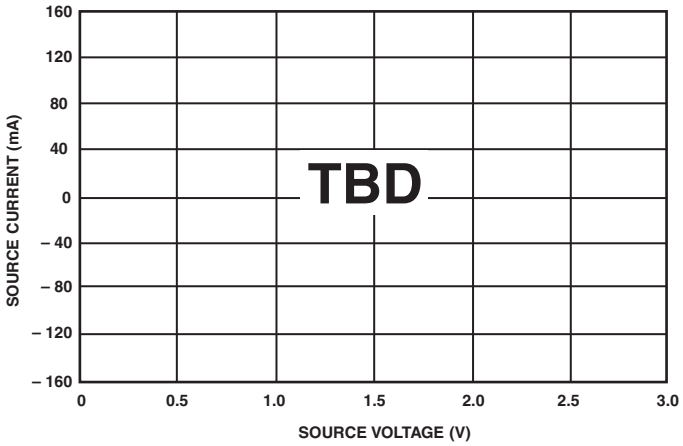


Figure 74. Driver Type A Current

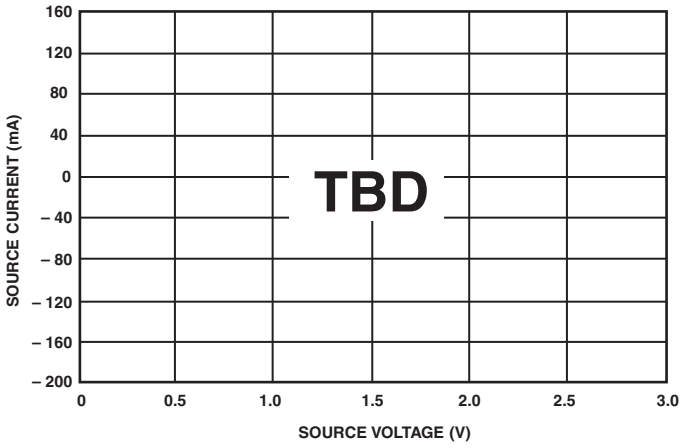
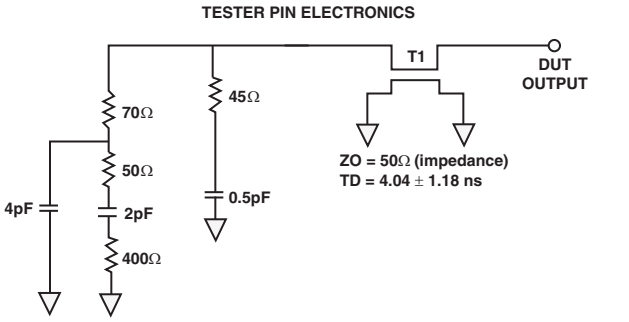


Figure 75. Driver Type B Current

Capacitive Loading

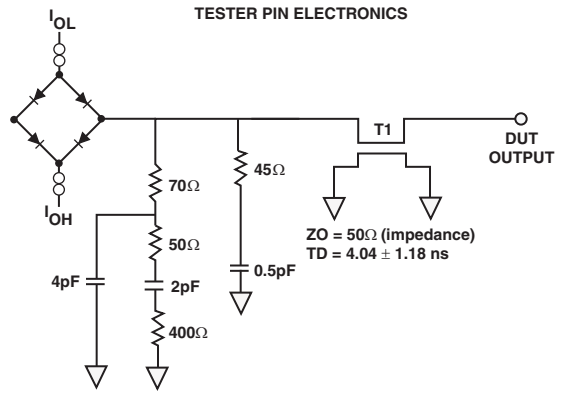
Output delay, hold, enable, and disable times are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 76 and Figure 77). V_{LOAD} is equal to $(V_{DD\_EXT})/2$.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD), IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 76. Equivalent Device Loading for AC Measurements For All GPIO Pins (Includes All Fixtures)



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD), IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 77. Equivalent Device Loading for AC Measurements For All Non GPIO Pins (Includes All Fixtures)

The graph of Figure 78 shows how output rise and fall times vary with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.

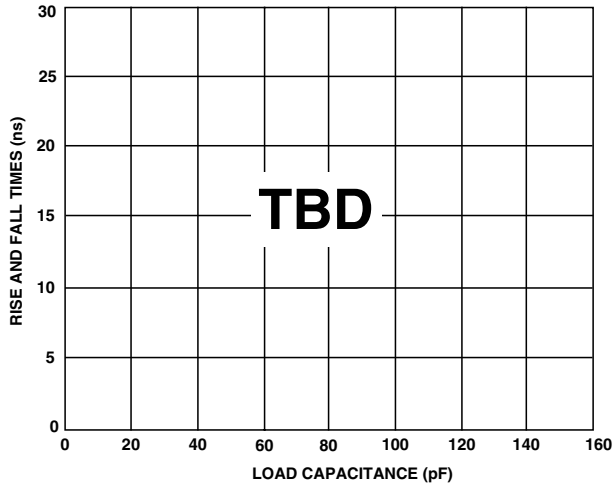


Figure 78. Driver Type A Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application PCB, use the following equation:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:
T_J = junction temperature (°C).
T_{CASE} = case temperature (°C) measured by customer at top center of package.
Ψ_{JT} = from Table 62 and Table 63.
P_D = power dissipation (see Total Power Dissipation (PD) for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the following equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where T_A = ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

In Table 62 and Table 63 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6. The junction to case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Table 62. Thermal Characteristics for 176-Lead LQFP_EP

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	20.8	°C/W
θ_{JA}	1 linear m/s air flow	18.2	°C/W
θ_{JA}	2 linear m/s air flow	17.4	°C/W
θ_{JC}		13.3	°C/W
Ψ_{JT}	0 linear m/s air flow	0.22	°C/W
Ψ_{JT}	1 linear m/s air flow	0.32	°C/W
Ψ_{JT}	2 linear m/s air flow	0.37	°C/W

Table 63. Thermal Characteristics for 210-Ball CSP_BGA

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	24.9	°C/W
θ_{JA}	1 linear m/s air flow	22.2	°C/W
θ_{JA}	2 linear m/s air flow	21.1	°C/W
θ_{JC}		11.2	°C/W
Ψ_{JT}	0 linear m/s air flow	1.74	°C/W
Ψ_{JT}	1 linear m/s air flow	1.68	°C/W
Ψ_{JT}	2 linear m/s air flow	1.69	°C/W

ADSP-CM41xF 176-LEAD LQFP_EP LEAD ASSIGNMENTS

The ADSP-CM41xF 176-Lead LQFP_EP Lead Assignments (Numerical by Lead Number) table lists the 176-lead LQFP_EP package by lead number.

The ADSP-CM41xF 176-Lead LQFP_EP Lead Assignments (Alphabetical by Pin Name) table lists the 176-lead LQFP_EP package by pin name.

ADSP-CM41xF 176-LEAD LQFP_EP LEAD ASSIGNMENTS (NUMERICAL BY LEAD NUMBER)

Lead No.	Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.	Pin Name
1	PD_00	42	TWI0_SCL	83	VDD_ANA0	124	ADC_VIN_A1
2	PD_01	43	TWI0_SDA	84	GND_ANA0	125	ADC_VIN_A2
3	PB_00	44	GND	85	BYP_A0	126	ADC_VIN_A3
4	PB_01	45	JTG_TDI	86	DAC0_VOUT	127	ADC_VIN_A4
5	PE_00	46	JTG_TCK/SWCLK	87	GND_ANA5_DAC	128	ADC_VIN_A5
6	PE_01	47	JTG_TDO/SWO	88	GND_ANA3	129	ADC_VIN_A6
7	VDD_EXT	48	JTG_TMS/SWDIO	89	GND_ANA1	130	ADC_VIN_A7
8	PB_02	49	$\overline{\text{JTG\_TRST}}$	90	BYP_A1	131	GND_ANA2
9	PB_03	50	PE_08	91	VDD_ANA1	132	GND_ANA4_COMP
10	PE_02	51	PE_09	92	GND_REFCAP0	133	VDD_COMP
11	PE_03	52	PE_10	93	REFCAP0	134	COMP_OUT_A
12	VDD_EXT	53	PE_11	94	VREF0	135	COMP_OUT_B
13	PB_04	54	PB_12	95	GND_VREF0	136	COMP_OUT_C
14	PB_05	55	PB_13	96	ADC_VIN_D6	137	VDD_EXT
15	PE_04	56	VDD_EXT	97	ADC_VIN_D5	138	BYP_D0
16	PE_05	57	PB_14	98	ADC_VIN_D4	139	VDD_EXT
17	VDD_EXT	58	PB_15	99	ADC_VIN_D3	140	VDD_EXT
18	PB_06	59	PE_12	100	ADC_VIN_D2	141	$\overline{\text{SYS\_NMI}}$
19	PB_07	60	PE_13	101	ADC_VIN_D1	142	VDD_EXT
20	PE_06	61	PE_14	102	ADC_VIN_D0	143	VDD_EXT
21	PE_07	62	PE_15	103	GND_REFCAP1	144	PC_00
22	VDD_EXT	63	VDD_EXT	104	REFCAP1	145	PC_01
23	$\overline{\text{SYS\_RESOUT}}$	64	VDD_INT	105	VREF1	146	PC_02
24	$\overline{\text{SYS\_FAULT}}$	65	VDD_INT	106	GND_VREF1	147	PC_03
25	$\overline{\text{SYS\_HWRST}}$	66	PA_00	107	ADC_VIN_C7	148	PF_00
26	VDD_INT	67	PA_01	108	ADC_VIN_C6	149	PF_01
27	VDD_INT	68	PA_02	109	ADC_VIN_C5	150	VDD_EXT
28	PB_08	69	PA_03	110	ADC_VIN_C4	151	PC_04
29	PB_09	70	VDD_EXT	111	ADC_VIN_C3	152	PC_05
30	PB_10	71	PA_04	112	ADC_VIN_C2	153	PC_06
31	PB_11	72	PA_05	113	ADC_VIN_C1	154	PC_07
32	VDD_INT	73	PA_06	114	ADC_VIN_C0	155	PF_02
33	VDD_INT	74	PA_07	115	ADC_VIN_B0	156	PF_03
34	VDD_EXT	75	VDD_EXT	116	ADC_VIN_B1	157	VDD_INT
35	VDD_EXT	76	PA_08	117	ADC_VIN_B2	158	VDD_INT
36	SYS_CLKIN0	77	PA_09	118	ADC_VIN_B3	159	VDD_EXT
37	SYS_XTAL0	78	PA_10	119	ADC_VIN_B4	160	PC_08
38	VDD_EXT	79	PA_11	120	ADC_VIN_B5	161	PC_09
39	VREG_BASE	80	PA_12	121	ADC_VIN_B6	162	PC_10
40	SYS_CLKIN1	81	PA_13	122	ADC_VIN_B7	163	PC_11
41	SYS_XTAL1	82	VDD_EXT	123	ADC_VIN_A0	164	PF_04

Lead No.	Pin Name
165	PF_05
166	VDD_EXT
167	PC_12
168	PC_13
169	PC_14
170	PC_15
171	PF_06
172	PF_07
173	VDD_EXT
174	PF_08
175	SYS_CLKOUT
176	SYS_BMODE0
177[1]	GND

[1] Pin no. 177 is the GND supply (see Figure 80) for the processor; this pad must connect to GND.

ADSP-CM41xF 176-LEAD LQFP_EP LEAD ASSIGNMENTS (ALPHABETICAL BY PIN NAME)

Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.
ADC_VIN_A0	123	GND_REFCAP0	92	PC_07	154	SYS_XTAL0	37
ADC_VIN_A1	124	GND_REFCAP1	103	PC_08	160	SYS_XTAL1	41
ADC_VIN_A2	125	GND_VREF0	95	PC_09	161	TWI0_SCL	42
ADC_VIN_A3	126	GND_VREF1	106	PC_10	162	TWI0_SDA	43
ADC_VIN_A4	127	JTG_TCK/SWCLK	46	PC_11	163	VDD_ANA0	83
ADC_VIN_A5	128	JTG_TDI	45	PC_12	167	VDD_ANA1	91
ADC_VIN_A6	129	JTG_TDO/SWO	47	PC_13	168	VDD_COMP	133
ADC_VIN_A7	130	JTG_TMS/SWDIO	48	PC_14	169	VDD_EXT	7
ADC_VIN_B0	115	$\overline{\text{JTG\_TRST}}$	49	PC_15	170	VDD_EXT	12
ADC_VIN_B1	116	PA_00	66	PD_00	1	VDD_EXT	17
ADC_VIN_B2	117	PA_01	67	PD_01	2	VDD_EXT	22
ADC_VIN_B3	118	PA_02	68	PE_00	5	VDD_EXT	34
ADC_VIN_B4	119	PA_03	69	PE_01	6	VDD_EXT	35
ADC_VIN_B5	120	PA_04	71	PE_02	10	VDD_EXT	38
ADC_VIN_B6	121	PA_05	72	PE_03	11	VDD_EXT	56
ADC_VIN_B7	122	PA_06	73	PE_04	15	VDD_EXT	63
ADC_VIN_C0	114	PA_07	74	PE_05	16	VDD_EXT	70
ADC_VIN_C1	113	PA_08	76	PE_06	20	VDD_EXT	75
ADC_VIN_C2	112	PA_09	77	PE_07	21	VDD_EXT	82
ADC_VIN_C3	111	PA_10	78	PE_08	50	VDD_EXT	137
ADC_VIN_C4	110	PA_11	79	PE_09	51	VDD_EXT	139
ADC_VIN_C5	109	PA_12	80	PE_10	52	VDD_EXT	140
ADC_VIN_C6	108	PA_13	81	PE_11	53	VDD_EXT	142
ADC_VIN_C7	107	PB_00	3	PE_12	59	VDD_EXT	143
ADC_VIN_D0	102	PB_01	4	PE_13	60	VDD_EXT	150
ADC_VIN_D1	101	PB_02	8	PE_14	61	VDD_EXT	159
ADC_VIN_D2	100	PB_03	9	PE_15	62	VDD_EXT	166
ADC_VIN_D3	99	PB_04	13	PF_00	148	VDD_EXT	173
ADC_VIN_D4	98	PB_05	14	PF_01	149	VDD_INT	26
ADC_VIN_D5	97	PB_06	18	PF_02	155	VDD_INT	27
ADC_VIN_D6	96	PB_07	19	PF_03	156	VDD_INT	32
BYP_A0	85	PB_08	28	PF_04	164	VDD_INT	33
BYP_A1	90	PB_09	29	PF_05	165	VDD_INT	64
BYP_D0	138	PB_10	30	PF_06	171	VDD_INT	65
COMP_OUT_A	134	PB_11	31	PF_07	172	VDD_INT	157
COMP_OUT_B	135	PB_12	54	PF_08	174	VDD_INT	158
COMP_OUT_C	136	PB_13	55	REFCAP0	93	VREF0	94
DAC0_VOUT	86	PB_14	57	REFCAP1	104	VREF1	105
GND	44	PB_15	58	SYS_BMODE0	176	VREG_BASE	39
GND	177[1]	PC_00	144	SYS_CLKIN0	36		
GND_ANA0	84	PC_01	145	SYS_CLKIN1	40		
GND_ANA1	89	PC_02	146	SYS_CLKOUT	175		
GND_ANA2	131	PC_03	147	$\overline{\text{SYS\_FAULT}}$	24		
GND_ANA3	88	PC_04	151	$\overline{\text{SYS\_HWRST}}$	25		
GND_ANA4_COMP	132	PC_05	152	$\overline{\text{SYS\_NMI}}$	141		
GND_ANA5_DAC	87	PC_06	153	$\overline{\text{SYS\_RESOUT}}$	23		

[1] Pin no. 177 is the GND supply (see Figure 80) for the processor; this pad must connect to GND.

Figure 79 shows the top view of the 176-lead LQFP_EP lead configuration and Figure 80 shows the bottom view of the 176-lead LQFP_EP lead configuration.

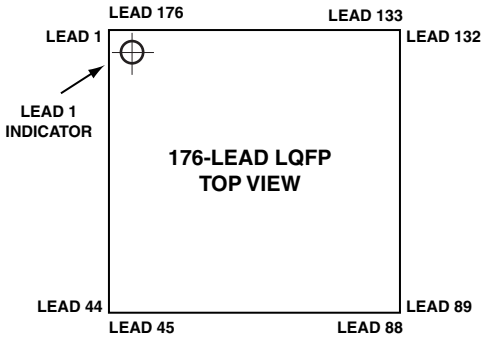


Figure 79. 176-Lead LQFP_EP Lead Configuration (Top View)

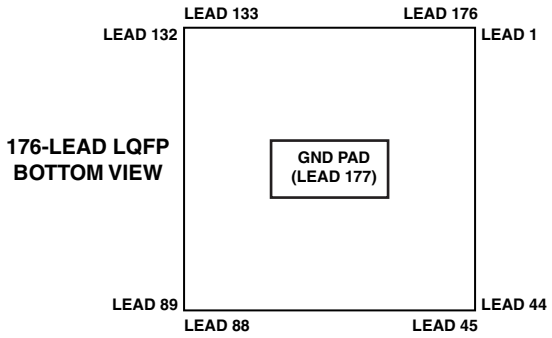


Figure 80. 176-Lead LQFP_EP Lead Configuration (Bottom View)

ADSP-CM41xF 210-BALL CSP_BGA BALL ASSIGNMENTS

The ADSP-CM41xF 210-Ball CSP_BGA Ball Assignments (Numerical by Ball Number) table lists the 210-ball CSP_BGA package by ball number.

The ADSP-CM41xF 210-Ball CSP_BGA Ball Assignments (Alphabetical by Pin Name) table lists the 210-ball CSP_BGA package by pin name.

ADSP-CM41xF 210-BALL CSP_BGA BALL ASSIGNMENTS (NUMERICAL BY BALL NUMBER)

Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name
A01	GND	C06	PC_12	G18	ADC_VIN_B5	L12	GND_ANA
A02	SYS_BMODE0	C07	PC_11	H01	PB_07	L16	REFCAP1
A03	SYS_CLKOUT	C08	PC_09	H02	PB_06	L17	ADC_VIN_C0
A04	PF_06	C09	PC_07	H03	VDD_EXT	L18	ADC_VIN_C2
A05	PC_14	C10	PC_05	H07	GND	M01	PB_10
A06	PF_04	C11	PC_02	H08	GND	M02	PB_11
A07	PC_08	C12	VDD_EXT	H09	GND	M03	VDD_EXT
A08	PF_03	C13	GND_ANA	H11	GND_ANA	M16	GND_REFCAP1
A09	PC_04	C14	VDD_EXT	H12	GND_ANA	M17	ADC_VIN_C4
A10	PF_00	C15	VDD_COMP	H16	GND_VREF1	M18	ADC_VIN_C3
A11	PC_00	C16	GND_ANA	H17	ADC_VIN_B4	N01	SYS_CLKIN0
A12	PC_01	C17	ADC_VIN_A7	H18	ADC_VIN_B3	N02	TWI0_SCL
A13	DNC	C18	ADC_VIN_A4	J01	PE_06	N03	VREG_BASE
A14	GND_ANA	D01	PB_02	J02	PE_07	N16	DNC
A15	COMP_OUT_C	D02	PB_03	J03	VDD_INT	N17	ADC_VIN_C5
A16	COMP_OUT_B	D03	PF_07	J07	GND	N18	ADC_VIN_C6
A17	DNC	D07	VDD_INT	J08	GND	P01	SYS_XTAL0
A18	GND_ANA	D08	VDD_EXT	J09	GND	P02	TWI0_SDA
B01	PD_01	D09	VDD_EXT	J11	GND_ANA	P03	JTG_TCK/SWCLK
B02	GND	D10	VDD_EXT	J12	GND_ANA	P16	VREF0
B03	PF_08	D11	VDD_EXT	J16	VREF1	P17	ADC_VIN_D2
B04	PC_15	D16	BYP_A2	J17	ADC_VIN_B0	P18	ADC_VIN_C7
B05	PC_13	D17	ADC_VIN_A6	J18	ADC_VIN_B2	R01	SYS_CLKIN1
B06	PF_05	D18	ADC_VIN_A3	K01	$\overline{\text{SYS\_FAULT}}$	R02	JTG_TDI
B07	PC_10	E01	PB_05	K02	$\overline{\text{SYS\_HWRST}}$	R03	$\overline{\text{JTG\_TRST}}$
B08	PF_02	E02	PE_00	K03	VDD_INT	R07	VDD_INT
B09	PC_06	E03	PD_00	K07	GND	R08	VDD_EXT
B10	PF_01	E16	GND_VREF2	K08	GND	R09	VDD_EXT
B11	PC_03	E17	ADC_VIN_A2	K09	GND	R10	VDD_EXT
B12	$\overline{\text{SYS\_NMI}}$	E18	ADC_VIN_A1	K11	GND_ANA	R11	VDD_EXT
B13	DNC	F01	PB_04	K12	GND_ANA	R16	GND_VREF0
B14	GND_ANA	F02	PE_03	K16	DNC	R17	ADC_VIN_D3
B15	BYP_D0	F03	PE_01	K17	ADC_VIN_C1	R18	ADC_VIN_D0
B16	COMP_OUT_A	F16	VREF2	K18	ADC_VIN_B1	T01	SYS_XTAL1
B17	GND_ANA	F17	ADC_VIN_A0	L01	PB_08	T02	JTG_TMS/SWDIO
B18	ADC_VIN_A5	F18	ADC_VIN_B6	L02	PB_09	T03	GND
C01	PB_01	G01	PE_05	L03	$\overline{\text{SYS\_RESOUT}}$	T04	GND
C02	PB_00	G02	PE_04	L07	GND	T05	VDD_EXT
C03	GND	G03	PE_02	L08	GND	T06	PE_13
C04	VDD_INT	G16	DNC	L09	GND	T07	PA_00
C05	VDD_EXT	G17	ADC_VIN_B7	L11	GND_ANA	T08	PA_01

Ball No.	Pin Name
T09	PA_05
T10	PA_09
T11	PA_13
T12	DNC
T13	GND_ANA
T14	VDD_ANA0
T15	VDD_ANA1
T16	GND_ANA
T17	ADC_VIN_D4
T18	ADC_VIN_D1
U01	JTG_TDO/SWO
U02	GND
U03	PE_09
U04	PE_11
U05	PB_13
U06	PE_12
U07	PE_15
U08	PA_03
U09	PA_07
U10	PA_06
U11	PA_10
U12	DNC
U13	GND_ANA
U14	REFCAP0
U15	GND_REFCAP0
U16	GND_ANA
U17	ADC_VIN_D6
U18	ADC_VIN_D5
V01	GND
V02	PE_08
V03	PE_10
V04	PB_12
V05	PB_14
V06	PB_15
V07	PE_14
V08	PA_02
V09	PA_04
V10	PA_08
V11	PA_11
V12	PA_12
V13	GND_ANA
V14	BYP_A0
V15	DAC0_VOUT
V16	BYP_A1
V17	GND_ANA
V18	GND_ANA

ADSP-CM41xF 210-BALL CSP_BGA BALL ASSIGNMENTS (ALPHABETICAL BY PIN NAME)

Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.
ADC_VIN_A0	F17	DNC	U12	JTG_TCK/SWCLK	P03	PC_11	C07
ADC_VIN_A1	E18	GND	A01	JTG_TDI	R02	PC_12	C06
ADC_VIN_A2	E17	GND	B02	JTG_TDO/SWO	U01	PC_13	B05
ADC_VIN_A3	D18	GND	C03	JTG_TMS/SWDIO	T02	PC_14	A05
ADC_VIN_A4	C18	GND	H07	$\overline{\text{JTG\_TRST}}$	R03	PC_15	B04
ADC_VIN_A5	B18	GND	H08	PA_00	T07	PD_00	E03
ADC_VIN_A6	D17	GND	H09	PA_01	T08	PD_01	B01
ADC_VIN_A7	C17	GND	J07	PA_02	V08	PE_00	E02
ADC_VIN_B0	J17	GND	J08	PA_03	U08	PE_01	F03
ADC_VIN_B1	K18	GND	J09	PA_04	V09	PE_02	G03
ADC_VIN_B2	J18	GND	K07	PA_05	T09	PE_03	F02
ADC_VIN_B3	H18	GND	K08	PA_06	U10	PE_04	G02
ADC_VIN_B4	H17	GND	K09	PA_07	U09	PE_05	G01
ADC_VIN_B5	G18	GND	L07	PA_08	V10	PE_06	J01
ADC_VIN_B6	F18	GND	L08	PA_09	T10	PE_07	J02
ADC_VIN_B7	G17	GND	L09	PA_10	U11	PE_08	V02
ADC_VIN_C0	L17	GND	T03	PA_11	V11	PE_09	U03
ADC_VIN_C1	K17	GND	T04	PA_12	V12	PE_10	V03
ADC_VIN_C2	L18	GND	U02	PA_13	T11	PE_11	U04
ADC_VIN_C3	M18	GND	V01	PB_00	C02	PE_12	U06
ADC_VIN_C4	M17	GND_ANA	A14	PB_01	C01	PE_13	T06
ADC_VIN_C5	N17	GND_ANA	A18	PB_02	D01	PE_14	V07
ADC_VIN_C6	N18	GND_ANA	B14	PB_03	D02	PE_15	U07
ADC_VIN_C7	P18	GND_ANA	B17	PB_04	F01	PF_00	A10
ADC_VIN_D0	R18	GND_ANA	C13	PB_05	E01	PF_01	B10
ADC_VIN_D1	T18	GND_ANA	C16	PB_06	H02	PF_02	B08
ADC_VIN_D2	P17	GND_ANA	H11	PB_07	H01	PF_03	A08
ADC_VIN_D3	R17	GND_ANA	H12	PB_08	L01	PF_04	A06
ADC_VIN_D4	T17	GND_ANA	J11	PB_09	L02	PF_05	B06
ADC_VIN_D5	U18	GND_ANA	J12	PB_10	M01	PF_06	A04
ADC_VIN_D6	U17	GND_ANA	K11	PB_11	M02	PF_07	D03
BYP_A0	V14	GND_ANA	K12	PB_12	V04	PF_08	B03
BYP_A1	V16	GND_ANA	L11	PB_13	U05	REFCAP0	U14
BYP_A2	D16	GND_ANA	L12	PB_14	V05	REFCAP1	L16
BYP_D0	B15	GND_ANA	T13	PB_15	V06	SYS_BMODE0	A02
COMP_OUT_A	B16	GND_ANA	T16	PC_00	A11	SYS_CLKIN0	N01
COMP_OUT_B	A16	GND_ANA	U13	PC_01	A12	SYS_CLKIN1	R01
COMP_OUT_C	A15	GND_ANA	U16	PC_02	C11	SYS_CLKOUT	A03
DAC0_VOUT	V15	GND_ANA	V13	PC_03	B11	$\overline{\text{SYS\_FAULT}}$	K01
DNC	A13	GND_ANA	V17	PC_04	A09	$\overline{\text{SYS\_HWRST}}$	K02
DNC	A17	GND_ANA	V18	PC_05	C10	$\overline{\text{SYS\_NMI}}$	B12
DNC	B13	GND_REFCAP0	U15	PC_06	B09	$\overline{\text{SYS\_RESOUT}}$	L03
DNC	G16	GND_REFCAP1	M16	PC_07	C09	SYS_XTAL0	P01
DNC	K16	GND_VREF0	R16	PC_08	A07	SYS_XTAL1	T01
DNC	N16	GND_VREF1	H16	PC_09	C08	TWI0_SCL	N02
DNC	T12	GND_VREF2	E16	PC_10	B07	TWI0_SDA	P02

Pin Name	Ball No.
VDD_ANA0	T14
VDD_ANA1	T15
VDD_COMP	C15
VDD_EXT	C05
VDD_EXT	C12
VDD_EXT	C14
VDD_EXT	D08
VDD_EXT	D09
VDD_EXT	D10
VDD_EXT	D11
VDD_EXT	H03
VDD_EXT	M03
VDD_EXT	R08
VDD_EXT	R09
VDD_EXT	R10
VDD_EXT	R11
VDD_EXT	T05
VDD_INT	C04
VDD_INT	D07
VDD_INT	J03
VDD_INT	K03
VDD_INT	R07
VREF0	P16
VREF1	J16
VREF2	F16
VREG_BASE	N03

Figure 81 shows an overview of signal placement on the 210-ball CSP_BGA package.

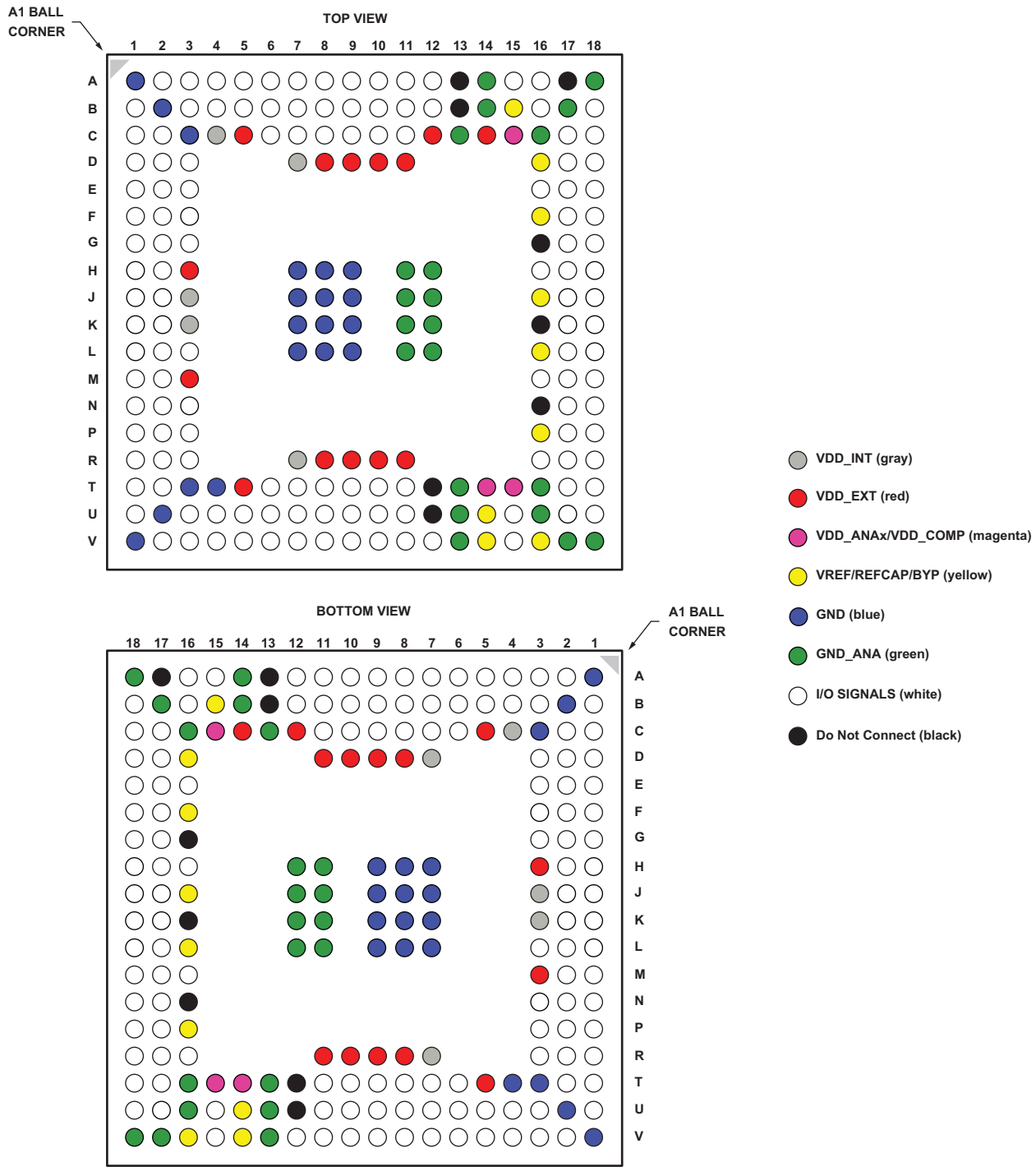


Figure 81. 210-Ball CSP_BGA Ball Configuration

OUTLINE DIMENSIONS

Dimensions in Figure 82 (for the 176-lead LQFP_EP) and Figure 83 (for the 210-ball CSP_BGA) are shown in millimeters.

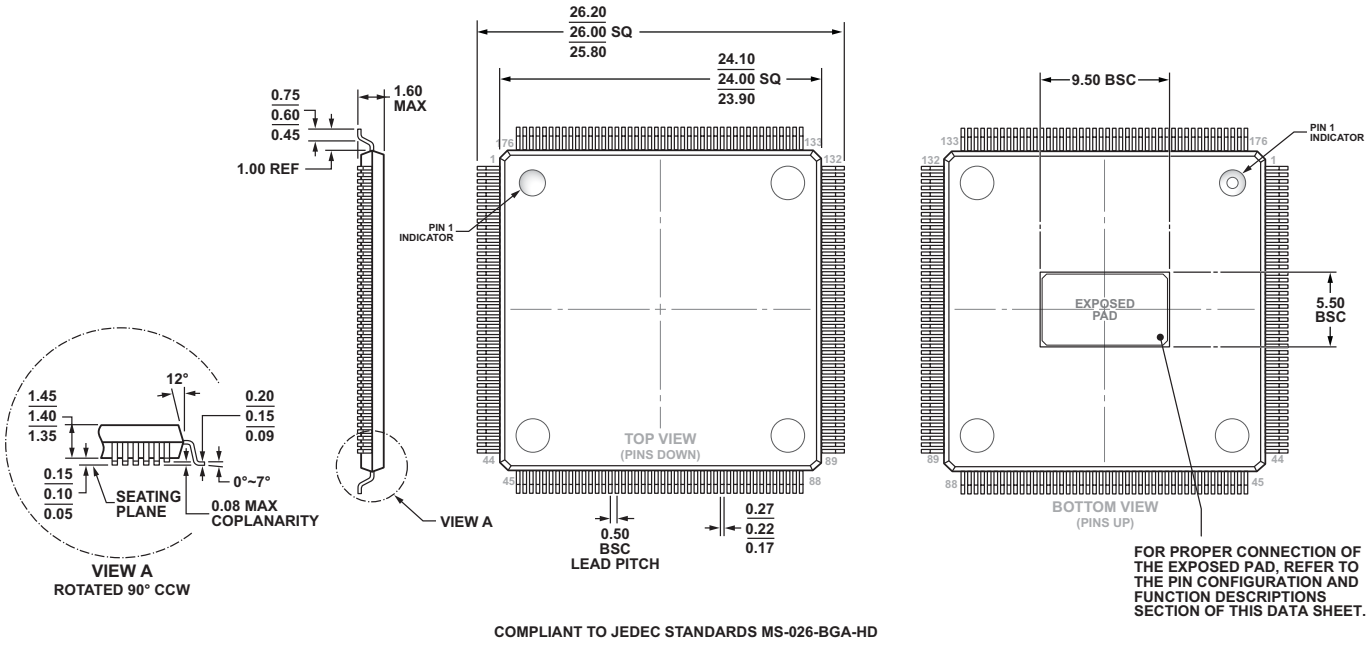
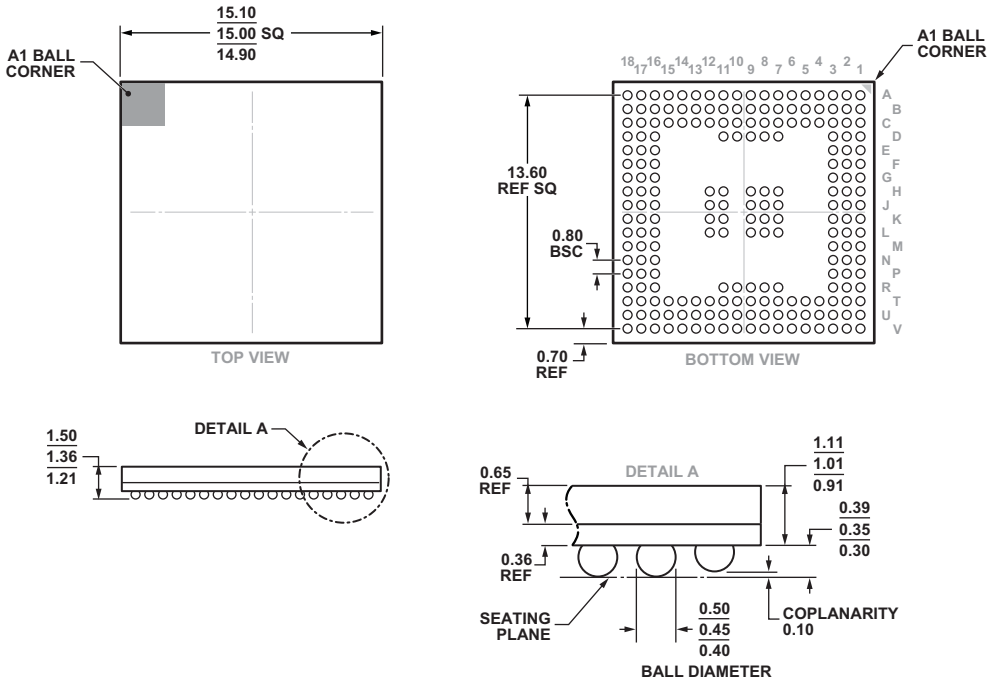


Figure 82. 176-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP][1]
(SW-176-4)
Dimensions shown in millimeters

[1] For information relating to the SW-176-4 package's exposed pad, see the table endnote in ADSP-CM41xF 176-Lead LQFP_EP Lead Assignments.



COMPLIANT TO JEDEC STANDARDS MO-275-KKAB-2

Figure 83. 210-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-210-1)
Dimensions shown in millimeters

PRE RELEASE PRODUCTS

Model	Processor Instruction Rate (Max)	Temperature Range[1, 2, 3]	Package Description	Package Option
ADSP-CM417F-SWZENG	TBD MHz	N/A	176-Lead LQFP_EP	SW-176-4
ADSP-CM419F-BCZENG	TBD MHz	N/A	210-Ball CSP_BGA	BC-210-1

[1] Referenced temperature is ambient temperature. The ambient temperature is not a specification. See Operating Conditions for the junction temperature (TJ) specification which is the only temperature specification.

[2] These are pre production parts. See ENG-Grade agreement for details.

[3] N/A means not applicable.

PR13706-0-3/18(PrC)