

300 mA very low quiescent current linear regulator IC with automatic green mode



Flip-chip 4



DFN6 1.2x1.3

Features

- Input voltage from 1.4 to 5.5 V
- Ultra low dropout voltage (300 mV typ. at 300 mA load)
- Automatic green mode
- Very low quiescent current (1 μ A in green mode, 45 μ A in normal mode and 0.1 μ A typ. in off mode)
- Output voltage tolerance: $\pm 1.0\%$ at 25 $^{\circ}$ C
- 300 mA guaranteed output current
- Wide range of output voltages available on request: adjustable from 0.8 V, fixed up to 4.0 V in 100 mV step
- Logic-controlled electronic shutdown
- Internal soft-start
- Compatible with ceramic capacitor $C_{OUT} = 330$ nF
- Internal current foldback and thermal protections
- Available in DFN6 1.2x1.3 mm and Flip-chip 4 bumps 0.69 x 0.69 mm. 0.4 pitch
- Operating temperature range: -40 $^{\circ}$ C to 125 $^{\circ}$ C
- Available in 5 k or 10 k bulk depending on output voltage

Applications

- Mobile phones
- Digital still cameras (DSC)
- Cordless phones and similar battery-powered systems
- Portable media players

Maturity status link

[LD39130S](#)

Description

The **LD39130S** is a high accuracy voltage regulator that provides 300 mA maximum current from an input voltage ranging from 1.4 V to 5.5 V, with a typical dropout voltage of 300 mV.

It is available in DFN6 1.2 x 1.3 mm package and in ultra-small CSP 4 bumps package, allowing the maximum space saving.

The device is stabilized with a ceramic capacitor on the output. The ultra-low drop voltage, low quiescent current and low noise features make it suitable for low power battery-operated applications. It integrates an internal logic circuitry, which allows the regulator to be in ultra-low consumption mode (green mode), when the output current required is very low. The normal working mode, with fast transient response, is restored when the load current increases.

The enable logic control function puts the **LD39130S** in shutdown mode allowing a total current consumption lower than 0.1 μ A. The current foldback and thermal protection are provided.

1 Block diagrams

Figure 1. Block diagram (adjustable version)

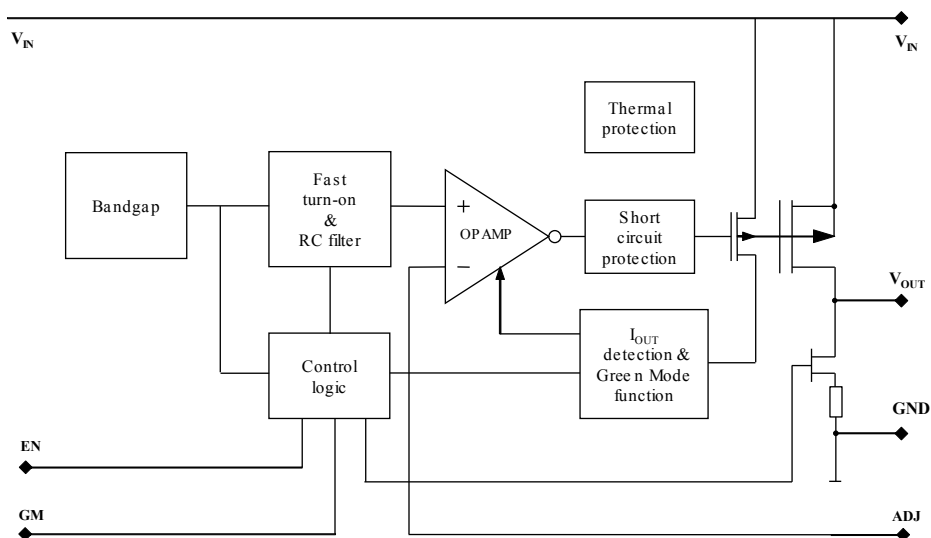
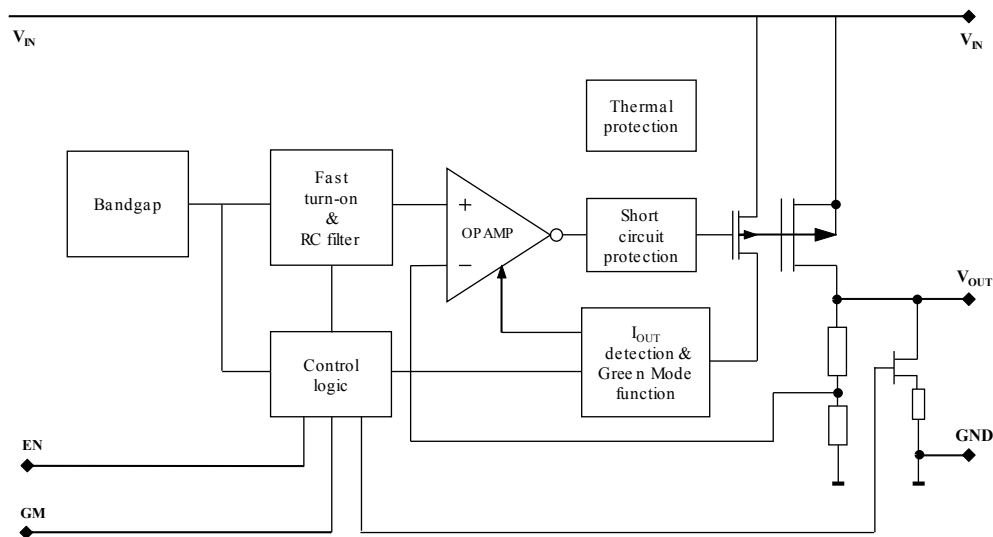


Figure 2. Block diagram (fixed version)



2 Pin configuration

Figure 3. Pin connection (top view)

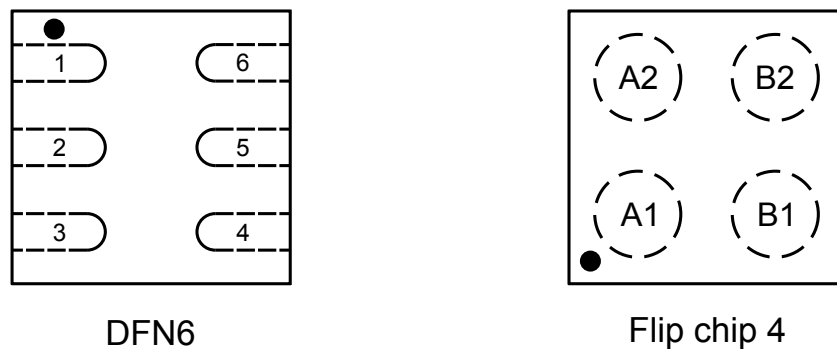


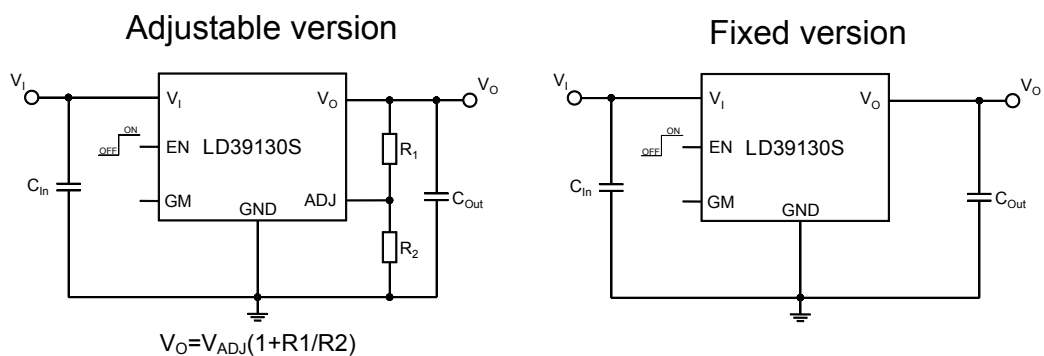
Table 1. Pin description

Pin n°		Symbol	Function
DFN6	Flip chip		
1		GM	Auto green mode selection: low = active, high = disabled. This pin is internally pulled-down to GND.
2	B2	GND	Common ground
3	B1	EN	Enable pin logic input: low = shutdown, high = active. This pin is internally pulled-down to GND.
4	A1	IN	Input voltage
5		ADJ/NC ⁽¹⁾	Adjust pin
6	A2	OUT	Output voltage

1. Not connected in the fixed output voltage version.

3 Typical applications

Figure 4. Typical application circuits



Note: **GM and ADJ pins are available on the DFN6 package only.**

4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	DC input voltage	-0.3 to 7	V
V_{OUT}	DC output voltage	-0.3 to $V_I + 0.3$	V
V_{EN}	Enable input voltage	-0.3 to $V_I + 0.3$	V
V_{GM}	Auto green mode input voltage	-0.3 to $V_I + 0.3$	V
V_{ADJ}	Adjust pin voltage	-0.3 to 2	V
I_{OUT}	Output current	Internally limited	mA
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	-65 to 150	°C
T_{OP}	Operating junction temperature range	-40 to 125	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		DFN6	Flip chip 4	
R_{thJA}	Thermal resistance junction-ambient	237	130	°C/W
R_{thJC}	Thermal resistance junction-case	104		°C/W

Table 4. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
		CDM(DFN version)	200	V
		CDM(CSP version)	300	V

5 Electrical characteristics

$T_J = 25\text{ }^{\circ}\text{C}$, $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$, $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, unless otherwise specified.

Table 5. LD39130S/LD39130SJ electrical characteristics (fixed versions)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1.4		5.5	V
V_{OUT}	V_{OUT} accuracy (normal mode)	$V_{OUT} > 2\text{ V}$, $I_{OUT} = 10\text{ mA}$, $T_J = 25\text{ }^{\circ}\text{C}$	-1.0		1.0	%
		$V_{OUT} > 2\text{ V}$, $I_{OUT} = 10\text{ mA}$, $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$	-2		2	%
		$V_{OUT} \leq 2\text{ V}$, $I_{OUT} = 10\text{ mA}$, $T_J = 25\text{ }^{\circ}\text{C}$	-20		20	mV
		$V_{OUT} \leq 2\text{ V}$, $I_{OUT} = 10\text{ mA}$, $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$	-30		30	mV
	V_{OUT} accuracy (green mode)	$V_{OUT} > 2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $T_J = 25\text{ }^{\circ}\text{C}$	-1.0		1.0	%
		$V_{OUT} > 2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$	-2		2	%
		$V_{OUT} \leq 2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $T_J = 25\text{ }^{\circ}\text{C}$	-20		20	mV
		$V_{OUT} \leq 2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$	-30		30	mV
ΔV_{OUT}	Static line regulation (normal mode)	$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $I_{OUT} = 10\text{ mA}$ $V_{IN} > 1.4\text{ V}$		0.02	0.20	%/V
	Static line regulation (green mode)	$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $I_{OUT} = 1\text{ mA}$ $V_{IN} > 1.4\text{ V}$			0.50	%/V
ΔV_{OUT}	Static load regulation	$V_{OUT} > 2\text{ V}$, $I_{OUT} = 1\text{ mA}$ to 12 mA	-1.5		1.5	%
		12 mA to 300 mA (normal mode)		0.004		%/mA
V_{DROP}	Dropout voltage ⁽¹⁾	$I_{OUT} = 300\text{ mA}$, $V_{OUT} > 2\text{ V}$, $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$		300		mV
e_N	Output noise voltage	10 Hz to 100 kHz, $I_{OUT} = 1\text{ mA}$		100		$\mu\text{V}_{RMS}/$ V_{OUT}
		10 Hz to 100 kHz, $I_{OUT} = 15\text{ mA}$		38		
SVR	Supply voltage rejection $V_{OUT} = 1.5\text{ V}$ (normal mode)	$V_{IN} = V_{OUT(NOM)} + 1\text{ V} \pm V_{RIPPLE}$, $V_{RIPPLE} = 0.1\text{ V}$, freq. = 1 kHz, $I_{OUT} = 30\text{ mA}$		70		dB
		$V_{IN} = V_{OUT(NOM)} + 0.5\text{ V} \pm V_{RIPPLE}$, $V_{RIPPLE} = 0.1\text{ V}$, freq. = 10 kHz, $I_{OUT} = 30\text{ mA}$		65		
I_Q	Quiescent current (normal mode)	$I_{OUT} = 10\text{ mA}$		45		μA
	Quiescent current (Green mode)	$I_{OUT} = 0\text{ mA}$		1	4	μA
$I_{Standby}$	Standby current	V_{IN} input current in off mode: $V_{EN} = \text{GND}$		0.1	1	μA
I_{SC}	Short-circuit current	$R_L = 0$ (current foldback protection)		50		mA
I_{OUT}	Output current		300			mA
V_{EN}	Enable input logic low	$V_{IN} = 1.4\text{ V}$ to 5.5 V , $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$			0.4	V
	Enable input logic high	$V_{IN} = 1.4\text{ V}$ to 5.5 V , $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$	1			
I_{EN}	Enable pin input current	$V_{SHDN} = V_{IN}$			100	nA
I_{GH}	Normal mode switch threshold	Change from light load to normal load $V_{GM} = \text{GND}$ ⁽²⁾			10	mA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{GL}	Green mode switch threshold	Change from normal load to light load $V_{GM} = GND$ (2)	1	2		mA
V_{GM} (2)	Green mode input logic low	$V_{IN} = 1.4\text{ V to }5.5\text{ V}, -40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$			0.4	V
	Green mode input logic high	$V_{IN} = 1.4\text{ V to }5.5\text{ V}, -40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$	1			
I_{GM} (2)	Green mode pin current				100	nA
T_{ON} (3)	Turn-on time			100		μs
R_{ON}	Output voltage discharge path resistance	$V_{EN} = GND$		100		Ω
T_{SHDN}	Thermal shutdown			160		$^{\circ}\text{C}$
	Hysteresis			20		
C_{OUT}	Output capacitor	Capacitance (see Section 7 Typical characteristics)	0.33		22	μF

- Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.
- On DFN6 package version only.
- Turn-on time is time measured between the enable input just exceeding V_{EN} high value and the output voltage just reaching 95% of its nominal value.

$T_J = 25\text{ }^{\circ}\text{C}$, $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$, $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, unless otherwise specified.

Table 6. LD39130S electrical characteristics (adjustable version)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1.4		5.5	V
V_{ADJ}	V_{ADJ} accuracy (fixed normal mode)	$I_{OUT} = 5\text{ mA}, T_J = 25\text{ }^{\circ}\text{C}$	780	800	820	mV
		$I_{OUT} = 5\text{ mA}, V_{GM} = V_{IN}, -40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$	770	800	830	mV
ΔV_{OUT}	Static line regulation (normal mode)	$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}, I_{OUT} = 10\text{ mA}, V_{IN} > 1.4\text{ V}$		0.02	0.20	%/V
	Static line regulation (green mode)	$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}, I_{OUT} = 1\text{ mA}, V_{IN} > 1.4\text{ V}$			0.20	%/V
ΔV_{OUT}	Static load regulation	$V_{OUT} > 2\text{ V}, I_{OUT} = 1\text{ mA to }12\text{ mA}$	-1.5		1.5	%
		10 mA to 300 mA (normal mode)		0.004		%/mA
V_{DROP}	Dropout voltage (1)	$I_{OUT} = 300\text{ mA}, V_{OUT} > 2\text{ V}, -40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$		300		mV
e_N	Output noise voltage	10 Hz to 100 kHz, $I_{OUT} = 1\text{ mA}, V_{OUT} = V_{ADJ}$		97		μVRMS
		10 Hz to 100 kHz, $I_{OUT} = 15\text{ mA}, V_{OUT} = V_{ADJ}$		41		
SVR	Supply voltage rejection $V_{OUT} = 1.5\text{ V}$ (normal mode)	$V_{IN} = V_{OUTNOM} + 1\text{ V} \pm V_{RIPPLE}, V_{RIPPLE} = 0.1\text{ V}, \text{freq.} = 1\text{ kHz}, I_{OUT} = 30\text{ mA}$		70		dB
		$V_{IN} = V_{OUTNOM} + 0.5\text{ V} \pm V_{RIPPLE}, V_{RIPPLE} = 0.1\text{ V}, \text{Freq.} = 10\text{ kHz}, I_{OUT} = 30\text{ mA}$		65		
I_Q	Quiescent current (normal mode)	$I_{OUT} = 10\text{ mA}$		45		μA
	Quiescent current (Green mode)	$I_{OUT} = 0\text{ mA}$		0.8	4	μA
$I_{Standby}$	Standby current	V_{IN} input current in OFF MODE: $V_{EN} = GND$		0.1	1	μA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SC}	Short-circuit current	$R_L = 0$ (current foldback protection)		50		mA
I_{OUT}	Output current		300			mA
V_{EN}	Enable input logic low	$V_{IN} = 1.4\text{ V to } 5.5\text{ V}, -40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$			0.4	V
	Enable input logic high	$V_{IN} = 1.4\text{ V to } 5.5\text{ V}, -40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$	1			
I_{EN}	Enable pin input current	$V_{SHDN} = V_{IN}$			100	nA
I_{GH}	Normal mode switch threshold	Change from light load to normal load $V_{GM} = \text{GND}$			10	mA
I_{GL}	Green mode switch threshold	Change from normal load to light load $V_{GM} = \text{GND}$	1	2		mA
V_{GM}	Green mode input logic low	$V_{IN} = 1.4\text{ V to } 5.5\text{ V}, -40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$			0.4	V
	Green mode input logic high	$V_{IN} = 1.4\text{ V to } 5.5\text{ V}, -40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$	1			
I_{GM}	Green mode pin current				100	nA
$T_{ON}^{(2)}$	Turn on time			100		μs
R_{ON}	Output voltage discharge path resistance	$V_{EN} = \text{GND}$		100		Ω
T_{SHDN}	Thermal shutdown			160		$^{\circ}\text{C}$
	Hysteresis			20		
C_{OUT}	Output capacitor	Capacitance (see Section 7 Typical characteristics)	0.33		22	μF

1. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.
2. Turn-on time is time measured between the enable input just exceeding V_{EN} high value and the output voltage just reaching 95% of its nominal value

6 Application information

6.1 Output voltage setting for ADJ version

In the adjustable version, the output voltage can be set from 0.8 V to the input voltage minus the voltage drop across the pass transistor (dropout voltage), by connecting a resistor divider between the ADJ pin and the output, allowing remote voltage sensing. The resistor divider can be determined using the following equation:

Equation 2

$$V_{OUT} = V_{ADJ} \times \left(1 + \frac{R_1}{R_2}\right) \text{ with } V_{ADJ} = 0.8V_{(typ.)} \quad (1)$$

Even if the regulator is stable with no load, the maximum value for R_2 should not exceed 2 MΩ in order to ensure the best dynamic performance.

6.2 Soft-start function

The LD39130S has an internal soft-start circuit. By increasing the startup time up to 100 μs, without the need of any external soft-start capacitor, this feature keeps the regulator inrush current at startup under control.

6.3 Auto green mode function

The LD39130S integrates an internal logic circuitry, which allows the regulator to be in ultra-low consumption mode (green mode), when the output current required is very low.

When the auto green mode is enabled, the regulator automatically selects its operating mode, switching from a very low consumption operation at light loads, to a very fast transient response mode when the load current increases.

In the LD39130S, in DFN6 package, this function can be disabled by the user, by means of an external logic pin (GM). When the GM pin is set at high logic level, the device always operates in normal mode (fast transient response), while if the GM pin is set low, the auto green mode is enabled.

The LD39130SJ (CSP version) always operates in auto green mode.

6.4 Input and output capacitors

The LD39130S requires external capacitors to ensure the regulator control loop stability. These capacitors must be selected to meet the requirements of minimum capacitance and equivalent series resistance (see [Figure 32. Stability plan vs. \(COUT, ESR\)](#)). Locating the input/output capacitors as close as possible to the relative pins, is suggested.

6.4.1 Input capacitor

A capacitor with a minimum value of 1 μF is required at the input voltage of the LD39130S. This capacitor must be located as close as possible to the input pin of the device and returned to a clean analog ground. Any good quality ceramic capacitor can be used.

6.4.2 Output capacitor

The control loop of the LD39130S is designed to work with ceramic capacitors at the output.

The output capacitor must meet the requirements for the minimum amount of capacitance and E.S.R. (equivalent series resistance) as shown in [Figure 32. Stability plan vs. \(COUT, ESR\)](#).

The suggested value of 1 μF is a good choice to guarantee the stability of the regulator and to provide the optimum transient response. The output capacitor must maintain its ESR and capacitance in the stable region, over the full operating temperature range, to assure stability.

6.5 Output discharge function

The LD39130S integrates a MOSFET connected between V_{OUT} and GND. This transistor is activated when the EN pin goes to low logic level and has the function to quickly discharge the output capacitor when the device is disabled by the user.

7 Typical characteristics

($C_{IN} = C_{OUT} = 1 \mu F$, $V_{EN} = V_{IN} = 1.8 V$, $V_{OUT} = V_{ADJ}$, $T_j = 25^\circ C$ unless otherwise specified)

Figure 5. Output voltage vs. temperature
($V_{IN} = 1.8 V$, $I_{OUT} = 5 mA$, normal mode)

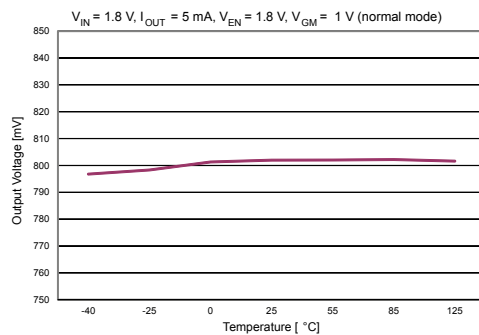


Figure 6. Output voltage vs. temperature
($V_{IN} = 1.8 V$, $I_{OUT} = 300 mA$, normal mode)

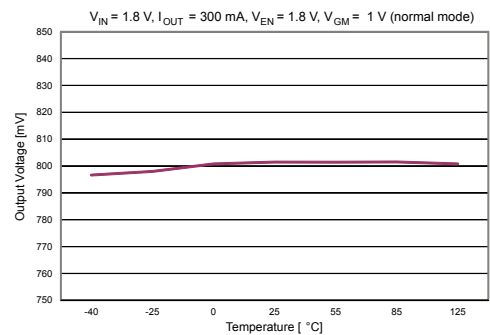


Figure 7. Output voltage vs. temperature
($V_{IN} = 1.4 V$, $I_{OUT} = 1 mA$, auto green mode)

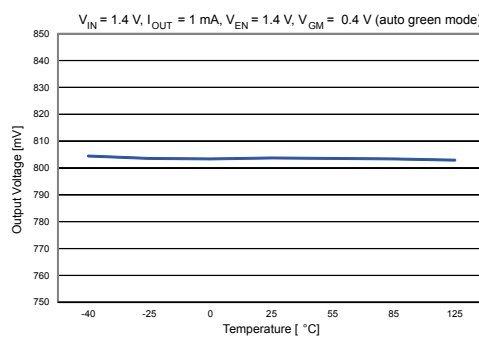


Figure 8. Output voltage vs. temperature
($V_{IN} = 5.5 V$, $I_{OUT} = 1 mA$, auto green mode)

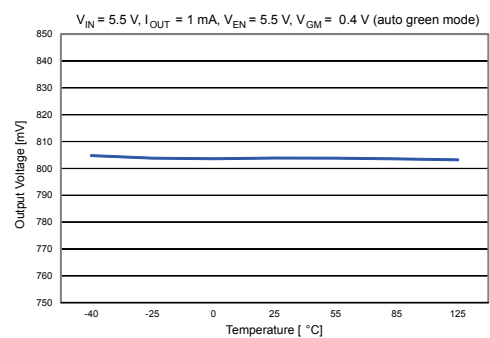


Figure 9. Line regulation vs. temperature (normal mode)

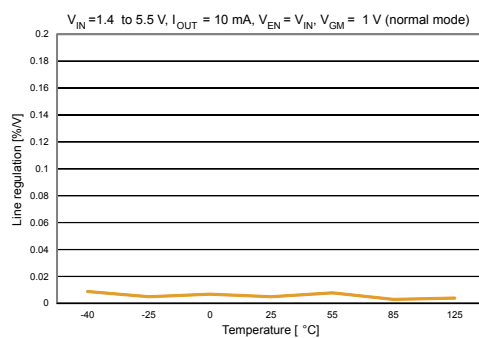


Figure 10. Line regulation vs. temperature (auto green mode)

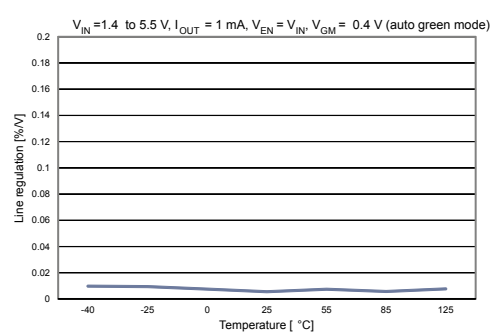


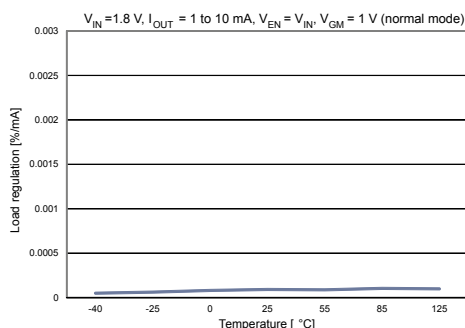
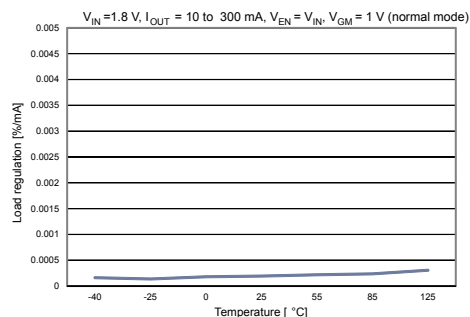
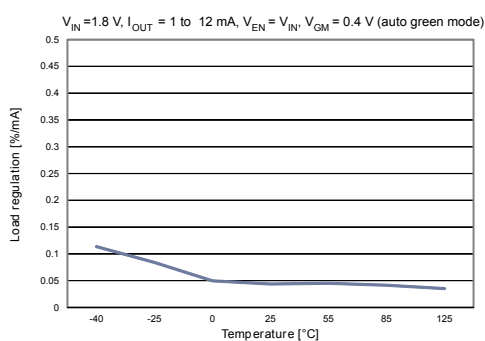
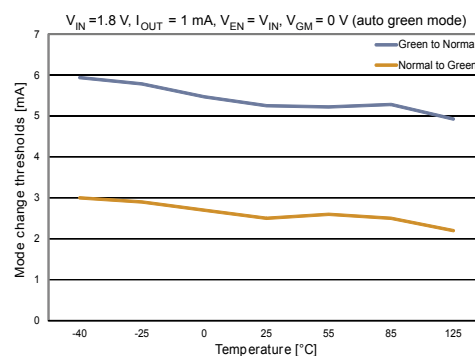
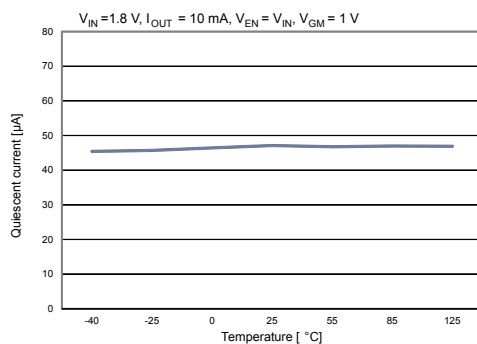
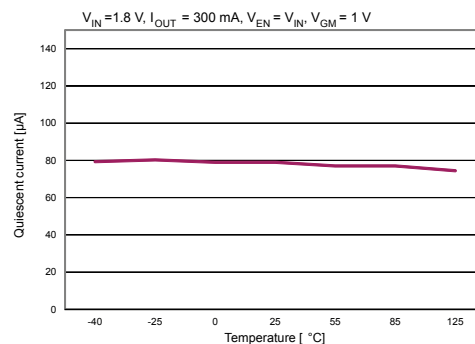
Figure 11. Load regulation vs. temperature ($I_{OUT} = 1$ to 10 mA, normal mode)

Figure 12. Load regulation vs. temperature ($I_{OUT} = 10$ to 300 mA, normal mode)

Figure 13. Load regulation vs. temperature ($I_{OUT} = 1$ to 12 mA, auto green mode)

Figure 14. Mode change thresholds vs. temperature

Figure 15. Quiescent current vs. temperature ($I_{OUT} = 10\text{ mA}$, normal mode)

Figure 16. Quiescent current vs. temperature ($I_{OUT} = 300\text{ mA}$, normal mode)


Figure 17. Quiescent current vs. temperature (no load, auto green mode)

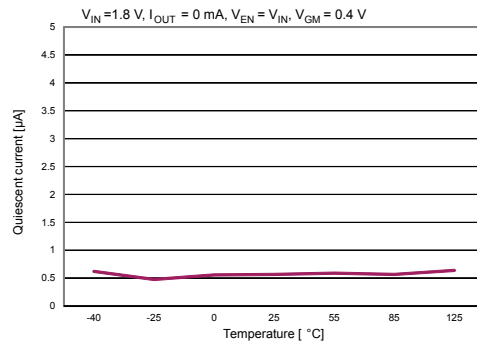


Figure 18. Shutdown current vs. temperature

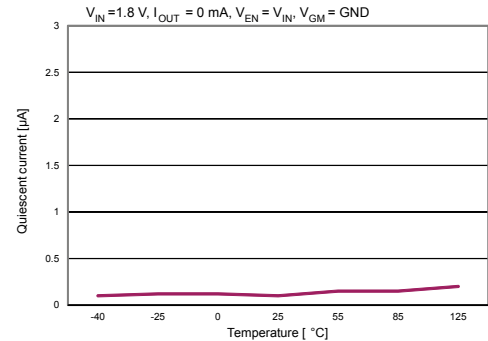


Figure 19. Quiescent current vs. input voltage (auto green mode)

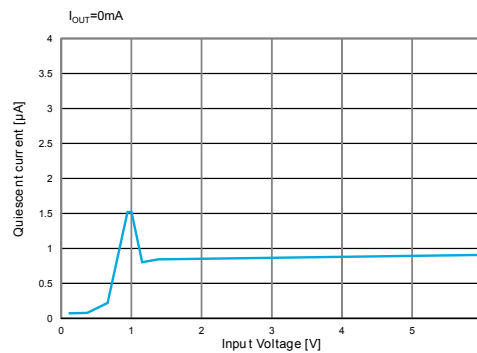


Figure 20. Quiescent current vs. input voltage (normal mode)

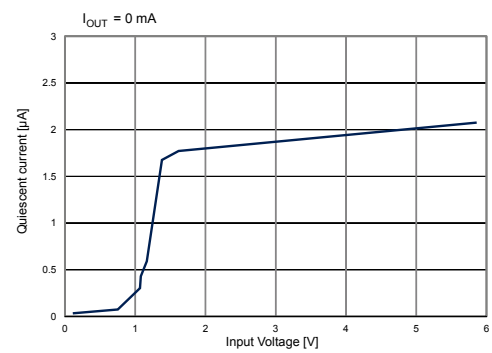


Figure 21. Quiescent current vs. output current (auto green mode)

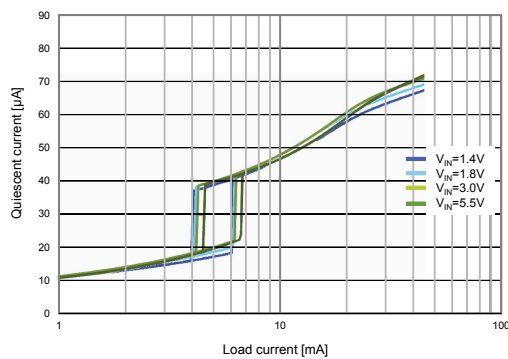


Figure 22. Quiescent current vs. load current (normal mode)

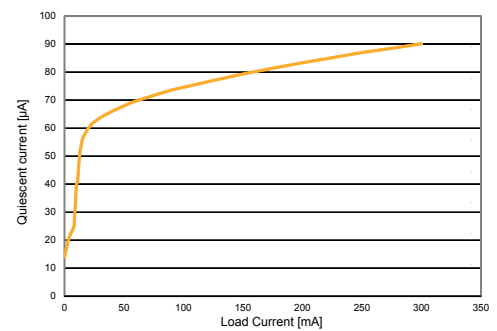


Figure 23. Quiescent current vs. load current (light load)

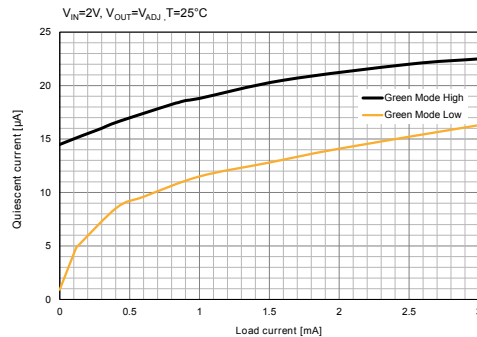


Figure 24. Short-circuit current vs. output voltage

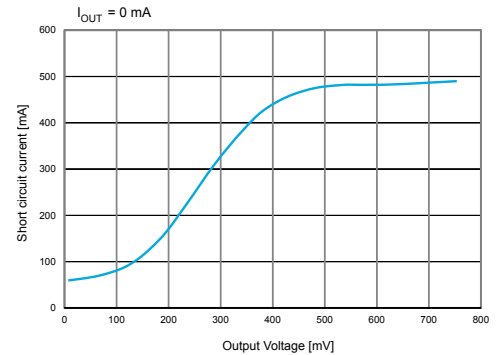


Figure 25. Foldback current vs. temperature

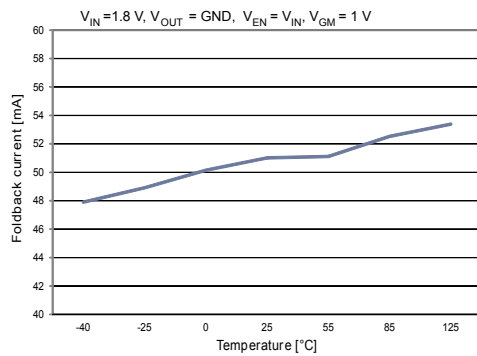


Figure 26. Dropout voltage vs. temperature

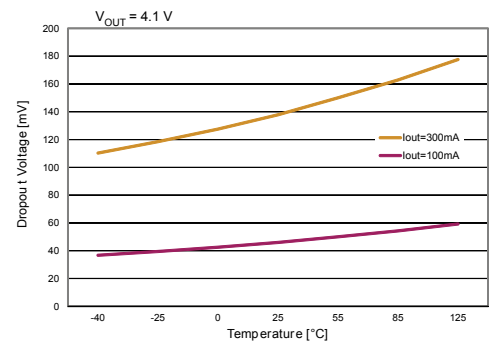


Figure 27. Dropout voltage vs. output current

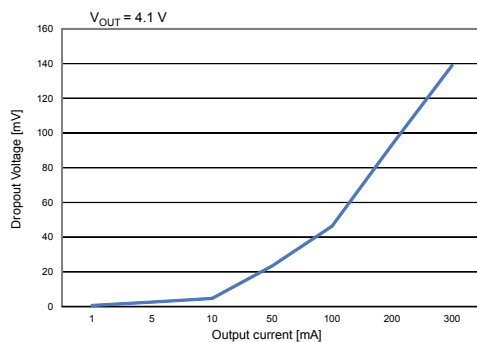


Figure 28. SVR vs. frequency (normal mode)

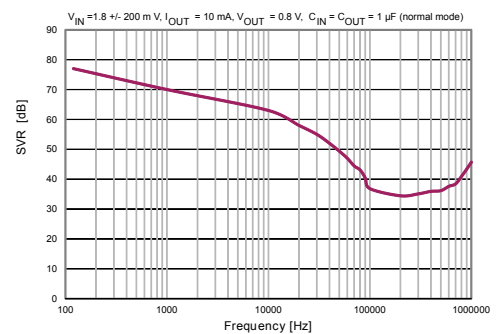


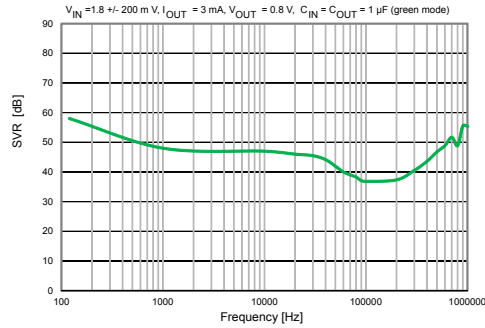
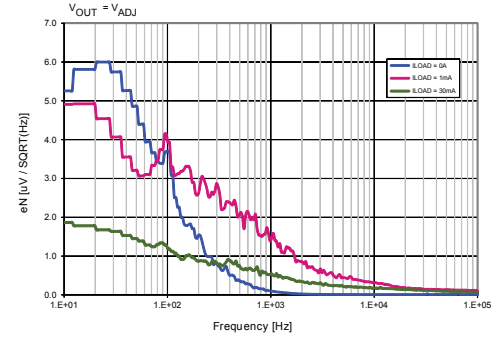
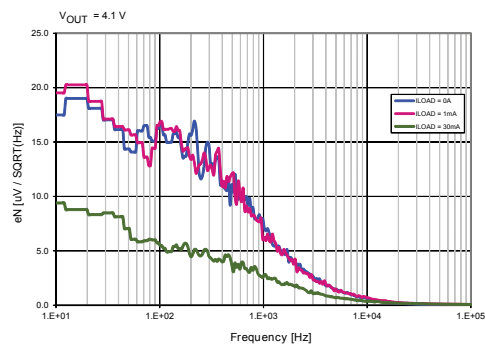
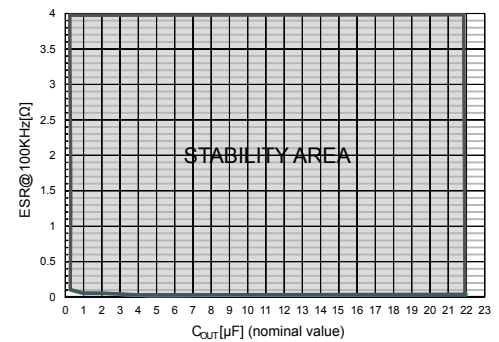
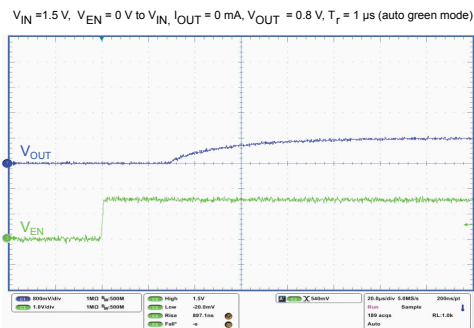
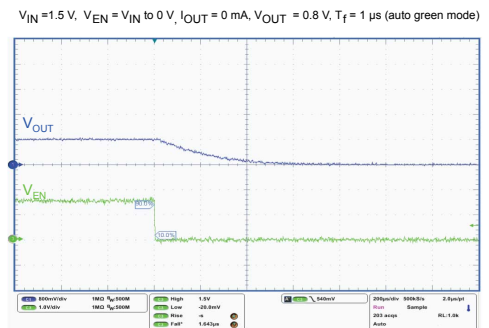
Figure 29. SVR vs. frequency (green mode)

Figure 30. Noise spectrum vs. frequency ($V_{OUT} = V_{ADJ}$)

Figure 31. Noise spectrum vs. frequency ($V_{OUT} = 4.1 \text{ V}$)

Figure 32. Stability plan vs. (C_{OUT} , ESR)

Figure 33. Startup by enable ($I_{OUT} = 0 \text{ mA}$, auto green mode)

Figure 34. Turn-off by enable ($I_{OUT} = 0 \text{ mA}$, auto green mode)


Figure 35. Startup by enable
 $V_{IN} = 1.5\text{ V}$, $V_{EN} = 0\text{ V to } V_{IN}$, $I_{OUT} = 300\text{ mA}$, $V_{OUT} = 0.8\text{ V}$, $T_f = 1\text{ }\mu\text{s}$ (auto green mode)

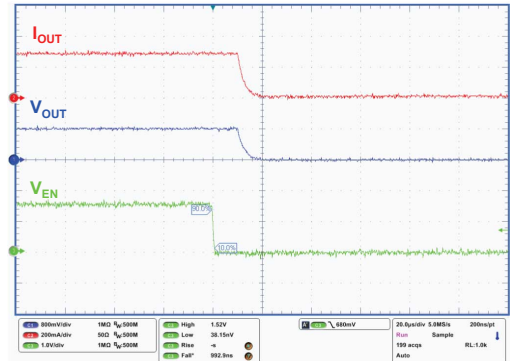
Figure 36. Turn-off by enable
 $V_{IN} = 1.5\text{ V}$, $V_{EN} = V_{IN}\text{ to } 0\text{ V}$, $I_{OUT} = 300\text{ mA}$, $V_{OUT} = 0.8\text{ V}$, $T_f = 1\text{ }\mu\text{s}$, (auto green mode)

Figure 37. Startup by enable ($I_{OUT} = 300\text{ mA}$, normal mode)
 $V_{IN} = 1.5\text{ V}$, $V_{EN} = 0\text{ V to } V_{IN}$, $V_{GM} = V_{IN}$, $I_{OUT} = 300\text{ mA}$, $V_{OUT} = 0.8\text{ V}$, $T_f = 1\text{ }\mu\text{s}$ (fixed normal mode)

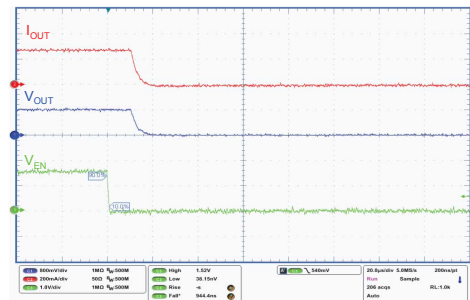
Figure 38. Turn-off by enable ($I_{OUT} = 300\text{ mA}$, normal mode)
 $V_{IN} = 1.5\text{ V}$, $V_{EN} = V_{IN}\text{ to } 0\text{ V}$, $V_{GM} = V_{IN}$, $I_{OUT} = 300\text{ mA}$, $V_{OUT} = 0.8\text{ V}$, $T_f = 1\text{ }\mu\text{s}$ (fixed normal mode)

Figure 39. Turn-on time
 $V_{IN} = V_{EN} = 0\text{ V to } 5.5\text{ V}$, $I_{OUT} = 300\text{ mA}$, $V_{OUT} = 0.8\text{ V}$, $T_f = 5\text{ }\mu\text{s}$

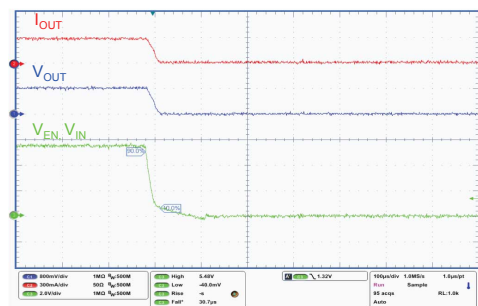
Figure 40. Turn-off time
 $V_{IN} = V_{EN} = 5.5\text{ V to } 0\text{ V}$, $I_{OUT} = 300\text{ mA}$, $V_{OUT} = 0.8\text{ V}$, $T_f = 5\text{ }\mu\text{s}$


Figure 41. Line transient (auto green mode)

$V_{IN} = V_{EN} = 1.8 \text{ V to } 2.3 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $V_{OUT} = 0.8 \text{ V}$, $T_r = 5 \mu\text{s}$ (green mode)

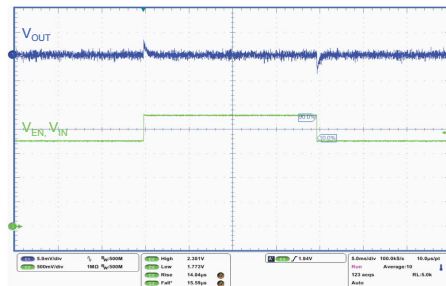


Figure 42. Line transient (normal mode)

$V_{IN} = V_{EN} = 1.8 \text{ V to } 2.3 \text{ V}$, $I_{OUT} = 12 \text{ mA}$, $V_{OUT} = 0.8 \text{ V}$, $T_r = 5 \mu\text{s}$ (normal mode)

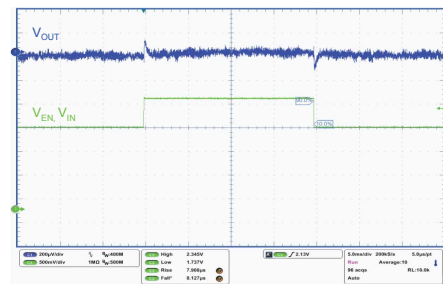


Figure 43. Load transient ($I_{OUT} = 1$ to 30 mA , auto green mode)

I_{OUT} = from 1 to 30 mA, $V_{OUT} = 0.8 \text{ V}$, $T_r = T_f = 0.5 \mu\text{s}$ (auto green mode)

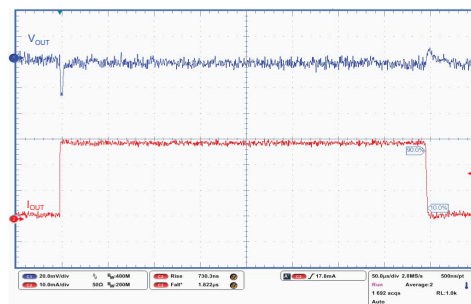


Figure 44. Load transient ($I_{OUT} = 0$ to 300 mA , auto green mode)

I_{OUT} = from 0 to 300 mA, $V_{OUT} = 0.8 \text{ V}$, $T_r = T_f = 0.5 \mu\text{s}$ (auto green mode)

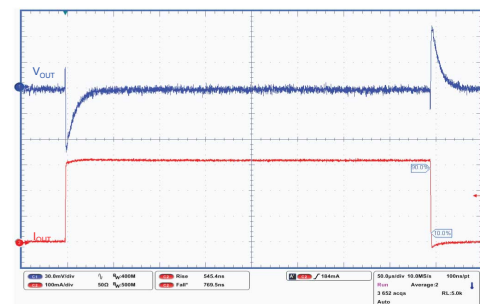


Figure 45. Load transient ($I_{OUT} = 1$ to 300 mA , normal mode)

I_{OUT} = from 1 to 300 mA, $V_{OUT} = 0.8 \text{ V}$, $T_r = T_f = 5 \mu\text{s}$, $V_{GM} = V_{IN}$ (normal mode)

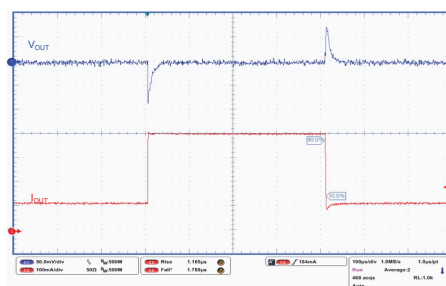
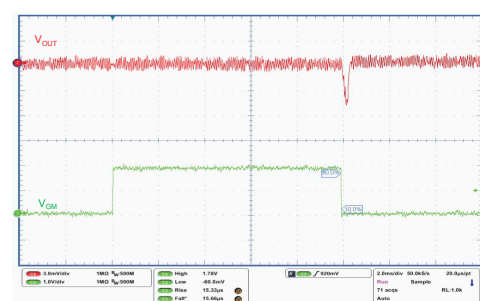


Figure 46. Green mode transient

$I_{OUT} = 0 \text{ mA}$, $V_{OUT} = 0.8 \text{ V}$, $T_r = T_f = 1 \mu\text{s}$, V_{GM} = from 0 V to V_{IN}

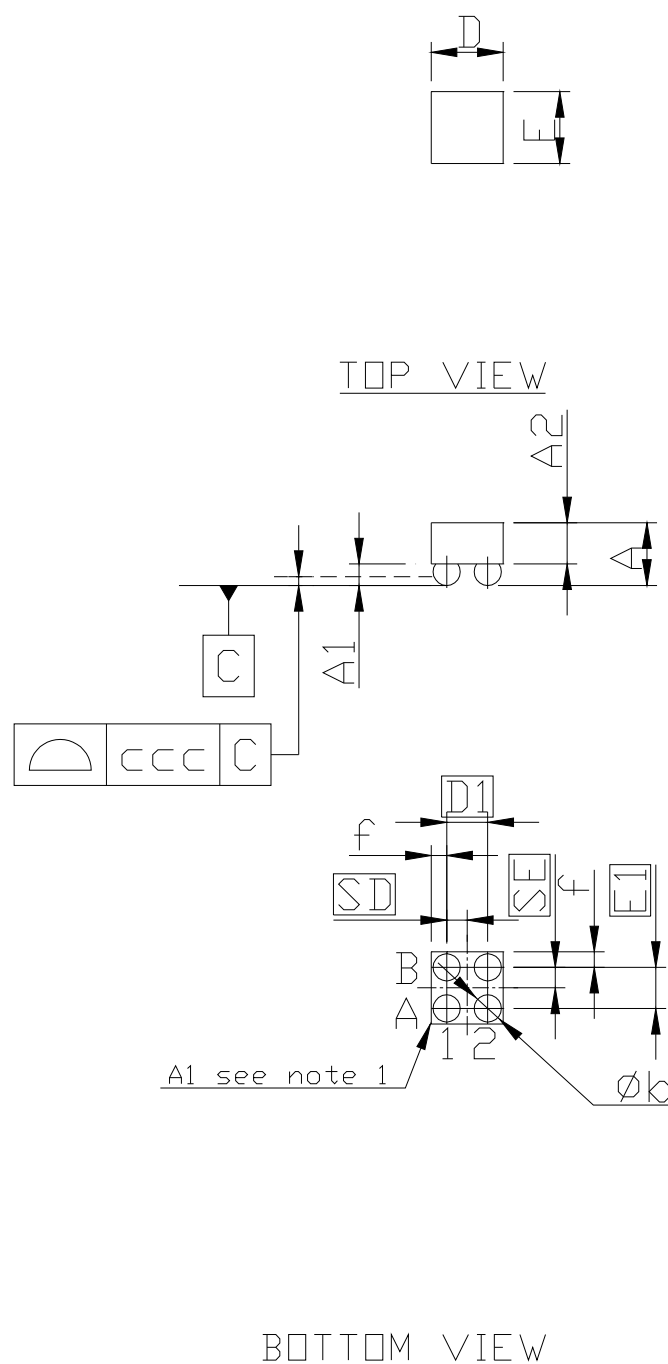


8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 Flip-chip 4 package information

Figure 47. Flip-chip 4 package mechanical outline

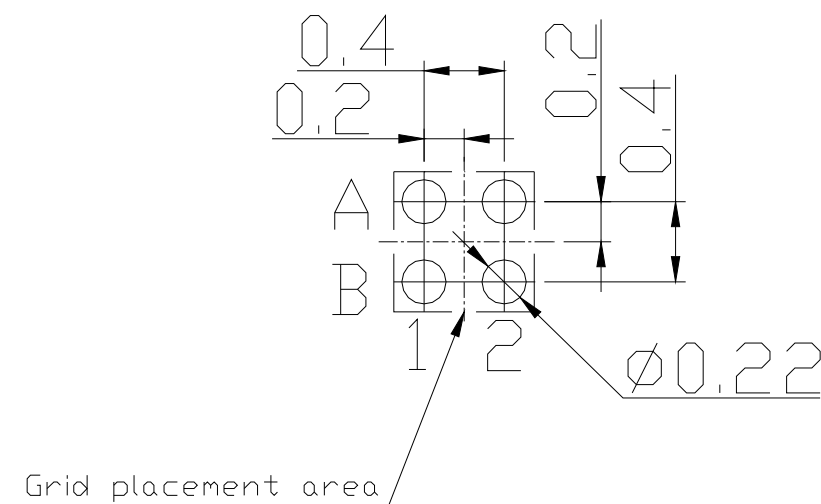


8288567 rev 5

Table 7. Flip-chip 4 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.445	0.48	0.515
A1	0.065	0.08	0.095
A2	0.38	0.40	0.42
b	0.12	0.16	0.2
D	0.66	0.69	0.72
D1		0.40	
E	0.66	0.69	0.72
E1		0.40	
f	0.135	0.145	0.155
SD/SE		0.20	
ccc			0.02

Figure 48. Flip-chip 4 package footprint



8288567 rev 5

8.2 DFN6 1.2x1.3 mm package information

Figure 49. DFN6 1.2x1.3 mm package mechanical outline

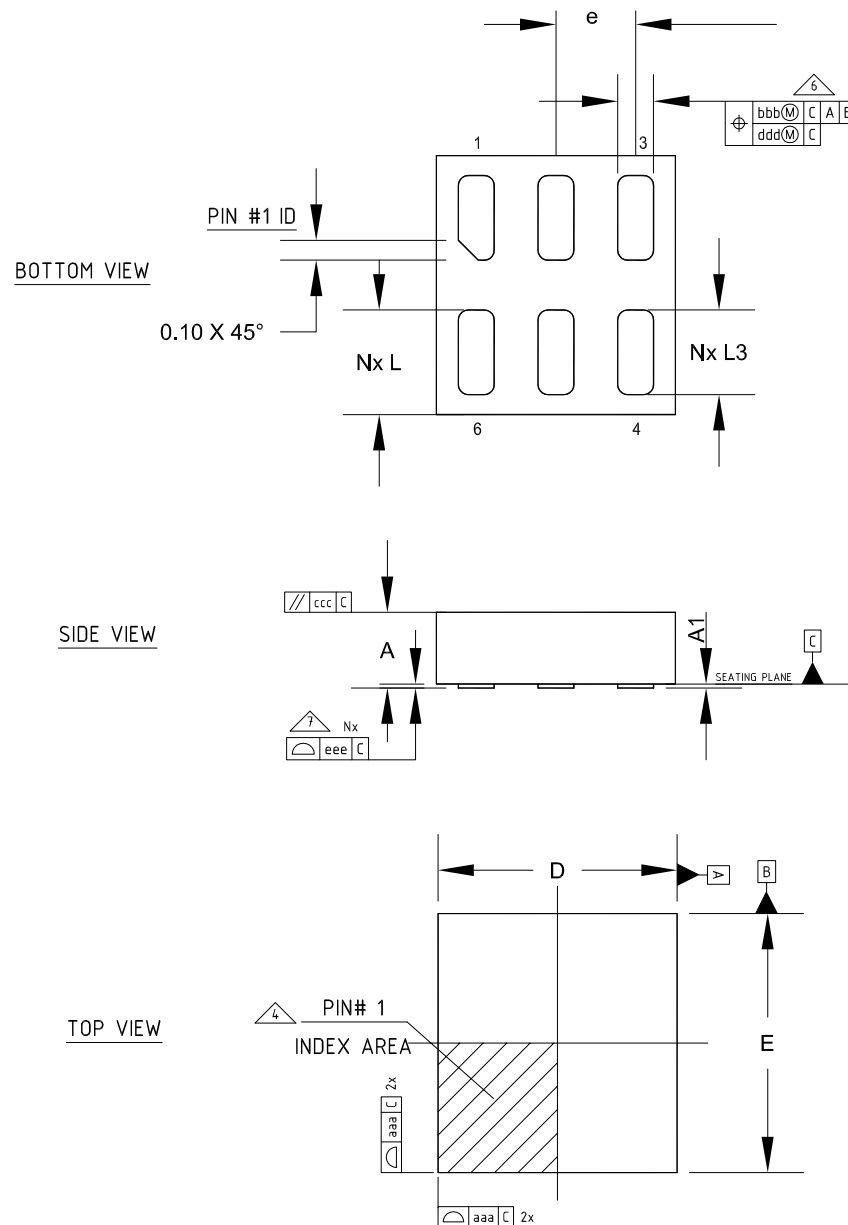
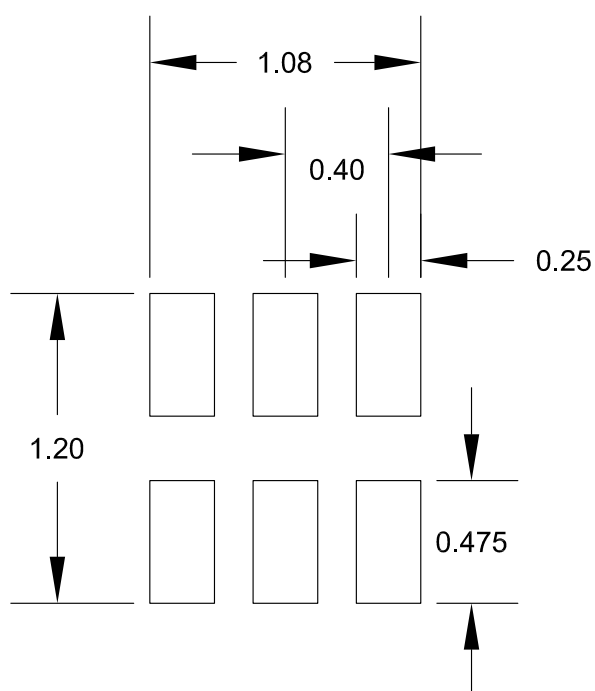


Table 8. DFN6 1.2x1.3 mm mechanical data

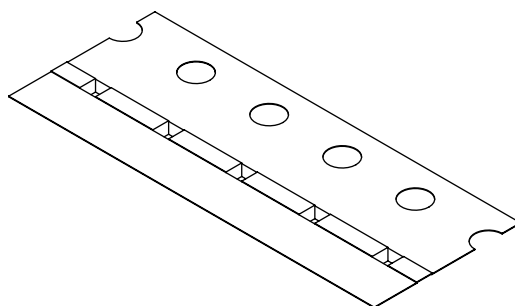
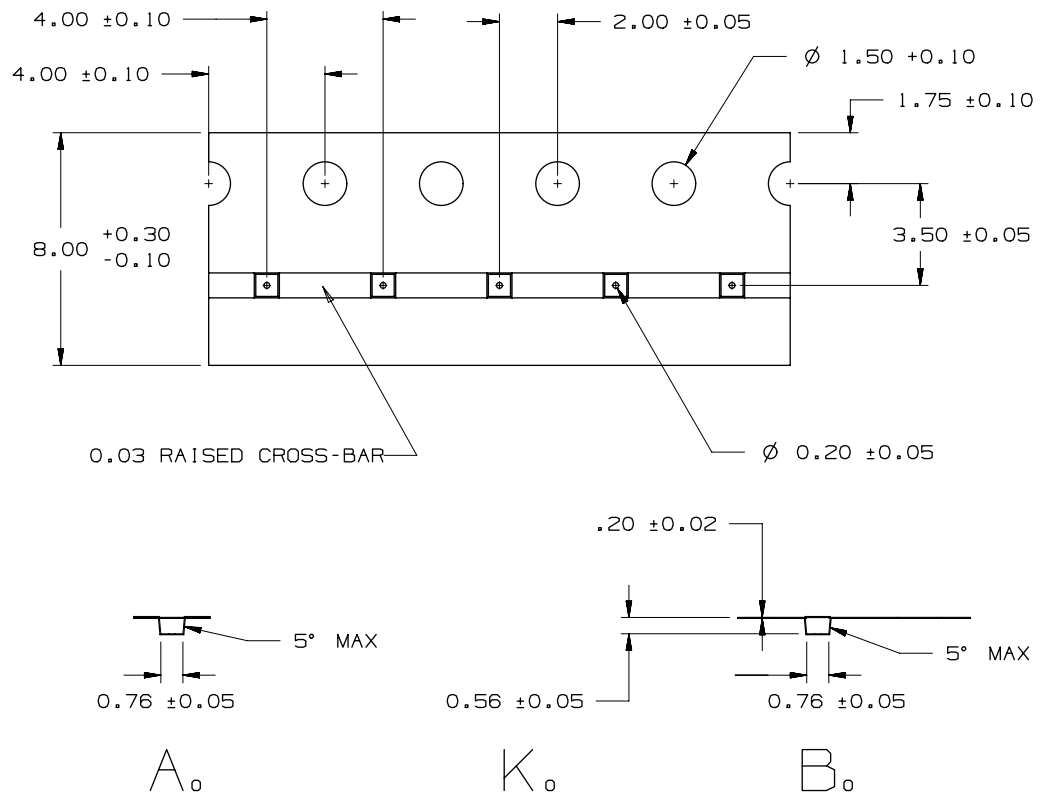
Dim.	mm		
	Min.	Typ.	Max.
A	0.31	0.38	0.40
A1	0.00	0.02	0.05
b	0.15	0.18	0.25
D	1.10	1.20	1.30
E	1.20	1.30	1.40
e	0.40 BSC		
L	0.475	0.525	0.575
L3	0.375	0.425	0.475
N	6		
ND	3		

Figure 50. DFN6 1.2x1.3 mm package footprint



9 Packing information

Figure 51. Flip-chip 4 tape



THE DIMENSIONS SHOWN ON THIS PROPOSED DRAWING ARE FOR ILLUSTRATIVE PURPOSE. DIMENSIONS FROM ACTUAL CARRIER MAY VARY SLIGHTLY.

Figure 52. Flip-chip 4 tape for LD39130SJ30R

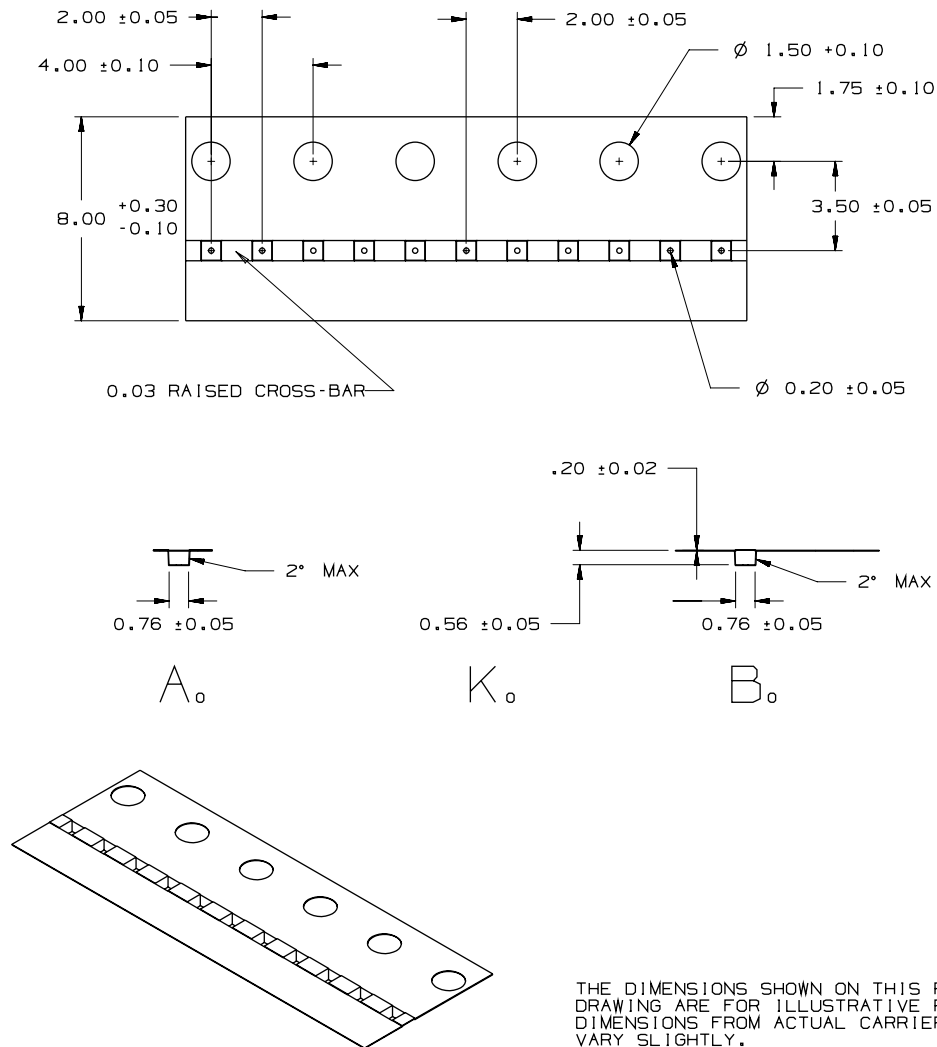


Figure 53. Flip-chip 4 reel oriented

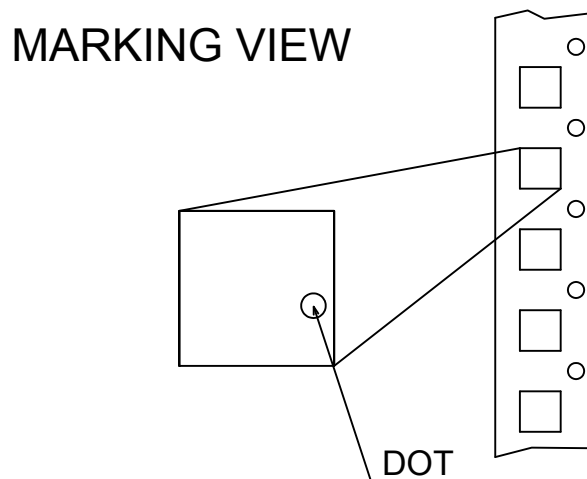
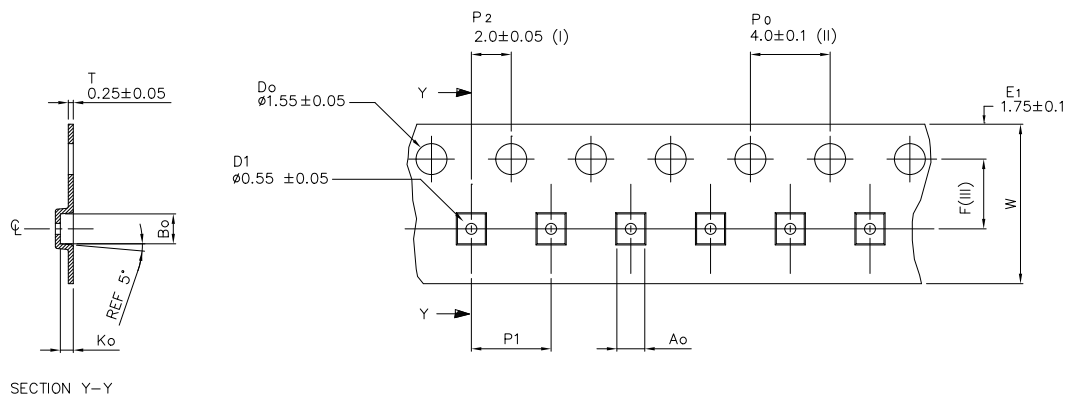


Figure 54. DFN6 tape



Ao	1.40 +/−0.05
B0	1.50 +/−0.05
K0	0.65 +/−0.05
F	3.50 +/−0.05
P1	4.00 +/−0.10
W	8.00 +/−0.30

- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
- (III) Measured from centreline of sprocket hole to centreline of pocket.
- (IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Figure 55. DFN6 reel oriented

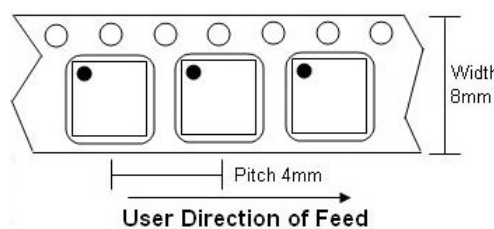
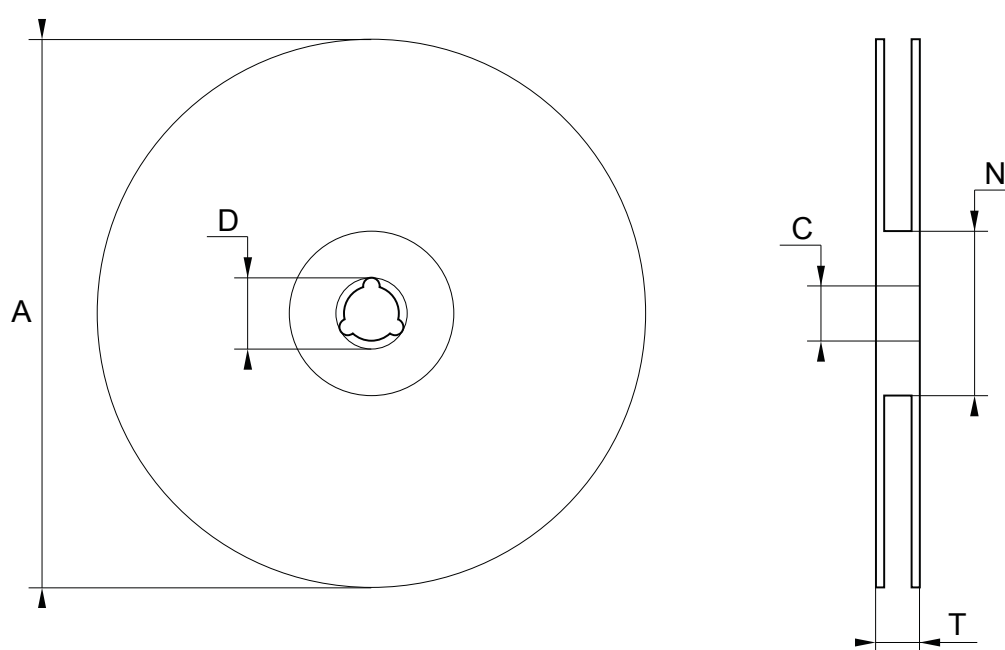


Table 9. Reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			180
C	12.8	13	13.2
D	20.2		
N	60		
T			14.4

Figure 56. Reel outline



Note: Drawing not in scale

10 Order codes

Table 10. Order codes

Order codes		Output voltages (V)	Marking digits (XY)
DFN6 1.2x1.3 mm	Flip-chip 4		
LD39130SPUR		Adjustable	AD
	LD39130SJ10R ⁽¹⁾	1.0	10
	LD39130SJ12R ⁽¹⁾	1.2	12
	LD39130SJ18R ⁽¹⁾	1.8	18
LD39130SPU25R	LD39130SJ25R ⁽¹⁾	2.5	25
	LD39130SJ29R ⁽¹⁾	2.9	29
	LD39130SJ30R ⁽²⁾	3.0	30
LD39130SPU31R		3.1	31
	LD39130SJ33R ⁽¹⁾	3.3	33
	LD39130SJ41R ⁽¹⁾	4.1	41

1. Packed in 4 mm cavity pitch, with 5 k pcs bulk.

2. Packed in 2 mm cavity pitch, with 10 k pcs bulk.

Note: Other output voltage versions available on request.

Figure 57. Flip-chip and DFN6 1.2x1.3 marking composition (marking view)


Note: “xy” indicates the marking digits, as per [Table 10. Order codes](#).

Revision history

Table 11. Document revision history

Date	Revision	Changes
08-Oct-2013	1	Initial release.
20-Jan-2015	2	Updated Figure 19: Quiescent current vs. input voltage (auto green mode) and Figure 23: Quiescent current vs. load current (light load) Updated Table 3: Thermal data, Table 4: ESD performance, Table 5: LD39130S/LD39130SJ electrical characteristics (fixed versions), Table 6: LD39130S electrical characteristics (adjustable version), Figure 19: Quiescent current vs. input voltage (auto green mode), Figure 23: Quiescent current vs. load current (light load), Figure 39: Turn-on time and Figure 41: Line transient (auto green mode). Minor text changes.
04-Apr-2018	3	Throughout document: - minor text and formatting changes In Table 1. Pin description: - updated GM and EN function descriptions Updated Figure 5. Typical application circuits Added Section 6.1 Output voltage setting for ADJ version Updated Section 7 Typical characteristics Updated Table 9. Order codes
13-Jun-2018	4	Updated Figure 50. DFN6 1.2x1.3 mm package mechanical outline.
06-Jul-2018	5	Updated Table 8. DFN6 1.2x1.3 mm mechanical data.
11-May-2020	6	Added new Figure 52 and footnote in Table 10

Contents

1	Block diagrams	2
2	Pin configuration	3
3	Typical applications	4
4	Maximum ratings	5
5	Electrical characteristics	6
6	Application information	9
6.1	Output voltage setting for ADJ version	9
6.2	Soft-start function	9
6.3	Auto green mode function	9
6.4	Input and output capacitors	9
6.4.1	Input capacitor	9
6.4.2	Output capacitor	9
6.5	Output discharge function	9
7	Typical characteristics	10
8	Package information	17
8.1	Flip-chip 4 package information	18
8.2	DFN6 1.2x1.3 mm package information	20
9	Packing information	22
10	Order codes	26
	Revision history	27
	Contents	28
	List of tables	29
	List of figures	30

List of tables

Table 1.	Pin description	3
Table 2.	Absolute maximum ratings	5
Table 3.	Thermal data	5
Table 4.	ESD performance	5
Table 5.	LD39130S/LD39130SJ electrical characteristics (fixed versions)	6
Table 6.	LD39130S electrical characteristics (adjustable version)	7
Table 7.	Flip-chip 4 mechanical data	19
Table 8.	DFN6 1.2x1.3 mm mechanical data	21
Table 9.	Reel mechanical data	25
Table 10.	Order codes	26
Table 11.	Document revision history	27

List of figures

Figure 1.	Block diagram (adjustable version)	2
Figure 2.	Block diagram (fixed version)	2
Figure 3.	Pin connection (top view)	3
Figure 4.	Typical application circuits	4
Figure 5.	Output voltage vs. temperature ($V_{IN} = 1.8\text{ V}$, $I_{OUT} = 5\text{ mA}$, normal mode)	10
Figure 6.	Output voltage vs. temperature ($V_{IN} = 1.8\text{ V}$, $I_{OUT} = 300\text{ mA}$, normal mode)	10
Figure 7.	Output voltage vs. temperature ($V_{IN} = 1.4\text{ V}$, $I_{OUT} = 1\text{ mA}$, auto green mode)	10
Figure 8.	Output voltage vs. temperature ($V_{IN} = 5.5\text{ V}$, $I_{OUT} = 1\text{ mA}$, auto green mode)	10
Figure 9.	Line regulation vs. temperature (normal mode)	10
Figure 10.	Line regulation vs. temperature (auto green mode)	10
Figure 11.	Load regulation vs. temperature ($I_{OUT} = 1\text{ to }10\text{ mA}$, normal mode)	11
Figure 12.	Load regulation vs. temperature ($I_{OUT} = 10\text{ to }300\text{ mA}$, normal mode)	11
Figure 13.	Load regulation vs. temperature ($I_{OUT} = 1\text{ to }12\text{ mA}$, auto green mode)	11
Figure 14.	Mode change thresholds vs. temperature	11
Figure 15.	Quiescent current vs. temperature ($I_{OUT} = 10\text{ mA}$, normal mode)	11
Figure 16.	Quiescent current vs. temperature ($I_{OUT} = 300\text{ mA}$, normal mode)	11
Figure 17.	Quiescent current vs. temperature (no load, auto green mode)	12
Figure 18.	Shutdown current vs. temperature	12
Figure 19.	Quiescent current vs. input voltage (auto green mode)	12
Figure 20.	Quiescent current vs. input voltage (normal mode)	12
Figure 21.	Quiescent current vs. output current (auto green mode)	12
Figure 22.	Quiescent current vs. load current (normal mode)	12
Figure 23.	Quiescent current vs. load current (light load)	13
Figure 24.	Short-circuit current vs. output voltage	13
Figure 25.	Foldback current vs. temperature	13
Figure 26.	Dropout voltage vs. temperature	13
Figure 27.	Dropout voltage vs. output current	13
Figure 28.	SVR vs. frequency (normal mode)	13
Figure 29.	SVR vs. frequency (green mode)	14
Figure 30.	Noise spectrum vs. frequency ($V_{OUT} = V_{ADJ}$)	14
Figure 31.	Noise spectrum vs. frequency ($V_{OUT} = 4.1\text{ V}$)	14
Figure 32.	Stability plan vs. (COUT, ESR)	14
Figure 33.	Startup by enable ($I_{OUT} = 0\text{ mA}$, auto green mode)	14
Figure 34.	Turn-off by enable ($I_{OUT} = 0\text{ mA}$, auto green mode)	14
Figure 35.	Startup by enable	15
Figure 36.	Turn-off by enable	15
Figure 37.	Startup by enable ($I_{OUT} = 300\text{ mA}$, normal mode)	15
Figure 38.	Turn-off by enable ($I_{OUT} = 300\text{ mA}$, normal mode)	15
Figure 39.	Turn-on time	15
Figure 40.	Turn-off time	15
Figure 41.	Line transient (auto green mode)	16
Figure 42.	Line transient (normal mode)	16
Figure 43.	Load transient ($I_{OUT} = 1\text{ to }30\text{ mA}$, auto green mode)	16
Figure 44.	Load transient ($I_{OUT} = 0\text{ to }300\text{ mA}$, auto green mode)	16
Figure 45.	Load transient ($I_{OUT} = 1\text{ to }300\text{ mA}$, normal mode)	16
Figure 46.	Green mode transient	16
Figure 47.	Flip-chip 4 package mechanical outline	18
Figure 48.	Flip-chip 4 package footprint	19
Figure 49.	DFN6 1.2x1.3 mm package mechanical outline	20
Figure 50.	DFN6 1.2x1.3 mm package footprint	21

Figure 51.	Flip-chip 4 tape	22
Figure 52.	Flip-chip 4 tape for LD39130SJ30R	23
Figure 53.	Flip-chip 4 reel oriented	24
Figure 54.	DFN6 tape	24
Figure 55.	DFN6 reel oriented	24
Figure 56.	Reel outline	25
Figure 57.	Flip-chip and DFN6 1.2x1.3 marking composition (marking view)	26

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2020 STMicroelectronics – All rights reserved