Rugged, Military Temperature Range, 10 kHz Bandwidth Isolation Amplifier

AD203SN

FEATURES

Rugged Design characterized to MIL-STD-883C
- **Environmental Test Methods**
  - **1004 (Moisture Resistance)**
  - **1010 Condition B (Temperature Cycling, −55°C to +125°C)**
  - **2002 Condition B (Mechanical Shock @ 1,500 g for 0.5 ms)**
  - **2004 (Lead Integrity)**
  - **2007 Condition A (Variable Frequency Vibration @ 20 g)**
  - **2015 (Resistance to Solvents)**

Reliable Design: Conforms to Stringent Quality and Reliability Standards
Characterized to the Full Military Temperature Range −55°C to +125°C Rated Performance
10 kHz Full Power Bandwidth
Low Nonlinearity: ±0.025% max
Wide Output Range: ±10 V min (Into a 2.5 kΩ Load)
High CMV Isolation: 1500 V RMS Continuous
Isolated Power: ±15 V DC @ ±5 mA
Small Size: 2.23″×0.83″×0.65″
56.6 mm×21.1 mm×16.5 mm
Uncommitted Input Amplifier
Two-Port Isolation Through Transformer Coupling

ISOLATION AMPLIFIERS

Provide Galvanic Isolation Between the Input and Output Stages
Eliminate Ground Loops
Reject High Common Mode Voltages and Noise
Protect Sensitive Electronic Signal Processing Systems from Transient and/or Fault Voltages

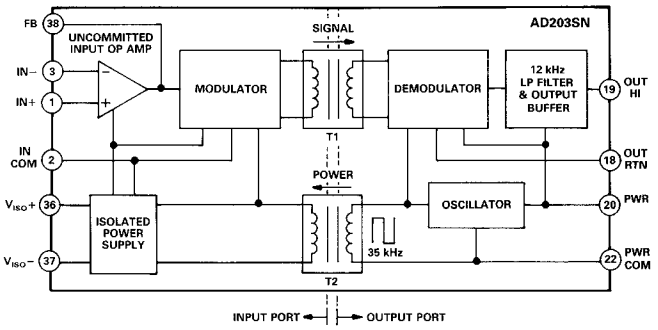
APPLICATIONS INCLUDE

Engine Monitoring and Control
Mobile Multichannel Data Acquisition Systems
Instrumentation and/or Control Signal Isolation
Current Shunt Measurements
High Voltage Instrumentation Amplifier

GENERAL DESCRIPTION

The AD203SN is designed and built expressly for use in hostile operating environments. The AD203SN is also an integral member of Analog Devices' AD200 Series of low cost, high performance, transformer coupled isolation amplifiers. Technological innovations in circuit design, transformer construction, surface mount components and assembly automation have resulted in a rugged, economical, military temperature range isolator that either retains or improves upon the key performance specifications of the AD202/AD204 line.

FUNCTIONAL BLOCK DIAGRAM



The AD203SN provides total galvanic isolation between the input and output stages of the isolation amplifier, including the power supplies, through the use of internal transformer coupling. The functionally complete design of the AD203SN, powered by a single +15 V dc supply, eliminates the need for an external dc/dc converter. This permits the designer to minimize the necessary circuit overhead and consequently reduce the overall design and component costs. Furthermore, the power consumption, nonlinearity and drift characteristics of transformer coupled devices are vastly superior to those achievable with other isolation technologies, without sacrificing bandwidth or noise performance. Finally, the AD203SN will maintain its high operating performance even under sustained common mode stress.

The design of the AD203SN emphasizes maximum flexibility and ease of use in a broad range of applications where signals must be measured or transmitted under high CMV conditions. The AD203SN has a ±10 V output range, an uncommitted input amplifier, an output buffer, a 10 kHz full power bandwidth and a front-end isolated power supply of ±15 V dc @ ±5 mA.

Rev. B
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
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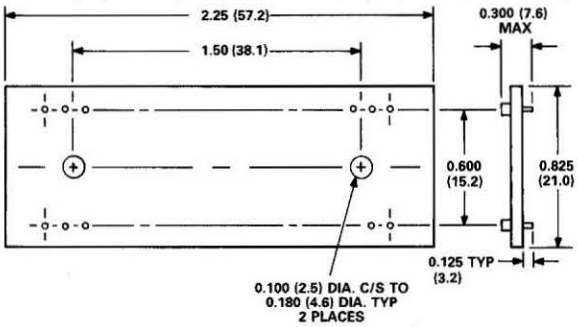
AD203SN—SPECIFICATIONS (typical @ +25°C, V_S = +15 V dc unless otherwise noted)

GAIN	
Range	1 V/V–100 V/V
Error	±1% typ (±4% max)
vs. Temperature[1]	
−55°C to +125°C	50 ppm/°C
−55°C to +25°C	100 ppm/°C
−40°C to +25°C	80 ppm/°C
−25°C to +25°C	60 ppm/°C
+25°C to +125°C	5 ppm/°C
vs. Time	±50 ppm/1000 hours
vs. Supply Voltage	±0.005%/V
Nonlinearity[2], G=1 V/V, ±10 V Output Swing	±0.012% (±0.025% max)
INPUT VOLTAGE RATINGS	
Linear Differential Range	±10 V
Max CMV Input to Output	
AC, 60 Hz, Continuous	1500 V rms
Continuous (ac and dc)	±2000 V peak
Common Mode Rejection (CMR) @ 60 Hz	
$R_S \leq 100\ \Omega$ (HI & LO Inputs), G = 1 V/V	106dB
G = 100 V/V	120dB
$R_S \leq 1\ k\Omega$ (Input, HI, LO or Both), G = 1–100 V/V	96dB (min)
Leakage Current, Input to Output @ 240 V rms, 60 Hz	4.0μA rms (max)
INPUT IMPEDANCE	
Differential (G = 1 V/V)	$10^{12}\ \Omega$
Common Mode	2 GΩ‖4.5 pF
INPUT BIAS CURRENT	
Initial @ +25°C	30 pA
Current @ +125°C	30 nA
INPUT DIFFERENCE CURRENT	
Initial @ +25°C	±5 pA
Current @ +125°C	±5 nA
INPUT NOISE	
Voltage, 0.1 Hz to 100 Hz	4 μV p–p
Voltage, Frequency > 200 Hz	50 nV/$\sqrt{\text{Hz}}$
FREQUENCY RESPONSE	
Bandwidth ($V_{OUT} \leq 20$ V p–p, G = 1–100 V/V)	10 kHz
Slew Rate	0.5 V/μs
Settling Time to ±0.10%	160 μs
OFFSET VOLTAGE, REFERRED TO INPUT (RTI)	
Initial @ +25°C (Adjustable to Zero)	± (5 + 25/G) mV (max)
vs. Temperature (−55°C to +125°C)	± (6 + 100/G) μV/°C
RATED OUTPUT[3]	
Voltage (Out HI to Out LO) @ R_L = 5.0 kΩ	±10 V (min)
Current	±4 mA
Maximum Capacitive Load[4]	270 pF
Output Resistance	0.2 Ω
Output Ripple, 100 kHz Bandwidth	15 mV p–p
5 kHz Bandwidth	0.7 mV rms
ISOLATED POWER OUTPUT[5]	
Voltage, No Load	±15 V
Accuracy	±5%
Current (Either Output)	5 mA
Regulation, No Load to Full Load	5%
Ripple, 100 kHz Bandwidth, Full Load	110 mV p–p
POWER SUPPLY	
Voltage, Rated Performance	+15 V dc (±5%)
Voltage, Operating Performance[6]	+12 V dc to +16 V dc
Current, No Load (V_S = +15 V dc)	20 mA

TEMPERATURE RANGE	
Rated Performance	−55°C to +125°C
Storage	−55°C to +125°C
PACKAGE DIMENSIONS	
Inches	2.23 × 0.83 × 0.65
Millimeters	56.6 × 21.1 × 16.5

NOTES
[1]Refer to Figure 1 for a plot of gain versus temperature.
[2]For gains greater than 50 V/V, a 100 pF capacitor from the feedback terminal of the input op amp (Pin 38) to the input common terminal (Pin 2) is recommended in order to minimize the gain nonlinearity. Refer to Figure 17 for a circuit schematic.
[3]For additional information on the Rated Output parameters, refer to Figure 9 for a plot of the Output Voltage Swing vs. Power Supply Voltage, and Figure 10 for the Output Current vs. Temperature and Power Supply Voltage relationship.
[4]For larger capacitive loads, it is recommended that a 4.7 Ω resistor be placed in series with the load in order to suppress possible output oscillations.
[5]1.0 μF (min) decoupling is required.
[6]Refer to Figure 9 for a plot of output voltage swing versus supply voltage.
Specifications subject to change without notice.

AC1062 MATING SOCKET



AD203SN PIN DESIGNATIONS

PIN	DESIGNATION	FUNCTION	PORT
1	IN+	INPUT OP AMP: NONINVERTING INPUT	INPUT
2	IN COM	INPUT COMMON	INPUT
3	IN−	INPUT OP AMP: INVERTING INPUT	INPUT
18	OUT RTN	OUTPUT RETURN	OUTPUT
19	OUT HI	OUTPUT SIGNAL	OUTPUT
20	PWR IN	DC POWER SUPPLY INPUT	OUTPUT
21	NONE	NONE	–
22	PWR COM	DC POWER SUPPLY COMMON	OUTPUT
36	V_{ISO}+	ISOLATED POWER: +DC	INPUT
37	V_{ISO}−	ISOLATED POWER: −DC	INPUT
38	FB	INPUT OP AMP: OUTPUT/FEEDBACK	INPUT

CONTROLLING DIMENSIONS ARE IN INCHES, MILLIMETER DIMENSIONS ARE CONVERTED EQUIVALENTS AND SHOULD NOT BE USED FOR DESIGN.

CAUTION

ESD (electrostatic discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be discharged to the destination socket before devices are removed.

Note: Per MIL-STD-883C, Method 3015, this device have been classified as a Category 2 ESD sensitive device.



PRODUCT HIGHLIGHTS

Rugged Design. The AD203SN is specifically designed for applications where ruggedness and high performance are the key requirements. The ruggedness of the AD203SN design meets MIL-STD-883C Methods 1004 (Moisture Resistance), 1010 Condition B (Temperature Cycling, −55°C to +125°C), 2002 Condition B (Mechanical Shock @ 1,500 g for 0.5 ms), 2004 (Lead Integrity), 2007 Condition A (Variable Frequency Vibration @ 20 g) and 2015 (Resistance to Solvents).

Engine and vehicular monitor/control systems as well as mobile instrumentation and control systems are some examples of applications for which the AD203SN is well suited.

Military Temperature Range Rating. With its performance rated over the −55°C to +125°C MIL specification temperature range, the AD203SN is an excellent choice in applications where severe environmental conditions may be encountered. Examples include engine monitoring/control systems and remote power line monitoring.

10 kHz Bandwidth. With a full power bandwidth of 10 kHz, the AD203SN is effective in control loop applications where a smaller bandwidth could induce control system instabilities.

Excellent Common Mode Performance. The AD203SN provides a 1.5 kV rms continuous common mode isolation. A low common mode input capacitance of 4.5 pF, inclusive of power isolation, results in a minimum 96 dB of CMR as well as a very low leakage current of 4.0 μA rms (max @ 240 V rms, 60 Hz).

High Accuracy. Exhibiting a maximum nonlinearity of ±0.025% and a low gain temperature coefficient, averaging 50 ppm/°C over the full temperature range, the AD203SN provides high isolation without loss of signal integrity and quality.

Isolated Power. An isolated power supply capable of delivering ±15 V dc @ ±5 mA is available at the input port of the isolator. This permits the AD203SN to power up floating signal conditioners, front-end amplifiers or remote transducers at the input.

Flexible Input Stage. An uncommitted op amp is provided on the input stage. This amplifier provides input buffering and gain as needed. It also facilitates a host of alternative input functions including filtering, summing, high voltage ranges and current (transimpedance) inputs.

DESCRIPTION OF KEY SPECIFICATIONS

Gain Nonlinearity. Nonlinearity is defined as the peak deviation of the output voltage from the best straight line and is expressed as a percent of peak-to-peak output voltage span. The nonlinearity of the model AD203SN, which operates at a 20 V p–p output span, is ±0.025% or ±5 mV. Good nonlinearity is critical for retaining signal fidelity.

Max CMV, Input to Output. Maximum common mode voltage (CMV) describes the amount of voltage that may be applied across both input terminals with respect to the output terminals without degrading the integrity of the isolation barrier. High input-to-output CMV capability is necessary in applications where high CMV inputs exist or high voltage transients may occur at the input.

Common Mode Rejection (CMR). CMR describes the isolator's ability to reject common mode voltages that may exist between the inputs and the outputs. High CMR is required when it is necessary to process small signals riding on high common mode voltages.

Leakage Current. This is the current that flows from the input common across the isolation barrier to the output common when the power-line voltage (either 115 V or 240 V rms, 60 Hz) is impressed on the inputs. Leakage current is dependent on the magnitude of the coupling capacitance between the input and the output ports. Line frequency leakage current levels are unaffected by the power ON or OFF condition of the AD203SN.

Common Mode Input Impedance. This is defined to be the impedance seen across either input terminal (i.e., +IN or −IN) and the input common.

Input Noise. This specification characterizes the voltage noise levels that are generated internally by the isolation amplifier. In order to facilitate a comparison between the "isolator background noise" levels and the expected input signal levels the input noise parameter is referred to the input.

Input noise is a function of the noise bandwidth, i.e., the frequency range over which the noise characteristics are measured.

Offset Voltage, Referred to Input (RTI). The offset voltage describes the isolation amplifier's total dc offset voltage with the inputs grounded. The offset voltage is referred to the input in order to allow for a comparison of the dc offset voltages with the expected input signal levels. The total offset comes from two sources, namely from the input and output stages, and is gain dependent. To compute the offset voltage, RTI, the isolator is modelled as two cascaded amplifier stages. The input stage has a variable gain G while the output isolation stage has a fixed gain of 1. RTI offset is then given by:

$$E_{OS}\,(RTI) = E_{OS1} + E_{OS2}/G$$

where:

E_{OS1} = Total input stage offset voltage

E_{OS2} = Output stage offset voltage

G = Input stage gain.

Offset voltage drift, RTI, is calculated in an identical manner.

Isolated Power Output. Dual supply voltages, completely isolated from the input power supply terminals, provide the capability to excite floating input signal conditioners as well as remote transducers.

PERFORMANCE CHARACTERISTICS

This section details the key specifications of the AD203SN that exhibit a functional dependence on such variables as frequency, power supply load, output voltage swing, bypass capacitance and temperature. Table I summarizes the performance characteristics that will be discussed in this section. For the sake of completeness, a typical dynamic output response of the AD203SN is included.

Gain Temperature Coefficient. Figure 1 presents the AD203SN's gain temperature coefficient over the entire −55°C to +125°C temperature range.

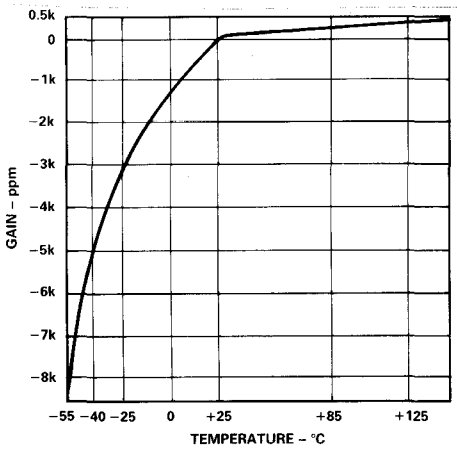


Figure 1. Gain (ppm of Span) vs. Temperature (°C)

Note: 1 ppm (part per million) is equivalent to 0.0001%.

Gain Nonlinearity. The maximum nonlinearity error of the AD203SN, at a gain of 1 V/V, is specified as ±0.025% or ±5 mV. The nonlinearity performance of the AD203SN is dependent on the output voltage swing and this dependency is illustrated in Figure 2. The horizontal axis represents the gain error, expressed either in percent of peak-to-peak output span (i.e., % of 20 V) on the left axis or in mV on the right axis. The vertical axis indicates the magnitude of the output voltage swing.

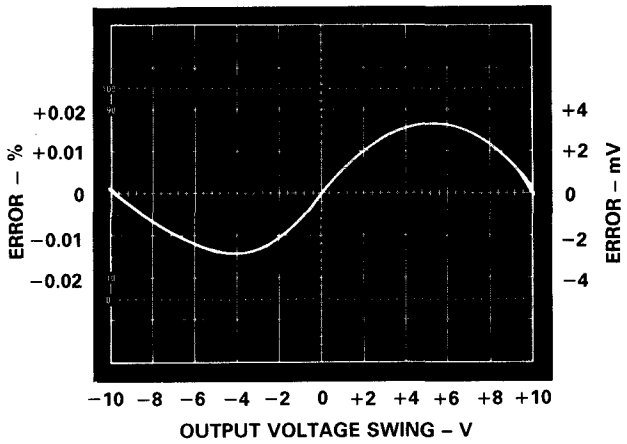


Figure 2. Gain Nonlinearity Error (% p–p Output Range and mV) vs. Output Voltage Swing (V), with a Gain of 1 V/V

Parameter	Key Specifications	As a Function of	Shown In
Gain	Gain (ppm of Span) Gain Nonlinearity (Expressed in mV and % of p–p Output)	Temperature (°C) Output Voltage Swing (V)	Figure 1 Figure 2
Input Voltage Rating	Common Mode Rejection (dB)	Common Mode Signal Frequency (Hz), Amplifier Gain (V/V) and Input Source Resistance (Ω)	Figure 3
Input Noise	Input Noise (nV/$\sqrt{\text{Hz}}$)	Frequency (Hz)	Figure 4
Frequency Response	Frequency Response: Gain (dB) Frequency Response: Phase Shift (Degree) Dynamic Response	Frequency (Hz) Frequency (Hz) N/A	Figure 5 Figure 6 Figure 7
Offset	Output Offset Voltage (mV)	Temperature (°C)	Figure 8
Rated Out	Output Voltage Swing (V) Output Current (mA)	Supply Voltage (V dc) Supply Voltage (V dc)	Figure 9 Figure 10
Isolated Power Supply	Isolated Power Supply Voltage (V) Isolated Power Supply Ripple (mV p–p) Isolated Power Supply Ripple (V p–p)	Current Delivered to the Load (mA) Current Delivered to the Load (mA) Bypass Capacitance (μF)	Figure 11 Figure 12 Figure 13

Table I. Performance Characteristics Detailed in the AD203SN Data Sheet

Common Mode Rejection. Figure 3 illustrates the common mode rejection (CMR), expressed in dB, of the AD203SN versus frequency (Hz), gain (V/V) and source impedance imbalance (Ω). To achieve the optimal common mode rejection of unwanted signals, it is recommended that the source imbalance be kept as low as possible and that the input circuitry be carefully laid out so as to avoid adding excessive stray capacitances at the isolator's input terminals.

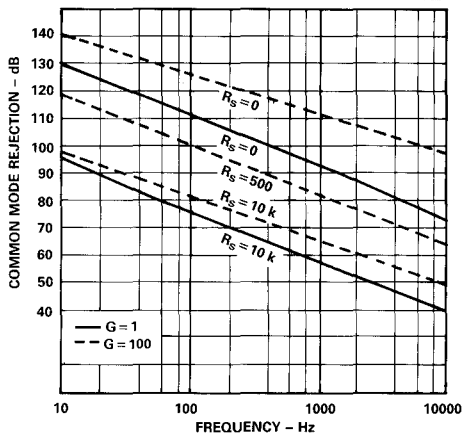


Figure 3. Common Mode Rejection (CMR) vs. Frequency (Hz), Gain (V/V) and Resistance (Ω)

Input Noise. Figure 4 presents the typical input noise characteristics, in nV/$\sqrt{\text{Hz}}$, of the AD203SN for a frequency range from 1 Hz to 100 kHz.

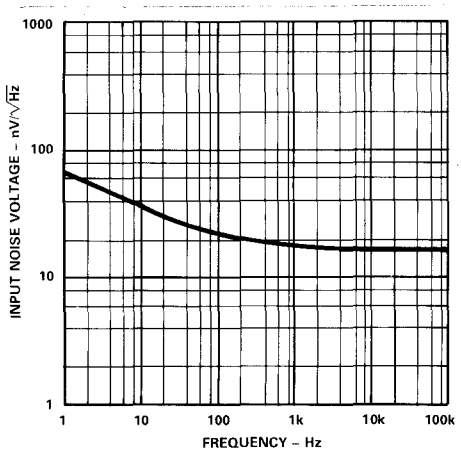


Figure 4. Input Noise (nV/$\sqrt{\text{Hz}}$) vs. Frequency (Hz)

Frequency Response: Gain and Phase Shift. Figure 5 illustrates the AD203SN's gain as a function of frequency while Figure 6 illustrates the corresponding phase shift vs. frequency. The AD203SN's low phase shift and 10 kHz bandwidth performance make it ideal in power monitoring and control system applications.

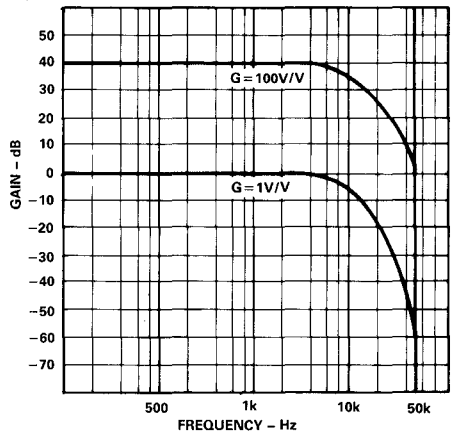


Figure 5. Gain (dB) as a Function of Frequency (Hz)

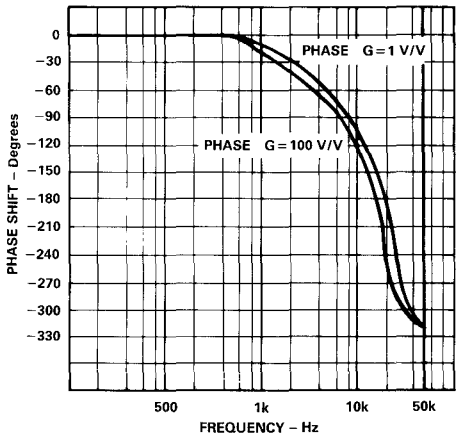


Figure 6. Phase Shift (Δ°) as a Function of Frequency (Hz)

Dynamic Response of the AD203SN. To illustrate the speed, dynamic range and rapid settling time of the AD203SN, the isolator's output response to a 20 V p–p step function is shown in Figure 7.

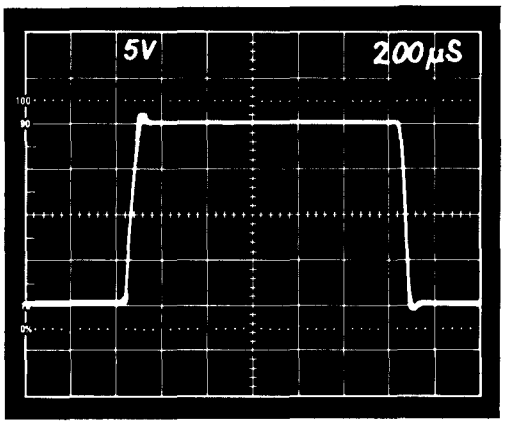


Figure 7. Dynamic Response of the AD203SN (20 V p–p Step)

Output Offset Voltage. The AD203SN exhibits a low output offset voltage temperature coefficient over the +25°C to +125°C temperature range as shown in Figure 8.

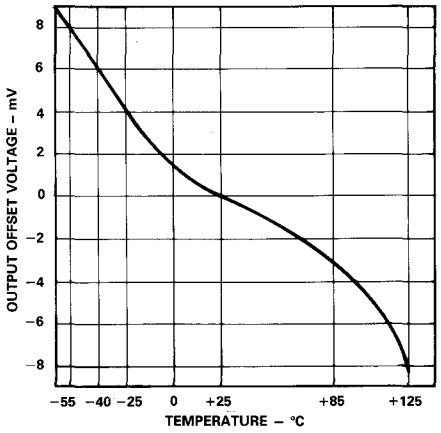


Figure 8. Output Offset Voltage (mV) vs. Temperature (°C) with G=1 V/V

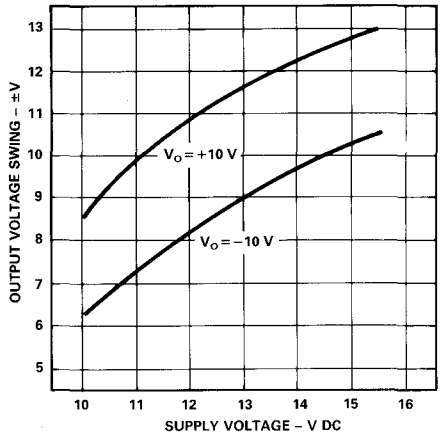


Figure 9. Output Voltage Swing (±V) vs. Power Supply Input Voltage (V DC), with a 2.5 kΩ Load

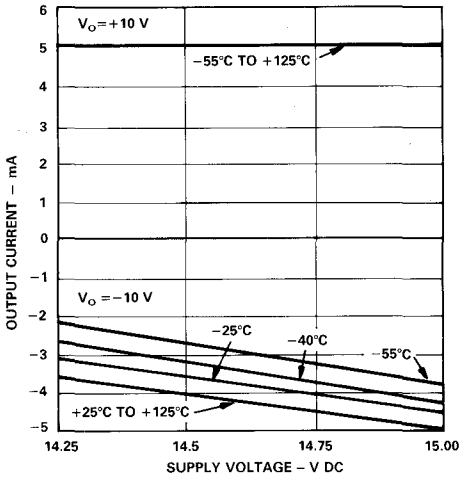


Figure 10. Output Current (mA) vs. Supply Voltage (V DC) and Temperature (°C), with V_{ISO} Loaded at 5 mA

Rated Output. The rated output voltage, across the OUT HI and OUT LO terminals, for the AD203SN is specified at ±10 V. This specification applies when the AD203SN is powered by a +15 V dc supply. The rated output voltage level is, however, affected by the input power supply voltage and the loads placed on the isolated power supply. This dependency is illustrated in Figure 9.

The current delivered by the output terminals of the AD203SN will vary as a function of the supply voltage and operating temperature. These relationships are illustrated in Figure 10.

Isolated Power. The load characteristics of the AD203SN's isolated power supplies (i.e., +15 V dc and −15 V dc) are plotted in Figure 11.

The isolated power supply exhibits some ripple which varies as a function of the load current. Figure 12 demonstrates this relationship. The AD203SN has internal bypass capacitors that optimize the tradeoff between output ripple and power supply performance, even under full load. If a specific application requires more bypassing on the isolated power supplies, external capacitors may be added. Figure 13 plots the isolated power supply ripple as a function of external bypass capacitance under full load conditions (i.e., 5 mA).

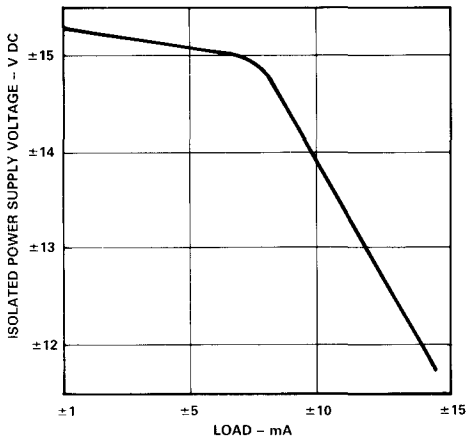


Figure 11. Isolated Power Supply Voltage (V DC) vs. Load (mA)

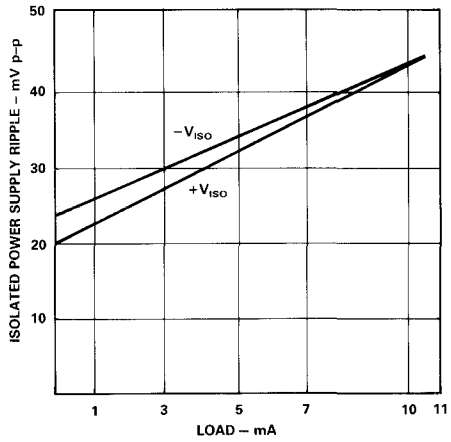


Figure 12. Isolated Power Supply Ripple (mV p–p) vs. Load (mA)

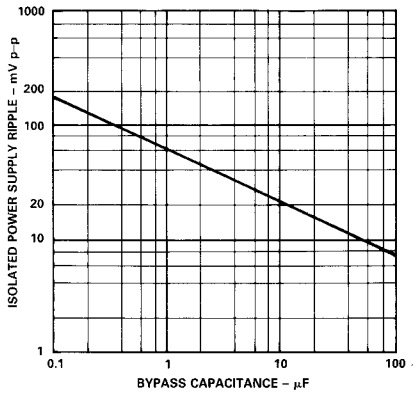


Figure 13. Isolated Power Supply Ripple (mV p–p) vs. Bypass Capacitance (μF), with a 5 mA Load on $\pm V_{ISO}$, and Noise Bandwidth of 1 MHz.

The curves in Figures 12 and 13 were generated by measuring the power supply ripple over a 1 MHz bandwidth.

CAUTION: The AD203SN does not provide for short circuit protection of its isolated power supply. A current limiting resistor may be placed in series with the isolated power terminals and the load in order to protect the supply against inadvertent shorts.

APPLICABLE STANDARDS

The tests and methods employed in the design verification process are summarized in Table II. A copy of the *AD203SN Quality & Reliability Summaries* test report, which documents the results of the tests listed in Table II, is available on request.

Test Method	Test Description
MIL-STD-883C, Method 1004	Moisture Resistance
MIL-STD-883C, Method 1010 Condition B	Temperature Cycling, −55°C to +125°C
MIL-STD-883C, Method 2002, Condition B	Mechanical Shock @ 1,500 g for 0.5 ms
MIL-STD-883C, Method 2003	Solderability of Terminations
MIL-STD-883C, Method 2004	Integrity of Microelectronic Device Leads
MIL-STD-883C, Method 2007, Condition A	Variable Frequency Vibration @ 20 g
MIL-STD-883C, Method 2015	Resistance to Solvents
MIL-STD-883C, Method 3015.5	Electrostatic Discharge Sensitivity Classification
Analog Devices Product Reliability Program	MTBF Calculation (per MIL-HDBK-217D) and Verification

Table II. Tests Used to Verify the Ruggedness, Reliability and Quality of the AD203SN Design

Per 883C Method 3015.5, the AD203SN has been classified as a Class 2 ESD (electrostatic discharge) sensitive device. As a Class 2 device, the AD203SN is insensitive to static discharge voltages of less than 2000 V.

INSIDE THE AD203SN

The functional block diagram of the AD203SN is shown in Figure 14. The AD203SN employs amplitude modulation techniques to implement transformer coupling of signals down to dc.

The 35 kHz, 30 V p–p square wave carrier used by the AD203SN is generated by an internal oscillator located in the output port of the isolator. This oscillator is powered by a +15 V dc supply.

A full wave modulator translates the input signal to the carrier frequency which is then transmitted across transformer T1. The synchronous demodulator in the output port extracts the input signal from the carrier. The 12 kHz two-pole filter is employed to minimize output noise and ripple. Furthermore, the filter serves as a low impedance output buffer.

The input port of the AD203SN contains an uncommitted input op amp, a modulator and the power transformer T2. The primary of the power transformer is driven by the 35 kHz square wave while the secondary, in conjunction with a rectifier network, supplies isolated power to the modulator, input op amp and any external load. The uncommitted input amplifier can be used to supply gain or to buffer the input signals.

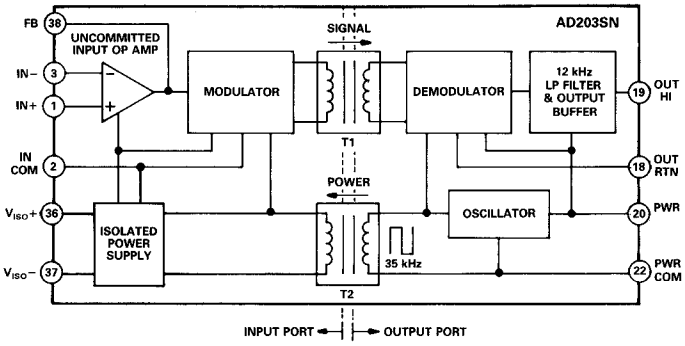


Figure 14. Functional Block Diagram

USING THE AD203SN

Powering the AD203SN. The AD203SN requires only a single +15 V dc power supply connected as shown in Figure 15. A bypass capacitor is provided in the module.

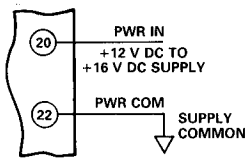


Figure 15. Powering the AD203SN

Unity Gain Input Configuration. The basic unity gain configuration for input signals of up to ±10 V is shown in Figure 16.

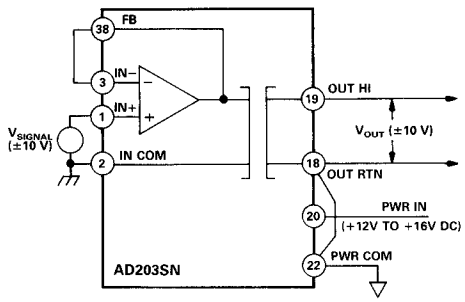


Figure 16. Basic Unity Gain Configuration

Input Configuration for a Gain Greater Than 1 (G>1). When small input signal levels must be amplified and isolated, Figure 17 shows how to get a gain greater than 1 while continuing to preserve a very high input impedance.

In this circuit, the gain equation may be written as:

$$V_O = (1+R_F/R_G)\times V_{SIG}$$

where

V_O = Output Voltage (V)
V_{SIG} = Input Signal Voltage (V)
R_F = Feedback Resistor Value (Ω)
R_G = Gain Resistor Value (Ω).

Note on the 100 pF Capacitor. Whenever a gain of 50 V/V or greater is required, a 100 pF capacitor from the FB (input op amp feedback) terminal to the IN COM (input common) terminal, as shown with the dotted lines in Figure 17, is highly recommended. The capacitor acts to filter out switching noise and will minimize the isolator's nonlinearity parameter.

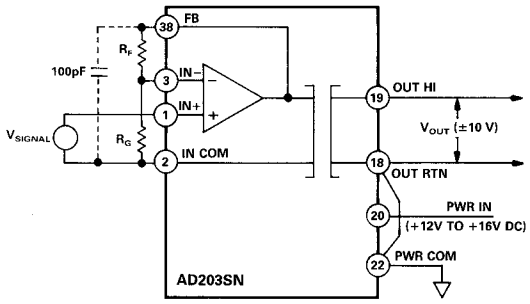


Figure 17. Input Configuration for a Gain Greater than 1

Compensating the Uncommitted Input Op Amp. The open loop gain and phase versus frequency for the uncommitted input op amp are given in Figure 18. These curves are to be used to determine the appropriate values for the feedback resistor and compensation capacitor in order to ensure frequency stability when a gain greater than unity is required. The final values for these components should also be chosen so as to satisfy the following constraints:

- The current drawn in the feedback resistor (R_F) is no greater than 1 mA.
- The feedback (R_F) and gain resistor (R_G) result in the desired amplifier gain.

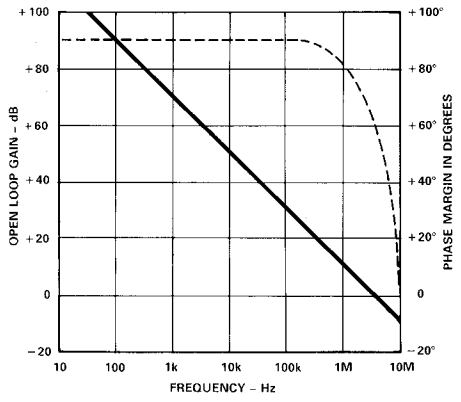


Figure 18. Open Loop Gain and Phase vs. Frequency for the Uncommitted Input Op Amp

Inverting, Summing or Current Input Configuration. Figure 19 shows how the AD203SN can accommodate current inputs or sum currents or voltages.

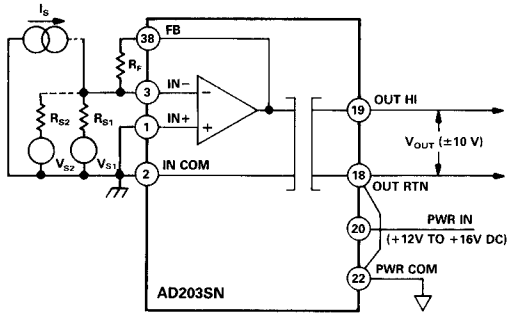


Figure 19. Input Configuration for Summing or Current Input

In this circuit the output voltage equation can be written as:

$$V_O = -R_F\times(I_S+V_{S1}/R_{S1}+V_{S2}/R_{S2}+\ldots)$$

where

V_O = Output Voltage (V)
V_{S1} = Voltage of Input Signal 1 (V)
V_{S2} = Voltage of Input Signal 2 (V)
I_S = Input Current Source (A)
R_F = Feedback Resistor Value (Ω)
R_{S1} = Source Resistance Associated with Input Signal 1 (Ω)
R_{S2} = Source Resistance Associated with Input Signal 2 (Ω).

The circuit of Figure 19 can also be used when the input signal is larger than the ±10 V input range of the isolator. For example, suppose that in Figure 19 only V_{S1}, R_{S1} and R_F are connected to the feedback, input and common terminals as shown by the solid lines in Figure 19. Now, a V_{S1} with a ±100 V span can be accommodated with $R_F = 20$ kΩ and a total $R_{S1} = 200$ kΩ.

GAIN AND OFFSET ADJUSTMENTS

General Comments. When gain and offset adjustments are required, the actual compensation circuit ultimately utilized will depend on:

- The input configuration mode of the isolation amplifier (i.e., noninverting or inverting).
- The placement of the adjusting potentiometer (i.e., on the isolator's input or output side).

As a general rule:

- Offset adjustments are best accomplished on the isolator's input side, as it is much easier and more efficient to null the offset ahead of any gain.
- Gain adjustments are mostly easily accomplished as part of the gain-setting resistor network at the isolator's input side.
- Input adjustments, of the offset and/or gain, are preferred when the adjusting potentiometers are as near as possible to the input end of the isolator (so as to minimize strays).
- Output side adjustments may be necessary under the conditions where adjusting potentiometers placed on the input side would present a hazard to the user due to the presence of high common mode voltages during the adjustment procedure.

- It is recommended that the offset adjustment precedes the gain adjustment.

Adjustments for the Noninverting Mode of Operation

Offset Adjustment. Figure 20 shows the suggested input adjustment connections when the isolator's input amplifier is configured for the noninverting mode of operation. The offset adjustment circuit injects a small voltage in series with the low side of the signal source. The adjustment potentiometer P1 modulates the injection voltage and is therefore responsible for nulling out the offset voltage.

Note:
- To minimize CMR degradation it is recommended that the resistor in series with the input LO (i.e., R_C) be below a few hundred ohms.
- The offset adjustment circuit of Figure 20 will not work if the signal source has another current path to input common, or if current flows in the signal source LO lead. If this is the case, use the output adjustment procedure.

Gain Adjustment. Figure 20 also shows the suggested gain adjustment circuit. Note that the gain adjustment potentiometer P2 is incorporated into the gain-setting resistor network at the isolator's input.

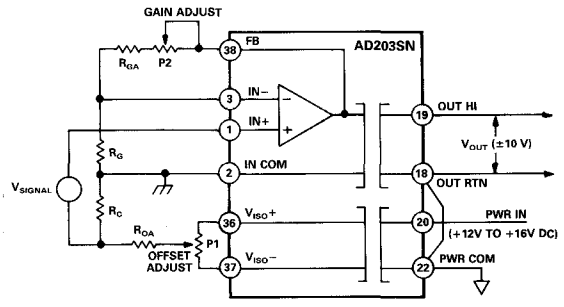


Figure 20. Input Adjustments for the Noninverting Mode of Operation

An R_{GA} of 47.5 kΩ and a 5 kΩ potentiometer, resulting in a median R_F value of 50 kΩ (i.e., R_{GA} + P2/2), will work nicely for gains of 10 V/V or greater. The gain adjustment becomes less effective at lower gains, in fact it is halved at G=2 V/V, so that potentiometer P2 will have to be a larger fraction of the total R_F. At a gain of 1 V/V attempting to adjust the gain downwards will compromise the isolator's input impedance. In this case it would be better to adjust the gain at the signal source or after the output.

Input Adjustments for the Inverting Mode of Operation

Offset Adjustment. Figure 21 shows the suggested input adjustment connections when the isolator's input amplifier is configured for the inverting mode of operation. Here the offset adjustment potentiometer P1 nulls the voltage at the summing node. This method is preferred over current injection since it is less affected by any subsequent gain adjustments.

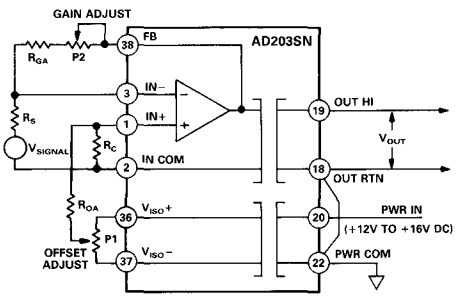


Figure 21. Input Adjustments for the Inverting Mode of Operation

Gain Adjustment. Figure 21 also shows the suggested gain adjustment circuit. In this circuit, the gain adjustment is made in the feedback loop using potentiometer P2. The adjustments will be effective for all gains in the 1 to 100 V/V range.

Output Adjustments

Offset Adjustment. Figure 22 shows the recommended technique for offset adjustment at the output. In this circuit, the ±15 V dc voltage is supplied by an independent source. With reference to the output circuitry shown in Figure 22, the maximum offset adjustment range is given by:

$$E_{OFFSET} = \frac{R_D \times V_S}{R_D + R_O}$$

where, V_S is the power supply voltage. A 20 kΩ potentiometer (P_O) should work well in this adjustment circuit.

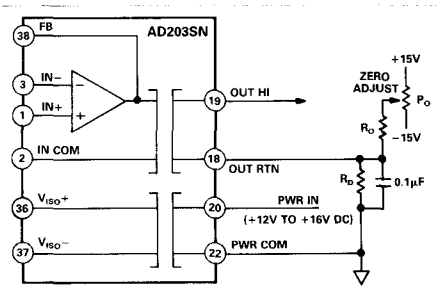


Figure 22. Output Side Offset Adjustment Circuit

Gain Adjustment. Since the AD203SN's output amplifier is fixed at unity, any desired output gain adjustments can only be made in a subsequent stage.

USING ISOLATED POWER

The AD203SN provides ±15 V dc power outputs referred to the input common. These may be used to power various accessory circuits which must operate at the input common mode level. The input offset adjustment circuits of the previous section are examples of this need.

The isolated power supply output has a current capacity of 5 mA which should be sufficient to operate adjustment circuits, references, op amps, signal conditioners and remote transducers.

CAUTION: The AD203SN does not provide for short circuit protection of its isolated power supply. A current limiting resistor may be placed in series with the isolated power terminals and the load in order to protect the supply against inadvertent shorts.

APPLICATIONS EXAMPLES

Isolated Process Current to Voltage Converter

Figure 23 shows how the AD203SN can be utilized as an isolated receiver that translates a 4-20 mA process current signal input into a 0 to +10 V output. The 25 Ω shunt resistor converts the 4-20 mA current into a +100 to +500 mV signal. The signal is then offset by −100 mV via the use of P_O to produce a 0 to +400 mV input. The signal is then amplified by a gain of 25 resulting in the desired 0 to +10 V output. With an open circuit on the input side, the AD203SN will have −2.5 V on the output, corresponding to the −100 mV offset voltage multiplied by a gain of 25 V/V.

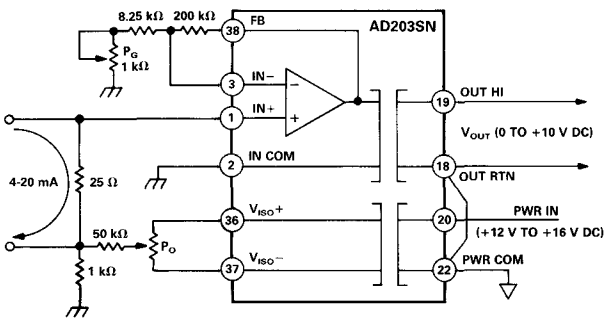


Figure 23. Using the AD203SN as an Isolated Process Current to Voltage Converter

For the circuit of Figure 23, the input to output transfer function can be expressed as:

$$V_{OUT} = 625 \times I_{IN} - 2.5\ V$$

where

V_{OUT} = Output Voltage (V)
I_{IN} = Input Current in milliamps (mA). This current is limited to the 4 to 20 mA range.

Current Shunt Measurements

In addition to isolating and converting process current signals into voltage signals, the AD203SN can be used to indicate the value of any loop current in general. Figure 24 illustrates a typical current shunt measurement application of the AD203SN. A small sensing resistor R_{SHUNT}, placed in series with the current loop, develops a small differential voltage that may be further scaled to provide an isolator output voltage that is directly proportional to the current. The voltage developed across the shunt can potentially be several hundred to a thousand volts above ground. In this circuit, the AD203SN provides the necessary scaling of the shunt signal while providing high common-mode voltage isolation and high common mode rejection of dc and 60 Hz components.

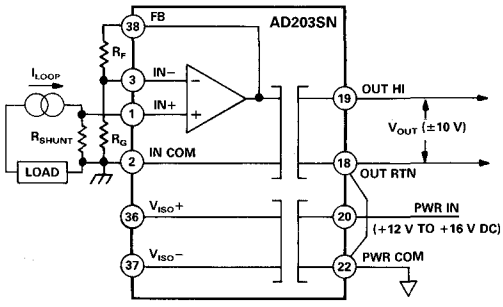


Figure 24. Using the AD203SN for Current Shunt Measurements

The transfer function for the circuit of Figure 24 can be written as:

$$V_{OUT} = R_{SHUNT} \times (1 + R_F/R_G) \times I_{LOOP}$$

where

V_{OUT} = Output Voltage (V)
R_{SHUNT} = Sense or Current Shunt Resistance (Ω)
R_F = Feedback Resistance (Ω)
R_G = Gain Resistance (Ω)
I_{LOOP} = Loop Current (A).

Low Level Inputs

In applications where low level signals need to be isolated (thermocouples are one such application), a low drift input amplifier can be used with the AD203SN. Figure 25 illustrates this implementation of the AD203SN. The circuit design also includes a three-pole active filter which provides for enhanced common mode rejection at 60 Hz and normal mode rejection of frequencies above a few Hz. If any offset adjustments are desired, they are best done at the trim pins of the low drift input amplifier. Gain adjustments can be done at the feedback resistor.

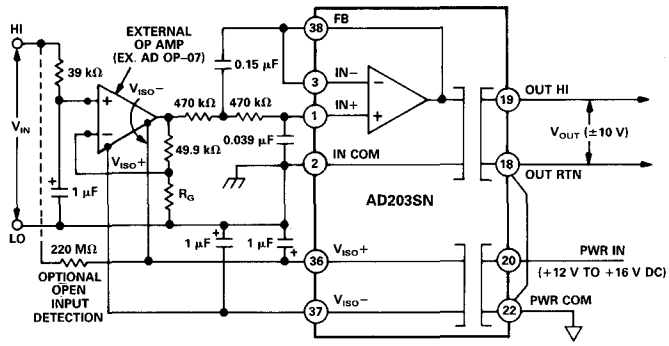


Figure 25. Using the AD203SN with Low Level Inputs

The input-output relationship for the circuit shown in Figure 25 can be written as:

$$V_{OUT} = V_{IN} \times (1 + 50\ k\Omega/R_G)$$

where

V_{OUT} = Output Voltage (V)
V_{IN} = Low Level Input Voltage (V)
R_G = Isolation Amplifier Gain Resistance (Ω).

Noise Reduction in Data Acquisition Systems

The AD203SN uses amplitude modulation techniques with a 35 kHz carrier to pass both ac and dc signals across the isolation barrier. Some of the carrier's harmonics are unavoidably passed through to the isolator output in the form of ripple. In most cases, this noise source is insignificant when compared to the measured signal. However, in some applications, particularly when a fast A/D converter is used following the isolator, it may be desirable to add filtering at the isolator's output in order to reduce the carrier ripple. Figure 26 shows a circuit that will reduce the carrier ripple through the use of a two-pole output filter.

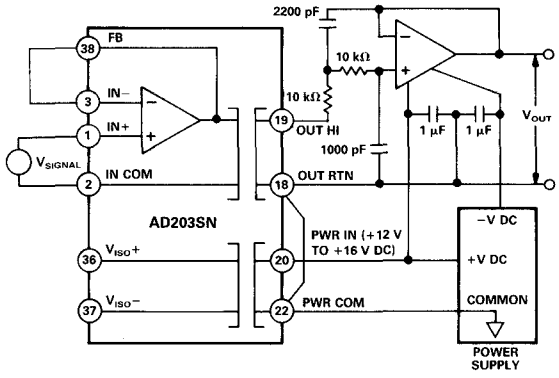


Figure 26. Noise Reduction in Data Acquisition Systems Using the AD203SN

SELECTION GUIDE FOR ANALOG DEVICES' FAMILY OF ISOLATION AMPLIFIERS

	Consider the: / If You Need:	AD202J	AD202K	AD203SN	AD204J	AD204K	AD210AN	AD210BN	AD210JN	284J
General	Isolator for Multichannel Applications Lowest Cost Isolator 3-Port Isolation Rugged, Military Temperature Range Isolator Medical Isolator									
Gain	Low Nonlinearity (≤±0.012%) Low Gain Temp. Co. (≤25 ppm/°C)	±0.05% 45 ppm/°C	±0.025% 45 ppm/°C	±0.025% 60 ppm/°C	±0.05% 45 ppm/°C	±0.025% 45 ppm/°C	±0.025% 25 ppm/°C	±0.012% 25 ppm/°C	±0.025% 25 ppm/°C	±0.05% 75 ppm/°C
Isolation	High CMV Rating (≥2.5 kV rms, Continuous) High CMR (≥104 dB, All Conditions) Low Leakage Current (≤2 μA rms, 240 V rms, 60 Hz)	750 V rms 100 dB 2 μA rms	1.5 kV rms 100 dB 2 μA rms	1.5 kV rms 96 dB 4 μA rms	750 V rms 104 dB 2 μA rms	1.5 kV rms 104 dB 2 μA rms	2.5 kV rms 120 dB 2 μA rms	2.5 kV rms 120 dB 2 μA rms	1.5 kV rms 120 dB 2 μA rms	3.5 kV rms 78 dB 2 μA rms[1]
Speed	20 kHz Full Signal Bandwidth 10 kHz Full Signal Bandwidth 5 kHz Full Signal Bandwidth Fast Settling Time (≤150 μs) Fast Slew Rate (≥1V/ μs)	 2 kHz 1ms	 2 kHz 1ms	 150 μs 0.5 V/ μs	 1ms	 1ms	 150 μs 1 V/ μs	 150 μs 1 V/ μs	 150 μs 1 V/ μs	 700 Hz 25 mV/ μs
Offset	Low Offset Drift Temp. Co. (≤20 μV/°C)	20 μV/°C	20 μV/°C	55 μV/°C	20 μV/°C	20 μV/°C	40 μV/°C	40 μV/°C	40 μV/°C	170 μV/°C
Rated Output	±10 V Differential Output Low Output Impedance (≤1 Ω)	±5 V 7 kΩ	±5 V 7 kΩ	±10 V 0.2 Ω	±5 V 3 k Ω	±5 V 3 k Ω	±10 V 1 Ω	±10 V 1 Ω	±10 V 1 Ω	±5 V 1 kΩ
Isolated Power Supply	Isolated Front End Power (≥75 mW)	6 mW	6 mW	150 mW	37.5 mW	37.5 mW	150 mW	150 mW	150 mW	85 mW
Input Power Supply	Isolator Powered by a dc Supply	+15 V dc	+15 V dc	+15 V dc	15 V p-p @ 25 kHz	15 V p-p @ 25 kHz	+15 V dc	+15 V dc	+15 V dc	+15 V dc
Rated Performance Temperature	−55°C to +125°C, Rated Range −40°C to +85°C, Rated Range −25°C to +85°C, Rated Range 0 to +70°C, Rated Range[2]									
Packaging	Small Size (0.325 in^3 typ) SIP Package DIP Package	SIP Pkg.	SIP Pkg.	1.021 in^3	SIP Pkg.	SIP Pkg.	0.735 in^3	0.735 in^3	0.735 in^3	1.395 in^3

NOTES

All performance specification numbers apply for G=1 V/V and 0 to +70°C.

Quotations for nonlinearity, gain temperature coefficient, CMV rating and leakage current are max numbers; CMR and offset temperature coefficient are min, all other are typical.

Isolated front end power specifications are for both the + and − terminals.

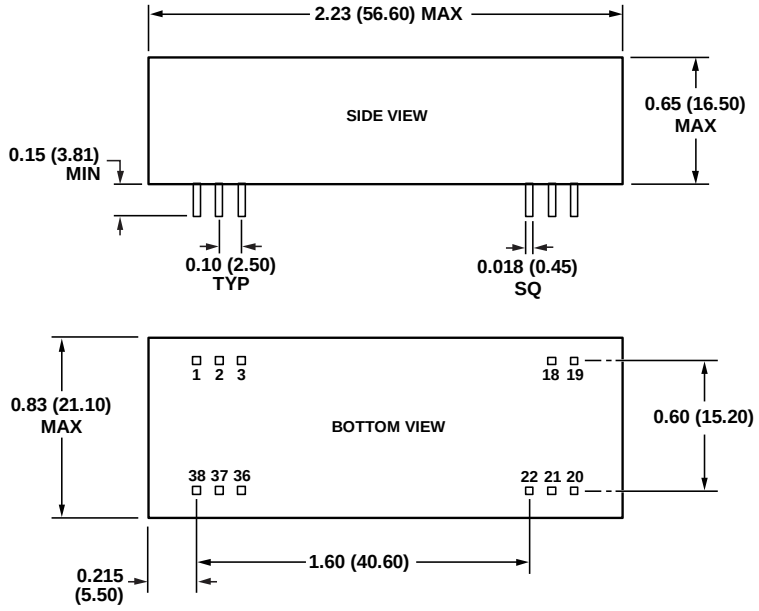
[1]The 284J leakage applies for 115 V rms.

[2]The AD202, AD204 and AD210 series will operate in the −40°C to+85°C temperature range.

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OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

072508-A

Figure 27. AD203 SIP Package
(N-11)
11-Lead Count with 38-Lead Spacing
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD203SN	−55°C to +125°C	11-Lead SIP Package	N-11

REVISION HISTORY

8/2016—Rev. A to Rev. B

Changes to Features Section 1
Deleted Prices 3

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