

HIGH-SPEED QUAD DIGITAL ISOLATORS

Check for Samples: [ISO7240CF-Q1](#), [ISO7241C-Q1](#)

FEATURES

- Qualified for Automotive Applications
- Selectable Failsafe Output (ISO7240CF)
- 25 and 150-Mbps Signaling Rate Options
 - Low Channel-to-Channel Output Skew; 1 ns Max
 - Low Pulse-Width Distortion (PWD); 2 ns Max
 - Low Jitter Content; 1 ns Typ at 150 Mbps
- Typical 25-Year Life at Rated Working Voltage (see application note [SLLA197](#) and [Figure 17](#))
- 4000-V_{peak} Isolation, 560-V_{peak} V_{IORM}
 - UL 1577, IEC 60747-5-2 (VDE 0884, Rev 2), IEC 61010-1, IEC 60950-1 and CSA Approved
- 4 kV ESD Protection
- Operate With 3.3-V or 5-V Supplies
- High Electromagnetic Immunity (see application report [SLLA181](#))
- –40°C to 125°C Operating Range

DESCRIPTION

The ISO7240, ISO7241 and ISO7242 are quad-channel digital isolators with multiple channel configurations and output enable functions. These devices have logic input and output buffers separated by TI's silicon dioxide (SiO₂) isolation barrier. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

The ISO7240 has all four channels in the same direction while the ISO7241 has three channels the same direction and one channel in opposition. The ISO7242 has two channels in each direction.

The C option devices have TTL input thresholds and a noise-filter at the input that prevents transient pulses from being passed to the output of the device. The M option devices have CMOS $V_{CC}/2$ input thresholds and do not have the input noise-filter or the additional propagation delay.

The ISO7240CF has an input disable function on pin 7, and a selectable high or low failsafe-output function with the CTRL pin (pin 10). The failsafe-output is a logic high when a logic-high is placed on the CTRL pin or it is left unconnected. If a logic-low signal is applied to the CTRL pin, the failsafe-output becomes a logic-low output state. The ISO7240CF input disable function prevents data from being passed across the isolation barrier to the output. When the inputs are disabled, the outputs are set by the CTRL pin.

These devices may be powered from either 3.3-V or 5-V supplies on either side in any 3.3-V / 3.3-V, 5-V / 5-V, 5-V / 3.3-V, or 3.3-V / 5-V combination. Note that the signal input pins are 5-V tolerant regardless of the voltage supply level being used.

These devices are characterized for operation over the ambient temperature range of –40°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – DW	Reel of 2000	ISO7240CFQDWRQ1	ISO7240CFQ
			ISO7240CQDWRQ1	Product Preview
			ISO7241CQDWRQ1	ISO7241CQ
			ISO7242CQDWRQ1	ISO7242CQ

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

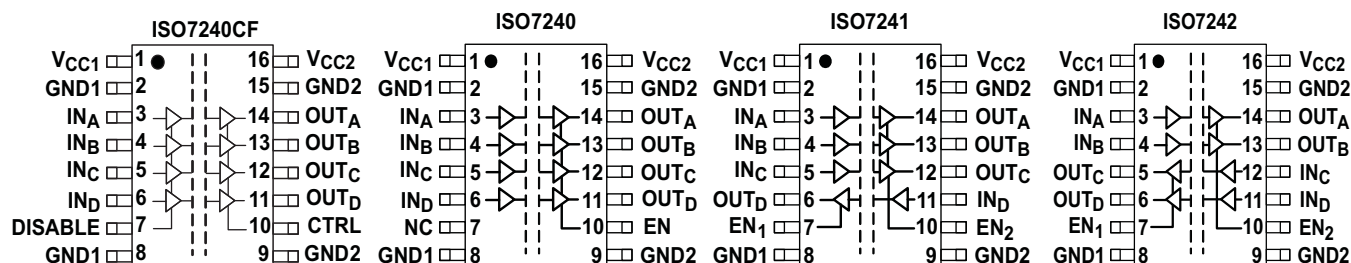


Table 1. ISO724xC Function Table⁽¹⁾

INPUT V _{CC}	OUTPUT V _{CC}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z

(1) PU = Powered Up; PD = Powered Down ; X = Irrelevant; H = High Level; L = Low Level

Table 2. ISO7240CF Function Table

V _{CC1}	V _{CC2}	DATA INPUT (IN)	DISABLE INPUT (DISABLE)	FAILSAFE CONTROL INPUT (CTRL)	DATA OUTPUT (OUT)
PU	PU	H	L or Open	X	H
PU	PU	L	L or Open	X	L
X	PU	X	H	H or Open	H
X	PU	X	H	L	L
PD	PU	X	X	H or Open	H
PD	PU	X	X	L	L

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

		VALUE	UNIT
V _{CC}	Supply voltage ⁽²⁾ , V _{CC1} , V _{CC2}	–0.5 to 6	V
V _I	Voltage at IN, OUT, EN, DISABLE, CTRL	–0.5 to 6	V
I _O	Output current	±15	mA
ESD	Electrostatic discharge	Human-Body Model	All pins
		Field-Induced-Charged Device Model	
		Machine Model	
		±4	kV
		±1	
		±200	V
T _J	Maximum junction temperature	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage ⁽¹⁾ , V _{CC1} , V _{CC2}	3.15	5.5	V
I _{OH}	High-level output current		4	mA
I _{OL}	Low-level output current	–4		mA
t _{ui}	Input pulse width	40		ns
1/t _{ui}	Signaling rate	0	30 ⁽²⁾	Mbps
V _{IH}	High-level input voltage (IN, DISABLE, CTRL, EN)	2	V _{CC}	V
V _{IL}	Low-level input voltage (IN, DISABLE, CTRL, EN)	0	0.8	V
T _A	Operating free-air temperature	–40	125	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification		1000	A/m

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.
- (2) Typical value at room temperature and well-regulated power supply.

IEC 60747-5-2 INSULATION CHARACTERISTICS⁽¹⁾

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SPECIFICATIONS	UNIT
V _{IORM}	Maximum working insulation voltage	560	V
V _{PR}	After Input/Output Safety Test Subgroup 2/3 V _{PR} = V _{IORM} × 1.2, t = 10 s, Partial discharge < 5 pC	672	V
	Method a, V _{PR} = V _{IORM} × 1.6, Type and sample test with t = 10 s, Partial discharge < 5 pC	896	V
	Method b1, V _{PR} = V _{IORM} × 1.875, 100 % Production test with t = 1 s, Partial discharge < 5 pC	1050	V
V _{IOTM}	Transient overvoltage	t = 60 s	4000
R _S	Insulation resistance	V _{IO} = 500 V at T _S	>10 ⁹
	Pollution degree	2	

- (1) Climatic Classification 40/125/21

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V⁽¹⁾ OPERATION

, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I _{CC1}	ISO7240C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₂ at 3 V	1		3	mA
		25 Mbps		7		10.5	
	ISO7241C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V	6.5		11	mA
		25 Mbps		12		18	
	ISO7242C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V	10		16	mA
		25 Mbps		15		24	
I _{CC2}	ISO7240C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₂ at 3 V	15		22	mA
		25 Mbps		17		25	
	ISO7241C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V	13		20	mA
		25 Mbps		18		28	
	ISO7242C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V	10		16	mA
		25 Mbps		15		24	
ELECTRICAL CHARACTERISTICS							
I _{OFF}	Sleep mode output current		EN at 0 V, Single channel	0			μA
V _{OH}	High-level output voltage		I _{OH} = −4 mA, See Figure 1	V _{CC} − 0.8			V
			I _{OH} = −20 μA, See Figure 1	V _{CC} − 0.1			
V _{OL}	Low-level output voltage		I _{OL} = 4 mA, See Figure 1			0.4	V
			I _{OL} = 20 μA, See Figure 1			0.1	
V _{I(HYS)}	Input voltage hysteresis			150			mV
I _{IH}	High-level input current		IN from 0 V to V _{CC}			10	μA
I _{IL}	Low-level input current			−10			
C _I	Input capacitance to ground		IN at V _{CC} , V _I = 0.4 sin (4E6πt)	2			pF
CMTI	Common-mode transient immunity		V _I = V _{CC} or 0 V, See Figure 5	25	50		kV/μs

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay	See Figure 1	18		45	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				5	
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾				8	ns
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾	ISO7240C, ISO7241C			3	ns
		ISO7242C			4	
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	25	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		12		μs
t_{wake}	Wake time from input disable	See Figure 4		15		μs

- (1) Also referred to as pulse skew.
- (2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
- (3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V⁽¹⁾ OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I _{CC1}	ISO7240C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₂ at 3 V		1	3	mA	
		25 Mbps			7	10.5		
	ISO7241C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V		6.5	11	mA	
		25 Mbps			12	18		
	ISO7242C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V		10	16	mA	
		25 Mbps			15	24		
I _{CC2}	ISO7240C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₂ at 3 V		9.5	15	mA	
		25 Mbps			10.5	17		
	ISO7241C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V		8	13	mA	
		25 Mbps			11.5	18		
	ISO7242C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V		6	10	mA	
		25 Mbps			9	14		
ELECTRICAL CHARACTERISTICS								
I _{OFF}	Sleep mode output current		EN at 0 V, Single channel		0		μA	
V _{OH}	High-level output voltage		I _{OH} = −4 mA, See Figure 1	ISO7240	V _{CC} − 0.4		V	
				ISO724x (5-V side)	V _{CC} − 0.8			
			I _{OH} = −20 μA, See Figure 1		V _{CC} − 0.1			
V _{OL}	Low-level output voltage		I _{OL} = 4 mA, See Figure 1		0.4		V	
			I _{OL} = 20 μA, See Figure 1		0.1			
V _{I(HYS)}	Input voltage hysteresis				150		mV	
I _{IH}	High-level input current		IN from 0 V to V _{CC}		10		μA	
I _{IL}	Low-level input current				−10			
C _I	Input capacitance to ground		IN at V _{CC} , V _I = 0.4 sin (4E6πt)		2		pF	
CMTI	Common-mode transient immunity		V _I = V _{CC} or 0 V, See Figure 5		25	50	kV/μs	

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay	See Figure 1	20		50	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $	ISO7240C, ISO7241C			3	
		ISO7242C			4	
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾				10	ns
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾	ISO7240C, ISO7241C			3	ns
		ISO7242C			4	
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	25	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		18		μs
t_{wake}	Wake time from input disable	See Figure 4		15		μs

- (1) Also known as pulse skew
- (2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
- (3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3-V, V_{CC2} at 5-V⁽¹⁾ OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I _{CC1}	ISO7240C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₂ at 3 V			0.5	1	mA
		25 Mbps				3	5	
	ISO7241C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V			4	7	mA
		25 Mbps				6.5	11	
	ISO7242C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V			6	10	mA
		25 Mbps				9	14	
I _{CC2}	ISO7240C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₂ at 3 V			15	22	mA
		25 Mbps				17	25	
	ISO7241C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V			13	20	mA
		25 Mbps				18	28	
	ISO7242C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V			10	16	mA
		25 Mbps				15	24	
ELECTRICAL CHARACTERISTICS								
I _{OFF}	Sleep mode output current		EN at 0 V, Single channel			0		μA
V _{OH}	High-level output voltage		I _{OH} = −4 mA, See Figure 1	ISO7240	V _{CC} − 0.4		V	
				ISO724x (5-V side)	V _{CC} − 0.8			
			I _{OH} = −20 μA, See Figure 1			V _{CC} − 0.1		
V _{OL}	Low-level output voltage		I _{OL} = 4 mA, See Figure 1			0.4		V
			I _{OL} = 20 μA, See Figure 1			0.1		
V _{I(HYS)}	Input voltage hysteresis					150		mV
I _{IH}	High-level input current		IN from 0 V to V _{CC}			10		μA
I _{IL}	Low-level input current					−10		
C _I	Input capacitance to ground		IN at V _{CC} , V _I = 0.4 sin (4E6πt)			2		pF
CMTI	Common-mode transient immunity		V _I = V _{CC} or 0 V, See Figure 5			25	50	kV/μs

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 3.3-V and V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay	See Figure 1		20		51	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $	See Figure 1	ISO7240C, ISO7241C			3	
			ISO7242C			4	
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾					10	ns
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾	ISO7240C, ISO7241C				3	ns
		ISO7242C				4	
t_r	Output signal rise time	See Figure 1			2		ns
t_f	Output signal fall time				2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2			15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output				15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				15	25	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3			12		μs
t_{wake}	Wake time from input disable	See Figure 4			15		μs

(1) Also known as pulse skew

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V⁽¹⁾ OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I _{CC1}	ISO7240C	Quiescent	V _I = V _{CC} or 0 V, all channels, no load, EN ₂ at 3 V		0.5	1	mA
		25 Mbps			3	5	
	ISO7241C	Quiescent	V _I = V _{CC} or 0 V, all channels, no load, EN ₁ at 3 V, EN ₂ at 3 V		4	7	mA
		25 Mbps			6.5	11	
	ISO7242C	Quiescent	V _I = V _{CC} or 0 V, all channels, no load, EN ₁ at 3 V, EN ₂ at 3 V		6	10	
		25 Mbps			9	14	
I _{CC2}	ISO7240C	Quiescent	V _I = V _{CC} or 0 V, all channels, no load, EN ₂ at 3 V		9.5	15	mA
		25 Mbps			10.5	17	
	ISO7241C	Quiescent	V _I = V _{CC} or 0 V, all channels, no load, EN ₁ at 3 V, EN ₂ at 3 V		8	13	mA
		25 Mbps			11.5	18	
	ISO7242C	Quiescent	V _I = V _{CC} or 0 V, all channels, no load, EN ₁ at 3 V, EN ₂ at 3 V		6	10	
		25 Mbps			9	14	
ELECTRICAL CHARACTERISTICS							
I _{OFF}	Sleep mode output current		EN at 0 V, single channel		0		μA
V _{OH}	High-level output voltage		I _{OH} = −4 mA, See Figure 1	V _{CC} − 0.4			V
			I _{OH} = −20 μA, See Figure 1	V _{CC} − 0.1			
V _{OL}	Low-level output voltage		I _{OL} = 4 mA, See Figure 1		0.4		V
			I _{OL} = 20 μA, See Figure 1		0.1		
V _{I(HYS)}	Input voltage hysteresis				150		mV
I _{IH}	High-level input current		IN from 0 V or V _{CC}		10		μA
I _{IL}	Low-level input current				−10		
C _I	Input capacitance to ground		IN at V _{CC} , V _I = 0.4 sin (4E6πt)		2		pF
CMTI	Common-mode transient immunity		V _I = V _{CC} or 0 V, See Figure 5		25	50	kV/μs

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

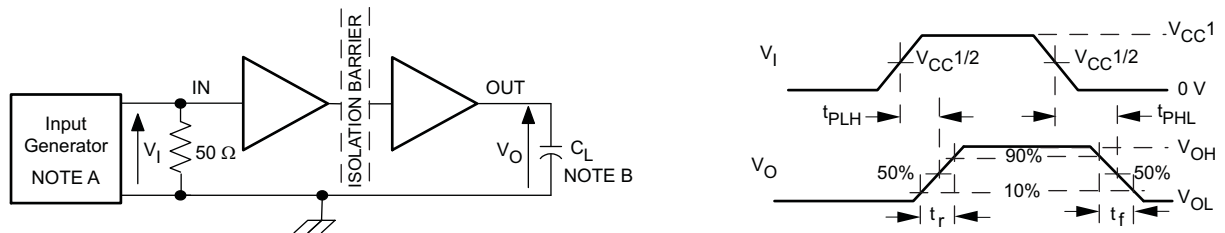
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay	See Figure 1		25		56	ns
PWD	Pulse-width distortion $ t_{PHL} - t_{PLH} ^{(1)}$					4	
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾					10	ns
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾	ISO7240C, ISO7241C				3.5	ns
		ISO7242C				4	
t_r	Output signal rise time	See Figure 1			2		ns
t_f	Output signal fall time				2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2	ISO7240C, ISO7241C	15		20	ns
			ISO7242C	15		25	
t_{PZH}	Propagation delay, high-impedance-to-high-level output		ISO7240C, ISO7241C	15		20	
			ISO7242C	15		25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		ISO7240C, ISO7241C	15		20	
			ISO7242C	15		25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output		ISO7240C, ISO7241C	15		20	
			ISO7242C	15		25	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3			18		μs
t_{wake}	Wake time from input disable	See Figure 4			15		μs

(1) Also referred to as pulse skew.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

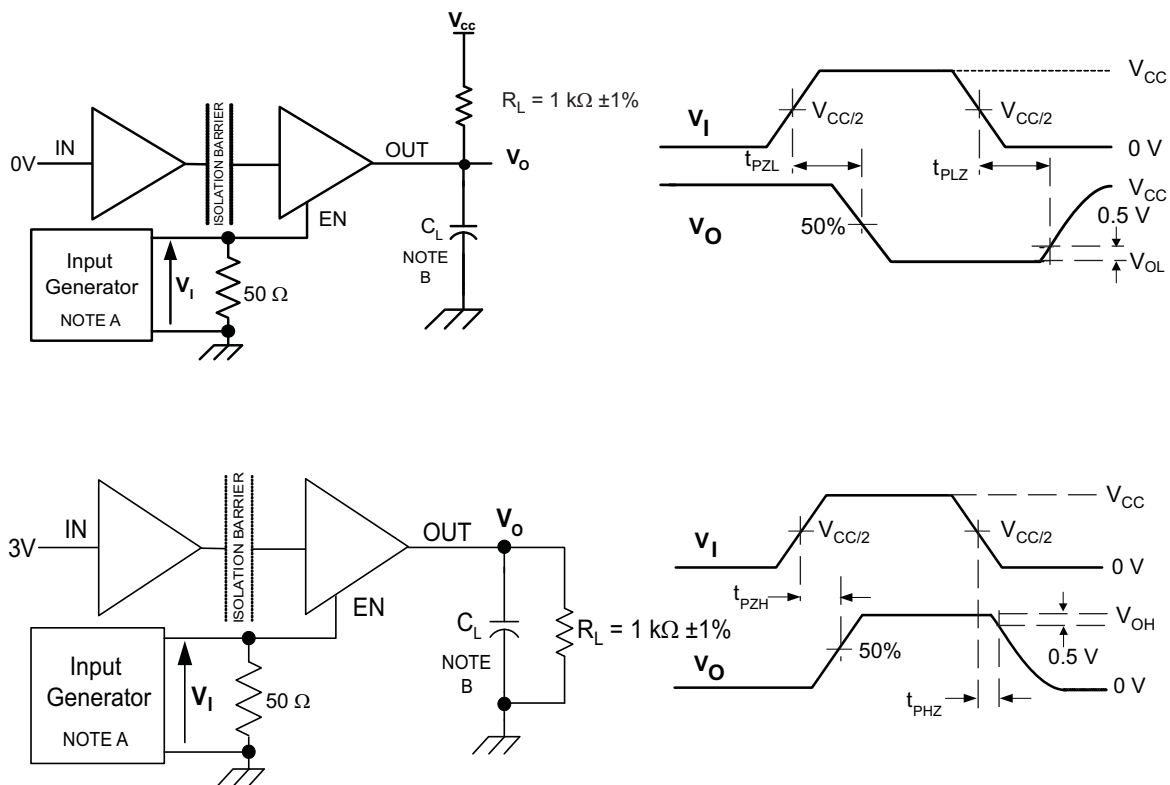
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

PARAMETER MEASUREMENT INFORMATION



- The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 50 \text{ kHz}$, 50% duty cycle, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$, $Z_O = 50 \Omega$.
- $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

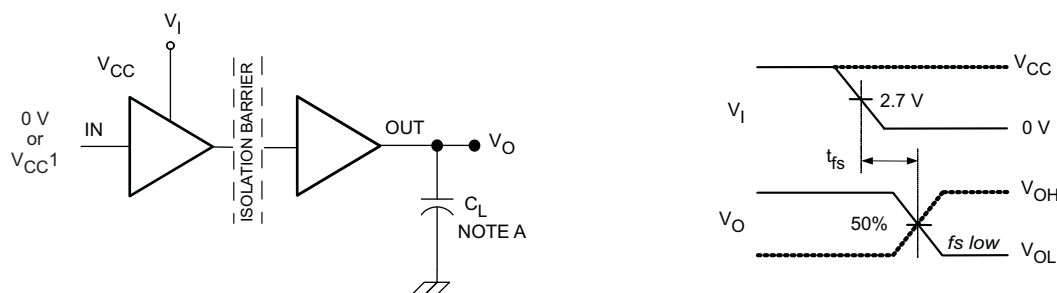
Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



- The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 50 \text{ kHz}$, 50% duty cycle, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$, $Z_O = 50 \Omega$.
- $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

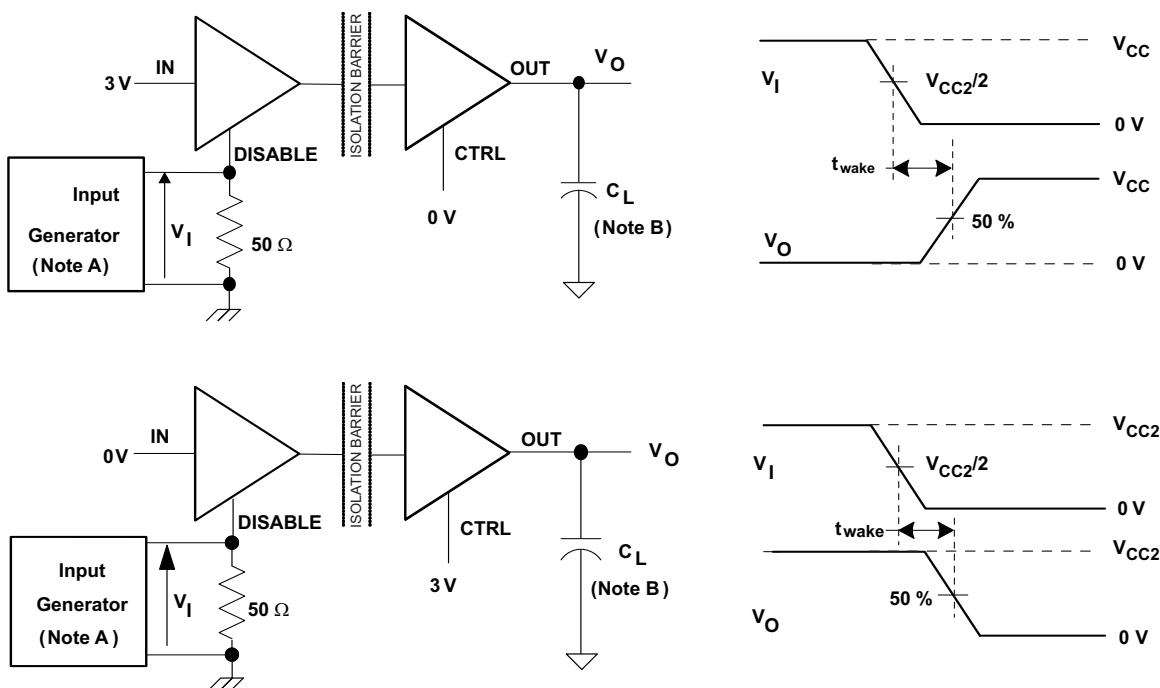
Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION (continued)



- A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50$ kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50\Omega$.

Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms

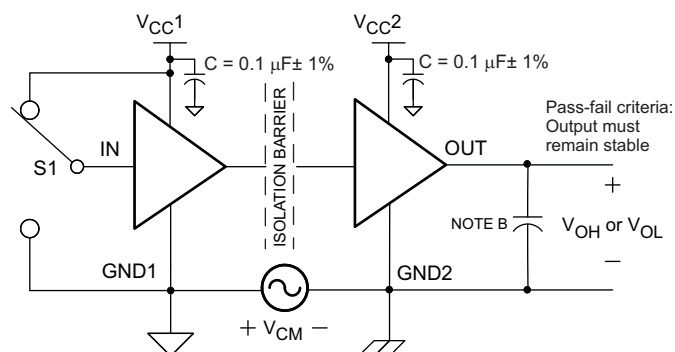


NOTE: Which ever test yields the longest time is used in this data sheet

- A. Whichever test yields the longest time is used in this data sheet.

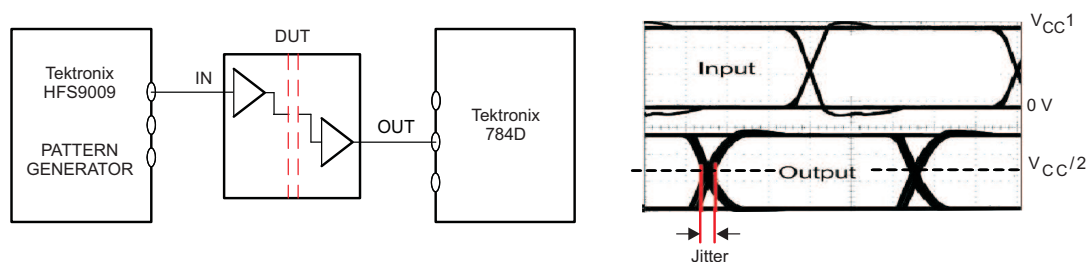
Figure 4. Wake Time From Input Disable Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



- A. $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 50 \text{ kHz}$, 50% duty cycle, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$, $Z_O = 50 \Omega$.

Figure 5. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



NOTE: PRBS bit pattern run length is $2^{16} - 1$. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 6. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

DEVICE INFORMATION

PACKAGE CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	8.34			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	8.1			mm
C _{TI}	Tracking resistance (comparative tracking index)	DIN IEC 60112/VDE 0303 Part 1	≥ 175			V
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R _{IO}	Isolation resistance	Input to output, V _{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device		>10 ¹²		Ω
C _{IO}	Barrier capacitance Input to output	V _I = 0.4 sin (4E6πt)		2		pF
C _I	Input capacitance to ground	V _I = 0.4 sin (4E6πt)		2		pF

IEC 60664-1 RATINGS TABLE

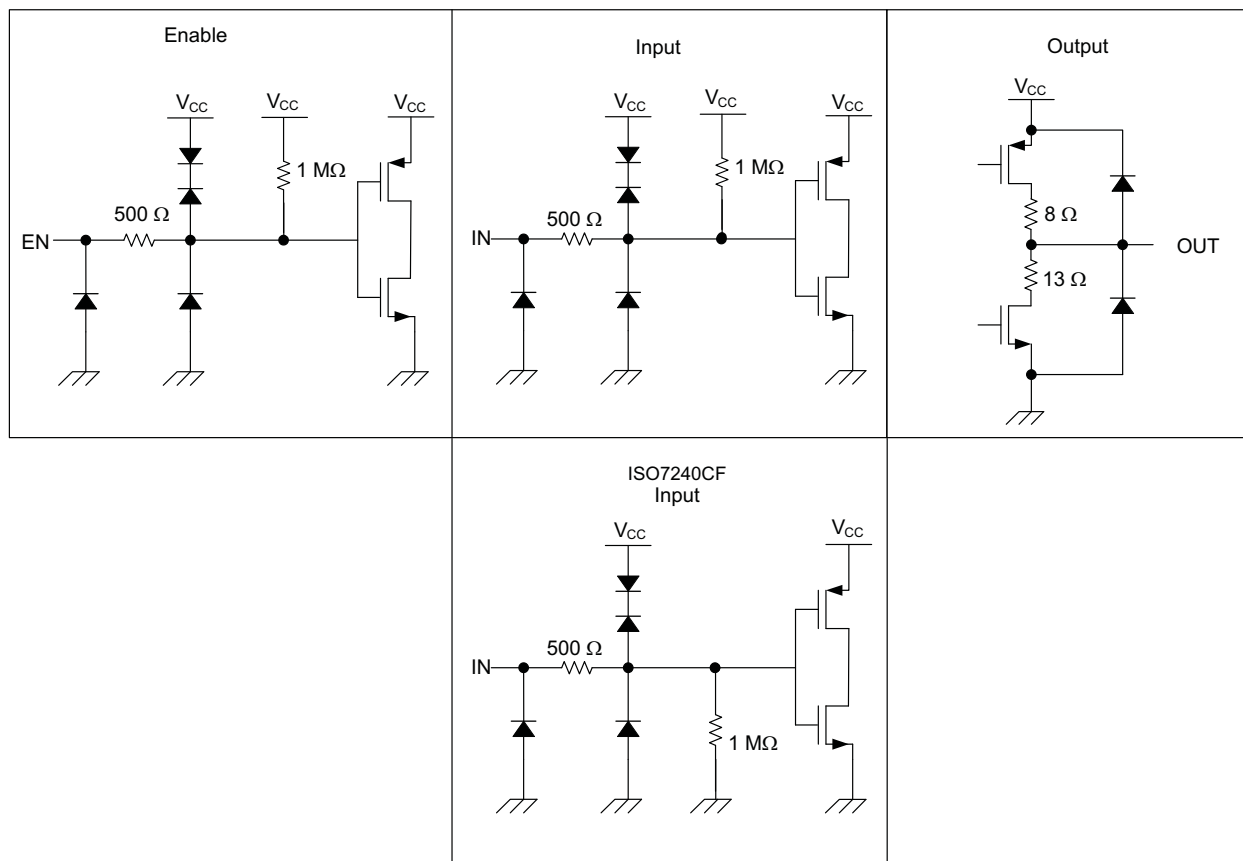
PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	IIIa
Installation classification	Rated mains voltage ≤150 VRMS	I-IV
	Rated mains voltage ≤300 VRMS	I-III

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program ⁽¹⁾
File Number: 40016131	File Number: 1698195	File Number: E181974

(1) Production tested ≥ 3000 Vrms for 1 second in accordance with UL 1577.

DEVICE I/O SCHEMATICS



THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA} Junction-to-air	Low-K Thermal Resistance ⁽¹⁾		168		°C/W
	High-K Thermal Resistance		96.1		
θ_{JB} Junction-to-Board Thermal Resistance			61		°C/W
θ_{JC} Junction-to-Case Thermal Resistance			48		°C/W
P_D Device Power Dissipation	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150^\circ$ C, $C_L = 15$ pF, Input a 50% duty cycle square wave			220	mW

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

TYPICAL CHARACTERISTIC CURVES

ISO7240C RMS SUPPLY CURRENT
VS
SIGNALING RATE

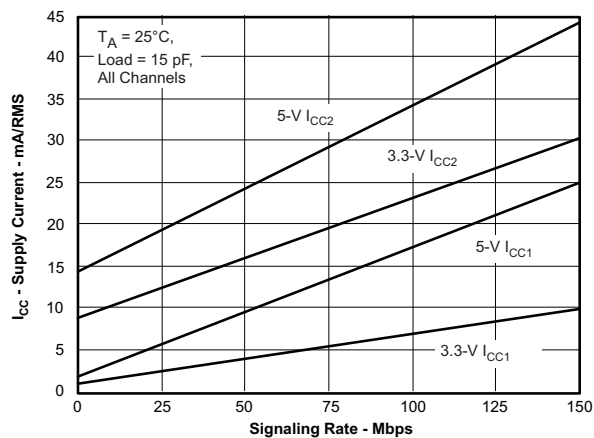


Figure 7.

ISO7241C RMS SUPPLY CURRENT
VS
SIGNALING RATE

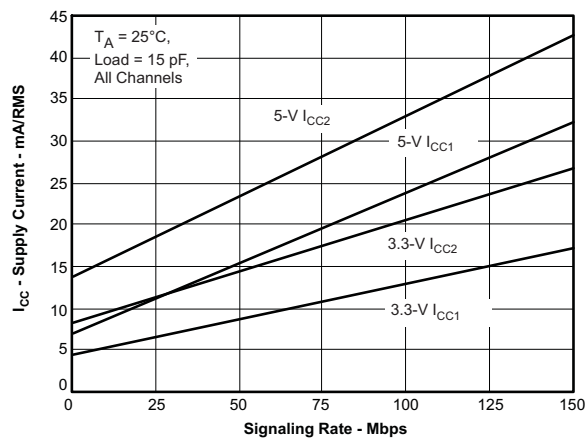


Figure 8.

ISO7242C RMS SUPPLY CURRENT
VS
SIGNALING RATE

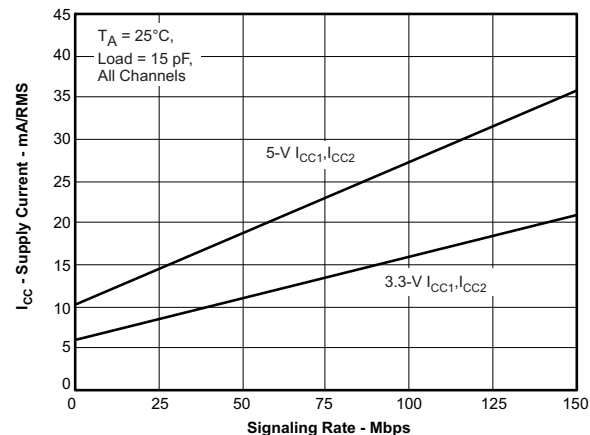


Figure 9.

PROPAGATION DELAY
VS
FREE-AIR TEMPERATURE

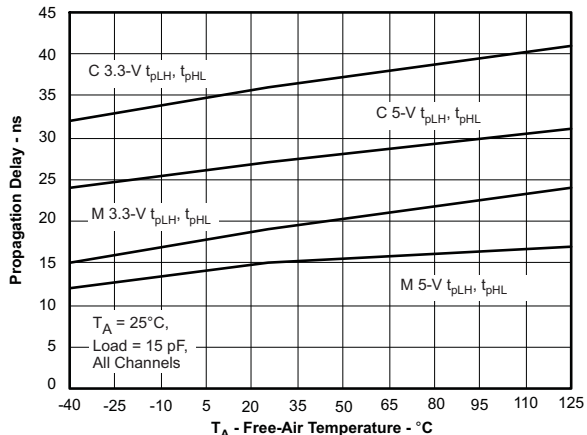


Figure 10.

TYPICAL CHARACTERISTIC CURVES (continued)

INPUT VOLTAGE THRESHOLD
VS
FREE-AIR TEMPERATURE

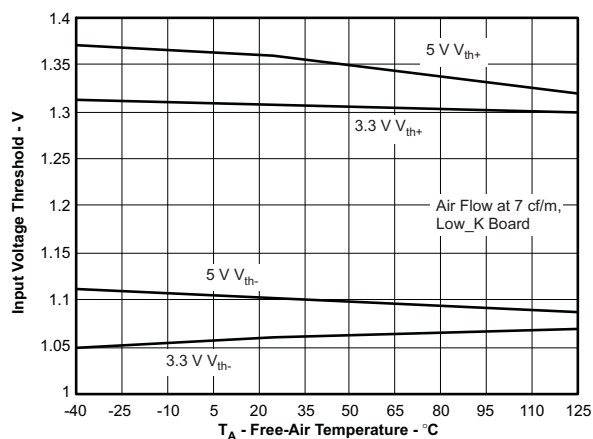


Figure 11.

V_{CC1} FAILSAFE THRESHOLD
VS
FREE-AIR TEMPERATURE

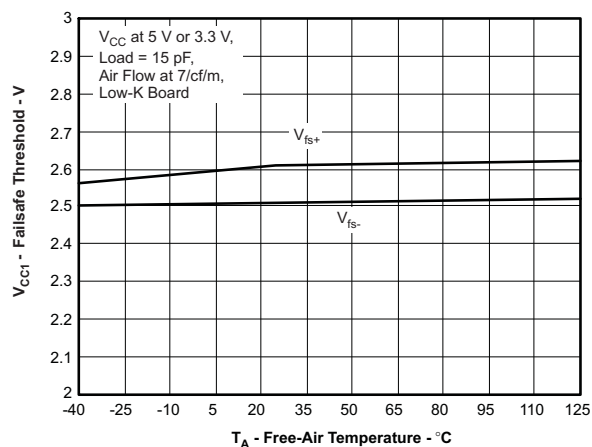


Figure 12.

HIGH-LEVEL OUTPUT CURRENT
VS
HIGH-LEVEL OUTPUT VOLTAGE

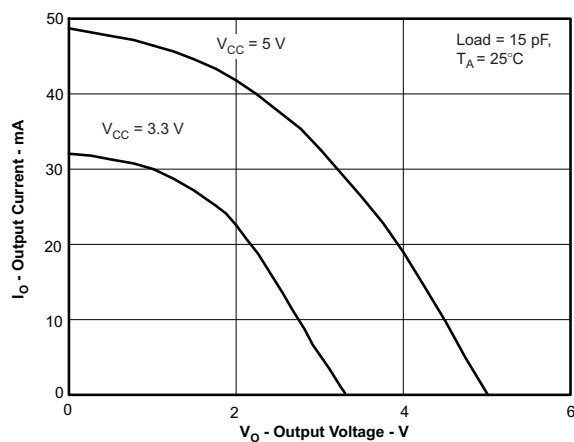


Figure 13.

LOW-LEVEL OUTPUT CURRENT
VS
LOW-LEVEL OUTPUT VOLTAGE

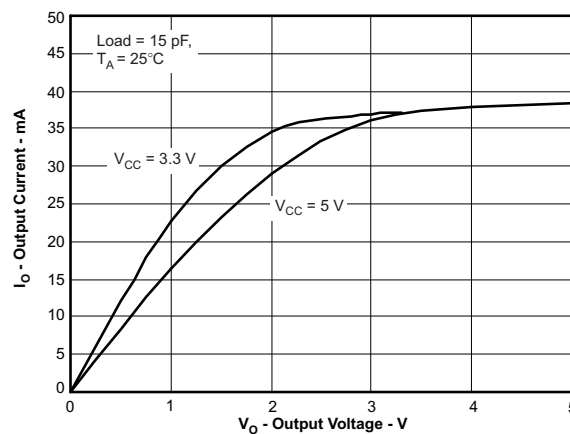


Figure 14.

APPLICATION INFORMATION

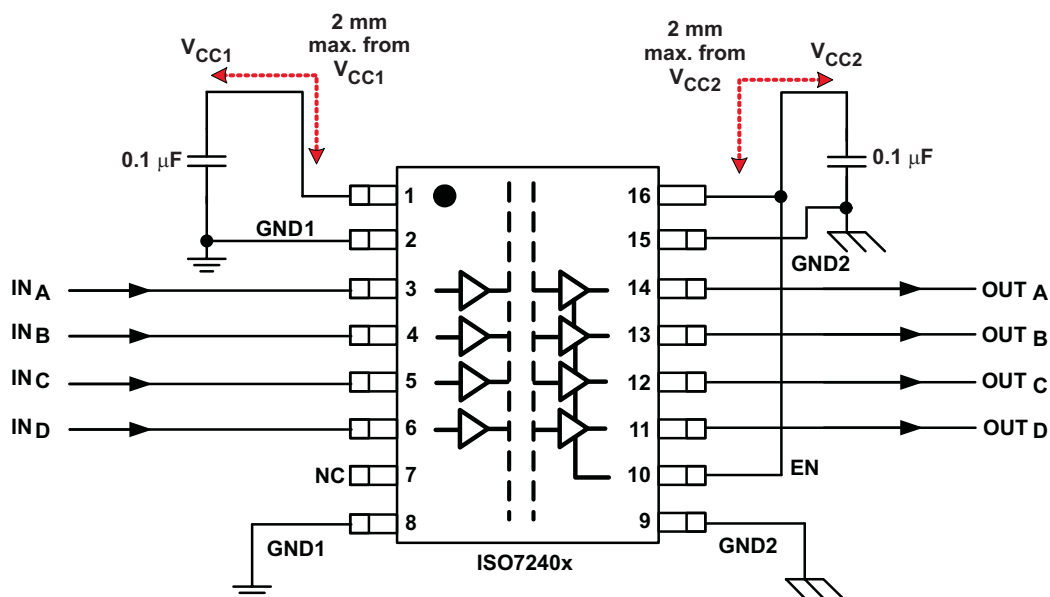


Figure 15. Typical ISO7240x Application Circuit

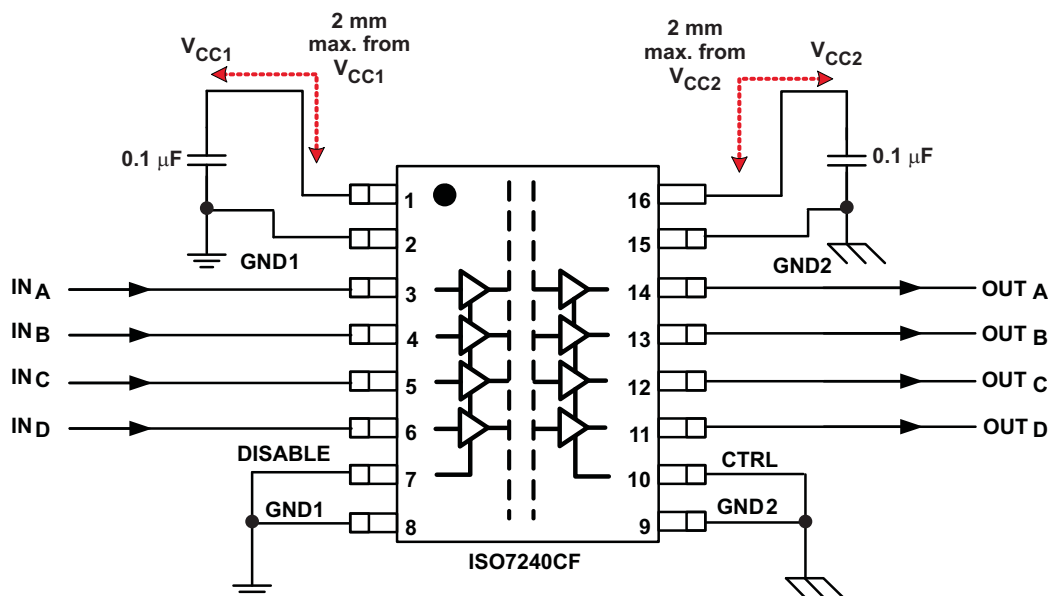


Figure 16. Typical ISO7240CF Failsafe-Low Application Circuit

LIFE EXPECTANCY vs WORKING VOLTAGE

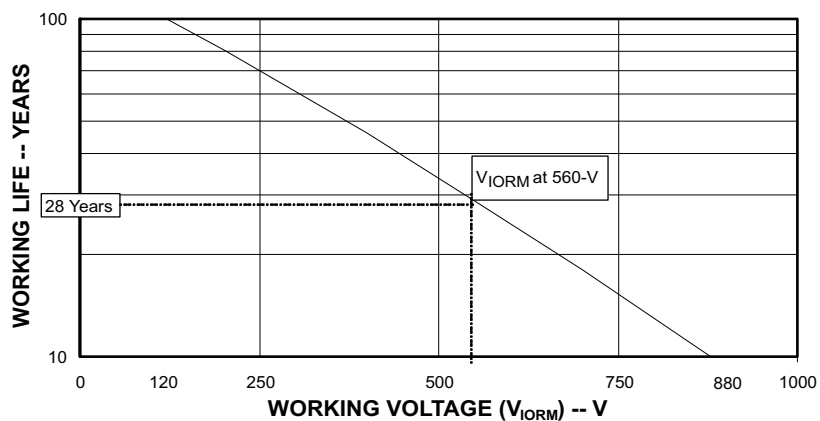


Figure 17. Time-Dependant Dielectric Breakdown Testing Results

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7240CFQDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7240CFQ	Samples
ISO7241CQDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7241CQ	Samples
ISO7242CQDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7242CQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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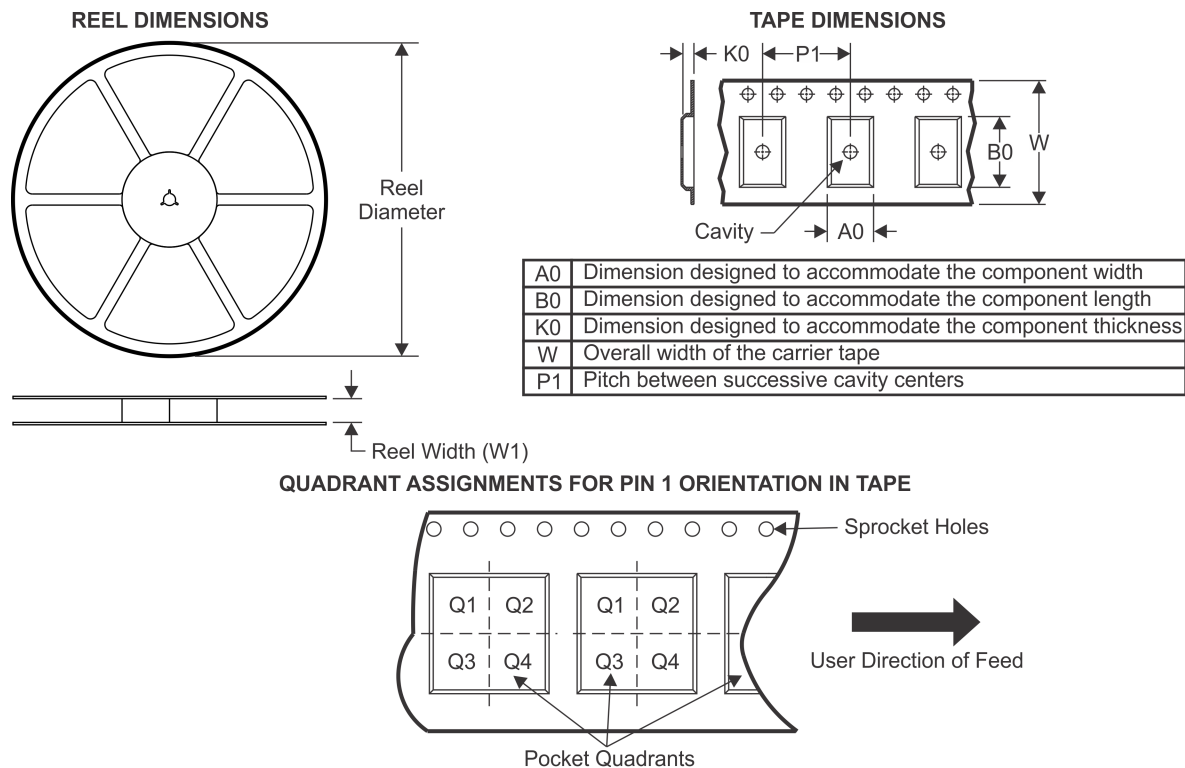
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ISO7240CF-Q1, ISO7241C-Q1, ISO7242C-Q1 :

- Catalog: [ISO7240CF](#), [ISO7241C](#), [ISO7242C](#)

NOTE: Qualified Version Definitions:

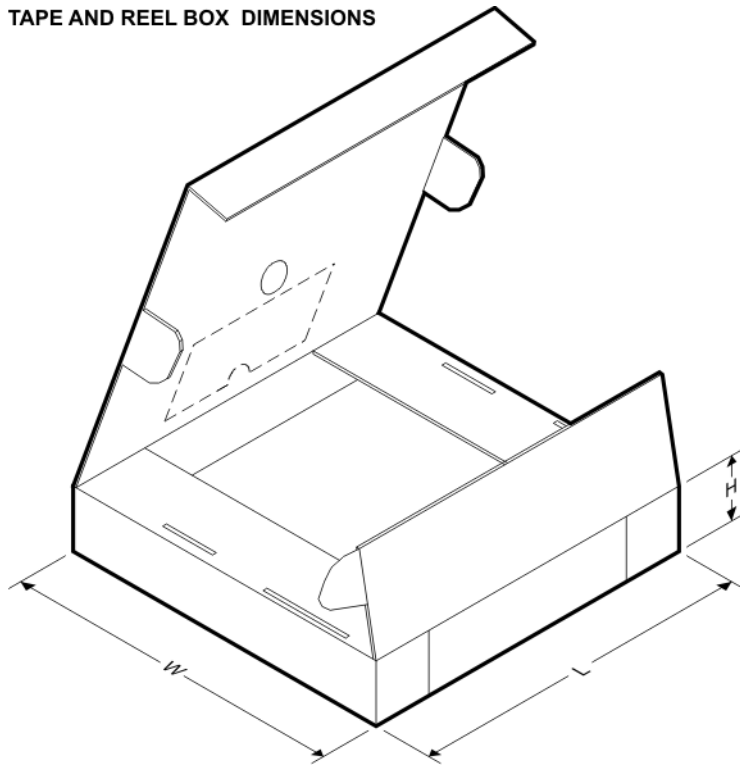
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7240CFQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7241CQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7242CQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7240CFQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7241CQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7242CQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

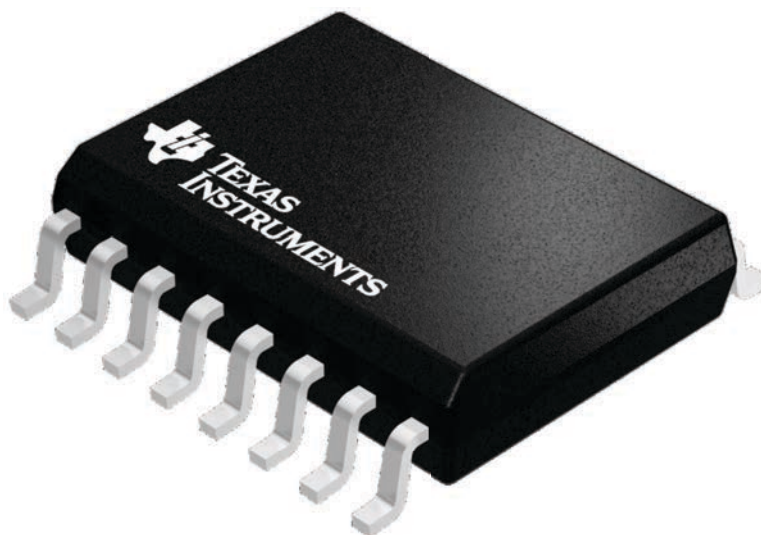
DW 16

SOIC - 2.65 mm max height

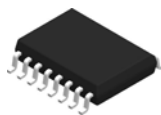
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

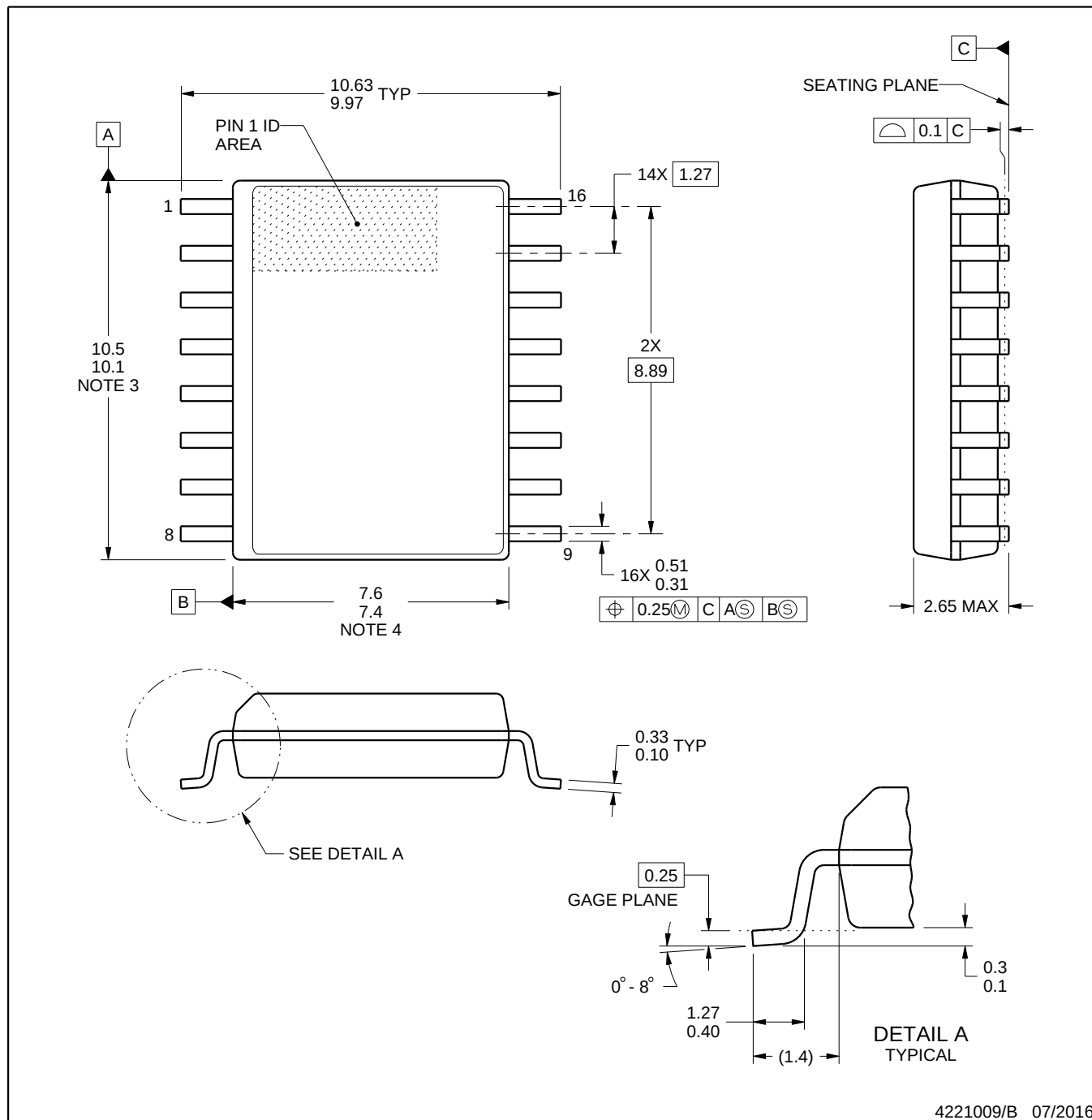


DW0016B

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

NOTES:

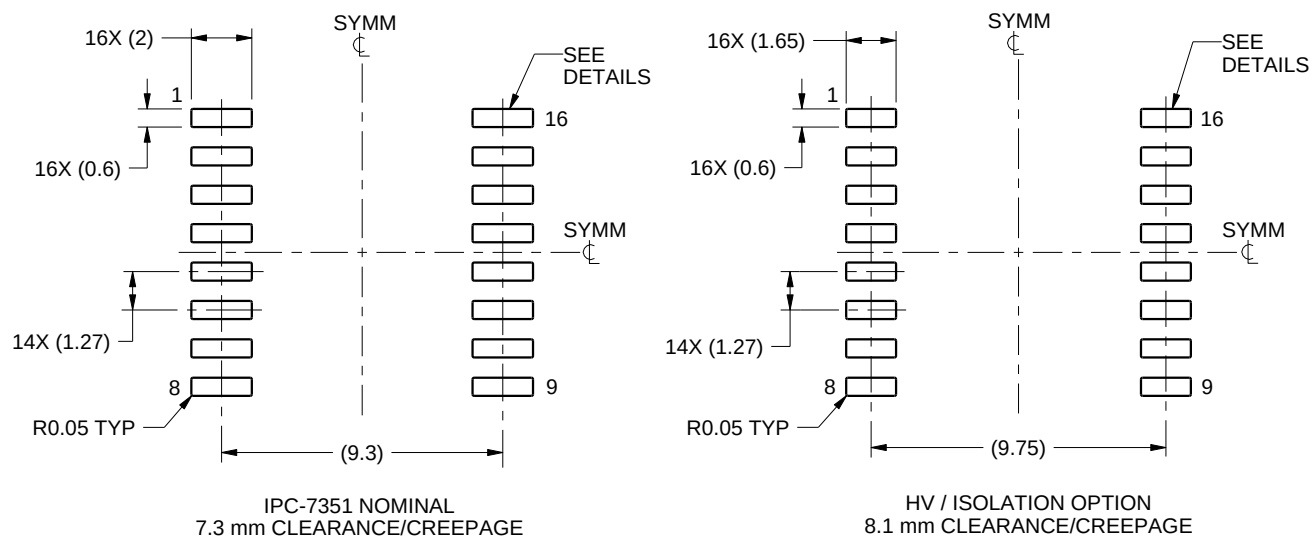
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

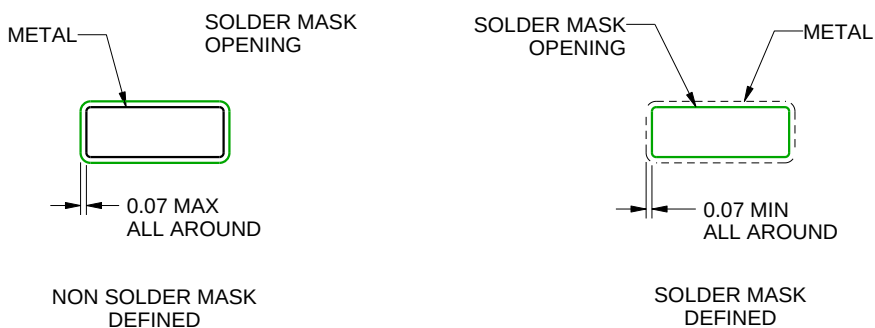
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

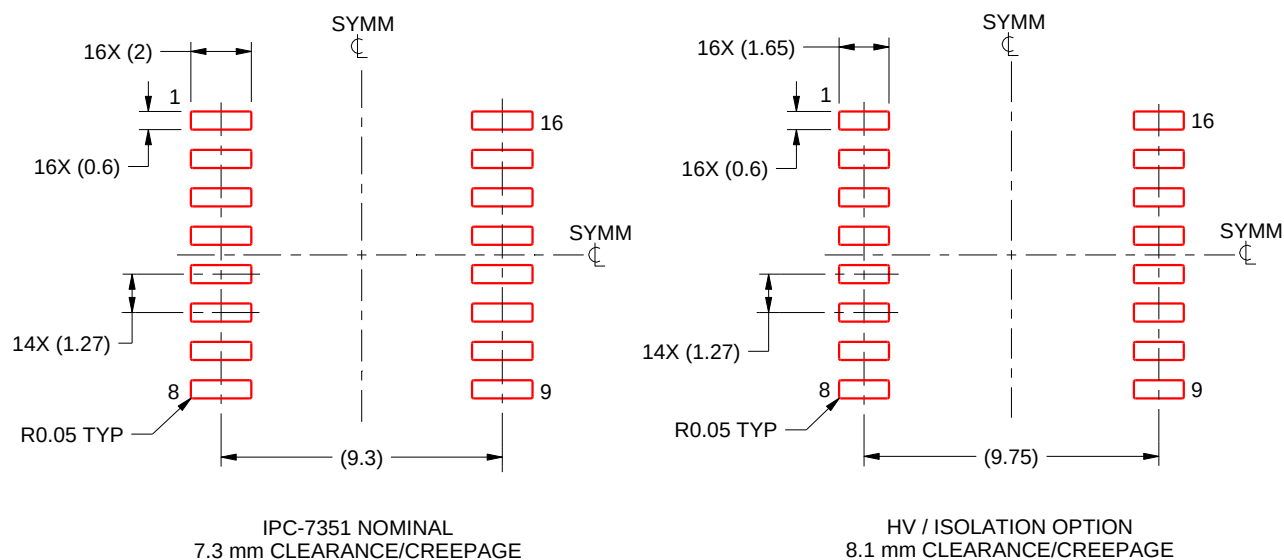
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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