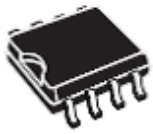
STCH03

Offline PWM controller for low standby adapters

Datasheet - production data



SO8

Features

- Advanced power management for ultra-low standby power consumption (under 10 mW at 230 VAC)
- Fully integrated primary side constant current output regulation (CC)
- 650 V embedded HV start-up circuit with zero power consumption.
- Quasi-resonant (QR) zero-voltage-switching (ZVS) operation
- Accurate and adjustable output OVP with options auto-restart (STCH03) or latched (STCH03L) after fault
- Output undervoltage protection (UVP) with auto-restart
- Input voltage feedforward compensation for mains-independent CC regulation
- Embedded thermal shutdown
- Intelligent frequency jitter for EMI suppression
- SO8 package

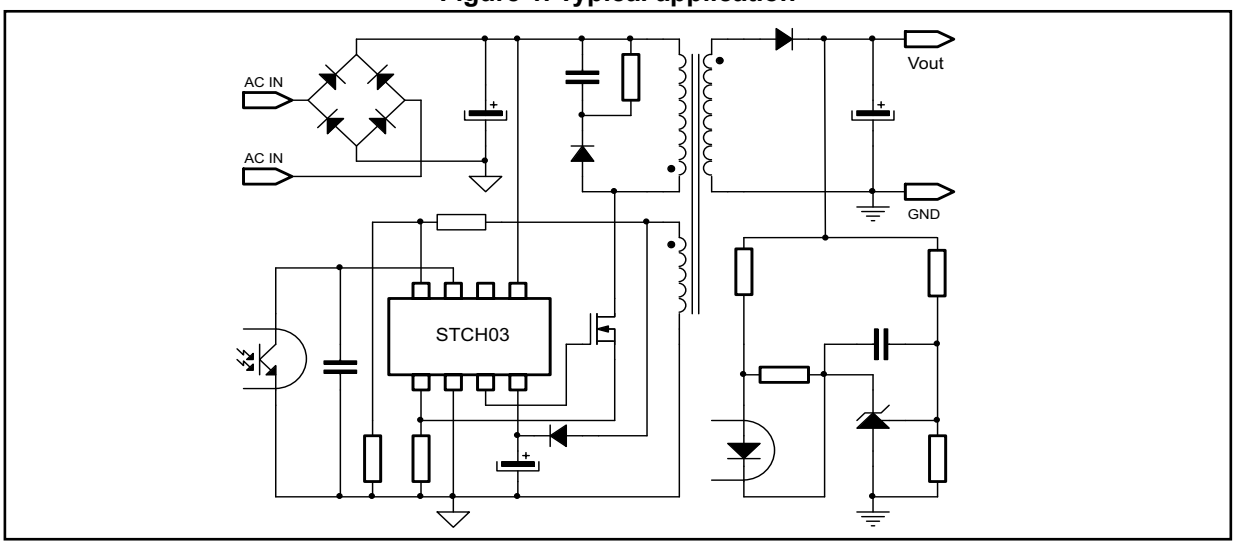
Applications

- AC-DC chargers for smartphones, tablets, camcorders and other handheld equipment
- AC/DC adapters for STB, notebooks and auxiliary power supplies
- USB power delivery fast charger

Table 1. Device summary

Order codes	Package	Packaging
STCH03	SO8	Tube
STCH03L		
STCH03TR		Tape and reel
STCH03LTR		

Figure 1. Typical application



This is information on a product in full production. www.st.com

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1 Description

The STCH03 current-mode controller is designed for an offline quasi-resonant ZVS (zero-voltage-switching at switch turn-on) flyback converter.

It combines a high-performance low-voltage PWM controller chip and a 650V HV start-up cell in the same package.

Constant output voltage (CV) regulation loop is achieved by secondary side feedback, the output voltage information is transfered via an optocoupler on the FB pin of the STCH03 to get the selected output voltage.

The device features a unique characteristic: it is capable of providing constant output current regulation (CC) using primary-sensing feedback. This eliminates the need for dedicated current reference IC, as well as the current sensor, still maintaining quite accurate output current regulation.

The quasi-resonant operation is achieved by means of a transformer demagnetization sensing input that triggers the turn-on of the MOSFET, connected on the ZCD pin. This input serves also as both output voltage monitor, to achieve mains-independent CC regulation (line voltage feedforward), and to implement OVP and UVP.

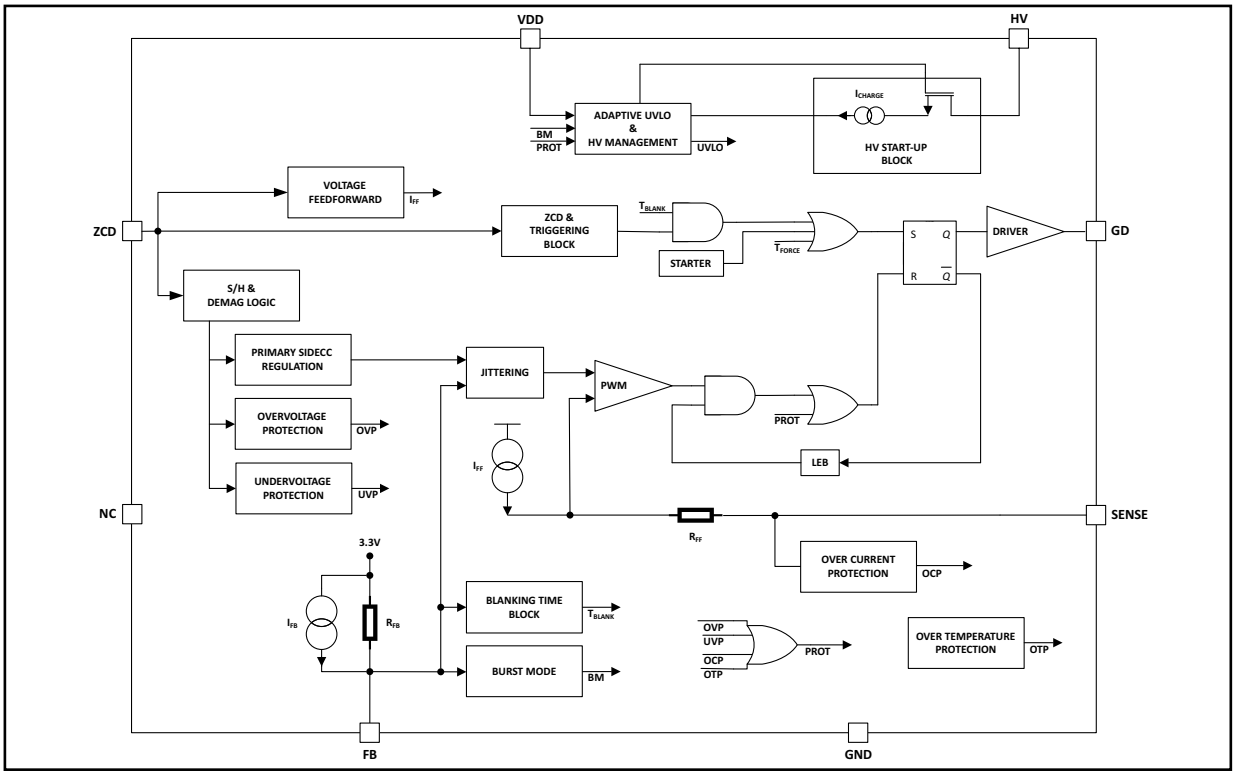
The maximum switching frequency is top-limited below 154 kHz, so that at the medium-light load a special function automatically lowers the operating frequency whilst still maintaining the operation as close to ZVS as possible. At the very light load, the device enters a controlled burst-mode operation that, along with the zero-power high-voltage start-up circuit, the extremely low quiescent current of the device, helps minimize the residual input consumption, thus meeting the requirements of the most stringent standards.

During the burst-mode operation the V_{DD} supply voltage has to be guaranteed by optimum application design. In any case, an innovative adaptive UVLO helps to minimize the issues related to the fluctuations of the auxiliary biasing voltage with the output load, due to parasitic capacitance of the transformer and further reducing the IC's bias consumption.

In addition to these functions that optimize power handling under different operating conditions, the device also offers the output overvoltage protection (OVP), overtemperature protection (OTP), hiccup-mode protection that is invoked when the transformer saturates or the secondary diode fails short and the output undervoltage protection (UVP) that limits the average output current in case of the output short-circuit. All the protections are auto-restart mode, except the OVP protection, that can be internally selected to be auto-restart or latched mode.

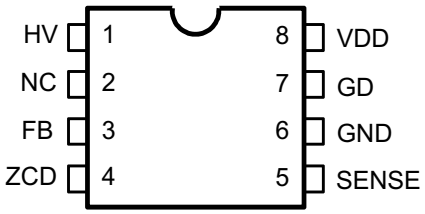
The embedded leading-edge blanking on the current sense input for greater noise immunity completes the equipment of this device.

Figure 2. Block diagram



2 Pin connection and functions

Figure 3. Pin connection (top view)



AM040303

Table 2. Pin functions

No.	Name	Function
1	HV	High-voltage start-up. This pin is able to withstand 650 V and is tied directly to the rectified mains voltage. When the voltage on the pin reaches the HV_{START} voltage (50 V typ.) a 7 mA internal current source charges the capacitor connected between V_{DD} and GND to start-up the IC. When the voltage on the V_{DD} pin reaches the turn-on threshold (17 V typ.) the generator is shut down.
2	NC	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
3	FB	Control input for peak current control. A voltage set 65 mV below the threshold V_{FBB} activates the burst-mode operation. A level higher than the threshold V_{FBH} corresponds to the maximum value of the current sense threshold (VCSx).
4	ZCD	The transformer demagnetization sensing for quasi-resonant operation and input/output voltage monitor. A negative-going edge triggers the MOSFET turn-on. The current sourced by the pin during the MOSFET ON time is monitored for an image of the input voltage to the converter, in order to compensate the internal delay of the current sensing circuit and achieve a CC regulation independent of the mains voltage. At the same time the pin voltage is sampled-and-held right at the end of the transformer demagnetization to get an accurate image of the output voltage to be used for overvoltage protection (OVP) and undervoltage protection (UVP) sensing. Please note that maximum I_{ZCD} sink/source current must not exceed 3 mA over the entire voltage range. No capacitor is allowed to be connected to this pin.
5	SENSE	Input to the PWM comparators. The current flowing in the MOSFET is sensed through a resistor connected between the pin and GND. The resulting voltage is compared with an internal reference, derived from the FB pin voltage, to determine MOSFET turn-off. The pin is equipped with 380 ns blanking time after the gate-drive output goes high for improved noise immunity. If a second comparison level located at V_{CSx}, is exceeded, the IC stops and restarts after V_{DD} has dropped below V_{DDR} (4.5 V typ.).
6	GND	Circuit ground reference and current return for both the signal part of the IC and the gate-drive. All of the ground connections of the bias components should be tied to an interconnect going to this pin and kept separate from any pulsed current return.
7	GD	Gate-driver with the totem pole output stage for the external power MOSFET.
8	V_{DD}	Supply voltage of the device. An electrolytic capacitor, connected between this pin and ground, is initially charged by the internal high-voltage start-up generator. It is recommended to place a small bypass capacitor (0.1 µF typ.) connected between the pin and GND.

3 Electrical data

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{HV}	1	Voltage range (referred to GND)	-0.3 to 650	V
I_{HV}	1	Charging current	Self-limited	mA
-	3 to 6	Analog inputs and outputs	-0.3 to 3.6	V
I_{ZCD}	4	Zero current detector current	± 3	mA
I_{GD}	6	Output totem pole peak current	Self-limited	-
V_{DD}	8	Supply voltage (I_{CC} < 25 mA)	Self-limited	V
I_{DD}	8	Device supply current + internal Zener capability	25	mA
T_J		Junction temperature range	-40 to 150	°C
T_{STG}		Storage temperature	-55 to 150	°C

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance, junction to ambient	150	°C/W

4 Electrical characteristics

Tj = - 25 °C to 125 °C, V_{DD} = 14 V[(a)], unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
HIGH-VOLTAGE START-UP GENERATOR						
V_{HV}	HV voltage	I_{HV} < 2 µA, Tj = 25 °C	-	-	650	V
$I_{LEAKAGE}$	HV leakage current	V_{HV} = 400 V, Tj = 25 °C	-	-	1	µA
HV_{START}	HV start voltage	-	40	50	60	V
I_{CHARGE}	V_{DD} startup charge current	V_{HV} > H_{VSTART}; V_{DD} ≤ VDD-FOLD	0.3	0.6	0.9	mA
		V_{HV} > H_{VSTART}; 2 V < V_{DD} < V_{DDOn}	4.5	7	10.3	
$V_{DD-FOLD}$	V_{DD} foldback threshold	V_{HV} > HV_{START}	1	1.4	2	V
SUPPLY VOLTAGE						
V_{DD}	Operating range	After turn-on	11.5	-	23	V
V_{DD-ON}	Turn-on threshold	-	15.7	17	18.3	V
V_{DD-OFF}	Restart threshold (latched version only)	V_{FB} > V_{FBF}	9	10	11	V
$V_{DD-UVLO}$	UVLO threshold	V_{FB} > V_{FBF}	8.55	9.5	10.45	V
		V_{FB} < (V_{FBB} - 65 mV)	6.75	7.5	8.25	V
V_{DDR}	V_{DD} restart voltage (falling)	After protection tripping	-	4.5	-	V
		In burst-mode	-	3.2	-	
V_Z	V_Z clamping voltage	I_{DD} = 25 mA	23	-	26.5	V
SUPPLY CURRENT						
I_Q	Quiescent current	Burst operation	-	290	335	µA
I_{DD}	Operating supply current	C_{GATE} = 1 nF, F_{SW} = 100 Khz	-	2.5	2.9	mA
$I_{DD-FAULT}$	Fault quiescent current	OCP, OVP, UVP, OTP	-	330	420	µA
START-UP TIMER AND FREQUENCY LIMIT						
T_{START}	Starter period	-	-	220	-	µs
F_{LIM_MAX}	Max. internal frequency limit	-	-	154	-	kHz
T_{SU}	Soft-start duration	-	12	20	28	ms
ZERO CURRENT DETECTOR						
I_{ZCDB}	Input bias current	V_{ZCD} = 0.1 to 2.7 V	-	-	1	µA
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 1 mA	2.7	3	3.5	V

a. Adjust V_{DD} above V_{DD-ON} start-up threshold before settings to 14 V.

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = - 1 mA	-90	-60	-30	mV
V_{ZCDA}	Arming voltage	Positive-going edge	100	110	120	mV
V_{ZCDT}	Triggering voltage	Negative-going edge	50	60	70	mV
T_{BLANK}	Trigger blanking time after MOSFET turn-on	$V_{FB} \geq 1.65$ V	4.68	6.2	7.76	µs
		V_{FB} = 0.6 V	29	38	47	
T_{D-ON}	Turn-on delay time after triggering	V_{GATE} = 6 V, C_{GATE} = 1 nF	-	270	-	ns
T_{FORCE}	Force turn-on time after blanking	-	5.1	6	6.9	µs
LINE FEEDFORWARD						
R_{FF}	Equivalent feedforward resistor	I_{ZCD} = 1 mA	60	70	80	Ω
GATE-DRIVER						
V_{GDH}	Output high voltage	V_{DD} = 8.5 V; I_{GATE} = 5 mA	7	-	-	V
		I_{GATE} = 5 mA	10.5	13	-	
T_{RISE}	Rising time	C_{GATE} = 1 nF	70	110	150	ns
T_{FALL}	Falling time	C_{GATE} = 1 nF	20	40	60	ns
V_{GDL}	Output low voltage	$I_{GD-SINK}$ = 50 mA	-	-	1	V
I_{source}	Source current	C_{GATE} = 1 nF	64	87	137	mA
I_{sink}	Sink current	C_{GATE} = 1 nF	160	240	480	mA
FEEDBACK INPUT						
V_{FBH}	Upper saturation	-	-	3.45	-	V
H_{FB}	Current sense gain(1)	-	3.22	3.29	3.36	-
I_{FB}	Feedback source current	-	70	100	130	µA
R_{FB}	Dynamic feedback resistor	-	25	30	41	kΩ
V_{FBR}	Frequency reduction threshold	-	1.4	1.65	1.9	V
V_{FBB}	Burst-mode threshold	Voltage falling	0.54	0.6	0.66	V
V_{FBF}	Adaptive UVLO mode exit threshold	Voltage rising	0.64	0.72	0.8	V
V_{HYST}	Burst-mode hysteresis	-	50	65	75	mV
CURRENT REFERENCE						
K_I	Current loop gain	-	0.19	0.2	0.21	V
OVERVOLTAGE PROTECTION						
V_{OVP}	OVP threshold	-	2.375	2.5	2.625	V
N_{OVP}	Consecutive cycles for OVP triggering	V_{OVP} = 2.5 V	-	4	-	-
UNDERVOLTAGE PROTECTION						
V_{UVP}	UVP threshold	-	0.522	0.55	0.578	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{UVP}	UVP blanking time	-	12	20	28	ms
N_{UVP}	Consecutive cycles for UVP triggering	V_{UVP} = 0.55 V	-	4	-	-
CURRENT SENSE						
T_{LEB}	Leading-edge blanking	V_{GATE} = 6 V, C_{OUT} = 1 nF	270	380	490	ns
T_D	Gate delay-to-output	V_{GATE} = 6 V, C_{OUT} = 1 nF	-	-	150	ns
V_{CSx}	Max. clamp value	dVCS/dt = 200 mV/µs	0.7	0.75	0.8	V
V_{OCP}	Hiccup-mode OCP level		0.95	1	1.05	V
V_{SENSE_BM}	Minimum burst-mode sense voltage	-	-	72	-	mV
FREQUENCY JITTERING						
F_D	Modulation frequency	-	-	9	-	kHz
V_{ZCDH}	Modulation duty cycle	-	-	50	-	%
ΔIpk	Peak current change	-	-	5	-	%
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature	Guaranteed by design and characterization	135	150	165	°C
T_{HYST}	Thermal shutdown hysteresis	Guaranteed by design and characterization	-	30	-	°C

1. $V_{CS} = (V_{FB} - V_{FBB}) / H_{FB}$

5 Operation overview

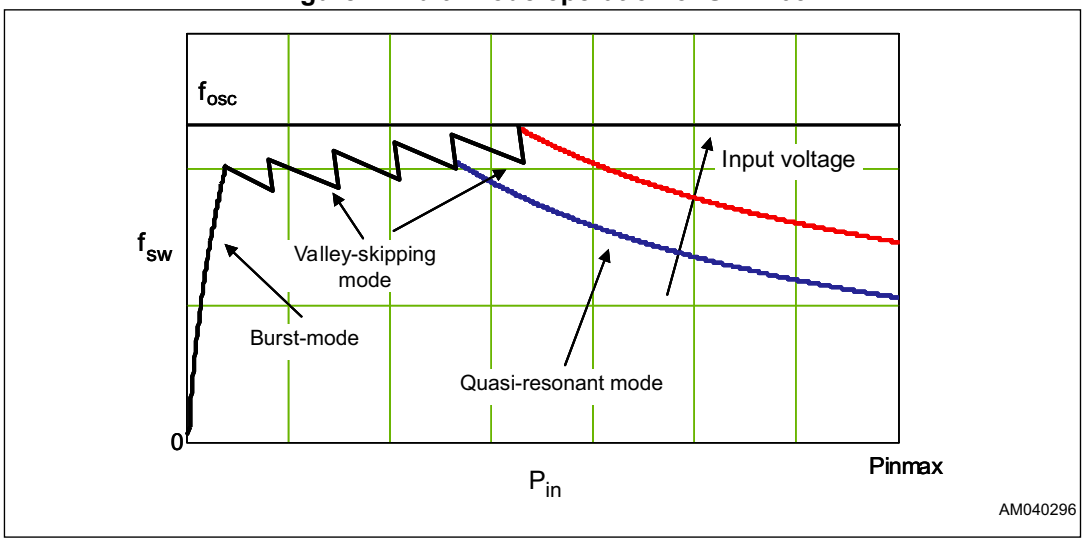
The STCH03 is an offline CC-mode primary sensing switching controller, specific for offline quasi-resonant ZVS (zero voltage switching) flyback converters.

The STCH03 controller can operate in different modes that depend on the input voltage VHV, the supply voltage VDD, and the output load conditions.

Start-up mode. When VHV exceeds the HVSTART threshold, the High Voltage Startup (HVSU) is enabled to charging the electrolytic capacitor connected to the VDD pin. After that, when VDD exceeds the VDD-ON threshold, the controller disabling the HVSU and starts switching to deliver power to the converter output. On initial power-up, as the output voltage is zero, the IC will start in the CC-mode with no high peak current operations. In this way, the voltage on the output capacitor increases slowly and the soft-start feature is ensured. The soft-start feature is automatically implemented by the constant current block, as the primary peak current is limited from the voltage on the internal CC block capacitor. Start-up mode ends when the voltage on the FB pin is in its operating range to regulate the output voltage. During the start-up period (TSU) the UVP protection is disabled.

Active mode. After start-up mode the device can operate in three different modes that depends on the output load level of the converter (see *Figure 4*), this allows reducing power losses and increasing the efficiency of the system under different load conditions.

Figure 4. Multi-mode operation of STCH03



QR mode at heavy load. Quasi-resonant operation is achieved by synchronizing the MOSFET turn-on to the transformer demagnetization by detecting the resulting negative-going edge of the voltage across any winding of the transformer. Then the system works close to the boundary between discontinuous (DCM) and continuous conduction (CCM) of the transformer. As a result, the switching frequency is different for different line/load conditions. The minimum turn-on losses, low EMI emission and safe behavior in short-circuit are the main benefits of this kind of operation.

Valley-skipping mode at medium/light load. Depending on voltage on the FB pin, the device defines the maximum operating frequency of the converter. As the load is reduced the MOSFET turn-on no longer occurs on the first valley but on the second one, the third one and so on. In this way the switching frequency, no longer increases.

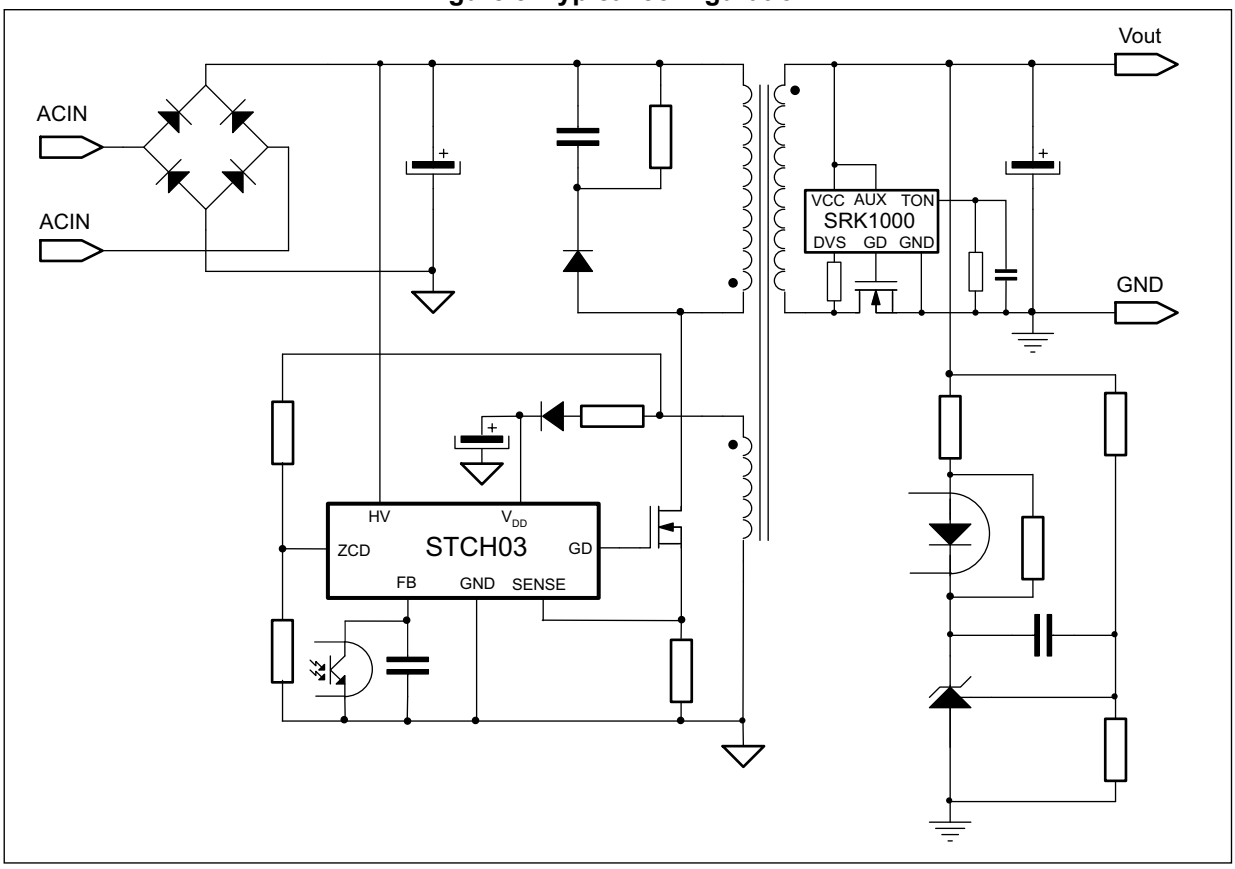
Burst-mode with no or very light load. When the load is extremely light or disconnected, the converter will enter a controlled on/off operation with constant peak current. Decreasing the load will then result in frequency reduction, which can go down even to a few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations or recommendations. As the peak current is very low, no issue of audible noise arises.

Stop mode. If a failure occurs or VDD drops below VDD-OFF threshold, the device stop the switching activity and the start-up sequence repeats. In case of failure, the device work in auto-restart mode: the fault is removed every time that VDD drops below the VDDR threshold and then the start-up sequence is initiated. Only for the OVP protection is possible choose between auto-restart mode and latched mode. In this last case, the device is latched off until VHV drops below HVSTART threshold and VDD drops below the VDDR threshold, then the start-up sequence is initiated.

6 Application information

The STCH03 is an offline switching controller specific for quasi-resonant ZVS (zero voltage switching) flyback converters. The STCH03 uses a feedback signal from the output to provide a very accurate output-voltage regulation. The device includes the PWM logic, ZCD logic for quasi-resonant and output voltage protections, oscillator, start-up circuit with soft-start, burst mode management, UVLO circuit, auto-restart circuit and thermal protection circuit. All these features allow implementing a highly efficient offline supply using the STCH03 controller. Application schematic of the main topology is reported in *Figure 5*.

Figure 5. Typical configuration



6.1 High voltage start-up generator

Based on a 650 V rated depletion MOSFET embedded into the start-up cell, the HV current generator is supplied through the DRAIN pin and is enabled only if the voltage on the HV pin is higher than the HV_{START} threshold (50 V typical value).

When the power is applied to the circuit and the voltage on the input bulk capacitor is high enough, the HV generator is sufficiently biased to start operating, thus it will draw the current I_{CHARGE} (7 mA typ. value) through the HV pin and will charge the capacitor connected between the V_{DD} pin and ground. This charging current will be reduced at 0.6 mA in case

the voltage on V_{DD} is lower than VDD-FOLD, in order to prevent exceeding the IC dissipation when the pin is accidentally shorted to ground.

As the V_{DD} voltage reaches the start-up threshold (17 V typ.) the chip starts operating and the control logic disables the HV generator.

While the generator is off, there are virtually no losses across the HV start-up cell, except a few hundred nA of leakage current through the depletion MOSFET.

The IC is powered by the energy stored in the V_{DD} capacitor until the auxiliary winding develops a voltage high enough to sustain the operation.

At converter power-down the system will lose regulation as soon as the input voltage falls below HV_{START}. This prevents the converter restarting and ensures the monotonic output voltage decay at system power-down.

Although the HV pin can be connected directly to input voltage, in some circumstances, a resistor can be placed between HV pin and input voltage in order to improve the application's ruggedness or to reduce the maximum charging current.

6.2 Zero current detection and triggering block

The zero current detection (ZCD) and triggering blocks switch on the power MOSFET if a negative-going edge falling below 60 mV is applied to the ZCD pin. To do so, the triggering block must be previously armed by a positive-going edge exceeding 110 mV.

This feature is used to detect transformer demagnetization for the QR operation, where the signal for the ZCD input is obtained from the transformer auxiliary windings used also to supply the IC.

The triggering block is blanked after MOSFET turn-on to prevent any negative-going edge that follows leakage inductance demagnetization from triggering the ZCD circuit erroneously.

The switching frequency is top-limited below 154 kHz.

To prevent the tendency of the system to excessively increase the frequency at the light load and high input voltage, a variable blanking time function is implemented.

This blanking time is dependent on the voltage on the FB pin: it is T_{BLANK} = 38 µs for V_{FB} = 0.6 V, and decreases linearly down to T_{BLANK} = 6.2 µs for $V_{FB} \geq$ 1.65 V. In this way, the switching frequency is progressively reduced, resulting in lower frequency-related losses.

If the demagnetization completes - hence a negative-going edge appears on the ZCD pin - after a time exceeding time T_{BLANK} from the previous turn-on, the MOSFET will be turned on again, with some delay to ensure minimum voltage at turn-on (“*QR mode*”).

If, instead, the negative-going edge appears before T_{BLANK} has elapsed, it will be ignored and only the first negative-going edge after T_{BLANK} will turn-on the MOSFET. In this way one or more drain ringing cycles will be skipped (“*valley-skipping mode*”) and the switching frequency will be prevented from exceeding $1/(T_{BLANK}+T_{D\text{-}ON})$.

The blanking time limits and the mode of operation are reported in *Figure 6*.

A forced turn-on time function is implemented in case the residual oscillation on ZCD are not enough to trigger again the switching, during the low frequency operation: the power MOSFET is forced to turn-on 6 µs (typical value) after the blanking time is elapsed.

A starter block is also used to start-up the system when the signal on the ZCD pin is not high enough to trigger the MOSFET.

After the first few cycles initiated by the starter, as the voltage developed across the auxiliary winding becomes large enough to arm the ZCD circuit, the MOSFET's turn-on will start to be locked to transformer demagnetization, hence setting up the QR operation.

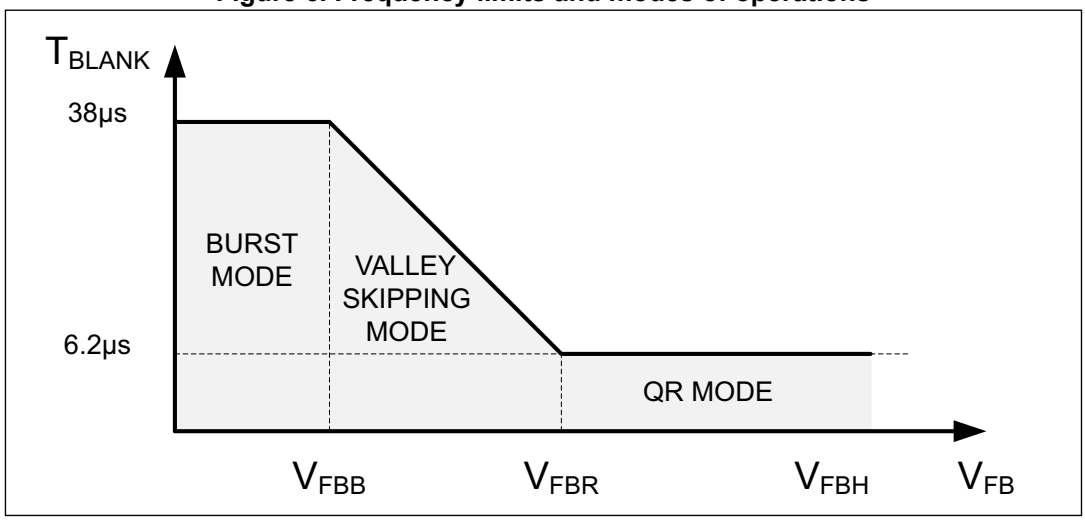
The starter is activated also when the IC is in CC regulation and the output voltage is not high enough to allow the ZCD triggering.

The voltage on the ZCD pin is both top and bottom limited by a double clamp. The upper clamp is typically located at 3 V, while the lower clamp is located at -60 mV. The interface between the pin and the auxiliary winding will be a resistor divider. Its resistance ratio as well as the individual resistance values will be properly chosen (see *Section 6.10: Overvoltage protection on page 19* and *Section 6.5: Voltage feedforward block on page 16*).

Please note that the maximum I_{ZCD} sink/source must not exceed ± 3 mA (AMR) in all the input voltage range conditions (88 - 265 VAC). No capacitor is allowed to be connected to this pin and other part of the application..

Note that when the system operates in the valley skipping-mode, uneven switching cycles may be observed under some line/load conditions, due to the fact that the OFF-time of the MOSFET is allowed to change with discrete steps of one ringing cycle, while the OFF-time needed for cycle-by-cycle energy balance may fall in between. Thus one or more longer switching cycles will be compensated by one or more shorter cycles and vice versa. However, this mechanism is absolutely normal and there is no appreciable effect on the performance of the converter or on its output voltage.

Figure 6. Frequency limits and modes of operations



6.3 Peak current mode operation

The device is specific for the secondary feedback. The FB pin is connected to an optocoupler which transmits the error signal from the regulation loop located on the secondary side of the converter. Typically, a TS431 is used as a voltage reference.

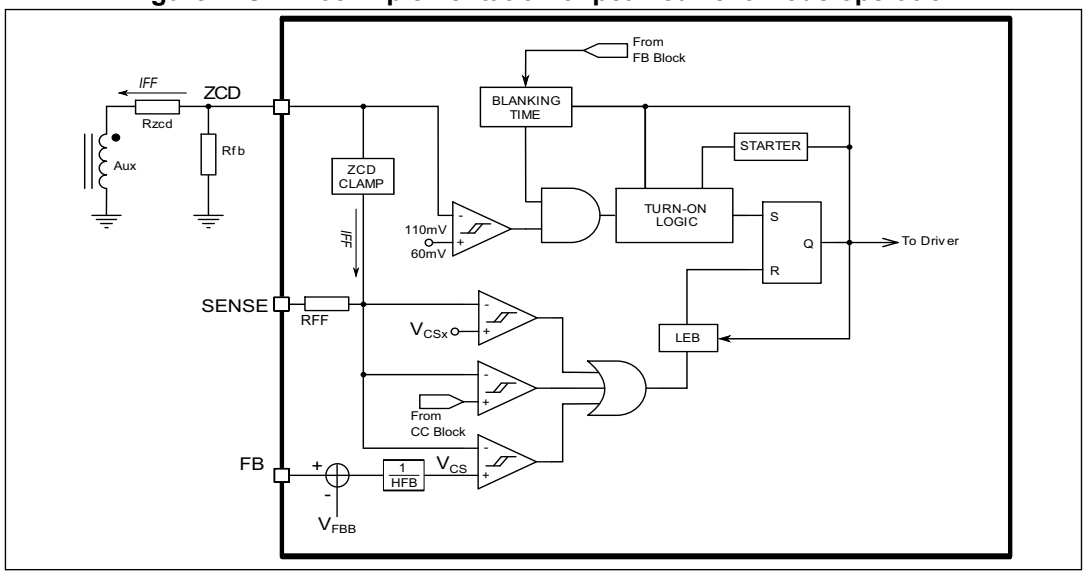
The FB pin is driven directly by the phototransistor's collector to set the threshold of the peak current comparator (VCS). *Equation 1* defines the relation between the FB pin's

voltage and the peak current mode threshold. V_{CS} is compared with the voltage across the sense resistor, controlling the peak drain current cycle-by-cycle.

Equation 1

$$V_{CS} = (V_{FB} - V_{FBB}) / H_{FB}$$

Figure 7. STCH03 implementation of peak current mode operation



6.4 Constant current operation

The voltage of the auxiliary winding is fed into the internal CC block trough the ZCD pin to achieve an output constant current regulation. A proprietary internal block, whose structure and signals are depicted in *Figure 8*, generates a voltage (V_C) that is fed to peak current control block (*Figure 7*).

An OR structure transmits the lower between V_C and V_{CS} to the PWM comparator.

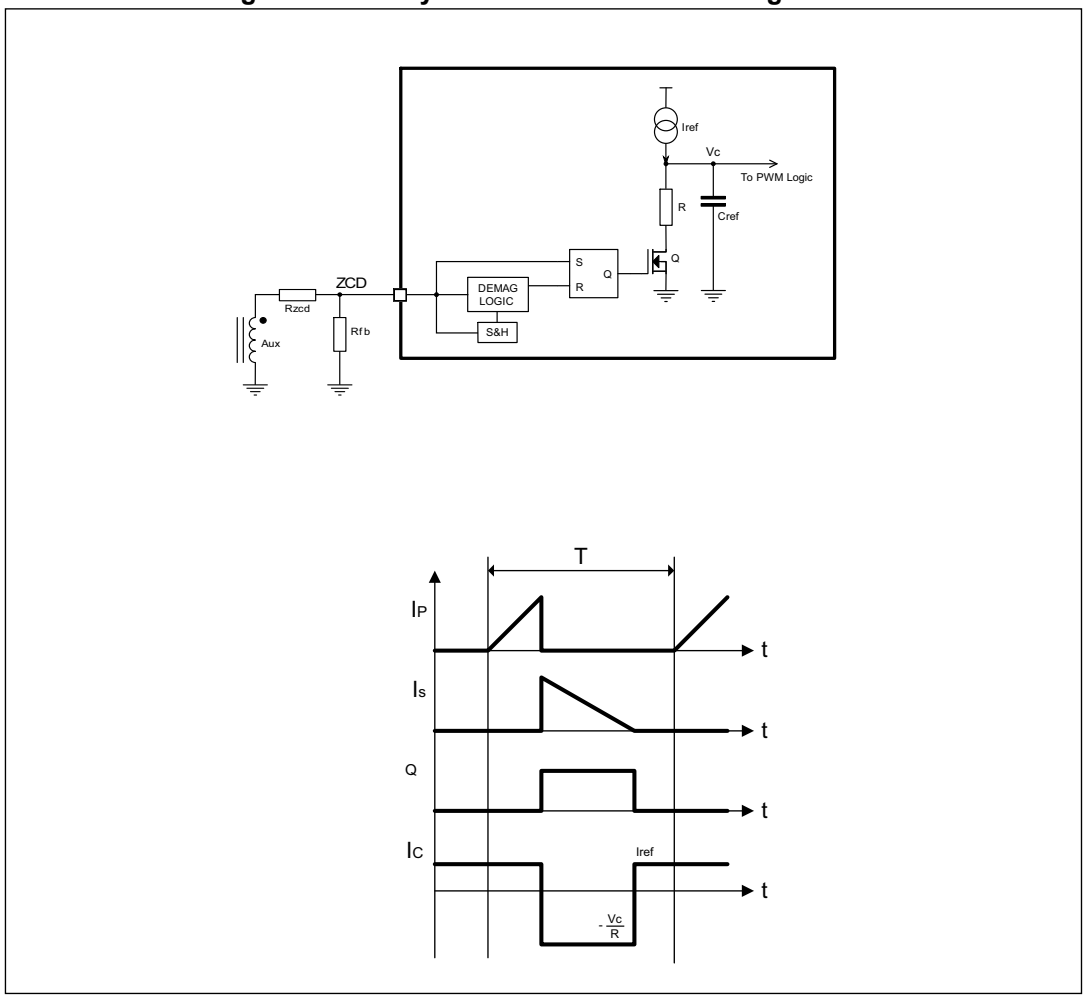
Equation 2 can be used to define the output current in the CC-mode.

Equation 2

$$I_{OUT} = \frac{N_{PRI}}{N_{SEC}} \cdot \frac{K_I}{2 \cdot R_{SENSE}}$$

This formula shows that the average output current does not depend anymore on the input or the output voltage, neither on transformer inductance values. The external parameters defining the output current are the transformer ratio and the sense resistor R_{SENSE}. The current loop gain K_I is internally defined.

Figure 8. Primary Side Constant Current Regulation



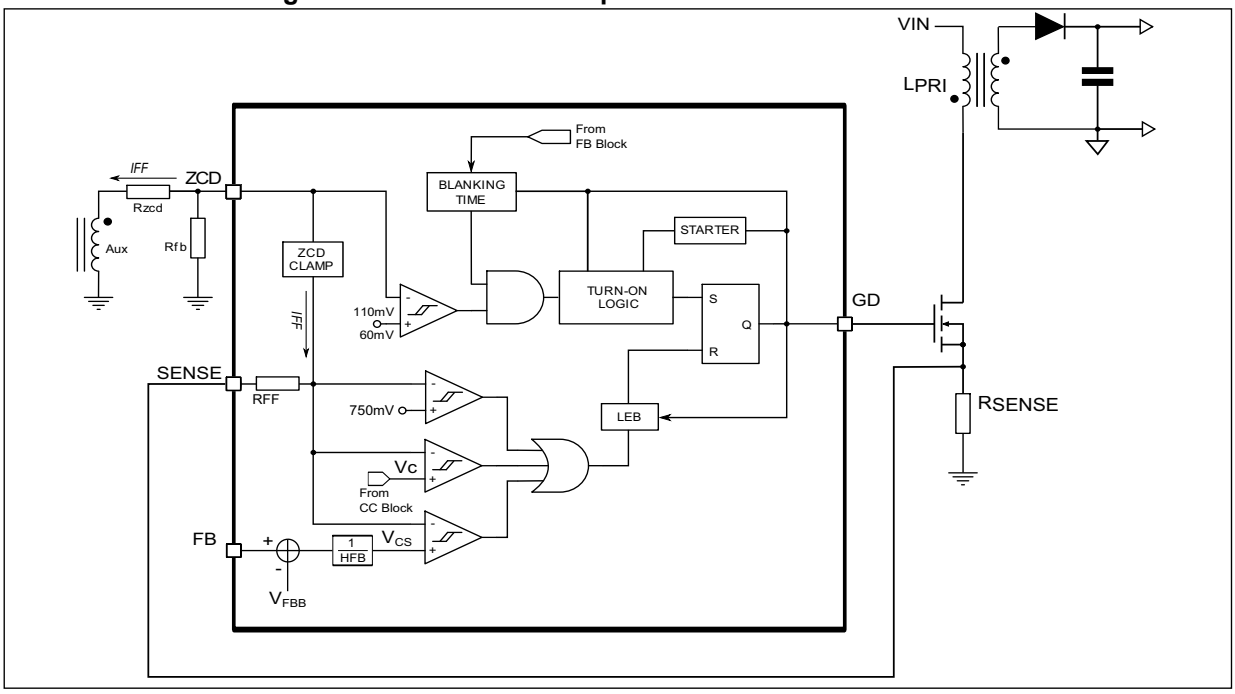
6.5 Voltage feedforward block

The current control structure uses the internal voltage V_C to define the output current, according to *Equation 2*. Actually, the PWM comparator will be affected by an internal propagation delay Td, which will switch off the MOSFET with a peak current higher than the foreseen value.

The STCH03 device implements a line feedforward function, which solves the issue by introducing an input voltage dependent offset on the current sense signal, in order to adjust the cycle-by-cycle current limitation.

The external schematic configuration is shown in *Figure 9*.

Figure 9. Feedforward compensation: internal schematic



The R_{ZCD} resistor can be calculated as follows:

Equation 3

$$R_{ZCD} = \frac{N_{AUX}}{N_{PRI}} \cdot \frac{L_{PRI} \cdot R_{FF}}{T_D \cdot R_{SENSE}}$$

where R_{FF} is an internal parameter, defined in *Table 5: Electrical characteristics on page 7*.

In this case the peak drain current does not depend on input voltage anymore.

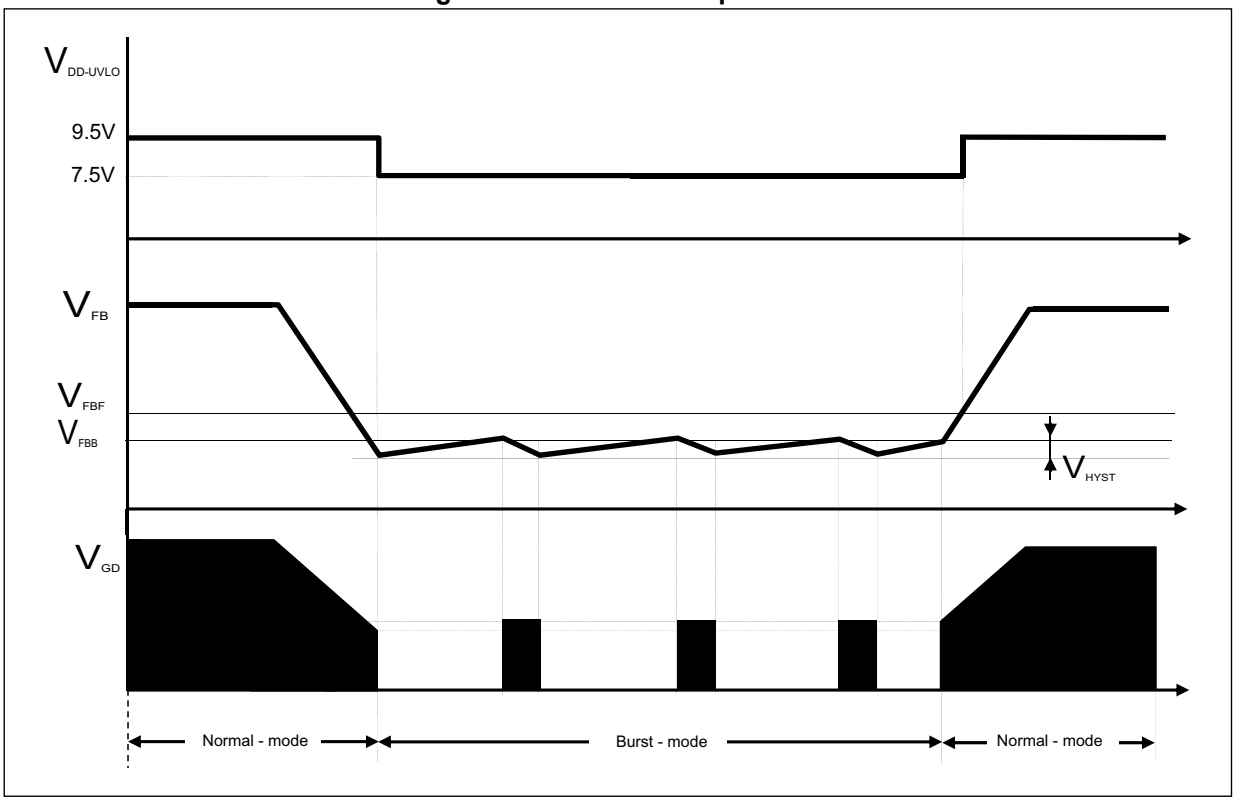
6.6 Burst-mode operation

When the voltage at the FB pin falls to 65 mV below V_{FBB}, the burst-mode operation starts: the MOSFET is turned OFF in order to reduce the consumption. After the MOSFET turns OFF, the FB pin voltage, as a result of the feedback reaction to the energy delivery stop, increase up to V_{FBB} and the device starts switching again.

During these switching cycles the max peak current is fixed by an internal clamp inside the current limit circuit. The effect of the burst-mode operation is to reduce the equivalent switching frequency, which can go down even to few hundred hertz, minimizing all frequency related losses and making it easier to comply with energy saving regulations.

This kind of operation, shown in the timing diagrams of *Figure 10* along with the other ones, is audible noise-free since the peak current is low.

Figure 10. Burst-mode operation



6.7 Adaptive UVLO

A major problem when optimizing a converter for minimum no-load consumption is that the voltage generated by the auxiliary winding under these conditions falls considerably as compared even to a few mA load. This very often causes the supply voltage VDD of the control IC to drop below the UVLO threshold so that the operation becomes intermittent, which is undesired.

Furthermore, this must be traded off against the need of generating a voltage not exceeding the maximum allowed by the control IC at full load but low enough to reduce the bias losses as much as possible.

To help the designer overcome this problem the device, besides reducing its own consumption during the burst-mode operation, also features a proprietary adaptive UVLO function.

It consists of shifting the $V_{DD\text{-}UVLO}$ threshold downwards at the light load, namely when the voltage at the pin FB falls 65 mV below the burst-mode threshold V_{FBB} (0.6 V typ.), to have more headroom.

To prevent any malfunction the normal threshold (9.5 V typ.) is re-established when the voltage at the pin FB exceeds the exit burst-mode threshold V_{FBF}.

The normal UVLO threshold ensures that at full medium-heavy loads the MOSFET will be driven with a proper gate-to-source voltage. The mode of the operation is reported in *Figure 10*.

6.8 Gate-driver

The gate-driver of the power MOSFET is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize the common mode EMI. Under UVLO conditions an internal pull-down circuit holds the gate low in order to ensure that the power MOSFET cannot be turned on accidentally.

6.9 Frequency jittering for EMI reduction

Although the STCH03 works in the QR mode and the switching frequency is already modulated at twice the mains frequency, a dedicated frequency jittering circuitry is embedded inside the IC to further reduce the EMI filtering. A proprietary frequency jitter technique is implemented in the controller, based on the injection of a modulating signal at 9 kHz (above the feedback loop bandwidth) with the 50% duty cycle on the current sense signal: this signal is a square waveform that modulates the amplitude of the peak primary current. The percentage of this amplitude is set at 5% as default. As the peak current reduces with decreasing load levels, the effect of this modulation automatically attenuates at lower loads, where the energy of EMI noise is highly reduced.

6.10 Overvoltage protection

The overvoltage function of the STCH03 device monitors the voltage on the ZCD pin during MOSFET's OFF-time, where the voltage generated by the auxiliary winding tracks the converter output voltage. A proprietary structure is able to acquire the ZCD voltage in correspondence of the demagnetization instant to maximize the accuracy of the output voltage detection. In fact, at this occurrence, no current is flowing in secondary side rectifier and the secondary side winding voltage equals output voltage. If the detected voltage exceeds an internal 2.5 V reference, a comparator is triggered, an overvoltage condition is assumed and the device is shut down.

Once R_{ZCD} is fixed by feedforward considerations (see *Section 6.5: Voltage feedforward block*), it is possible to calculate the value of the R_{OVP} resistor to activate the OVP protection for a certain output voltage level, $V_{OUT\text{-}OVP}$:

Equation 4

$$R_{OVP} = \frac{V_{OVP}}{\frac{N_{AUX}}{N_{SEC}} \cdot V_{OUT-OVP} - V_{OVP}} \cdot R_{ZCD}$$

where V_{OVP} is the internal OVP threshold, N_{SEC} and N_{AUX} are the secondary and auxiliary turns number respectively.

To reduce sensitivity to noise and prevent the protection from being erroneously activated, the OVP comparator must be triggered for four consecutive oscillator cycles before the STCH03 is stopped. A counter, which is reset every time the OVP comparator is not triggered in one oscillator cycle, is provided to this purpose.

STCH03 is available in two versions: STCH03 is equipped with Auto restart mode, while STCH03L is equipped with latched mode.

In the auto-restart mode, once the protection is tripped, the switching activity is stopped and the condition is maintained until V_{DD} goes below to V_{DDR} restart voltage and then rises-up

again to V_{DD-ON}. Ultimately, this will result in a low-frequency intermittent operation (hiccup-mode operation), see *Figure 11*.

In the latched mode the protection is maintained until the input main is removed. During this time the HV generator is activated periodically to recycle the supply voltage between V_{DD-ON} and V_{DD-OFF}. And the condition is indefinitely maintained until the AC main is removed and the V_{DD} voltage falls below V_{DDR} which resets the latch.

The latched OVP protection operation is shown in the time diagram of *Figure 12*.

Figure 13 illustrates the timing of the function.

Figure 11. OVP timing diagram with auto-restart option

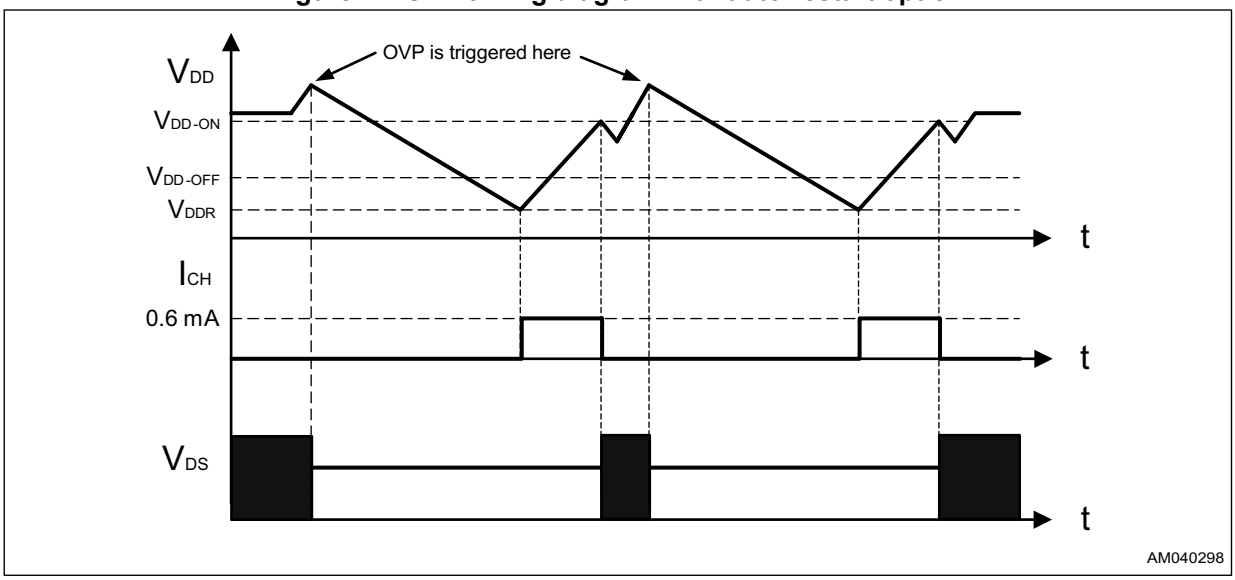


Figure 12. OVP timing diagram with latched option

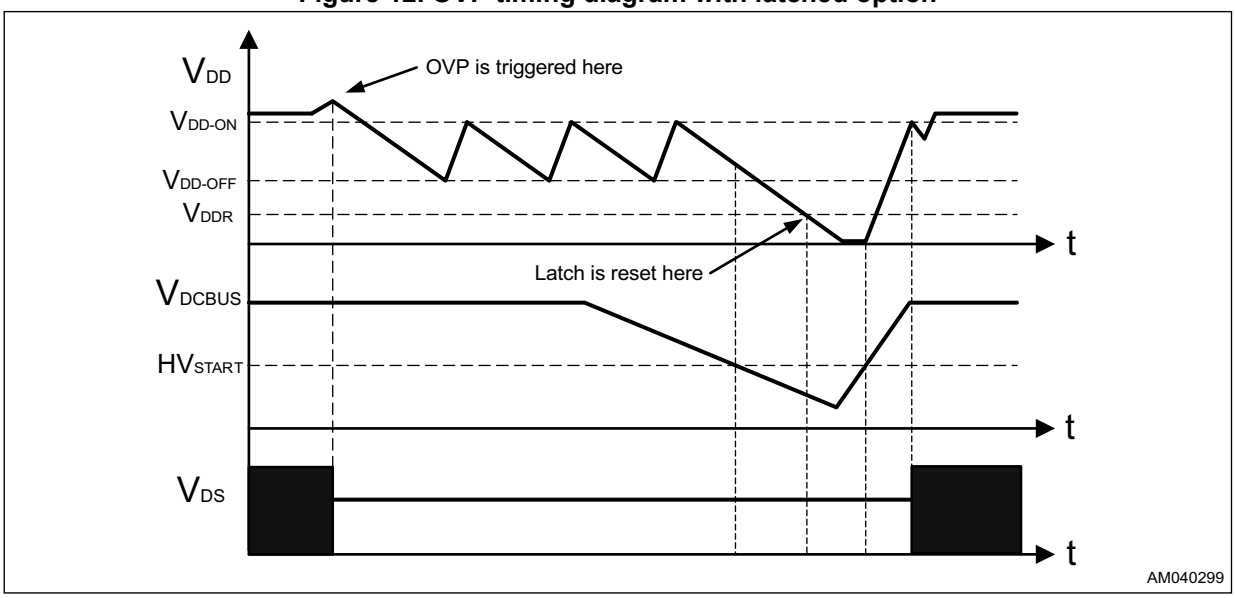
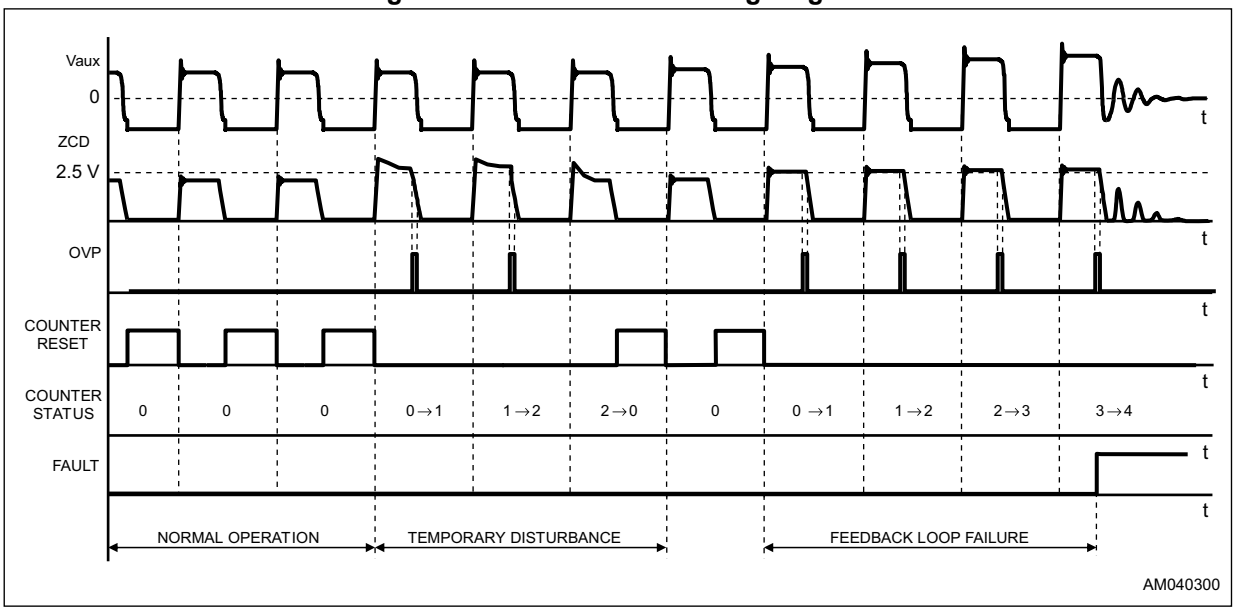


Figure 13. OVP function: timing diagram



6.11 Output undervoltage protection

The output undervoltage function (UVP) of the STCH03 device protects the converter in case of the output short-circuit or for the CC-mode operation at low output voltage, forcing the system in the hiccup-mode.

The voltage on the ZCD at the end of the transformer's demagnetization is monitored and compared with an internal threshold, V_{UVP} (0.55 V typ.). If the value goes down to the threshold, an output undervoltage condition is assumed and the device enters in hiccup-mode protection.

Similar to OVP, also the UVP protection must be triggered for four consecutive oscillator cycles before the STCH03 is stopped, in order to provide better noise immunity against false protection triggering.

A 20 ms (typ. value) UVP blanking time is provided to delay the protection during converter power-on and at any restart after protection, to avoid erroneous UVP triggering during the output voltage rise time.

Note that, without external structures, OVP and UVP are tracked together.

Once the OVP is fixed using *Equation 4*, the output voltage level to activate the UVP ($V_{OUT-UVP}$) is:

Equation 5

$$V_{OUT-UVP} = \frac{N_{SEC}}{N_{AUX}} \cdot \left(\frac{R_{OVP} + R_{ZCD}}{R_{OVP}}\right) \cdot V_{UVP}$$

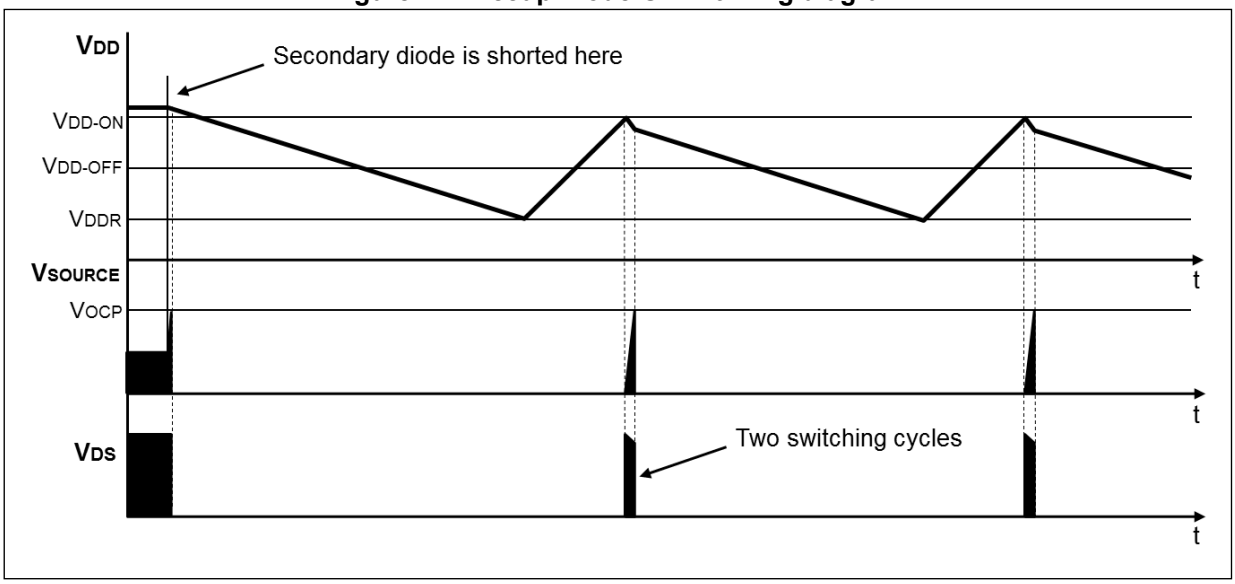
6.12 Overcurrent protection (OCP)

The device is also protected against the short-circuit of the secondary rectifier, the short-circuit on the secondary winding or a hard-saturated flyback transformer. A comparator monitors continuously the voltage on the R_{SENSE} and activates protection circuitry if this voltage exceeds the V_{OCP} value (1 V typ. value).

To distinguish an actual malfunction from a disturbance (e.g. induced during ESD tests), the first time the comparator is tripped the protection circuit enters a “warning state”. If in the subsequent switching cycle the comparator is not tripped, a temporary disturbance is assumed and the protection logic will be reset in its idle state; if the comparator trips again a real malfunction is assumed and the device will be stopped.

Once the protection is tripped, the condition is maintained until V_{DD} goes below V_{DDR} restart voltage. The internal start-up generator is still turned on and the V_{DD} capacitor is charged again to restart the device. Ultimately, this will result in a low-frequency intermittent operation (hiccup-mode operation), with very low stress on the power circuit. This special condition is illustrated in the timing diagram of *Figure 14*.

Figure 14. Hiccup-mode OCP: timing diagram



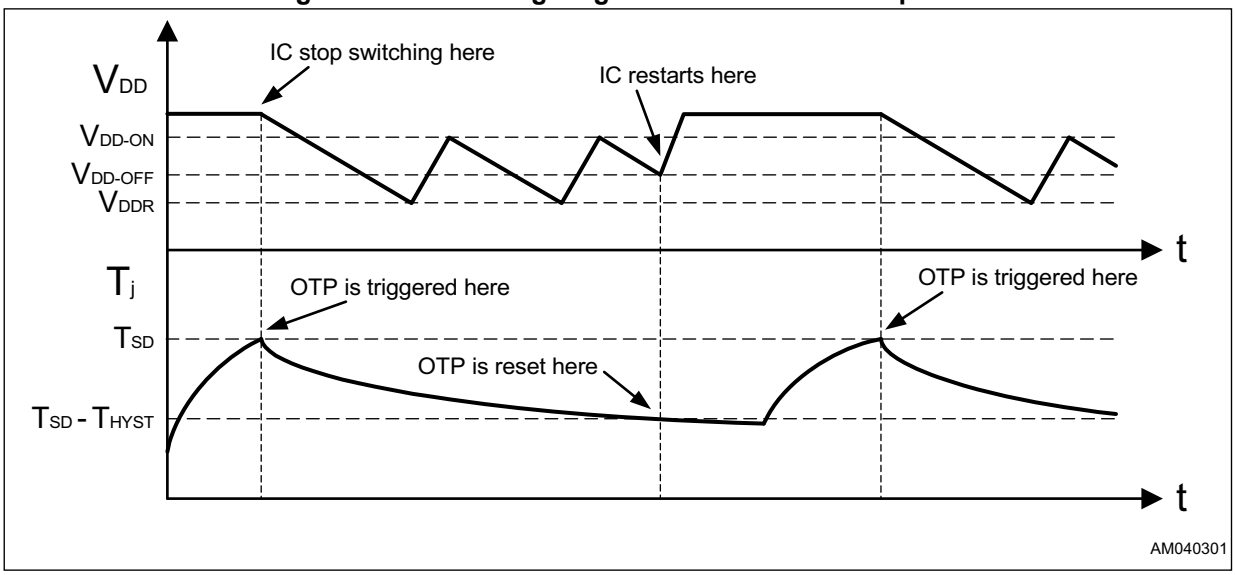
6.13 Thermal shutdown protection

When the IC temperature exceeds the shutdown threshold, T_{SD} (150 °C typ.) the device is shut down to prevent any dangerous overheating for the system and the V_{DD} pin will be continuously recycled between V_{DD-ON} and V_{DDR} to keep the controller alive.

Once the temperature falls T_{HYST} below restart time the IC will start again, unless the voltage on the V_{DD} pin is below V_{DD-OFF}. In this case the pin is discharged down to V_{DDR} and recycled to V_{DD-ON} before to start again.

This operation is shown in *Figure 15*.

Figure 15. OTP timing diagram with auto-restart option



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 SO8 package information

Figure 16. SO8 package outline

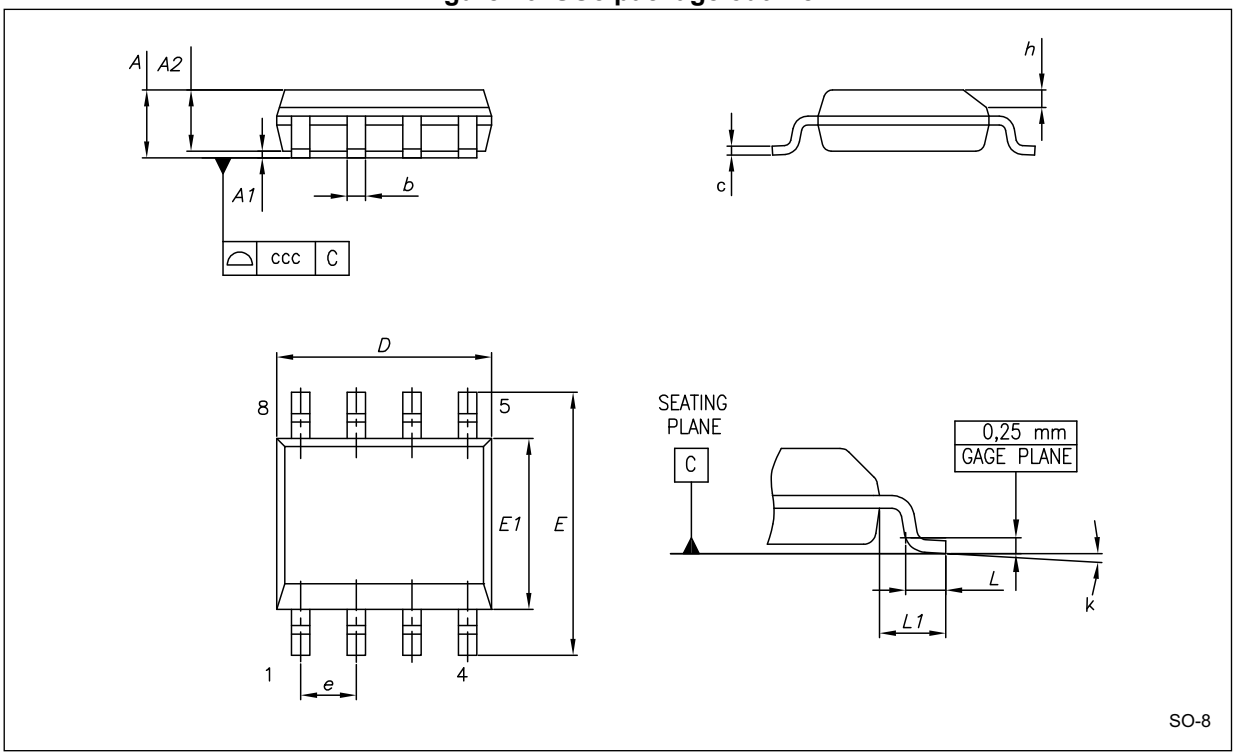


Table 6. SO8 package mechanical data

Symbol	Dimensions (mm)			Note
	Min.	Typ.	Max.	
A	-	-	1.75	-
A1	0.10	-	0.25	-
A2	1.25	-	-	-
b	0.28	-	0.48	-
c	0.17	-	0.23	-
D	4.80	4.90	5.00	(1)
E	5.80	6.00	6.20	-
E1	3.80	3.90	4.00	(2)
e	-	1.27	-	-
h	0.25	-	0.50	-
L	0.40	-	1.27	-
L1	-	1.04	-	-
k	0	-	8	(3)
ccc	-	-	0.10	-

1. The dimension “D” does not include the mold flash, protrusions or gate burrs. The mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both sides).
2. The dimension “E1” does not include the interlead flash or protrusions. The interlead flash or protrusions shall not exceed 0.25 mm per side.
3. Degrees.

8 Revision history

Table 7. Document revision history

Date	Revision	Changes
02-May-2018	1	Initial release.
20-Nov-2019	2	Change to Description and Applications. Contents structure amended. Updated *Figure 1*, Table 4, *Table 5*, *Figure 6*, *Figure 7*, *Figure 8*, *Section 6*. Changes to text throughout the document. *Figure 7* replaced.

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