

CSD18537NQ5A 60-V N-Channel NexFET™ Power MOSFETs

1 Features

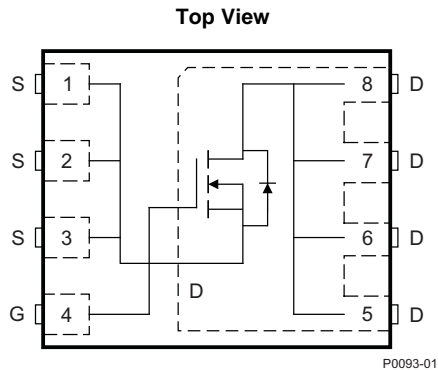
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5 mm x 6 mm Plastic Package

2 Applications

- High-Side Synchronous Buck Converter
- Motor Control

3 Description

This 10 mΩ, 60 V, SON 5 mm x 6 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

| $T_A = 25^\circ\text{C}$ | | TYPICAL VALUE | | UNIT |
|--------------------------|-------------------------------|------------------------|----|------|
| V_{DS} | Drain-to-Source Voltage | 60 | | V |
| Q_g | Gate Charge Total (10 V) | 14 | | nC |
| Q_{gd} | Gate Charge Gate-to-Drain | 2.3 | | nC |
| $R_{DS(on)}$ | Drain-to-Source On Resistance | $V_{GS} = 6\text{ V}$ | 13 | mΩ |
| | | $V_{GS} = 10\text{ V}$ | 10 | mΩ |
| $V_{GS(th)}$ | Threshold Voltage | 3 | | V |

Ordering Information⁽¹⁾

| Device | Qty | Media | Package | Ship |
|---------------|------|--------------|------------------------------|---------------|
| CSD18537NQ5A | 2500 | 13-Inch Reel | SON 5 x 6 mm Plastic Package | Tape and Reel |
| CSD18537NQ5AT | 250 | 7-Inch Reel | | |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

| $T_A = 25^\circ\text{C}$ | | VALUE | UNIT |
|--------------------------|--|------------|------------------|
| V_{DS} | Drain-to-Source Voltage | 60 | V |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| I_D | Continuous Drain Current (Package limited) | 50 | A |
| | Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$ | 54 | |
| | Continuous Drain Current ⁽¹⁾ | 11 | |
| I_{DM} | Pulsed Drain Current ⁽²⁾ | 151 | A |
| P_D | Power Dissipation ⁽¹⁾ | 3.2 | W |
| | Power Dissipation, $T_C = 25^\circ\text{C}$ | 75 | |
| T_J, T_{stg} | Operating Junction and Storage Temperature Range | -55 to 150 | $^\circ\text{C}$ |
| E_{AS} | Avalanche Energy, single pulse $I_D = 33\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$ | 55 | mJ |

(1) Typical $R_{\theta JA} = 40^\circ\text{C/W}$ on a 1-inch², 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

(2) Max $R_{\theta JC} = 2.1^\circ\text{C/W}$, pulse duration $\leq 100\ \mu\text{s}$, duty cycle $\leq 1\%$

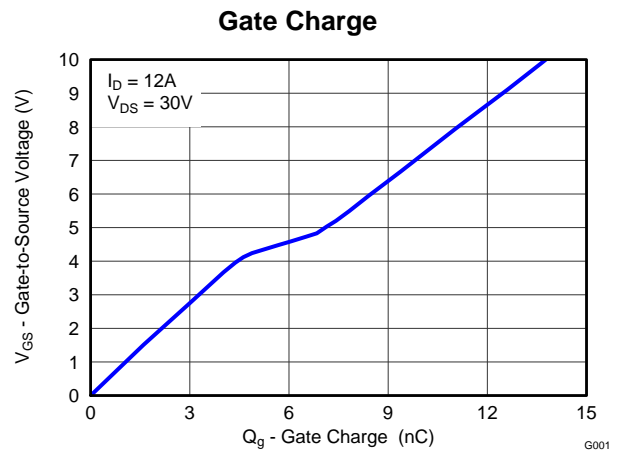
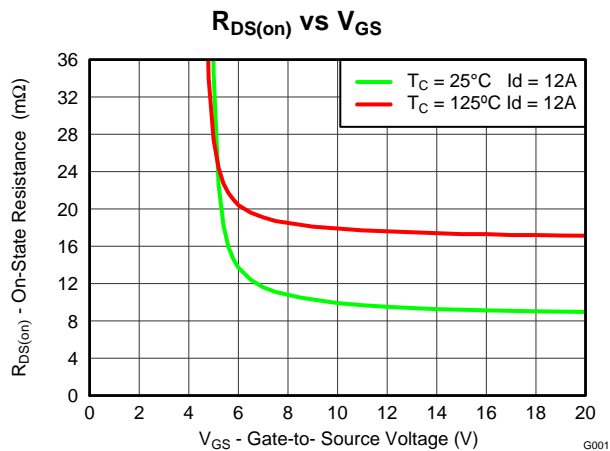


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (February 2014) to Revision B | Page |
|--|-------------|
| • Reduced silicon current limit to 54 A due to increase in $R_{\theta JC}$ | 1 |
| • Increased pulsed current limit to 151 | 1 |
| • Added line for maximum power dissipation with case temperature held to 25°C | 1 |
| • Updated the pulsed current conditions | 1 |
| • Increased the maximum $R_{\theta JC}$ to 2.1 °C/W | 3 |
| • Updated Figure 1 from a normalized $R_{\theta JA}$ curve to an $R_{\theta JC}$ curve | 4 |
| • Updated Figure 10 to show an improved SOA | 5 |
| • Updated Figure 12 to show a 50-A package current limit | 5 |

| Changes from Original (June 2013) to Revision A | Page |
|--|-------------|
| • Added part number to title | 1 |
| • Added more information to description | 1 |
| • Updated ordering information to include small reel information | 1 |
| • Removed $T_C = 25^\circ\text{C}$ condition from package limited continuous drain current | 1 |

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|----------------------------------|--|-----|------|------|------|
| STATIC CHARACTERISTICS | | | | | | |
| B _V DSS | Drain-to-Source Voltage | V _{GS} = 0 V, I _D = 250 μA | 60 | | | V |
| I _{DSS} | Drain-to-Source Leakage Current | V _{GS} = 0 V, V _{DS} = 48 V | | | 1 | μA |
| I _{GSS} | Gate-to-Source Leakage Current | V _{DS} = 0 V, V _{GS} = 20 V | | | 100 | nA |
| V _{GS(th)} | Gate-to-Source Threshold Voltage | V _{DS} = V _{GS} , I _D = 250 μA | 2.6 | 3 | 3.5 | V |
| R _{DS(on)} | Drain-to-Source On Resistance | V _{GS} = 6 V, I _D = 12 A | | 13 | 17 | mΩ |
| | | V _{GS} = 10 V, I _D = 12 A | | 10 | 13 | mΩ |
| g _{fs} | Transconductance | V _{DS} = 30 V, I _D = 12 A | | 62 | | S |
| DYNAMIC CHARACTERISTICS | | | | | | |
| C _{iss} | Input Capacitance | V _{GS} = 0 V, V _{DS} = 30 V, f = 1 MHz | | 1140 | 1480 | pF |
| C _{oss} | Output Capacitance | | | 136 | 177 | pF |
| C _{rss} | Reverse Transfer Capacitance | | | 4 | 5.2 | pF |
| R _G | Series Gate Resistance | | | 5.5 | 11 | Ω |
| Q _g | Gate Charge Total (10 V) | V _{DS} = 30 V, I _D = 12 A | | 14 | 18 | nC |
| Q _{gd} | Gate Charge Gate-to-Drain | | | 2.3 | | nC |
| Q _{gs} | Gate Charge Gate-to-Source | | | 4.7 | | nC |
| Q _{g(th)} | Gate Charge at V _{th} | | | 3.3 | | nC |
| Q _{oss} | Output Charge | V _{DS} = 30 V, V _{GS} = 0 V | | 25 | | nC |
| t _{d(on)} | Turn On Delay Time | V _{DS} = 30 V, V _{GS} = 10 V, I _{DS} = 12 A, R _G = 0 Ω | | 5.8 | | ns |
| t _r | Rise Time | | | 4 | | ns |
| t _{d(off)} | Turn Off Delay Time | | | 14.4 | | ns |
| t _f | Fall Time | | | 3.2 | | ns |
| DIODE CHARACTERISTICS | | | | | | |
| V _{SD} | Diode Forward Voltage | I _{SD} = 12 A, V _{GS} = 0 V | | 0.8 | 1 | V |
| Q _{rr} | Reverse Recovery Charge | V _{DS} = 30 V, I _F = 12 A, di/dt = 300 A/μs | | 54 | | nC |
| t _{rr} | Reverse Recovery Time | | | 40 | | ns |

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|------------------|--|-----|-----|-----|------|
| R _{θJC} | Junction-to-Case Thermal Resistance ⁽¹⁾ | | | 2.1 | °C/W |
| R _{θJA} | Junction-to-Ambient Thermal Resistance ⁽¹⁾⁽²⁾ | | | 50 | |

- (1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches × 1.5-inches (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.

CSD18537NQ5A

SLPS391B – JUNE 2013 – REVISED JULY 2014

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M0137-01

Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.



M0137-02

Max $R_{\theta JA} = 125^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

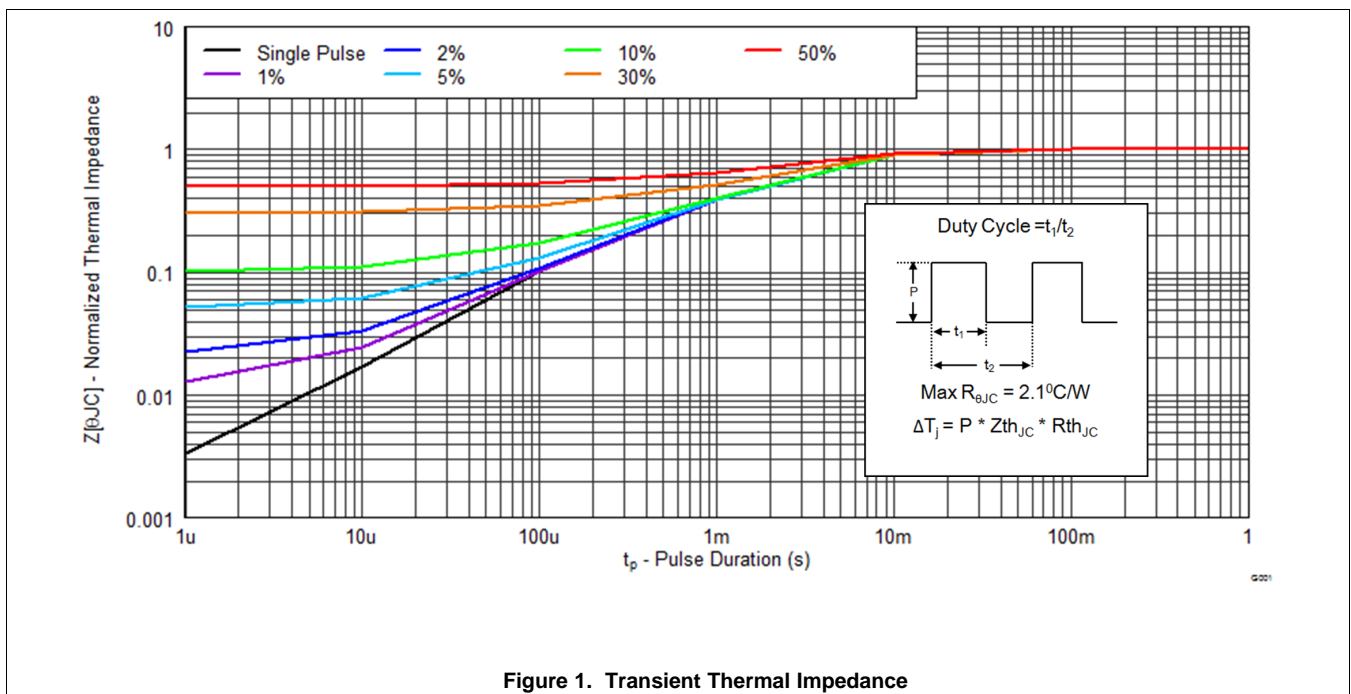


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

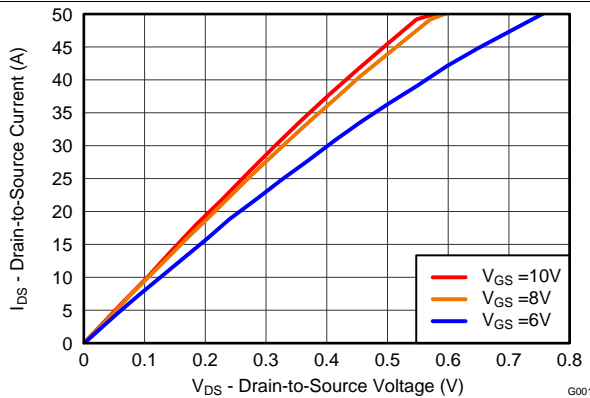


Figure 2. Saturation Characteristics

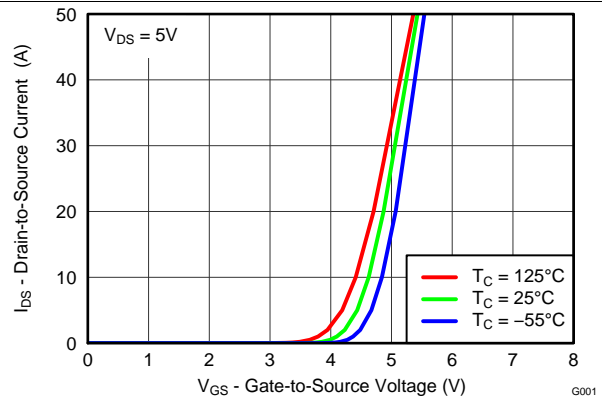


Figure 3. Transfer Characteristics

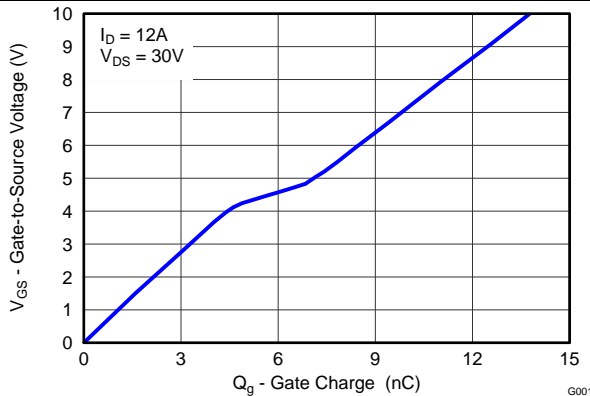


Figure 4. Gate Charge

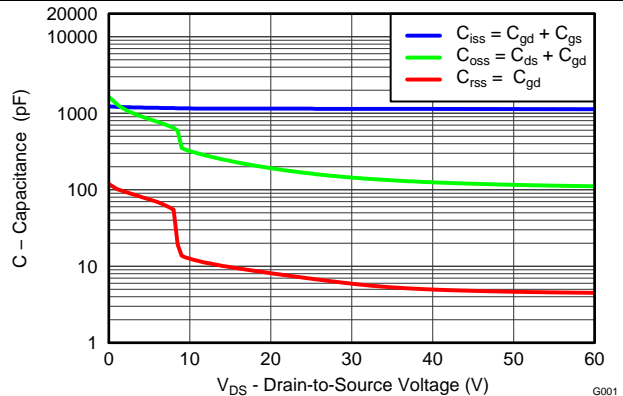


Figure 5. Capacitance

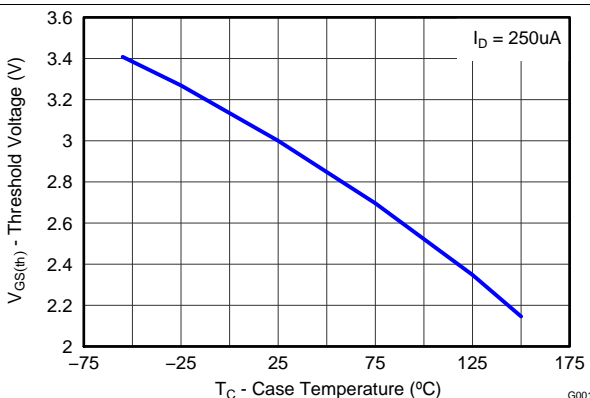


Figure 6. Threshold Voltage vs Temperature

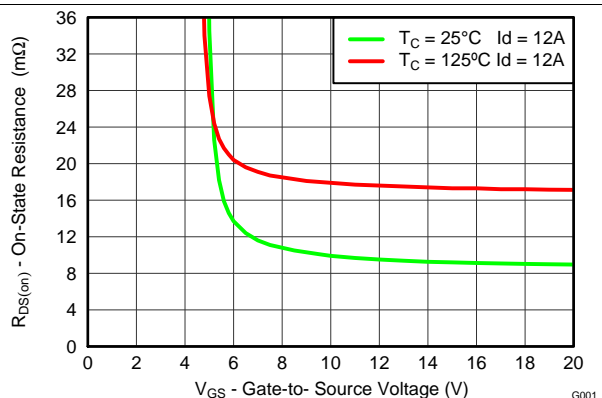


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

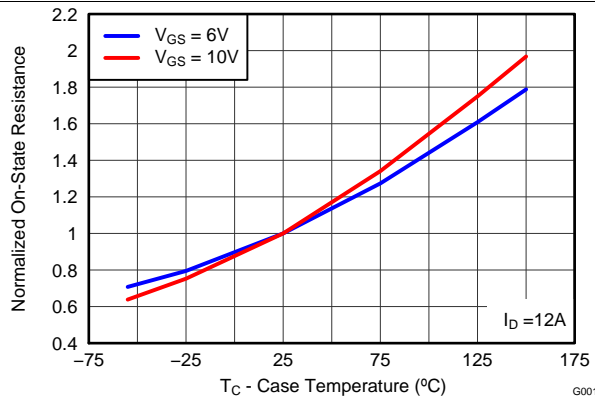


Figure 8. Normalized On-State Resistance vs Temperature

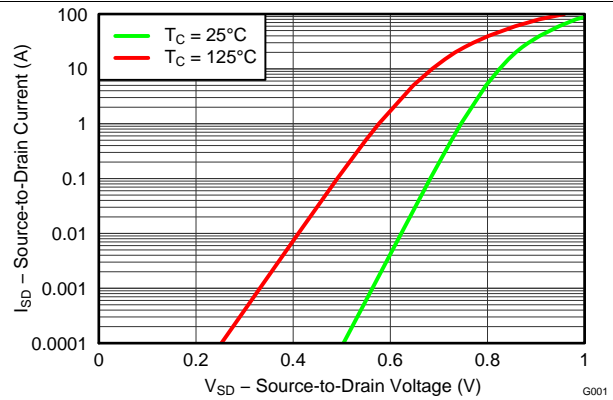


Figure 9. Typical Diode Forward Voltage

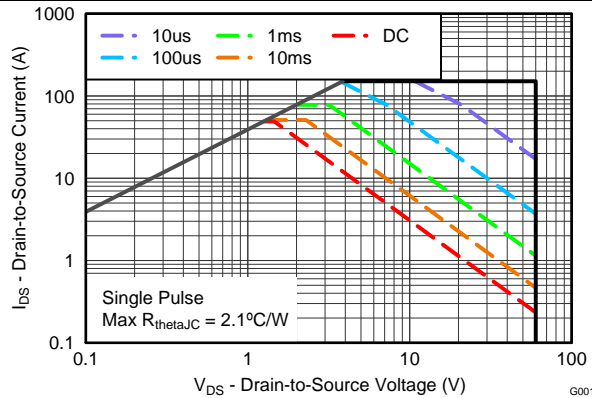


Figure 10. Maximum Safe Operating Area

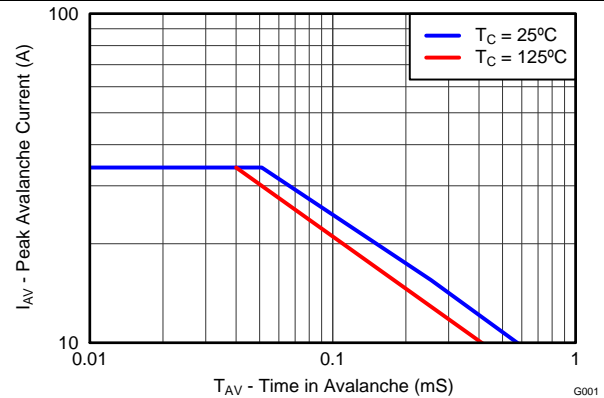


Figure 11. Single Pulse Unclamped Inductive Switching

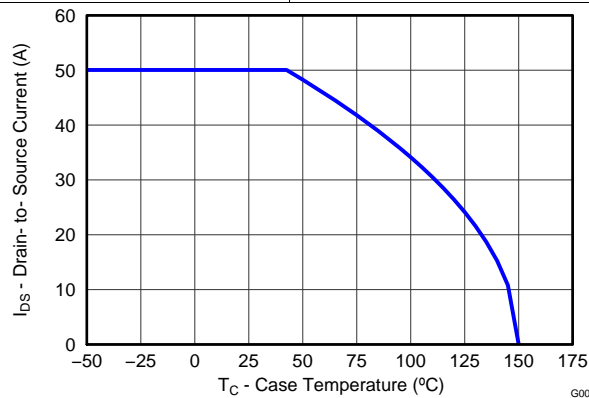


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

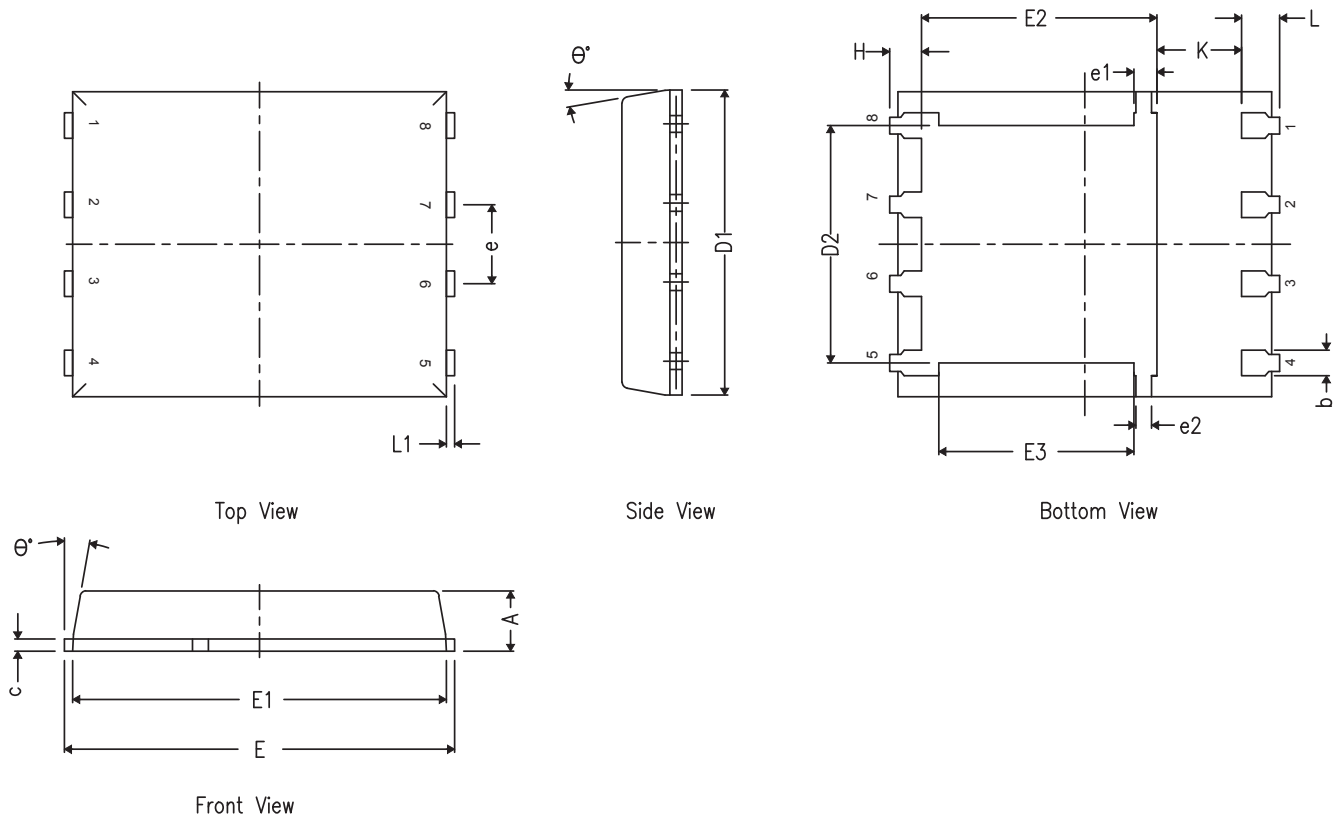
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q5A Package Dimensions



| DIM | MILLIMETERS | | |
|----------|-------------|------|------|
| | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| b | 0.33 | 0.41 | 0.51 |
| c | 0.20 | 0.25 | 0.34 |
| D1 | 4.80 | 4.90 | 5.00 |
| D2 | 3.61 | 3.81 | 4.02 |
| E | 5.90 | 6.00 | 6.10 |
| E1 | 5.70 | 5.75 | 5.80 |
| E2 | 3.38 | 3.58 | 3.78 |
| E3 | 3.03 | 3.13 | 3.23 |
| e | 1.17 | 1.27 | 1.37 |
| e1 | 0.27 | 0.37 | 0.47 |
| e2 | 0.15 | 0.25 | 0.35 |
| H | 0.41 | 0.56 | 0.71 |
| K | 1.10 | — | — |
| L | 0.51 | 0.61 | 0.71 |
| L1 | 0.06 | 0.13 | 0.20 |
| θ | 0° | — | 12° |

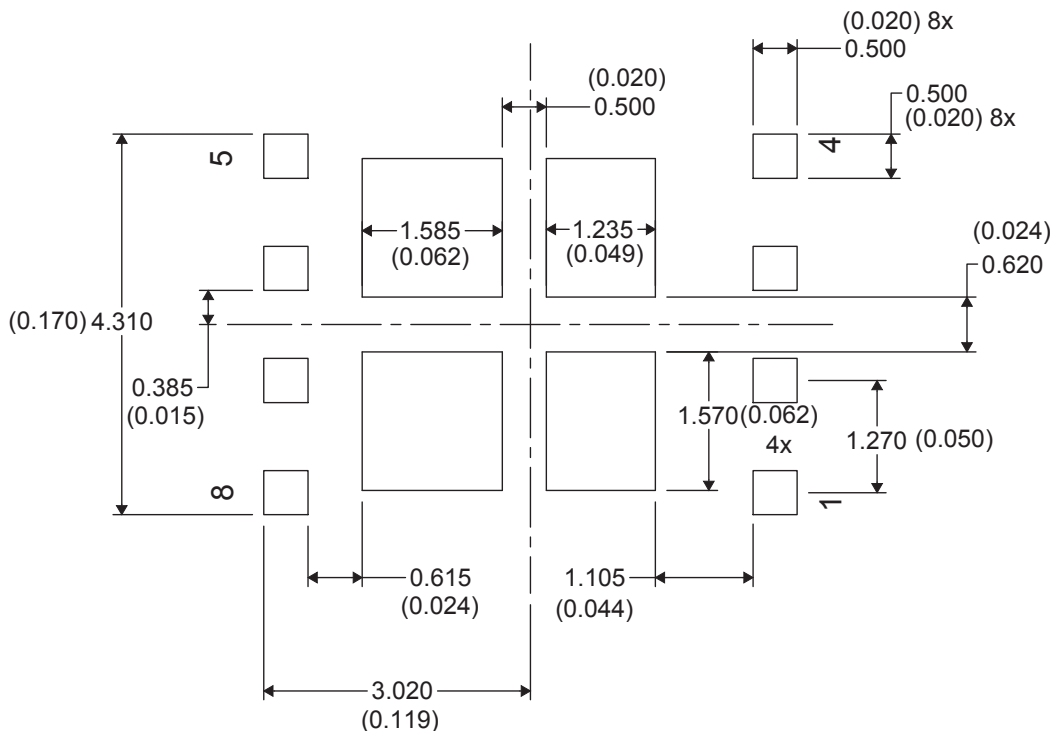
7.2 Recommended PCB Pattern



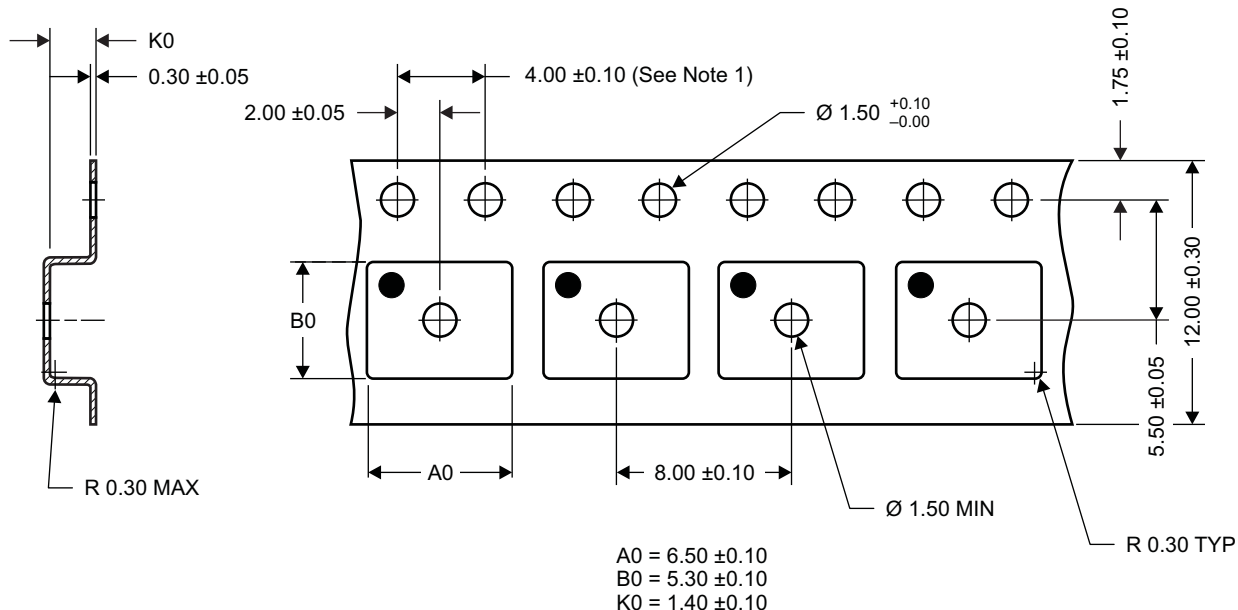
| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|--------|-------|
| | MIN | MAX | MIN | MAX |
| F1 | 6.205 | 6.305 | 0.244 | 0.248 |
| F2 | 4.46 | 4.56 | 0.176 | 0.18 |
| F3 | 4.46 | 4.56 | 0.176 | 0.18 |
| F4 | 0.65 | 0.7 | 0.026 | 0.028 |
| F5 | 0.62 | 0.67 | 0.024 | 0.026 |
| F6 | 0.63 | 0.68 | 0.025 | 0.027 |
| F7 | 0.7 | 0.8 | 0.028 | 0.031 |
| F8 | 0.65 | 0.7 | 0.026 | 0.028 |
| F9 | 0.62 | 0.67 | 0.024 | 0.026 |
| F10 | 4.9 | 5 | 0.193 | 0.197 |
| F11 | 4.46 | 4.56 | 0.176 | 0.18 |

For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening



7.4 Q5A Tape and Reel Information



M0138-01

Notes:

1. 10-sprocket hole-pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CSD18537NQ5A | ACTIVE | VSONP | DQJ | 8 | 2500 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -55 to 150 | 18537N | Samples |
| CSD18537NQ5AT | ACTIVE | VSONP | DQJ | 8 | 250 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -55 to 150 | 18537N | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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