

Using the Stacking TPS546C20A Two Phase Evaluation Module

The TPS546C20AEVM2-746 evaluation module (EVM) is a two phase buck converter with two TPS546C20A devices. The TPS546C20A device is a stackable synchronous buck with PMBus interface that can operate from a nominal 4.5-V to 18-V supply. The device allows programming and monitoring via the PMBus interface.

Two TPS546C20A devices are configured as two phase buck converter in factory default, output current is evenly distributed in the two devices; both the negative and positive output terminals are connected together.

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1 Description

The TPS546C20AEVM2-746 is a two phase buck converter with two stacked TPS546C20A devices. It uses a nominal 12-V bus to produce a regulated 0.9-V output at up to 70 A of load current. The TPS546C20AEVM2-746 is designed to demonstrate stacking operation of the TPS546C20A in a two phase low output voltage application while providing a number of test points to evaluate the performance of the devices. The TPS546C20AEVM2-746 can be modified to two separated single phase buck converters by changing the components assembled. Refer to the TPS546C20A ([SLUSCK1](#)) datasheet for more information on single-phase configuration.

1.1 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TPS546C20AEVM2-746. Observe all safety precautions.



Warning

The TPS546C20AEVM2-746 circuit module may become hot during operation due to dissipation of heat. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.



Caution

Do not leave the EVM powered when unattended.

WARNING

The circuit module has signal traces, components, and component leads on the bottom of the board. This may result in exposed voltages, hot surfaces or sharp edges. Do not reach under the board during operation.

CAUTION

The circuit module may be damaged by over temperature. To avoid damage, monitor the temperature during evaluation and provide cooling, as needed, for your system environment.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than 1 power supply, check your equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to your equipment.

CAUTION

The communication interface is not isolated on the EVM. Be sure no ground potential exists between the computer and the EVM. Also be aware that the computer is referenced to the Battery- potential of the EVM.

1.2 Typical Applications

- High-density power solutions
- Wireless infrastructure
- Switcher
- Router Network
- Server
- Storage
- Smart power systems

1.3 Features

- Regulated 0.9-V output up to 70-A DC steady-state output current
- The output voltage is marginable and trimmable via the PMBus interface
 - Programmable UVLO, soft-start, and enable via the PMBus interface
 - Programmable overcurrent warning and fault limits and programmable response to faults via the PMBus interface
 - Programmable overvoltage and undervoltage warning and fault limits and programmable response to faults via the PMBus interface
 - Programmable turn-on and turn-off delays
- Convenient test points for probing critical waveforms

2 Electrical Performance Specifications

Table 1 lists the electrical performance specifications under room temperature 25°C.

Table 1. TPS546C20AEVM2-746 Electrical Performance Specifications

| Parameter | Test Conditions | MIN | TYP | MAX | Unit |
|--|--|-----|-----|-----|---------|
| Input Characteristics | | | | | |
| Voltage range | V_{IN} | 5 | 12 | 18 | V |
| Maximum input current | $V_{IN} = 12\text{ V}$, $I_O = 70\text{ A}$ | | 6.5 | | A |
| No load input current | $V_{IN} = 12\text{ V}$, $I_O = 0\text{ A}$ | | 120 | | mA |
| Output Characteristics | | | | | |
| Output voltage, V_{OUT} | | | 0.9 | | V |
| Output load current, $I_{OUT}^{(1)}$ | | 0 | | 70 | A |
| Output voltage regulation | Line Regulation: Input voltage = 5 V to 18 V | | 1% | | |
| | Load Regulation: Output current = 0 A to 70 A | | 1% | | |
| Output voltage ripple, V_{OUT} | $V_{IN} = 12\text{ V}$, $I_{OUT} = 70\text{ A}$ | | 10 | | mVpp |
| Output Over-current Protection Threshold | Load current I_{OUT1} , default setting of U1 | | 42 | | A |
| | Load current I_{OUT2} , default setting of U2 | | 42 | | A |
| Systems Characteristics | | | | | |
| Switching frequency | $V_{IN} = 12\text{ V}$ | | 500 | | kHz |
| Full load efficiency, $V_{OUT}^{(2)}$ | $V_{IN} = 12\text{ V}$, $I_{OUT} = 70\text{ A}$, | | 83% | | |
| Operating temperature | $T_{ambient}$ | | 25 | | °C |
| PMBUS Interface and Pin-Strapping | | | | | |
| U1 PMBUS Address | Fixed | | 36 | | Decimal |
| U2 PMBus Address | Fixed | | 37 | | |
| U1 Voltage reference | Programmed by VSEL resistor R_{35} | | 900 | | mV |
| U2 Voltage reference | Programmed by VSEL resistor R_{36} | | 950 | | |
| U1 Soft-start time (TON_RISE) | Programmed by SS resistor R_{33} | | 5 | | ms |
| U2 Soft-start time (TON_RISE) | Programmed by SS resistor R_{37} | | 7 | | |

⁽¹⁾ The output current I_{OUT} can be up to 80 A, if the output overcurrent limit (IOUT_OC_FAULT_LIMIT) is set to 45 A.

⁽²⁾ The efficiency is measured based on Figure 2 and test setups, which includes power loss caused by on board copper traces.

3 Schematic

Figure 1 illustrates the TPS546C20AEVM2-746 EVM schematic.

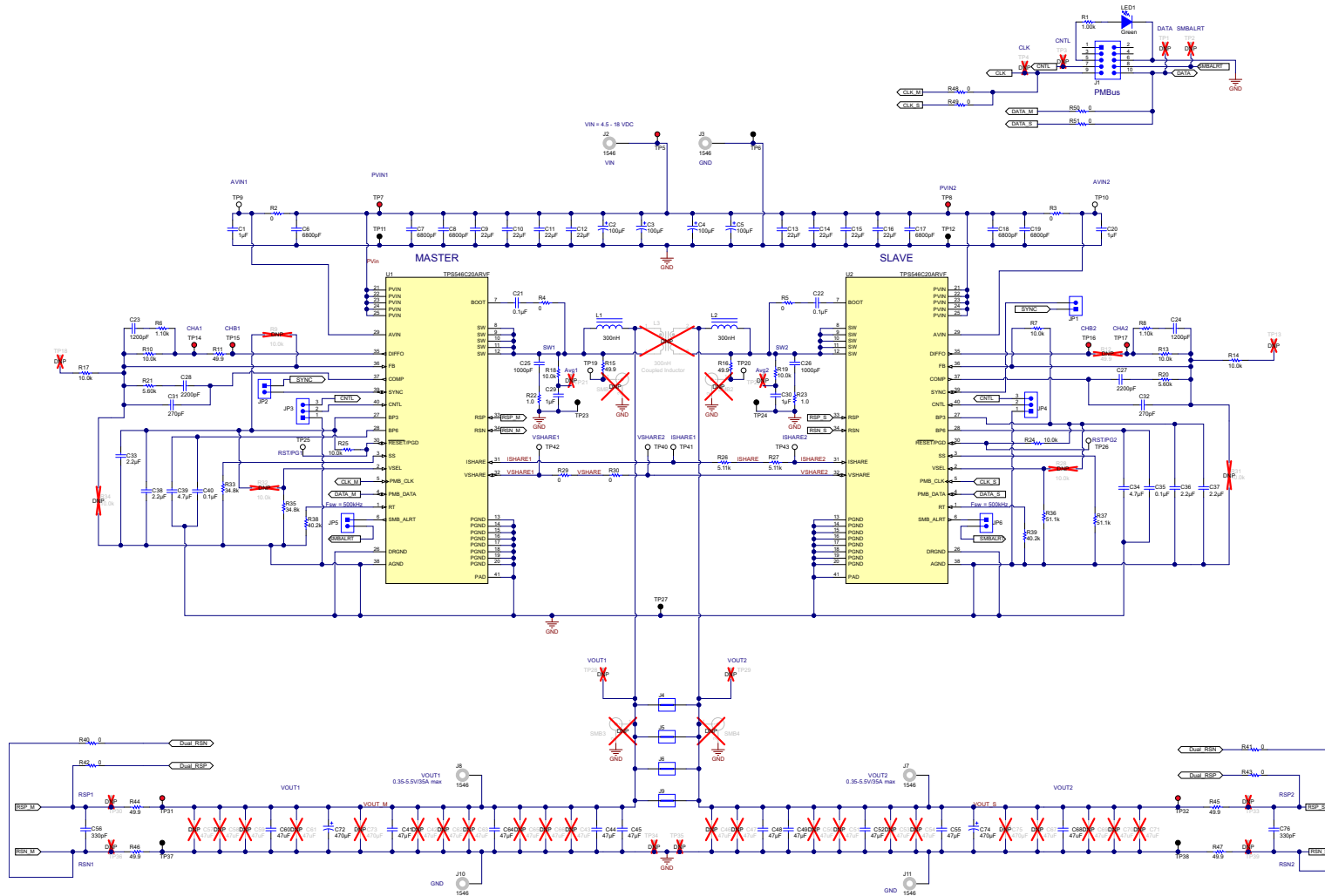


Figure 1. TPS546C20AEVM2-746 Schematic

4 Test Setup

4.1 Test and Configuration Software

In order to change any of the default configuration parameters on the EVM, it is necessary to obtain the TI Fusion Digital Power Designer software.

4.1.1 Description

The Fusion Digital Power Designer is the graphical user interface (GUI) used to configure and monitor the Texas Instruments TPS546C20A power converter installed on this evaluation module. The application uses the PMBus protocol to communicate with the controller over serial bus by way of a TI USB adapter. This adapter can be purchased at <http://www.ti.com/tool/usb-to-gpio>. (see).

4.1.2 Features

Some of the tasks you can perform with the GUI include:

- Turn on or off the power supply output, either through the hardware control line or the PMBus operation command.
- Monitor real-time data. Items such as output voltage, output current, die temperature, warnings and faults which are continuously monitored and displayed by the GUI.
- Configure common operating characteristics such as V_{OUT} trim and margin, UVLO, soft-start time, warning and fault thresholds, fault response, and ON/OFF modes.

This software is available for download at this location:

http://www.ti.com/tool/fusion_digital_power_designer

4.2 Test Equipment

4.2.1 Voltage Source

The input voltage source V_{IN} should be a 0-V to 20-V variable DC source capable of supplying 25 ADC. Connect input VIN and GND to J2 and J3 as shown in [Figure 2](#) and .

4.2.2 Multimeters

It is recommended to use two separate multi-meters as shown in [Figure 2](#) and . One meter to measure V_{IN} , the other to measure V_{OUT} .

4.2.3 Output Load:

A variable electronic load is recommended for the test setup as shown in [Figure 2](#) or . The load should be capable of 80 A.

4.2.4 Oscilloscope

An oscilloscope is recommended for measuring output noise and ripple. Output ripple should be measured using a *Tip-and-Barrel* method or better as shown in [Figure 3](#).

4.2.5 Fan:

During prolonged operation at high loads, it may be necessary to provide forced air cooling with a small fan aimed at the EVM. The surface temperature of the devices on the EVM should be maintained below 105°C.

4.2.6 USB-to-GPIO Interface Adapter:

A communications adapter is required between the EVM and the host computer. This EVM was designed to use the Texas Instruments USB-to-GPIO Adapter, see . This adapter can be purchased here:

<http://www.ti.com/tool/usb-to-gpio>.

4.2.7 Recommended Wire Gauge

- Input VIN and GND to J2 and J3 (GND) (12-V input) – The recommended wire size is AWG #12, with the total length of wire less than 2 feet (1 feet input, 1 feet return).
- Output J8/J7 and GND J10/J11 (0.9-V output) – The minimum recommended wire size is AWG #10, with the total length of wire less than 2 feet (1 feet OUTPUT, 1 feet return).

4.3 Recommended Test Setup

Figure 2 and shows the recommended test setup.

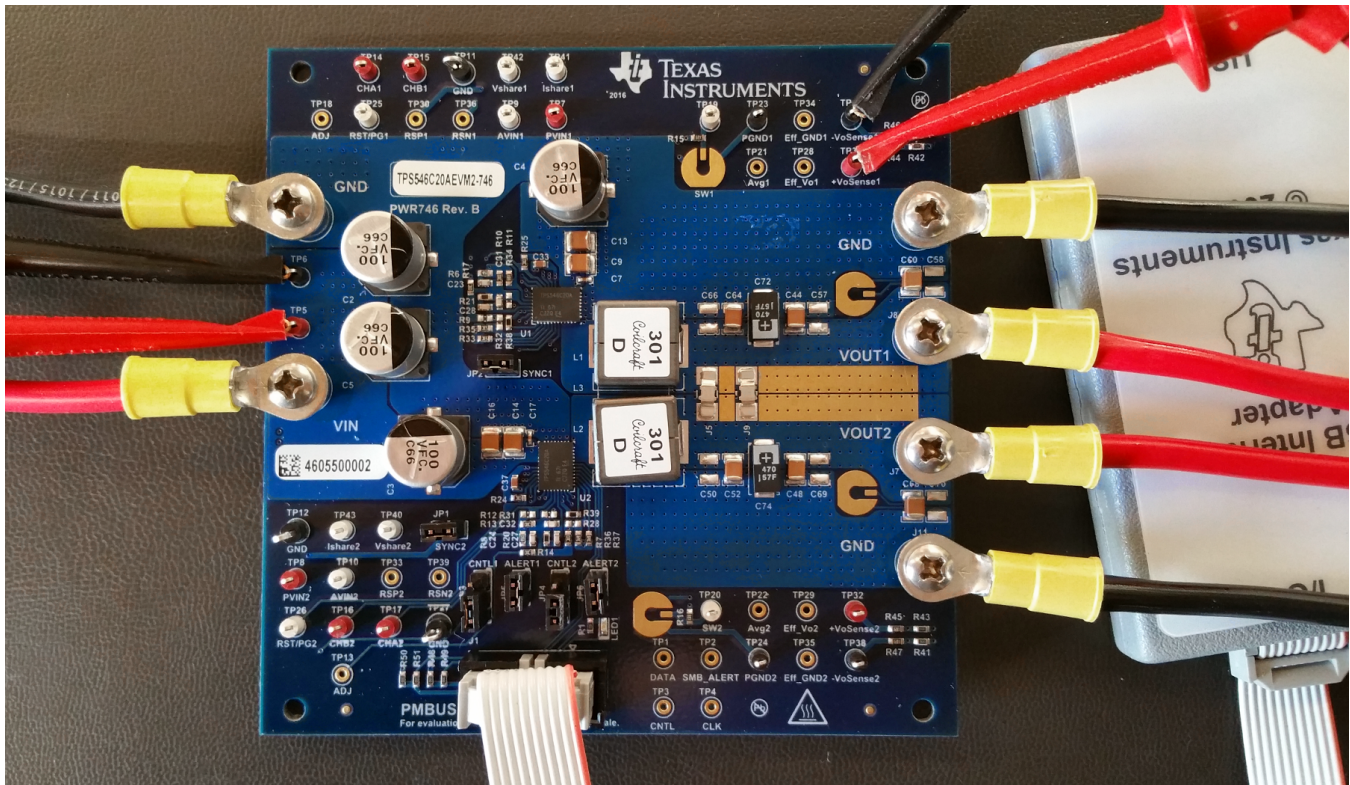
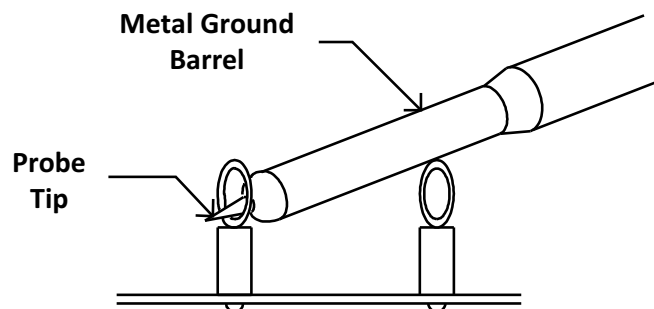


Figure 2. TPS546C20AEVM2-746 EVM Recommended Test Set Up

Figure 3 illustrates the tip and barrel measurement for switching node waveform on TP19 with TP23 or TP20 with TP24.



Tip and Barrel V_{OUT} Ripple Measurement

Figure 3. Tip and Barrel Measurement

4.4 List of Test Points, Jumpers and Connectors

Table 2 lists the test point functions.

Table 2. Test Point Functions

| Test Point | Type | Name | Description |
|------------|---------------|-----------|--|
| TP1 | Not Assembled | DATA | DATA signal on J1 socket |
| TP2 | Not Assembled | SMB_ALERT | SMBALERT signal on J1 socket |
| TP3 | Not Assembled | CNTL | CNTL signal on J1 socket |
| TP4 | Not Assembled | CLK | CLK signal on J1 socket |
| TP5 | T-H Loop | VIN | V_{IN+} measurement point |
| TP6 | T-H Loop | GND | V_{IN-} measurement point |
| TP7 | T-H Loop | PVIN1 | PVIN pin voltage of U1 device measurement point |
| TP8 | T-H Loop | PVIN2 | PVIN pin voltage of U2 device measurement point |
| TP9 | T-H Loop | AVIN1 | AVIN pin voltage of U1 device measurement point |
| TP10 | T-H Loop | AVIN2 | AVIN pin voltage of U2 device measurement point |
| TP11 | T-H Loop | GND | GND reference |
| TP12 | T-H Loop | GND | GND reference |
| TP13 | Not Assembled | ADJ | Analog input to adjust rail 2 output voltage |
| TP14 | T-H Loop | CHA1 | Input for small signal loop gain measurements for output rail 1 (B/A setup) |
| TP15 | T-H Loop | CHB1 | OUTPUT for small signal loop gain measurements for output rail 1 (B/A setup) |
| TP16 | T-H Loop | CHB2 | OUTPUT for small signal loop gain measurements for output rail 2 (B/A setup) |
| TP17 | T-H Loop | CHA2 | Input for small signal loop gain measurements for output rail 2 (B/A setup) |
| TP18 | Not Assembled | ADJ | Analog input to adjust rail 1 output voltage |
| TP19 | T-H Loop | SW1 | Switching node of output rail 1 measurement point, reference to TP23 |
| TP20 | T-H Loop | SW2 | Switching node of output rail 2 measurement point, reference to TP24 |
| TP21 | Not Assembled | AVG1 | Rail 1 switching node average voltage measurement point, reference to TP23 |
| TP22 | Not Assembled | AVG2 | Rail 2 switching node average voltage measurement point, reference to TP24 |
| TP23 | T-H Loop | PGND1 | GND reference for switching node measurement |
| TP24 | T-H Loop | PGND2 | GND reference for switching node measurement |
| TP25 | T-H Loop | RST/RG1 | PGOOD signal of output 1 |
| TP26 | T-H Loop | RST/PG2 | PGOOD signal of output 2 |
| TP27 | T-H Loop | GND | GND reference |
| TP28 | Not Assembled | EFF_VO1 | U1 output voltage measurement point for efficiency, reference to TP34 |
| TP29 | Not Assembled | EFF_VO2 | U2 output voltage measurement point for efficiency, reference to TP35 |
| TP30 | Not Assembled | RSP1 | Output 1 remote sense + voltage point |
| TP31 | T-H Loop | +VOSENSE1 | V_{OUT1+} measurement point |
| TP32 | T-H Loop | +VOSENSE2 | V_{OUT2+} measurement point |
| TP33 | Not Assembled | RSP2 | Output 2 remote sense + voltage point |
| TP34 | Not Assembled | EFF_GND1 | Rail 1 output voltage referencing GND for efficiency measurement |
| TP35 | Not Assembled | EFF_GND2 | Rail 1 output voltage referencing GND for efficiency measurement |
| TP36 | Not Assembled | RSN1 | Output 1 remote sense - voltage point |
| TP37 | T-H Loop | -VOSENSE1 | V_{OUT1-} measurement point |
| TP38 | T-H Loop | -VOSENSE2 | V_{OUT2-} measurement point |
| TP39 | Not Assembled | RSN2 | Output 2 remote sense - voltage point |
| TP40 | T-H Loop | Vshare2 | VSHARE of U2 measurement point. Sensitive signal. |
| TP41 | T-H Loop | Ishare1 | ISHARE of U1 measurement point. Sensitive signal. |
| TP42 | T-H Loop | Vshare1 | VSHARE of U1 measurement point. Sensitive signal. |
| TP43 | T-H Loop | Ishare2 | ISHARE of U2 measurement point. Sensitive signal. |

Table 3 lists the EVM jumpers.

Table 3. Jumpers

| Jumper | Type | Name | Description |
|--------|----------------------|--------|---|
| JP1 | Header, 100 mil, 2x1 | SYNC2 | Synchronization connection between U1 and U2. Jumper is plugged as default. |
| JP2 | Header, 100 mil, 2x1 | SYNC1 | Synchronization connection between U1 and U2. Jumper is plugged as default. |
| JP3 | Header, 100 mil, 3x1 | CNTL1 | PMBUS CNTL connection options for U1 to socket J1 or GND. Jumper connecting U1 to J1 is plugged as default. |
| JP4 | Header, 100 mil, 3x1 | CNTL2 | PMBUS CNTL connection options for U2 to socket J1 or GND. Jumper connecting U2 to J1 is plugged as default. |
| JP5 | Header, 100 mil, 2x1 | ALERT1 | PMBUS SMBALERT connection between U1 and socket J1. Jumper connecting U1 to J1 is plugged as default. |
| JP6 | Header, 100 mil, 2x1 | ALERT2 | PMBUS SMBALERT connection between U2 and socket J1. Jumper connecting U2 to J1 is plugged as default. |

Table 4 lists the EVM connector functions.

Table 4. Connector Functions

| Connector | Type | Name | Description |
|-----------|---------------------|-------|------------------------------------|
| J1 | Header, 100mil, 5x2 | PMBUS | PMBUS socket for TI FUSION adaptor |
| J2 | Keystone 1546 | VIN | VIN+ connector |
| J3 | Keystone 1546 | GND | VIN- (GND) connector |
| J8 | Keystone 1546 | VOUT1 | VOUT1+ connector |
| J10 | Keystone 1546 | GND | VOUT1- connector |
| J7 | Keystone 1546 | VOUT2 | VOUT2+ connector |
| J11 | Keystone 1546 | GND | VOUT2- connector |

5 EVM Configuration Using the Fusion GUI

The TPS546C20A on this EVM leave the factory pre-configured. See [Table 5](#) for a short list of key factory configuration parameters as obtained from the configuration file.

Table 5. Key Factory Configuration Parameters

| ADDRESS HEX | ADDRESS DEC | PART ID | DESIGNATOR | | |
|--------------------------|--------------|-------------|--|--|--|
| 0x44 | 36 | TPS546C20A | U1 | | |
| 0x44 | 37 | TPS546C20A | U2 | | |
| GENERAL | | | | | |
| CMD Code | CMD CODE HEX | ENCODED HEX | DECODED | COMMENTS | |
| VIN_OFF | 0x36 | 0xF010 | 4.0 V | Turn OFF voltage | |
| VIN_ON | 0x35 | 0xF012 | 4.5 V | Turn ON voltage | |
| IOUT_CAL_OFFSET | 0x39 | 0xE000 | 0.0000 A | Current offset for PMBUS readout | |
| IOUT_OC_FAULT_LIMIT | 0x46 | 0xF854 | 42 A | OC fault level | |
| IOUT_OC_FAULT_RESPONSE | 0x47 | 0xFF | Restart | Response to OC fault | |
| IOUT_OC_WARN_LIMIT | 0x4A | 0xF84A | 37 A | OC warning level | |
| VOUT_COMMAND | 0x21 | 0x0133 | 0.6 V | Reference voltage | |
| VOUT_MIN | 0x2B | 00B3h | 0.35V | minimum reference voltage | |
| VOUT_MAX | 0x24 | 0x034D | 1.65 V | maximum reference voltage | |
| VOUT_TRANSITION_RATE | 0x27 | 0xD03C | 1 mV/us | Vout transition rate | |
| VOUT_SCALE_LOOP | 0x29 | 0xF004 | 1 | Output sense scaling ratio for main control loop | |
| PCT_OV_UV_WRN_FLT_LIMITS | 0xD6 | 0x00 | UV FAULT | 83% | Output OV/UV Settings, reference to nominal reference voltage. |
| | | | UV WARN | 88% | |
| | | | OV WARN | 112% | |
| | | | OV FAULT | 117% | |
| VOUT_OV_FAULT_RESPONSE | 0x41 | 0xBF | Restart | Output overvoltage fault response | |
| VOUT_UV_FAULT_RESPONSE | 0x45 | 0xBF | Restart | Output undervoltage fault response | |
| ON_OFF_CONFIG | 0x02 | 0x16 | CNTL only, Active High. | Control signal and operation command | |
| OPERATION | 0x01 | 0x00 | Operation is not used to enable regulation | Can be used to control device On/Off | |
| OT_FAULT_LIMIT | 0x4F | 0x0091 | 145°C | OT fault level | |
| OT_WARN_LIMIT | 0x51 | 0x0078 | 120°C | OT warn level | |
| OT_FAULT_RESPONSE | 0x50 | 0x3F | Ignore | Response to over temperature faults | |
| TON_DELAY | 0x60 | 0x0000 | 0 ms | Turn-on delay | |
| TON_RISE | 0x61 | 0x0003 | 3 ms | Soft-start time | |
| TON_MAX_FAULT_LIMIT | 0x62 | 0x0000 | Disabled | Upper limit for Vout reaching regulation | |
| TOFF_DELAY | 0x64 | 0x0000 | 0 ms | Turn-off delay | |
| TOFF_FALL | 0x65 | 0x0000 | 0 ms | Soft-stop fall time | |

If it is desired to configure the EVM to settings other than the factory settings shown above, the TI Fusion Digital Power Designer software can be used for reconfiguration. It is necessary to have input voltage applied to the EVM prior to launching the software so that the TPS546C20A may respond to the GUI and the GUI can recognize the device. The default configuration for the EVM is to start converting at an input voltage of 4.5V, therefore to avoid any converter activity during configuration, an input voltage less than 4.5 V should be applied. An input voltage of 4 V is recommended.

5.1 Configuration Procedure

1. Adjust the input supply to provide 4 VDC, current limited to 1 A.
2. Apply the input voltage to the EVM. Refer to [Figure 2](#) for connections and test setup.
3. Launch the Fusion GUI software. Refer to the screenshots in [Section 10](#) for more information.
4. Configure the EVM operating parameters as desired.
5. VSEL and SS pin resistors on the EVM would program VOUT_COMMAND and TON_RISE at power up. By default, device would ignore the values stored in the internal non-volatile memory and write corresponding registers with the resistor programmed value. If **DIS_VSEL** bit in **OPTIONS (MFR_SPECIFIC_21) (E5h)** is modified to 1 (default 0), the initial VOUT_COMMAND would be same as the value stored in the internal non-volatile memory. Please see Datasheet for more details.

By default, U1 is configured as loop master, U2 is configured as loop slave, PMBUS address for U1 is 36 decimal and for U2 is 37 decimal. These two addresses are fixed.

Both device can be configured or monitored through PMBUS interface at different address.

6 Test Procedure

6.1 Line and Load Regulation and Efficiency Measurement Procedure

1. Set up the EVM as described in [Figure 2](#).
2. Ensure the electronic loads is set to draw 0 Adc.
3. Increase V_{IN} from 0 V to 12 V using voltage meter to measure input voltage.
4. Use the other voltage meter to measure output voltage V_{OUT} .
5. Vary the load from 0 to 70 Adc. V_{OUT} should remain in regulation as defined in [Table 1](#).
6. Vary V_{IN} from 5 V to 18 V. V_{OUT} should remain in regulation as defined in [Table 1](#).
7. Decrease the load to 0 A.
8. Decrease V_{IN} to 0 V.

6.2 Control Loop Gain and Phase Measurement Procedure

The TPS546C20AEVM2-746 EVM includes a 49.9- Ω series resistor in the feedback loop for V_{OUT} . The resistor is accessible at the test points TP14 / TP15 for loop response analysis. These test points should be used during loop response measurements as the perturbation injecting points for the loop. See the description in [Table 6](#).

Table 6. List of Test Points for Loop Response Measurements

| Test Point | Node Name | Description | Comment |
|------------|-----------|--|---|
| TP14 | CHA1 | Input to feedback divider of V_{OUT} | The amplitude of the perturbation at this node should be limited to less than 30 mV |
| TP15 | CHB1 | Resulting output of V_{OUT} | Bode can be measured by a network analyzer with a CH-B/CH-A configuration |

Measure only one output at a time, with the following procedure:

1. Set up the EVM as described in [Figure 2](#).
2. For V_{OUT} , connect the network analyzer's isolation transformer from TP14 to TP15,
3. Connect the input signal measurement probe to TP14. Connect the output signal measurement probe to TP15.
4. Connect the ground leads of both probe channels to TP11.
5. On the network analyzer, measure the Bode as TP15/TP14 (Out/In).

6.3 Efficiency Measurement

In order to evaluate the efficiency of the power train (device and inductor), it is important to measure the voltages at the correct location. This is necessary because otherwise the measurements will include losses that are not related to the power train itself. Losses incurred by the voltage drop in the copper traces and in the input and output connectors are not related to the efficiency of the power train, which should not be included in efficiency measurements.

Input current can be measured at any point in the input wires, and output current can be measured anywhere in the output wires of the output being measured.

[Table 7](#) shows the measurement points for input voltage and output voltage. VIN and VOUT are measured to calculate the efficiency. Using these measurement points will result in efficiency measurements that excluded losses due to the connectors and PCB traces.

Table 7. Test Points for Better Efficiency Measurements

| Test Point | Node Name | Description | Comment |
|-------------|-----------|---|--|
| VOUT | | | |
| TP7 | PVIN1 | Input voltage measurement point for VIN1+ | The pair of test points are connected to the PVIN/GND pins of U1. The voltage drop between input terminal to the device pins is excluded for efficiency measurement. |
| TP23 | PGND1 | Input voltage measurement point for VIN1- (GND) | |
| TP28 | Eff_Vo1 | Output voltage measurement point for VOUT1+ | The pair of test points are connected to the closest points of Vout /GND to the inductor. The voltage drop from the output point of inductor to the output terminals is excluded for efficiency measurement. |
| TP34 | Eff_GND1 | Output voltage measurement point for VOUT1- (GND) | |

7 Performance Data and Typical Characteristic Curves

Figure 4 through Figure 17 present typical performance curves for the TPS546C20AEM2-746 .

7.1 Efficiency

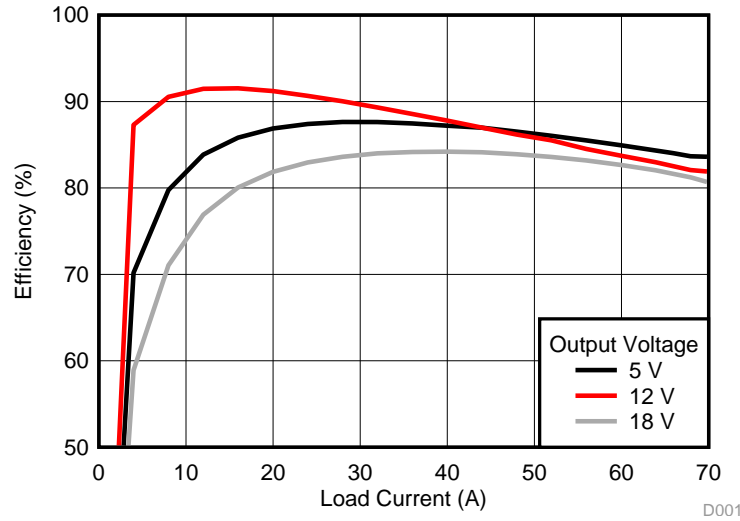


Figure 4. Efficiency of 0.9-V Output vs Line and Load

7.2 Load Regulation

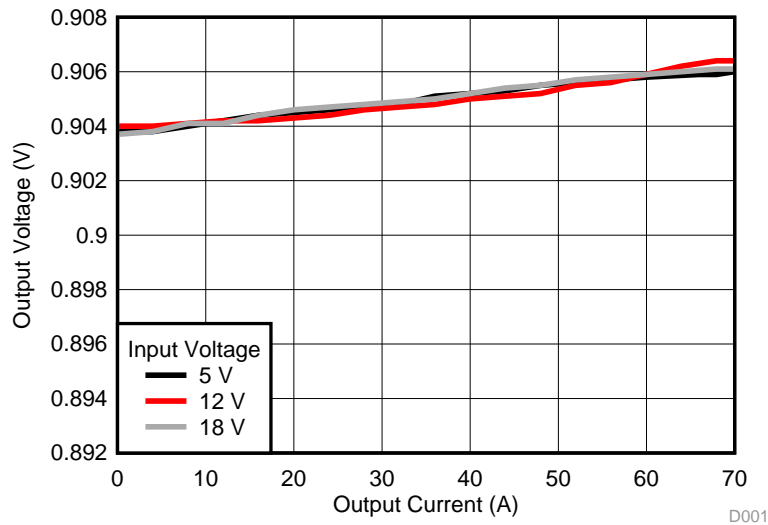


Figure 5. Load Regulation of 0.9-V Output

7.3 Line Regulation

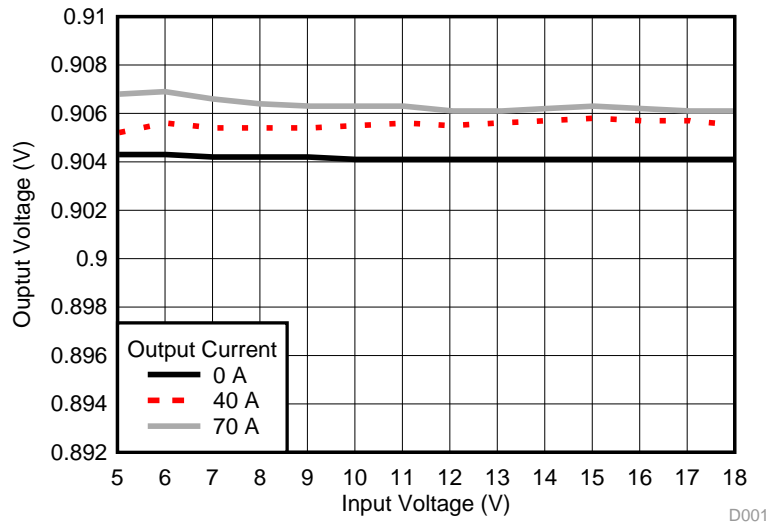
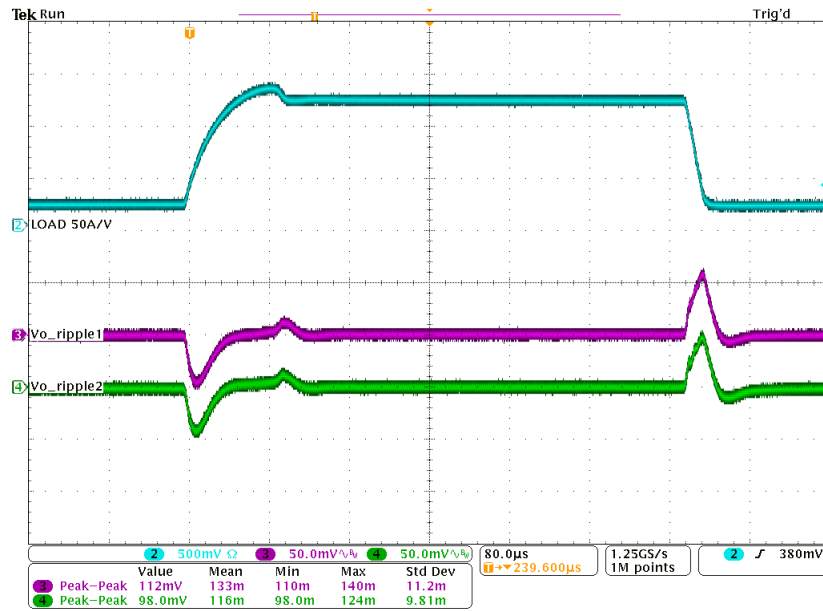


Figure 6. Line Regulation of 0.9-V Output (Different Board)

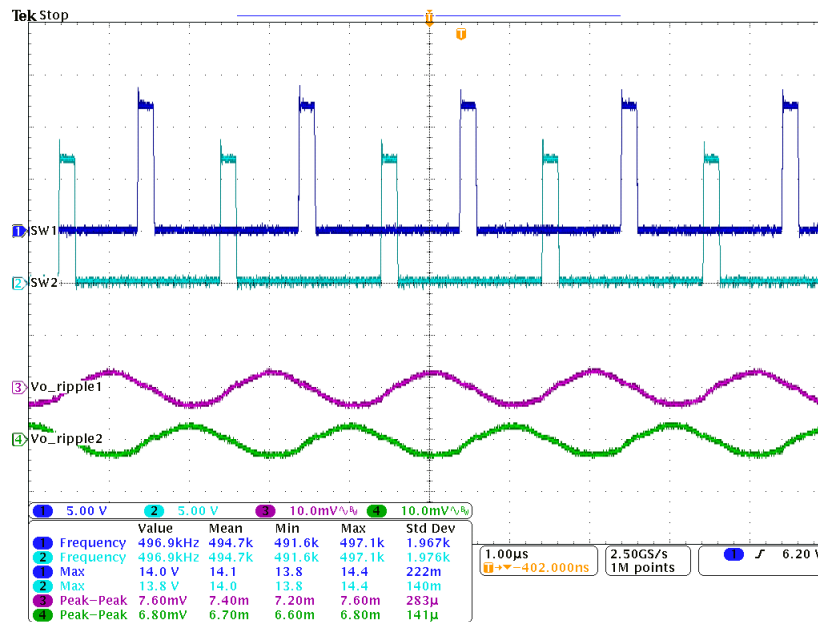
7.4 Transient Response



Ch1 = I_{OUT} at 25 A/division, Ch3 = V_{OUT} (AC coupled, measured at U1 side) at 50 mV/division, Ch4 = V_{OUT} (AC coupled, measured at U2 side) at 50 mV/division

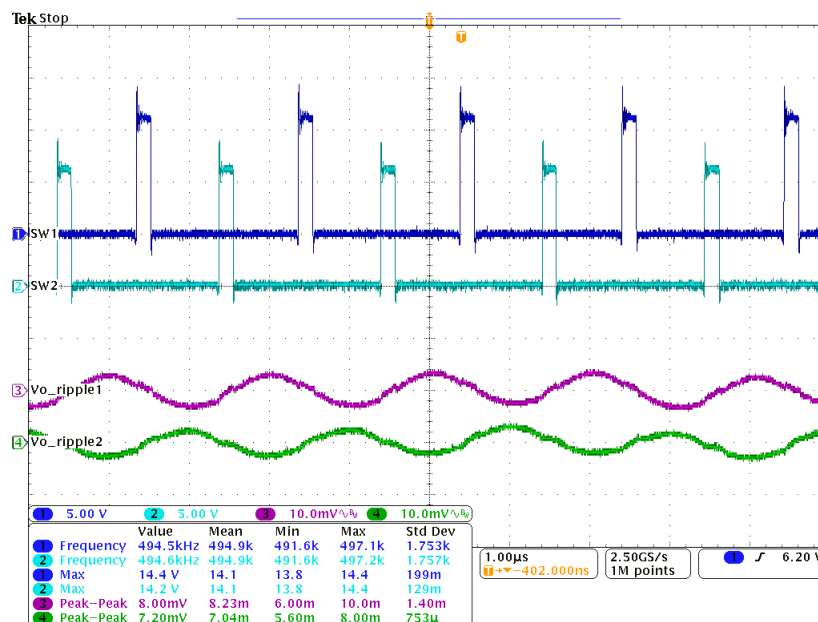
Figure 7. Transient Response of 0.9-V Output at 12 V_{IN} , Transient is 10 A to 60 A, 0.2 A/ μ s

7.5 Output Ripple



Ch1 = V_{SW1} at 5 V/division, Ch2 = V_{SW2} at 5 V/division, Ch3 = V_{OUT} (AC coupled, measured at U1 side) ripple at 10 mV/division, Ch4 = V_{OUT} (AC coupled, measured at U2 side) ripple at 10 mV/division

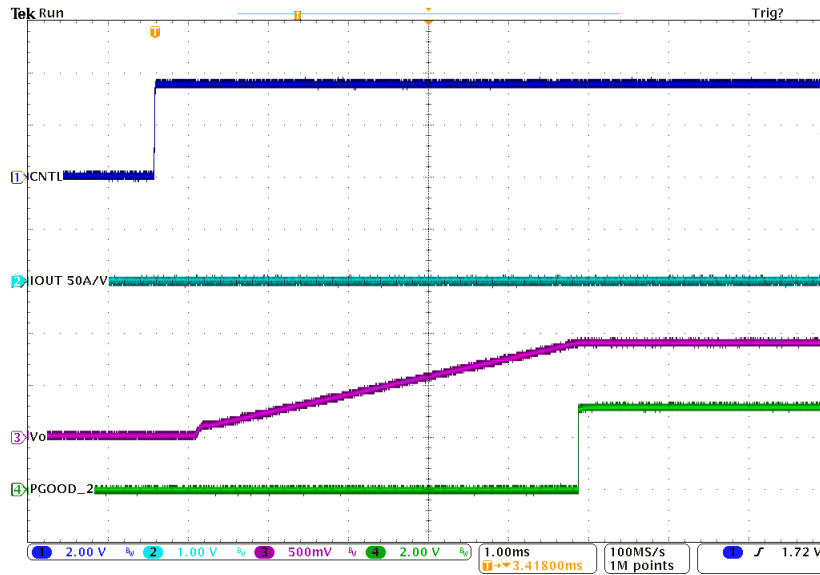
Figure 8. Output Ripple and SW Node of 0.9-V Output at 12 V_{IN} , 0-A Output



Ch1 = V_{SW1} at 5 V/division, Ch2 = V_{SW2} at 5 V/division, Ch3 = V_{OUT} (AC coupled, measured at U1 side) ripple at 10 mV/division, Ch4 = V_{OUT} (AC coupled, measured at U2 side) ripple at 10 mV/division

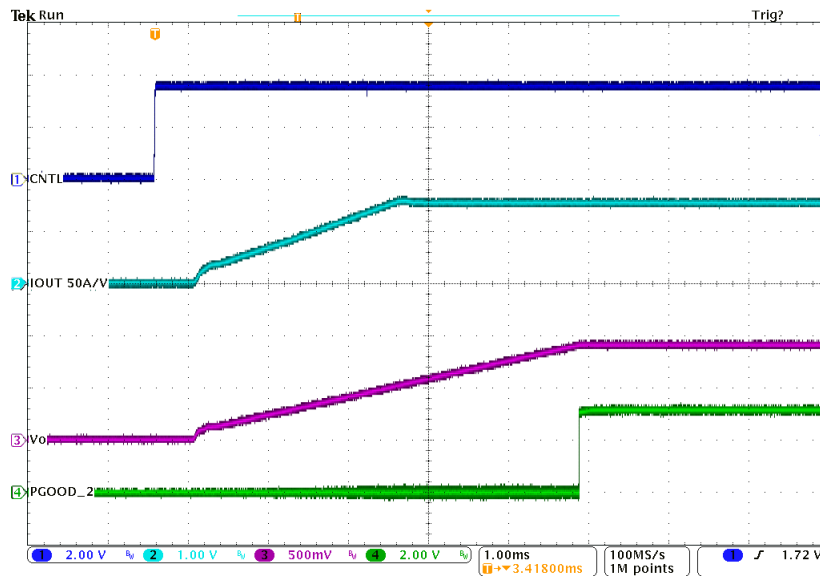
Figure 9. Output Ripple and SW Node of 0.9-V Output at 12 V_{IN} , 70-A Output

7.6 Control On



Ch1 = CNTL at 2 V/division, Ch2 = I_{OUT} at 50 A/division, Ch3 = V_{OUT} at 500 mV/division, Ch4 = PGOOD at 2 V/division

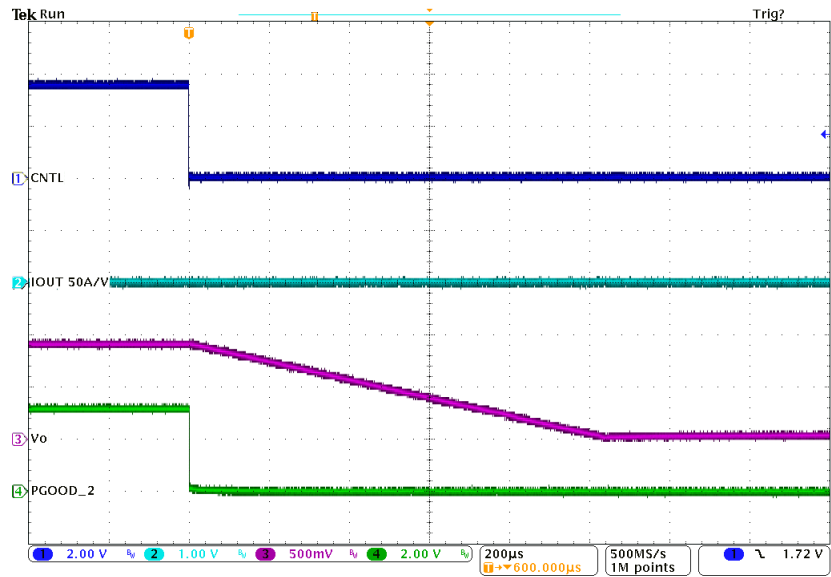
Figure 10. Start up from Control, 0.9-V Output at 12 V_{IN}, 0-A Output



Ch1 = CNTL at 2 V/division, Ch2 = I_{OUT} at 50 A/division, Ch3 = V_{OUT} at 500 mV/division, Ch4 = PGOOD at 2 V/division

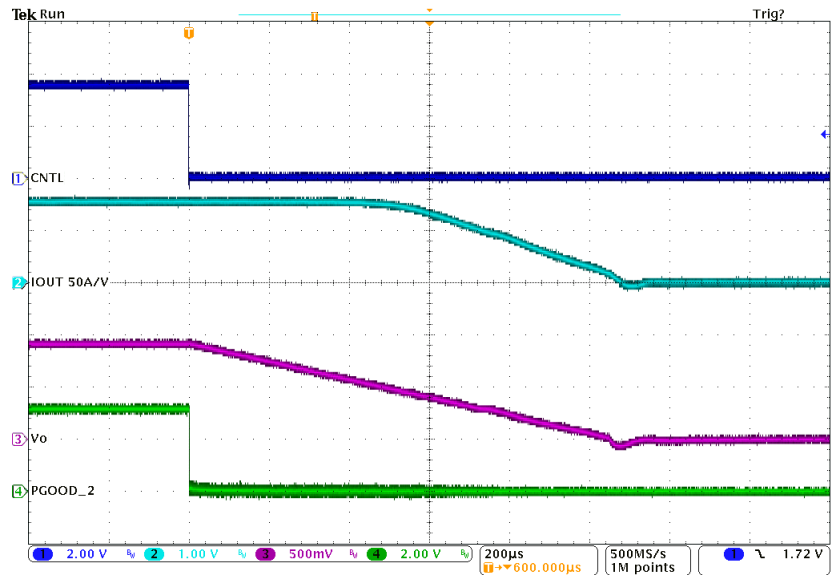
Figure 11. Start up from Control, 0.9-V Output at 12 V_{IN}, 70-A Output

7.7 Control Off



Ch1 = CNTL at 2 V/division, Ch2 = I_{OUT} at 50 A/division, Ch3 = V_{OUT} at 500 mV/division, Ch4 = PGOOD at 2 V/division

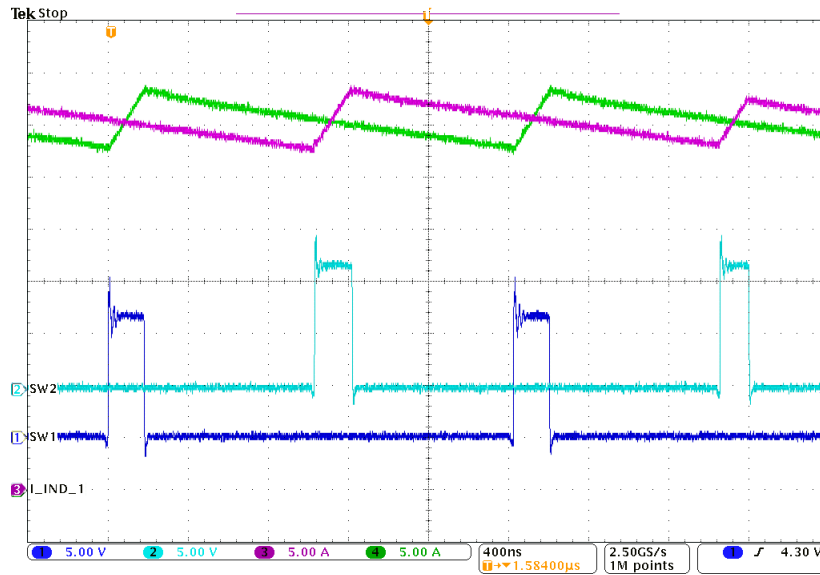
Figure 12. Soft Stop from Control, 0.9-V Output at 12 V_{IN}, 0-A Output



Ch1 = CNTL at 2 V/division, Ch2 = I_{OUT} at 50 A/division, Ch3 = V_{OUT} at 500 mV/division, Ch4 = PGOOD at 2 V/division

Figure 13. Soft Stop from Control, 0.9-V Output at 12 V_{IN}, 70-A Output

7.8 Current Sharing between two phases



Ch1 = V_{SW1} at 5 V/division, Ch2 = V_{SW2} at 5 V/division, Ch3 = I_{L2} at 5 A/division, Ch4 = I_{L1} at 5 A/division

Figure 14. Inductor Current and Switch Node Waveform, 0.9-V Output at 12 V_{IN} , 70-A Output

7.9 Control Loop Bode Plot

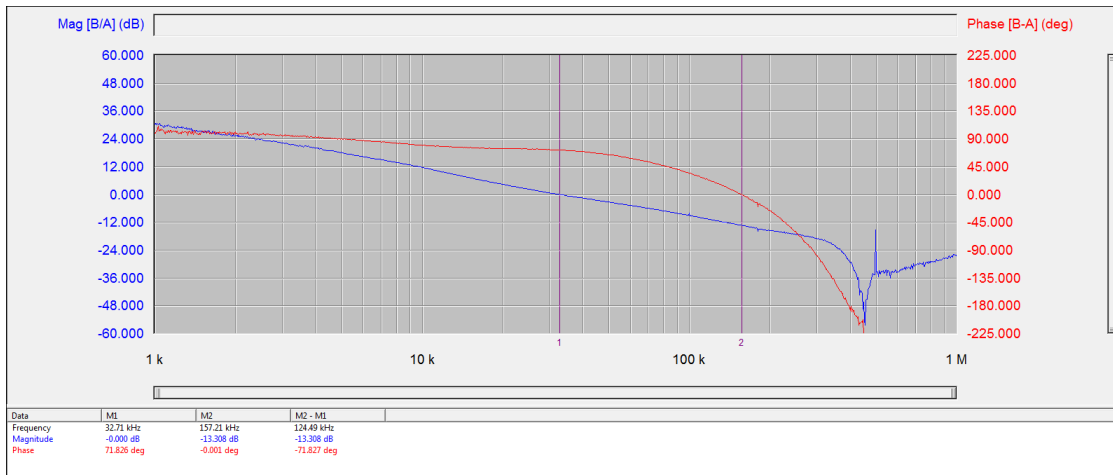


Figure 15. Bode Plot at 0.9-V Output at 12 V_{IN} , 0-A Output

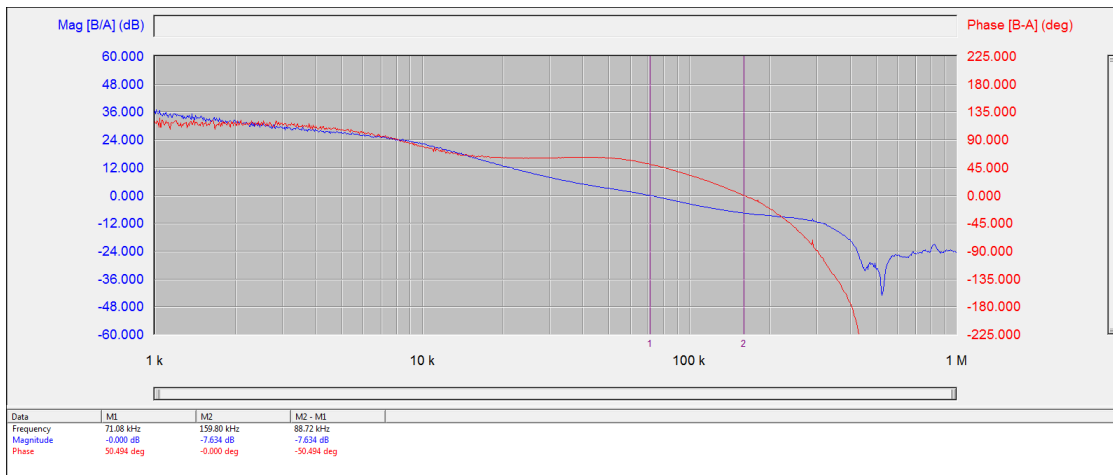
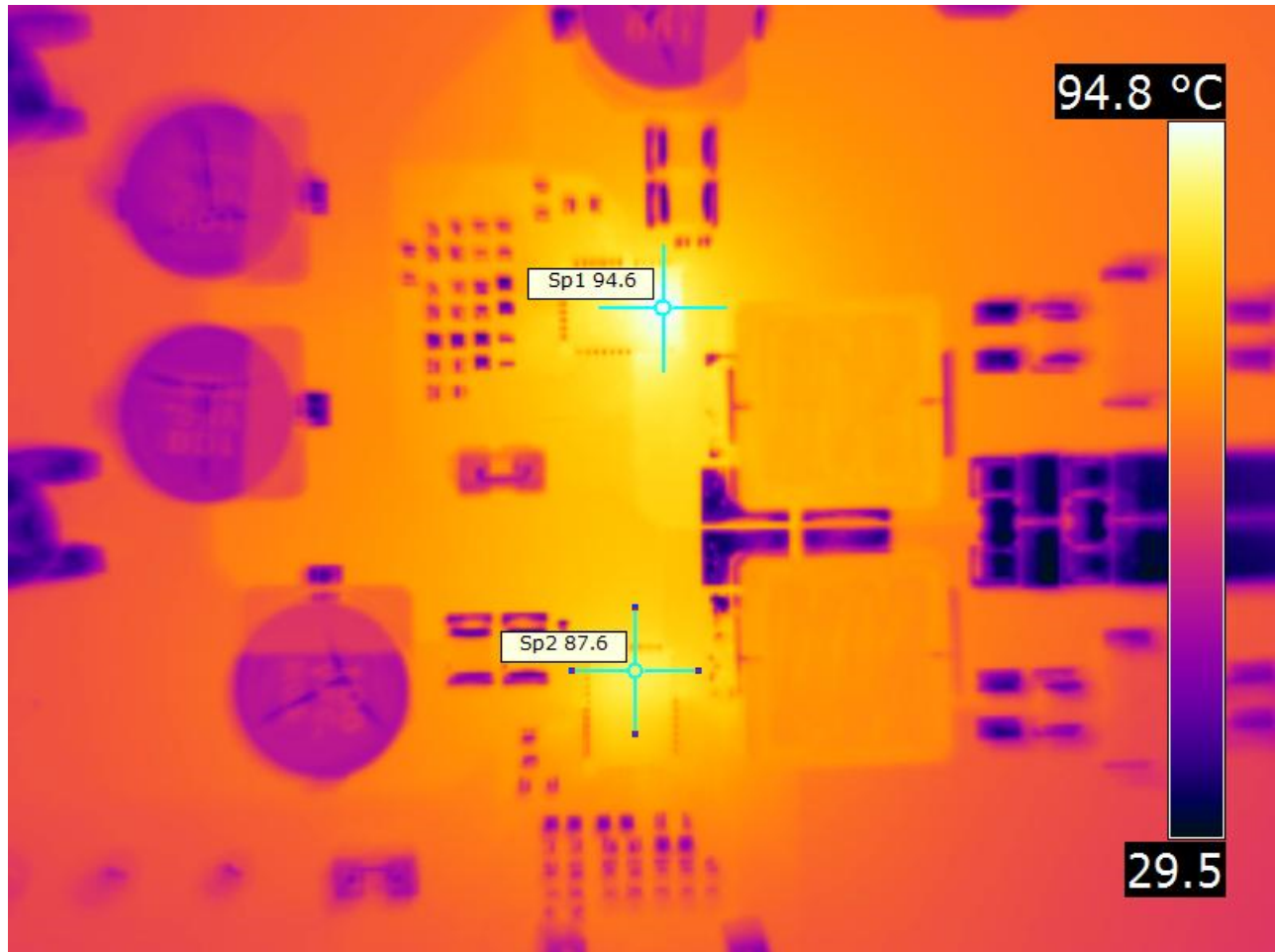


Figure 16. Bode Plot at 0.9-V Output at 12 V_{IN}, 70-A Output

7.10 Thermal Image



$V_{IN} = 12\text{ V}$, $I_{OUT} = 70\text{ A}$, $V_{OUT} = 0.9\text{ V}$, $F_{sw} = 500\text{ kHz}$

Figure 17. Thermal Image

8 EVM Assembly Drawing and PCB Layout

Figure 18 through Figure 26 show the design of the TPS546C20AEVM2-746 EVM printed circuit board.

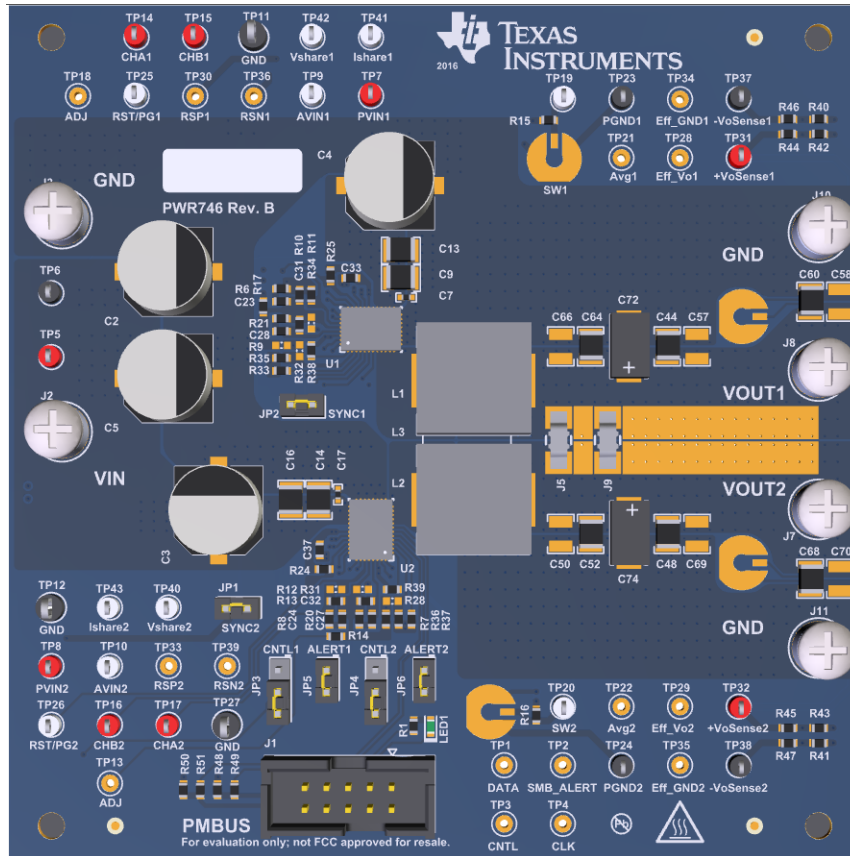


Figure 18. TPS546C20AEVM2-746 EVM 3D Top View

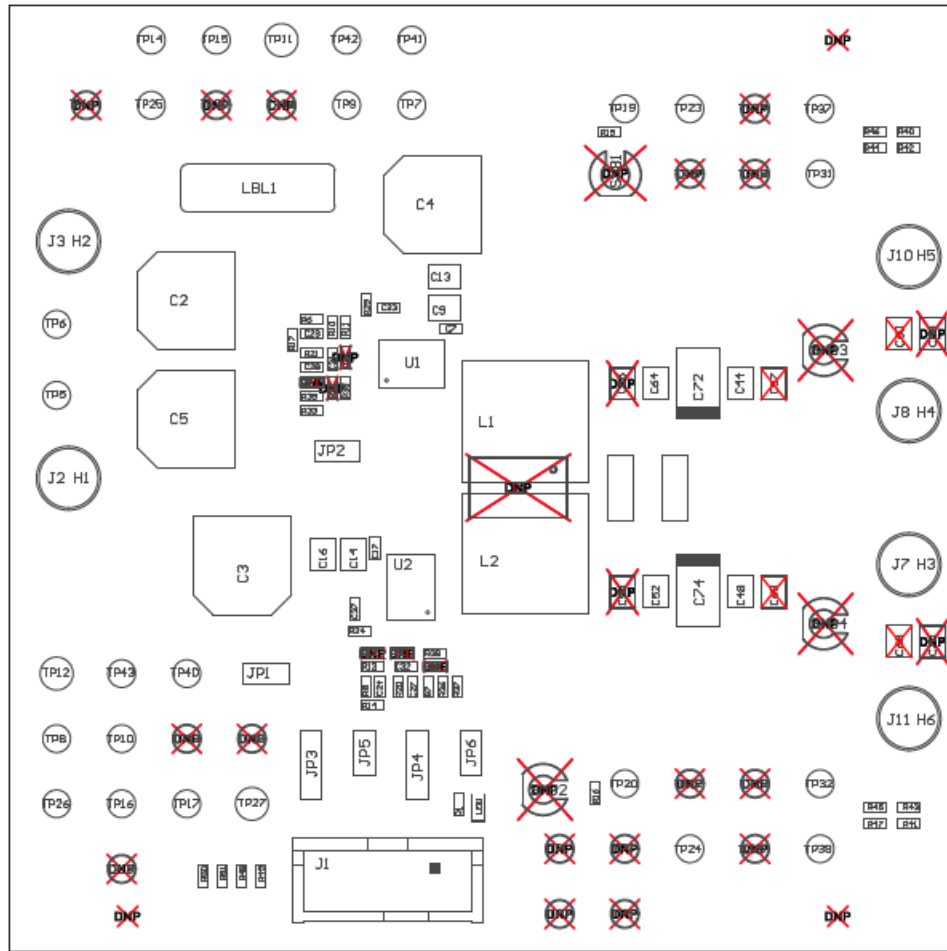


Figure 19. TPS546C20AEVM2-746 EVM Top Layer Assembly Drawing (Top View)

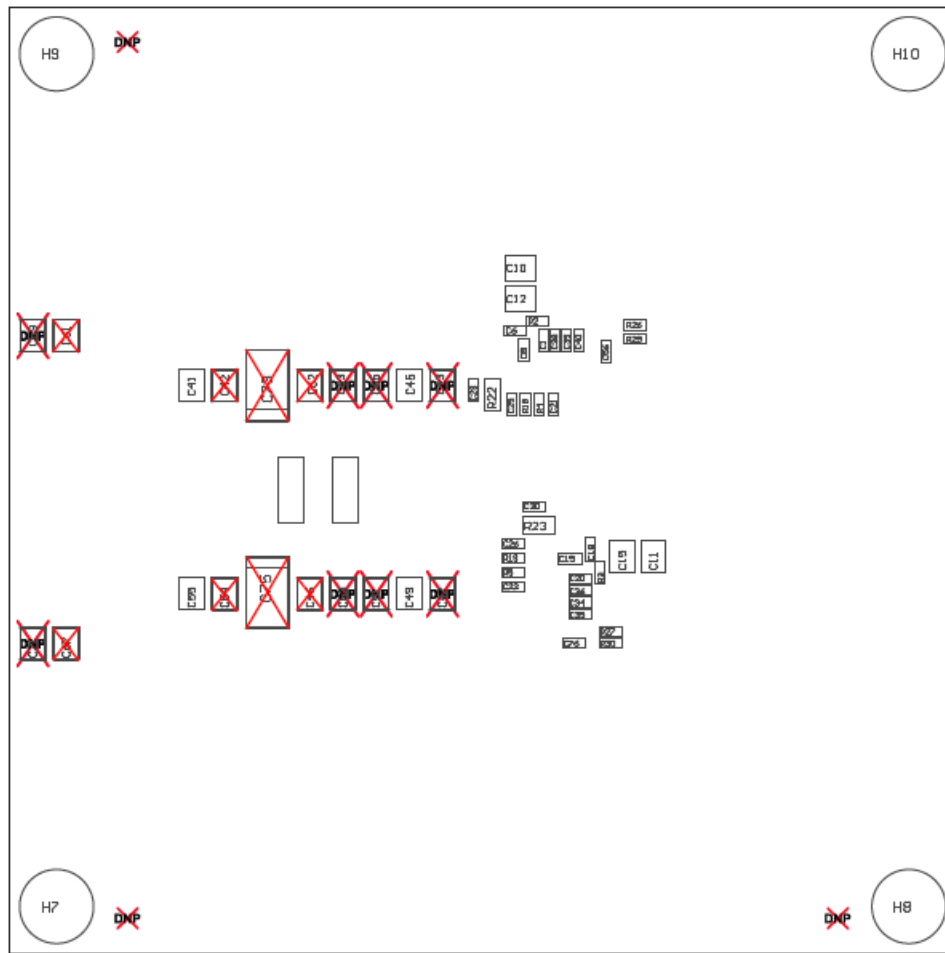


Figure 20. TPS546C20AEVM2-746 EVM Bottom Assembly Drawing (Bottom View)

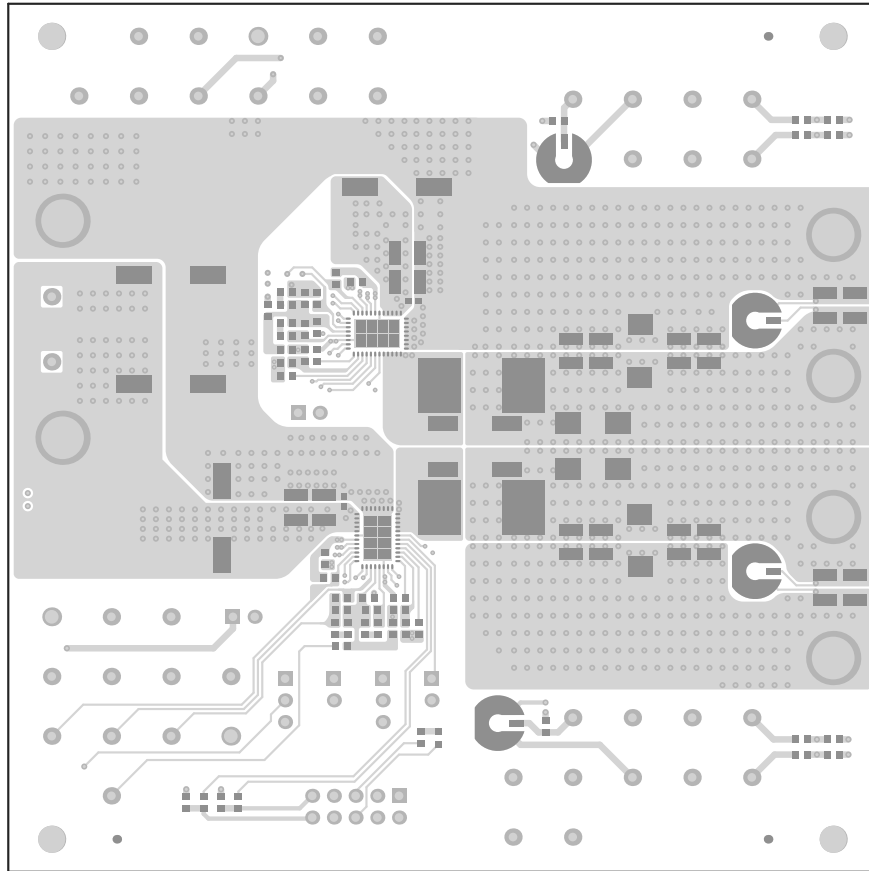


Figure 21. TPS546C20AEVM2-746 EVM Top Copper (Top View)

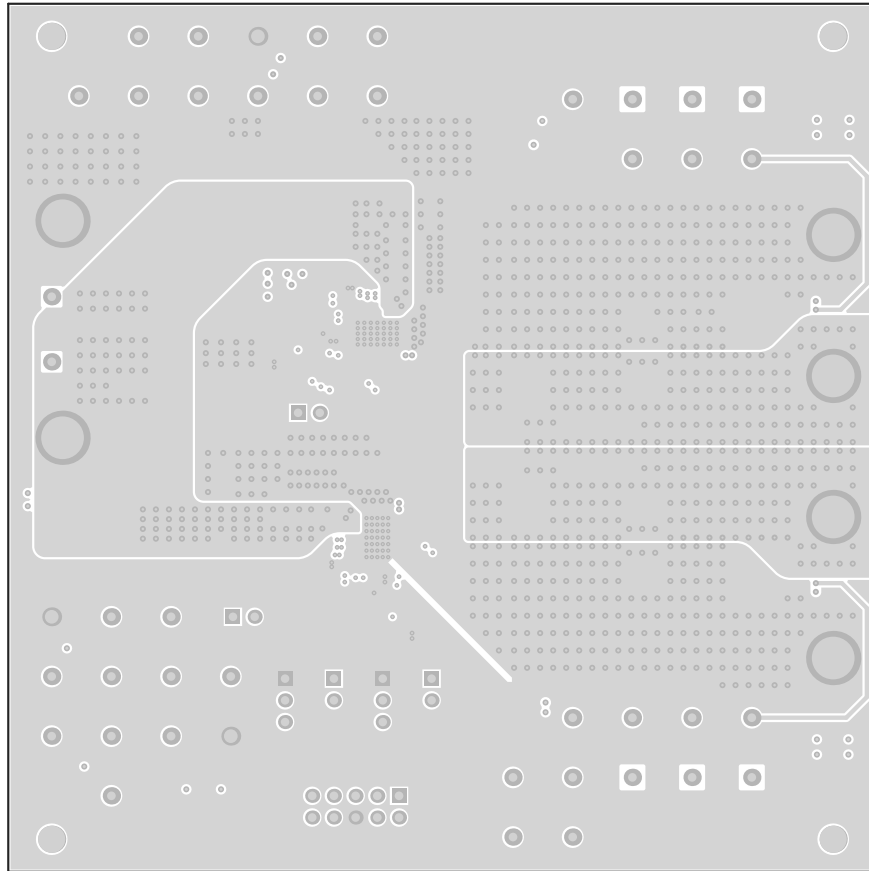


Figure 22. TPS546C20AEVM2-746 EVM Internal Layer 1 (Top View)

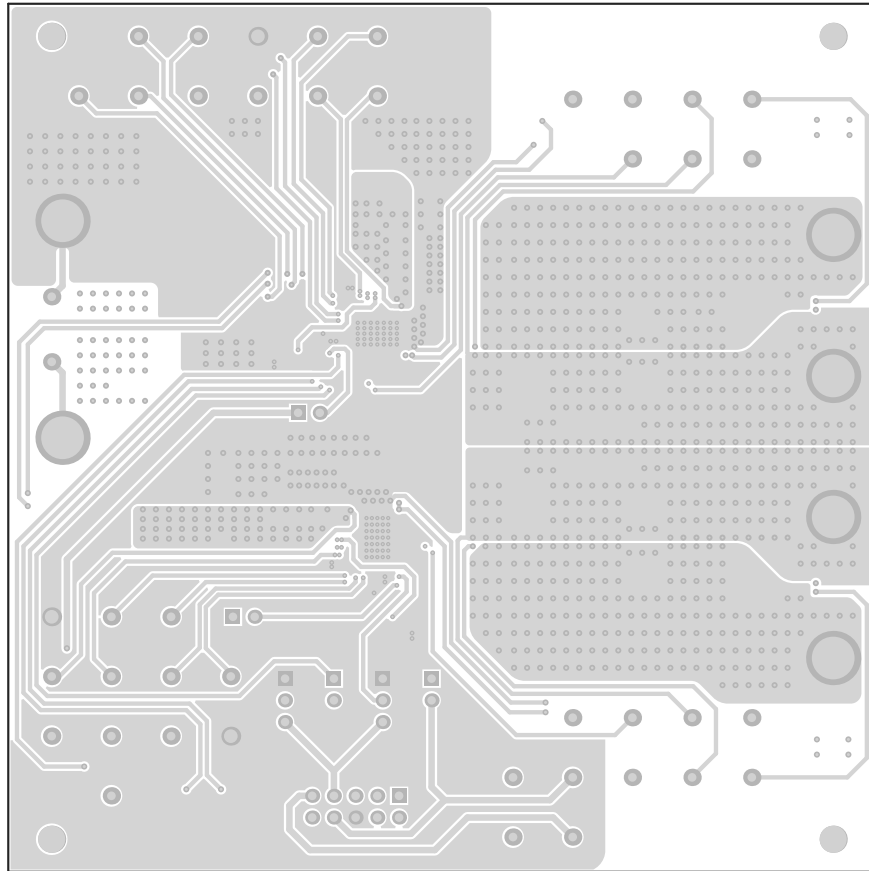


Figure 23. TPS546C20AEVM2-746 EVM Internal Layer 2 (Top View)

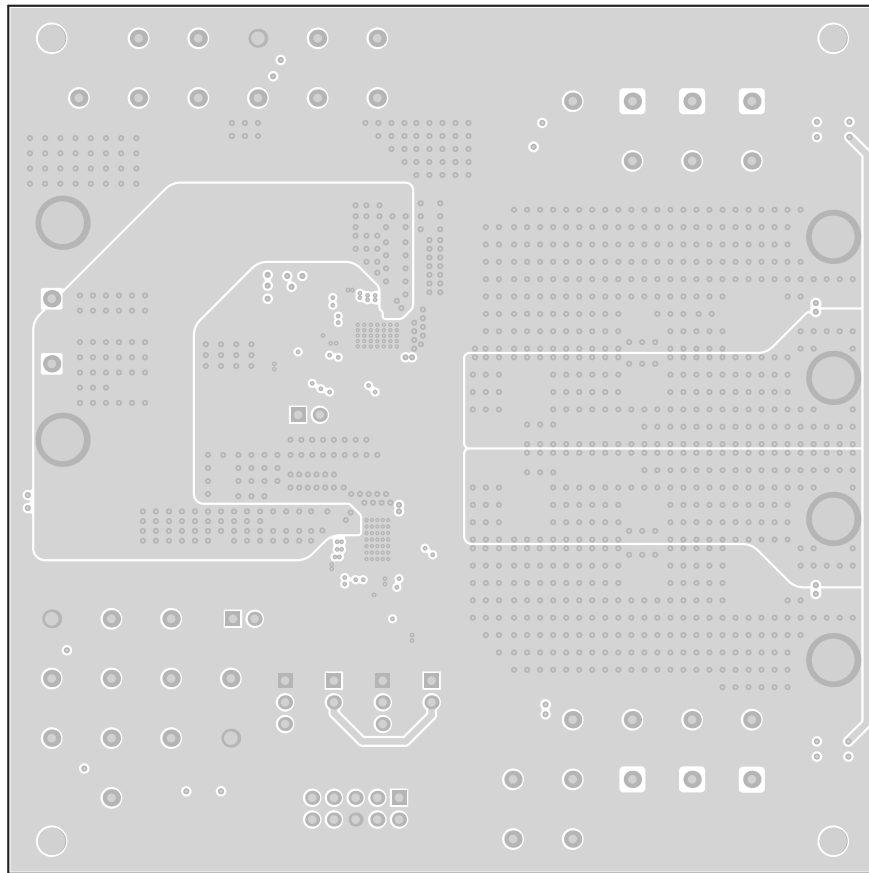


Figure 24. TPS546C20AEVM2-746 EVM Internal Layer 3 (Top View)

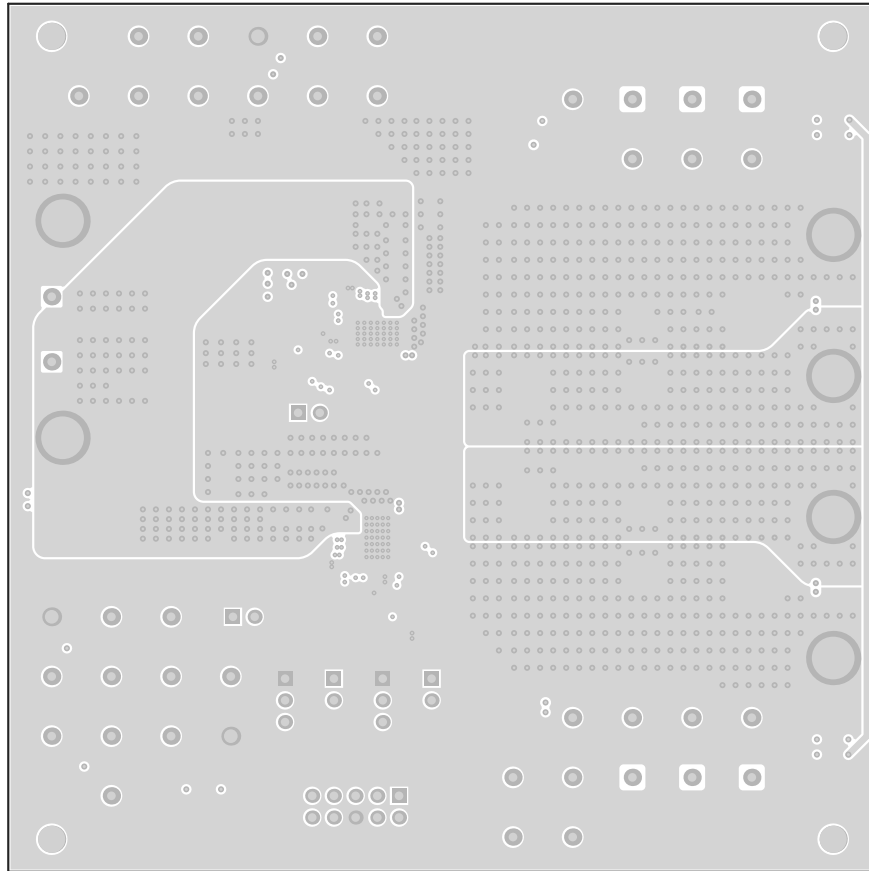


Figure 25. TPS546C20AEVM2-746 EVM Internal Layer 4 (Top View)

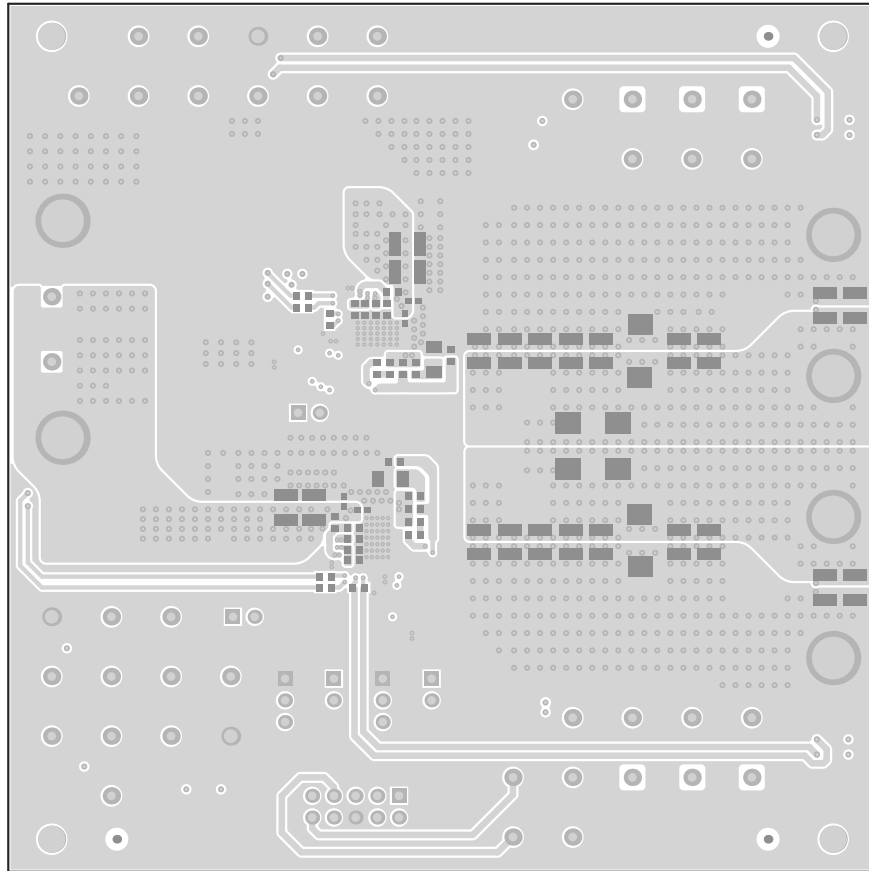


Figure 26. TPS546C20AEVM2-746 EVM Bottom Copper (Top View)

9 Bill of Materials

Table 8 lists the BOM for the TPS546C20AEVM2-746 (TPS546C20A EVM).

Table 8. TPS546C20AEVM2-746 Components List

| Qty | Designator | Description | Part Number | Manufacturer |
|-----|--|---|---------------------|---------------------|
| 4 | C1, C20, C29, C31 | CAP, CERM, 1 μ F, 25 V, +/- 10%, X7R, 0603 | GRM188R71E105KA12D | MuRata |
| 4 | C2, C3, C4, C5 | CAP, AL, 100 μ F, 35 V, +/- 20%, 0.15 ohm, SMD | EEE-FC1V101P | Panasonic |
| 6 | C6, C7, C8, C17, C18, C19 | CAP, CERM, 6800 pF, 50 V, +/- 10%, X7R, 0402 | GRM155R71H682KA88D | MuRata |
| 8 | C9, C10, C11, C12, C13, C14, C15, C16 | CAP, CERM, 22 μ F, 25 V, +/- 10%, X6S, 1210 | GRM32EC81E226KE15L | MuRata |
| 2 | C21, C22 | CAP, CERM, 0.1 μ F, 50 V, +/- 10%, X7R, 0603 | C0603C104K5RACTU | Kemet |
| 2 | C23, C24 | CAP, CERM, 1200 pF, 100 V, +/- 5%, C0G/NP0, 0603 | GRM1885C2A122JA01D | MuRata |
| 2 | C25, C26 | CAP, CERM, 1000 pF, 100 V, +/- 5%, X7R, 0603 | 06031C102JAT2A | AVX |
| 2 | C27, C28 | CAP, CERM, 2200 pF, 50 V, +/- 5%, C0G/NP0, 0603 | GRM1885C1H222JA01D | MuRata |
| 2 | C31, C32 | CAP, CERM, 270 pF, 50 V, +/- 5%, C0G/NP0, 0603 | GRM1885C1H271JA01D | MuRata |
| 4 | C33, C36, C37, C38 | CAP, CERM, 2.2 μ F, 16 V, +/- 10%, X7R, 0603 | GRM188Z71C225KE43 | MuRata |
| 2 | C34, C39 | CAP, CERM, 4.7 μ F, 10 V, +/- 10%, X5R, 0603 | C0603C475K8PACTU | Kemet |
| 2 | C35, C40 | CAP, CERM, 0.1 μ F, 16 V, +/- 10%, X7R, 0603 | C0603C104K4RACTU | Kemet |
| 10 | C41, C44, C45, C48, C49, C52, C55, C60, C64, C68 | CAP, CERM, 47 μ F, 10 V, +/- 10%, X7R, 1210 | GRM32ER71A476KE15L | MuRata |
| 2 | C56, C76 | CAP, CERM, 330 pF, 50 V, +/- 1%, C0G/NP0, 0603 | C1608C0G1H331F080AA | TDK |
| 2 | C72, C74 | CAP, Tantalum Polymer, 470 μ F, 6.3 V, +/- 20%, 0.01 ohm, 7343-40 SMD | 6TPF470MAH | Panasonic |
| 6 | H1, H2, H3, H4, H5, H6 | MACHINE SCREW PAN PHILLIPS 6-32 | PMSSS 632 0038 PH | B&F Fastener Supply |
| 4 | H7, H8, H9, H10 | Bumpon, Cylindrical, 0.312 X 0.200, Black | SJ61A1 | 3M |
| 1 | J1 | Header (shrouded), 100mil, 5x2, Gold, TH | 5103308-1 | TE Connectivity |
| 6 | J2, J3, J7, J8, J10, J11 | Swage Threaded Standoff, Brass, Swage Mount, TH | 1546 | Keystone |
| 4 | J4, J5, J6, J9 | JUMPER TIN SMD | S1911-46R | Harwin |
| 8 | JP1, JP2, JP5, JP6 | Header, 100mil, 2x1, Tin, TH | 5-146278-2 | TE Connectivity |
| 2 | JP3, JP4 | Header, 100mil, 3x1, Tin, TH | 5-146278-3 | TE Connectivity |
| 2 | L1, L2 | Inductor, Shielded, Ferrite, 300 nH, 52 A, 0.00015 ohm, SMD | SLC1480-301MLB | Coilcraft |
| 1 | LBL1 | Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll | THT-14-423-10 | Brady |
| 1 | LED1 | LED, Green, SMD | 150060GS75000 | Würth Elektronik |
| 1 | R1 | RES, 1.00 k, 1%, 0.1 W, 0603 | CRCW06031K00FKEA | Vishay-Dale |
| 14 | R2, R3, R4, R5, R29, R30, R40, R41, R42, R43, R48, R49, R50, R51 | RES, 0, 5%, 0.1 W, 0603 | ERJ-3GEY0R00V | Panasonic |
| 2 | R6, R8 | RES, 1.10 k, 1%, 0.1 W, 0603 | RC0603FR-071K1L | Yageo America |
| 9 | R7, R10, R13, R14, R17, R18, R19, R24, R25 | RES, 10.0 k, 0.1%, 0.1 W, 0603 | RT0603BRD0710KL | Yageo America |
| 7 | R11, R15, R16, R44, R45, R46, R47 | RES, 49.9, 1%, 0.1 W, 0603 | CRCW060349R9FKEA | Vishay-Dale |
| 8 | R14, R17, R18, R19, R20, R21, R24, R25 | RES, 10.0 k, 1%, 0.1 W, 0603 | RC0603FR-0710KL | Yageo America |
| 2 | R20, R21 | RES, 5.60 k, 1%, 0.1 W, 0603 | RC0603FR-075K6L | Yageo America |
| 2 | R22, R23 | RES, 1.0, 5%, 0.25 W, 1206 | CRCW12061R00JNEA | Vishay-Dale |
| 2 | R26, R27 | RES, 5.11 k, 1%, 0.1 W, 0603 | CRCW06035K11FKEA | Vishay-Dale |
| 2 | R33, R35 | RES, 34.8 k, 1%, 0.1 W, 0603 | RC0603FR-0734K8L | Yageo America |
| 2 | R36, R37 | RES, 51.1 k, 1%, 0.1 W, 0603 | RC0603FR-0751K1L | Yageo America |
| 2 | R38, R39 | RES, 40.2 k, 1%, 0.1 W, 0603 | CRCW060340K2FKEA | Vishay-Dale |
| 6 | SH-JP1, SH-JP2, SH-JP3, SH-JP4, SH-JP5, SH-JP6 | Shunt, 100mil, Gold plated, Black | 969102-0000-DA | 3M |
| 7 | TP5, TP14, TP15, TP16, TP17, TP31, TP32 | Test Point, Miniature, Red, TH | 5000 | Keystone |

Table 8. TPS546C20AEVM2-746 Components List (continued)

| Qty | Designator | Description | Part Number | Manufacturer |
|-----|---|--|-------------|-------------------|
| 3 | TP6, TP23, TP24 | Test Point, Miniature, Black, TH | 5001 | Keystone |
| 2 | TP7, TP8 | Test Point, Miniature, Red, TH | 5000 | Keystone |
| 10 | TP9, TP10, TP25, TP26, TP43, TP19, TP20, TP40, TP41, TP42 | Test Point, Miniature, White, TH | 5002 | Keystone |
| 3 | TP11, TP12, TP27 | Test Point, Multipurpose, Black, TH | 5011 | Keystone |
| 2 | TP37, TP38 | Test Point, Miniature, Black, TH | 5001 | Keystone |
| 2 | U1, U2 | 4.5V-18V, 35A PMBUS STACKABLE SYNCHRONOUS BUCK CONVERTER, RVF0040A | TPS546C20A | Texas Instruments |

10 Screenshots

10.1 Fusion GUI Screenshots

When launching the Fusion GUI, select **IC_DEVICE_ID** in [Figure 27](#) as scanning mode to find TPS546C20A.

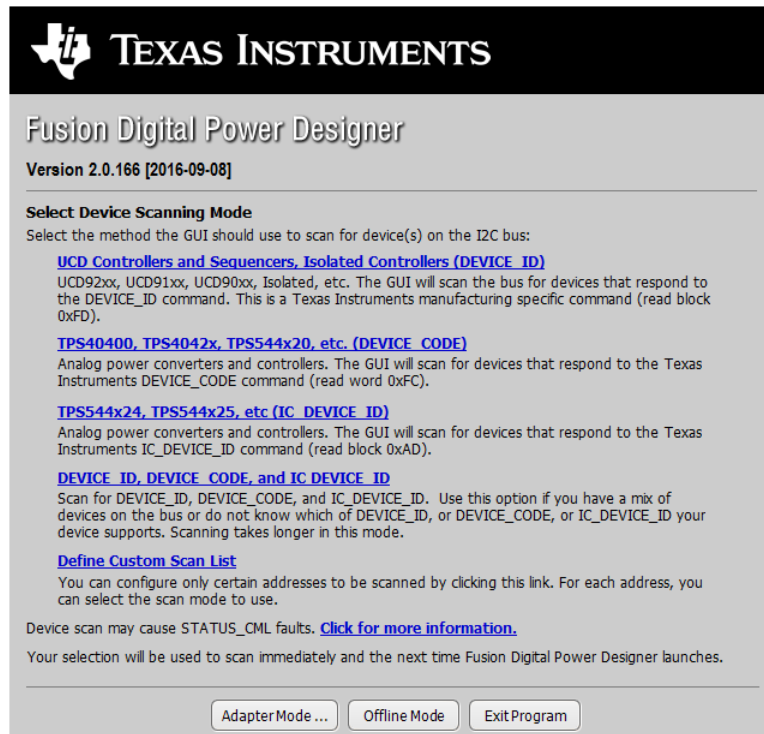


Figure 27. Select Device Scanning Mode

- Use the **Limits & On/Off** tab [Figure 28](#) to configure the following:
 - V_{ref} (Vout_Command)
 - OC Fault and OC Warn
 - OT Fault and OT Warn (Die Temperature)
 - Power Good Limits
 - Fault response
 - UVLO
 - On/Off Config
 - Soft Start time (Turn On Rise)
 - Margin voltage

After making changes to one or more configurable parameters, the changes can be committed to nonvolatile memory by clicking **Store DefaultAll**. This action prompts a **confirm selection** pop-up, and if confirmed, the changes are committed to nonvolatile memory to store all the modifications in non-volatile memory.

For modifications on V_{ref} and Soft Start time, to make the changes effective in next power up, **DIS_VSEL** in **Advanced** tab [Figure 30](#) should be checked and stored to non-volatile memory as well.

Both the loop master device and the loop slave device are tied to same bus interface, a scroll-down menu in the upper right corner can be used to switch view screens from one to the other. In two phase stacking system, most configurable parameters are disabled in GUI if the device is detected as loop slave. [Figure 33](#).

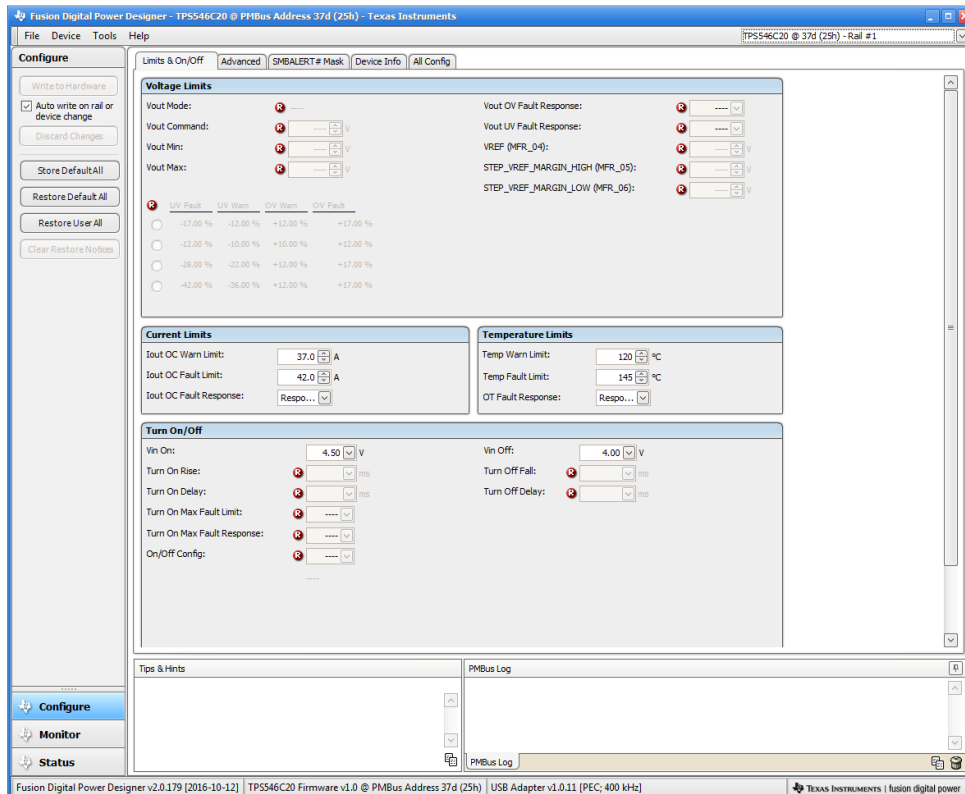
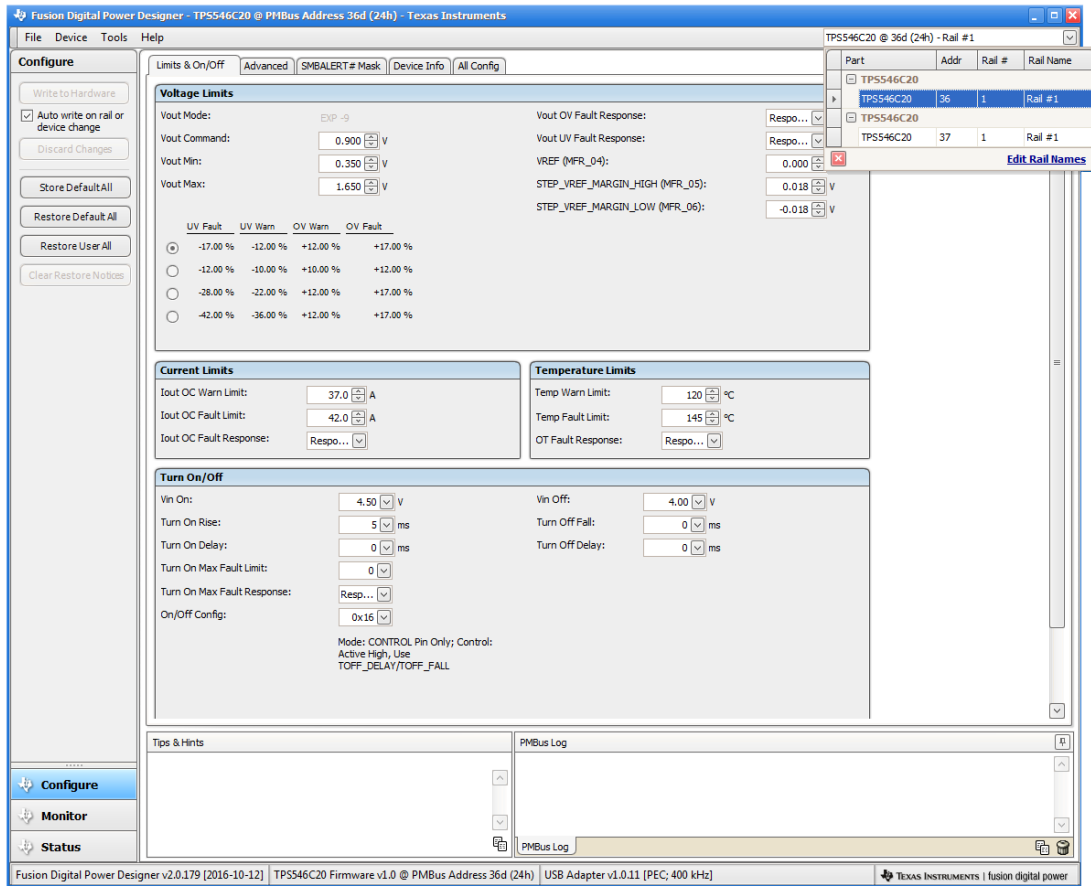


Figure 28. Configure- Limits and On/Off for U1 and U2

Changing the on/off configuration prompts a pop-up window with details of the options [Figure 29](#).

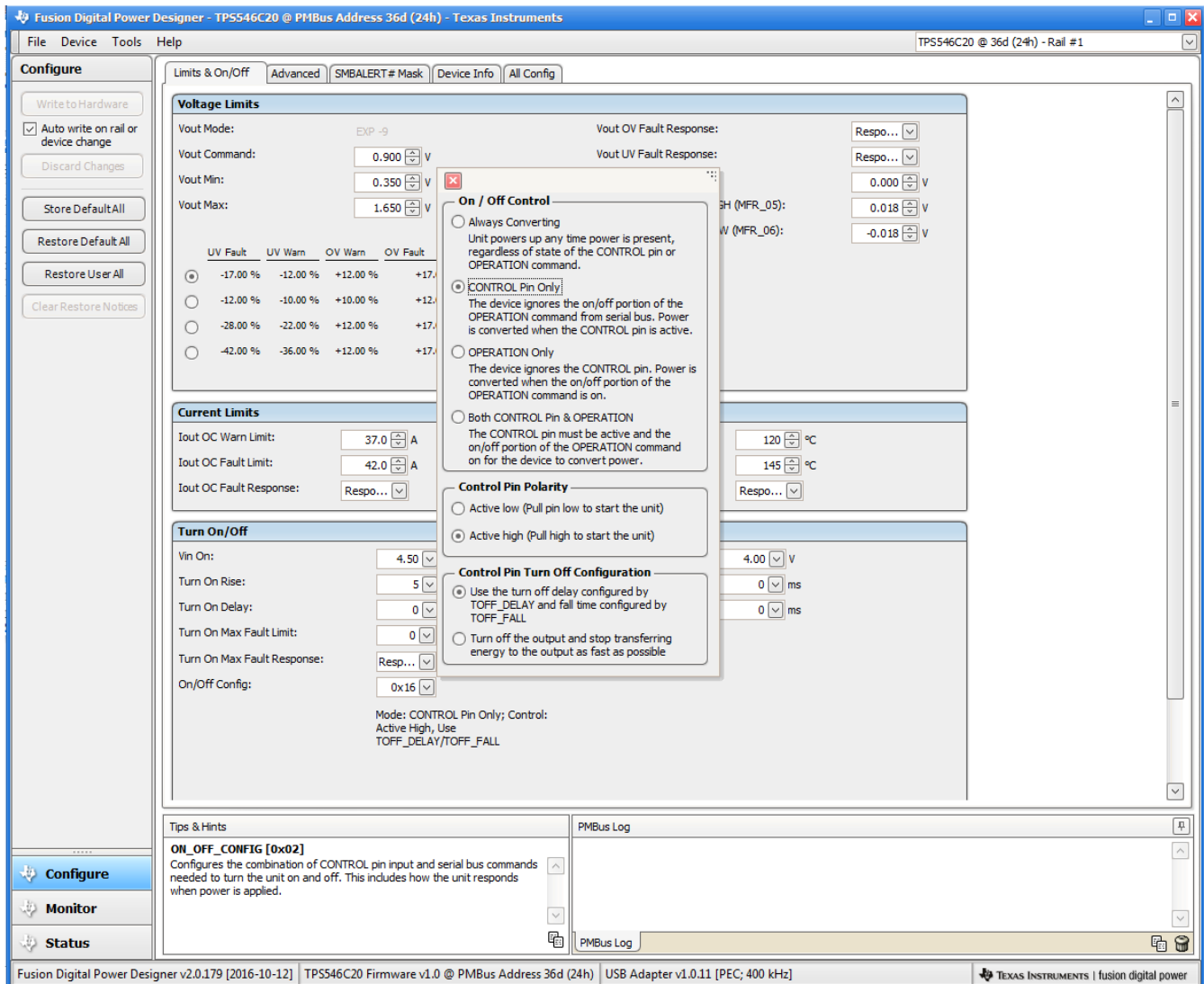


Figure 29. ON/OFF Control Pop-up

- Use the **Advanced** tab [Figure 30](#) to configure:
 - OPTIONS: MFR_SPECIFIC_21 register
 - API_OPTIONS: MFR_SPECIFIC_32 register

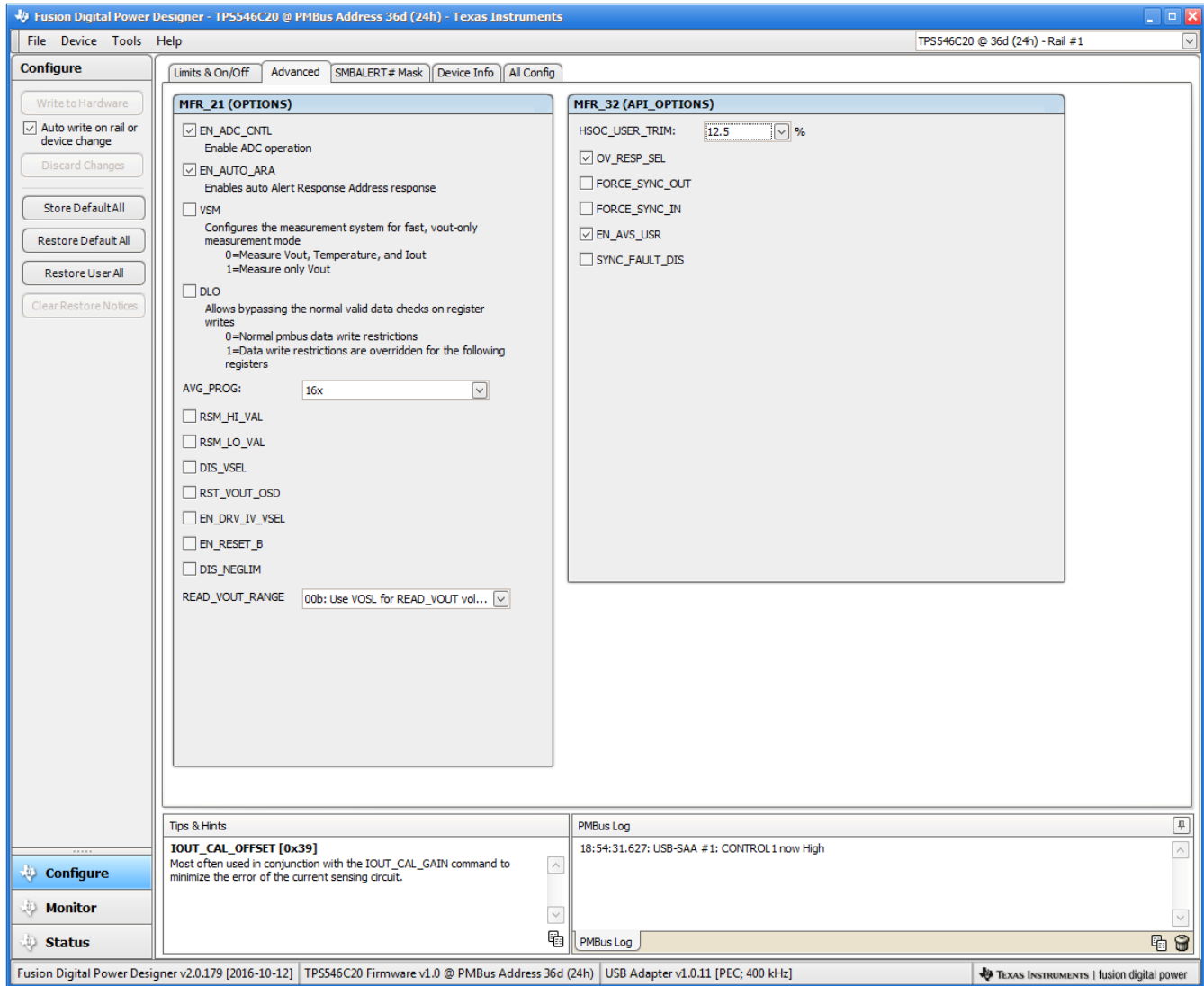


Figure 30. Configure - Advanced

The sources of SMBALERT which can be masked can be found and configured on the **SMBALERT # Mask** tab **Figure 31**

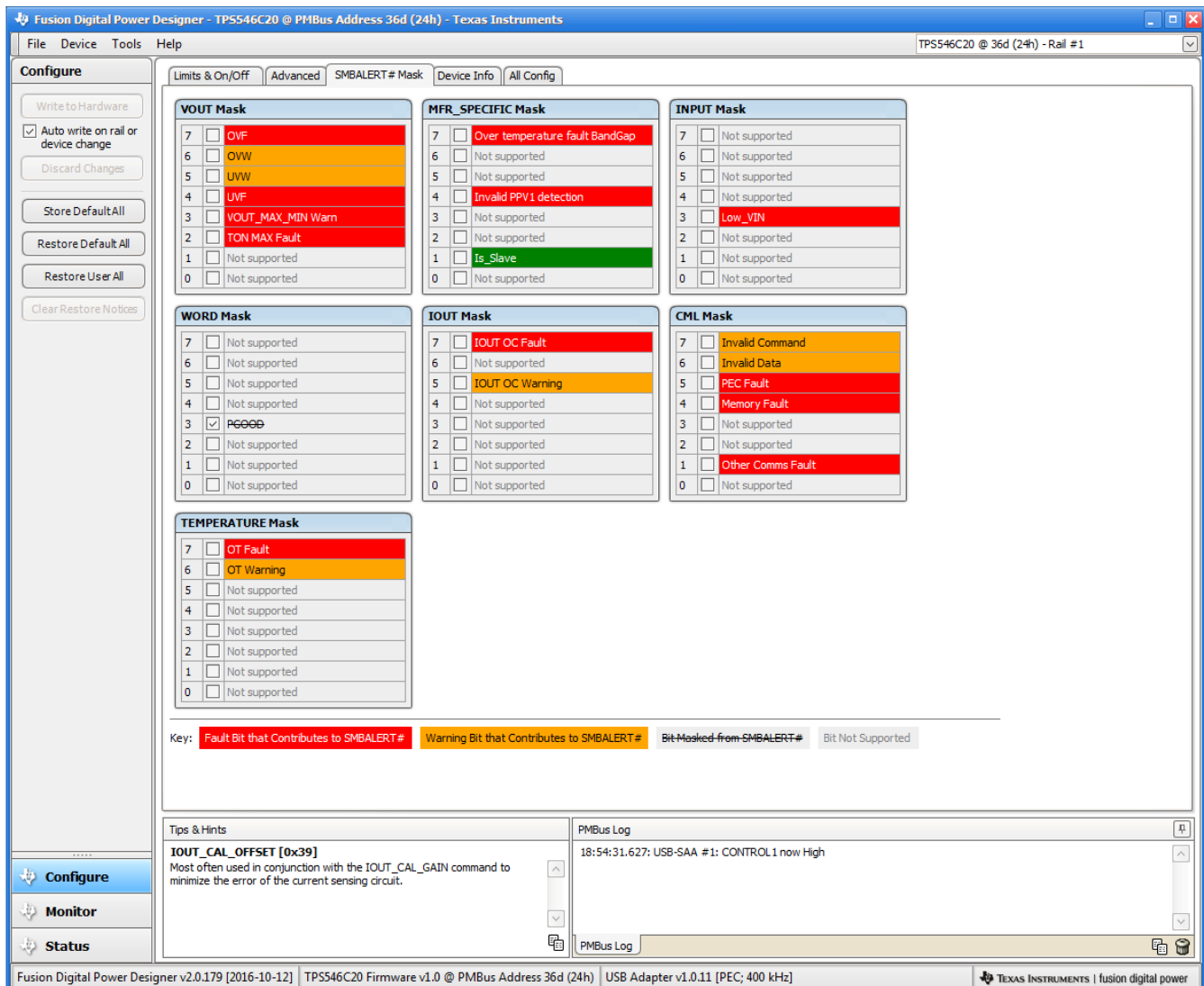


Figure 31. Configure - SMBALERT # Mask

The device information, User Scratch Pad, Write Protection options, the configuration of **Vout Scale Loop**, **Vout Transition Rate** and **Iout Cal Offset** can be found on **Device Info** tab [Figure 32](#).

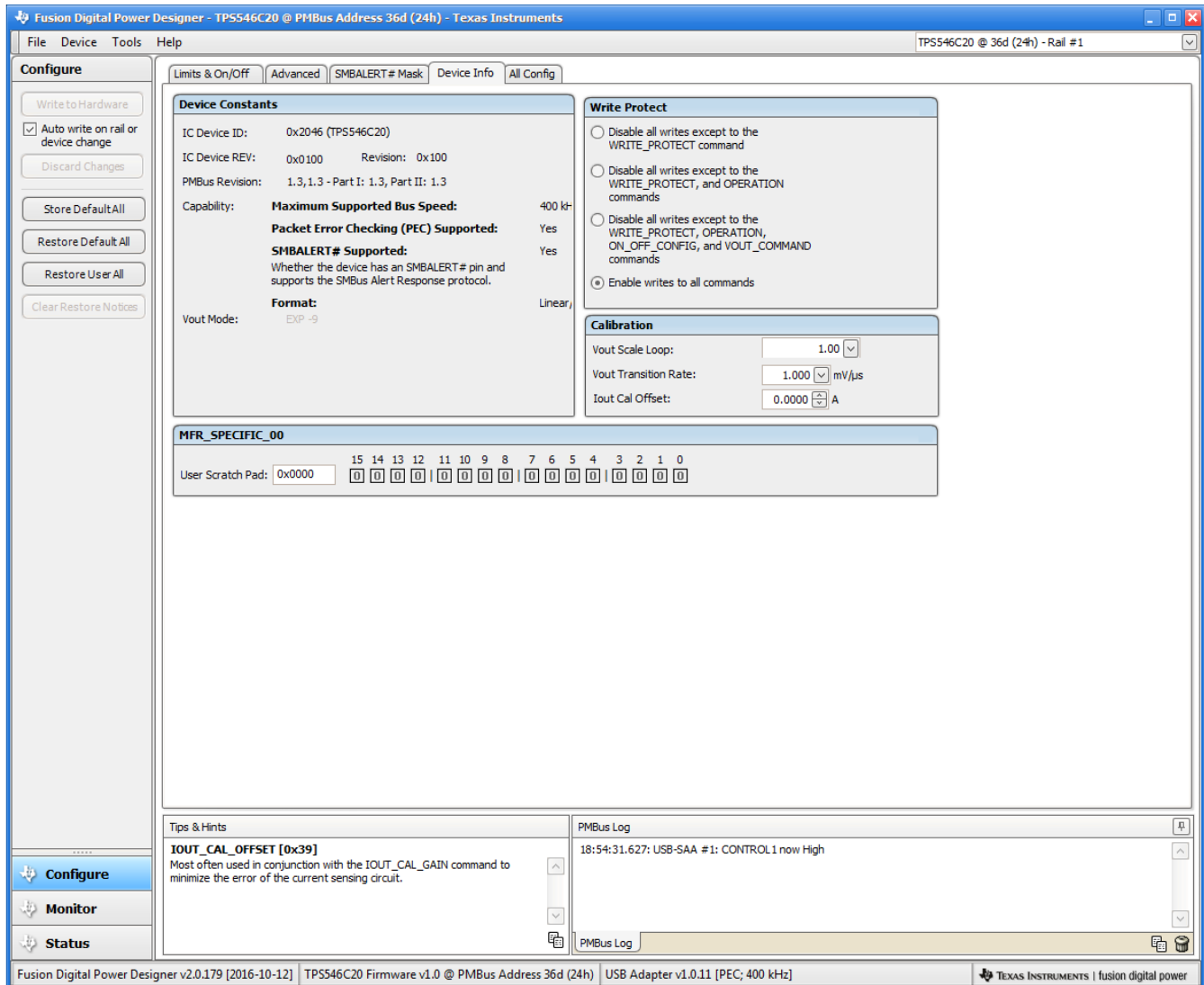


Figure 32. Configure - Device Info

Use the **All Config** tab [Figure 33](#) to configure all of the configurable parameters, which also shows other details like Hex encoding.

The screenshot shows the 'All Config' tab in the Fusion Digital Power Designer software. The interface is split into several sections:

- Left Sidebar:** Contains 'Configure', 'Monitor', and 'Status' tabs. Under 'Configure', there are buttons for 'Write to Hardware', 'Auto write on rail or device change', 'Discard Changes', 'Store Default All', 'Restore Default All', 'Restore User All', and 'Clear Restore Notices'. There are also options for 'Sort Parameters By:' (Command Name, Command Code) and a 'Group by Category' checkbox.
- Main Area:** Divided into two columns of configuration tables.

| Command | Code | Value/Edit | Hex/Edit |
|--------------------------------|------|-------------|----------|
| Calibration | | | |
| IOUT_CAL_OFFSET | 0x39 | 0.0000 A | 0xE000 |
| MFR_04 (VREF_TRIM) | 0xD4 | 0.000 V | 0x0000 |
| MFR_05 (STEP_VREF_MARGIN_HIGH) | 0xD5 | 0.018 V | 0x0009 |
| MFR_06 (STEP_VREF_MARGIN_LOW) | 0xD6 | -0.018 V | 0xFFFF |
| VOUT_SCALE_LOOP | 0x29 | 1.00 | 0xF004 |
| Configuration | | | |
| IC_DEVICE_ID | 0xAD | 0x2046 | 0x2046 |
| IC_DEVICE_REV | 0xAE | 0x0100 | 0x0100 |
| MFR_21 (OPTIONS) | 0xE5 | RSM_HI... | 0x0084 |
| MFR_32 (MISC_CONFIG_OPTIONS) | 0xF0 | OV_RES... | 0x0013 |
| SMBALERT_MASK_CML | 0x1B | 00000000 | 0x00 |
| SMBALERT_MASK_INPUT | 0x1B | 00000000 | 0x00 |
| SMBALERT_MASK_IOUT | 0x1B | 00000000 | 0x00 |
| SMBALERT_MASK_MFR_SPECIFIC | 0x1B | 00000000 | 0x00 |
| SMBALERT_MASK_TEMPERATURE | 0x1B | 00000000 | 0x00 |
| SMBALERT_MASK_VOUT | 0x1B | 00000000 | 0x00 |
| SMBALERT_MASK_WORD | 0x1B | 00001000 | 0x08 |
| VOUT_COMMAND | 0x21 | 0.900 V | 0x01CD |
| VOUT_MAX | 0x24 | 1.650 V | 0x034D |
| VOUT_MIN | 0x2B | 0.350 V | 0x00B3 |
| VOUT_MODE | 0x20 | EXP -9 | 0x17 |
| VOUT_TRANSITION_RATE | 0x27 | 1.000 mV/μs | 0xD03C |
| WRITE_PROTECT | 0x10 | 0x00 | 0x00 |

| Command | Code | Value/Edit | Hex/Edit |
|-----------------------------|------|------------|----------|
| On/Off Configuration | | | |
| ON_OFF_CONFIG | 0x02 | 0x16 | 0x16 |
| OPERATION | 0x01 | 0x00 | 0x00 |
| TOFF_DELAY | 0x64 | 0 ms | 0x0000 |
| TOFF_FALL | 0x65 | 0 ms | 0x0000 |
| TON_DELAY | 0x60 | 0 ms | 0x0000 |
| TON_MAX_FAULT_LIMIT | 0x62 | 0 ms | 0x0000 |
| TON_MAX_FAULT_RESPONSE | 0x63 | Click... | 0xBF |
| TON_RISE | 0x61 | 5 ms | 0x0005 |
| Status | | | |
| READ_IOUT | 0x8C | 5.63 A | 0xE05A |
| READ_TEMPERATURE_1 | 0x8D | 38 °C | 0x0026 |
| READ_VOUT | 0x8B | 0.902 V | 0x01CE |
| STATUS_BYTE | 0x78 | 00000000 | 0x00 |
| STATUS_CML | 0x7E | 00000000 | 0x00 |
| STATUS_INPUT | 0x7C | 00000000 | 0x00 |
| STATUS_IOUT | 0x7B | 00000000 | 0x00 |
| STATUS_MFR_SPECIFIC | 0x80 | 00000000 | 0x00 |
| STATUS_TEMPERATURE | 0x7D | 00000000 | 0x00 |
| STATUS_VOUT | 0x7A | 00000000 | 0x00 |
| STATUS_WORD | 0x79 | Click... | 0x0000 |
| User Parameters | | | |
| MFR_00 (FOR USER) | 0xD0 | 0x0000 | 0x0000 |
- Bottom Left:** 'Tips & Hints' section for 'OPERATION [0x01]' with a description: 'Used to turn the unit on and off in conjunction with the input from the CONTROL pin. It is also used to cause the unit to set the output voltage to the upper or lower margin voltages. The unit stays in the commanded operating mode until a subsequent OPERATION command or change in the state of the CONTROL pin instructs the device to change to another mode.'
- Bottom Right:** 'PMBus Log' section showing a log entry: '18:54:31.627: USB-SAA #1: CONTROL 1 now High'.
- Bottom Status Bar:** Displays 'Fusion Digital Power Designer v2.0.179 [2016-10-12] TPS546C20 Firmware v1.0 @ PMBus Address 36d (24h) USB Adapter v1.0.11 [PEC; 400 kHz] TEXAS INSTRUMENTS | fusion digital power'.

Figure 33. Configure - All Config

When the *Monitor* screen [Figure 34](#) is selected, the screen changes to display real-time data of the parameters that are measured by the device. This screen provides access to:

- Graphs of V_{OUT} , I_{out} , *Temperature*, and *Pout*.
- *Start/Stop Polling* which turns ON or OFF the real-time display of data.
- Quick access to On/Off config
- Control pin activation, and OPERATION command.
- Margin control.
- Clear Fault. Selecting **Clear Faults** clears any prior fault flags.

With two devices stacked together, the **IOUT** reading from either the loop master or the loop slave device is the load current supported by the device itself, thus the **Iout** reading is half of the total load.

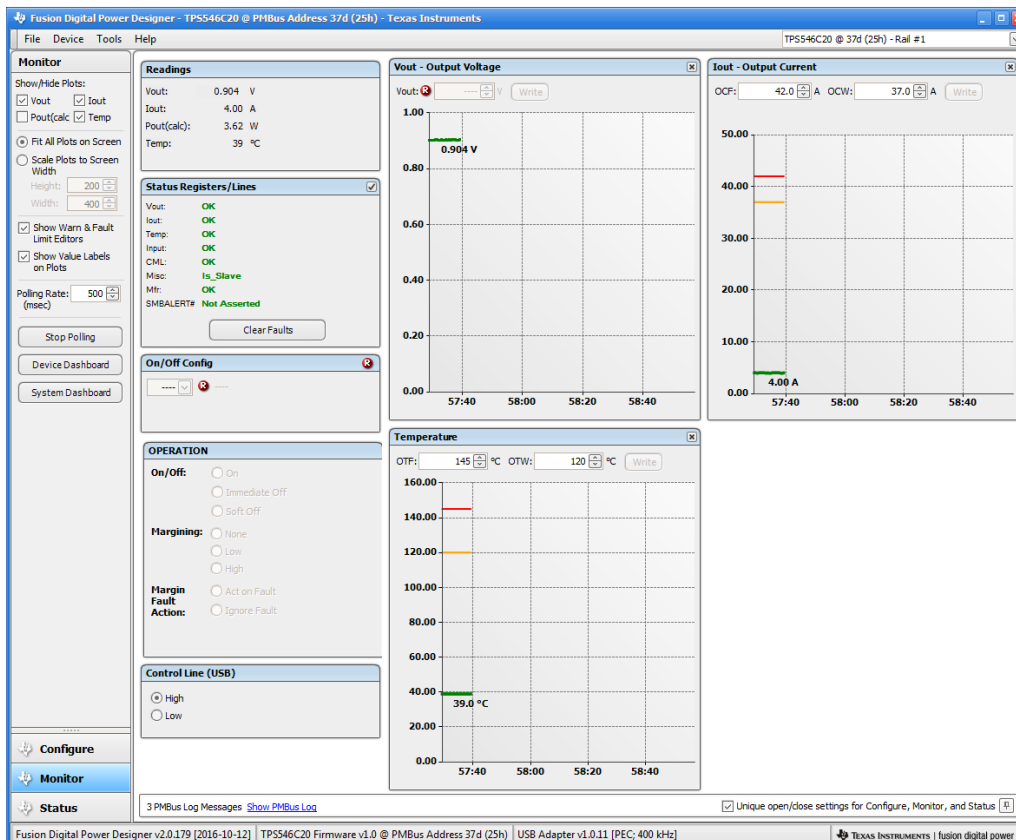
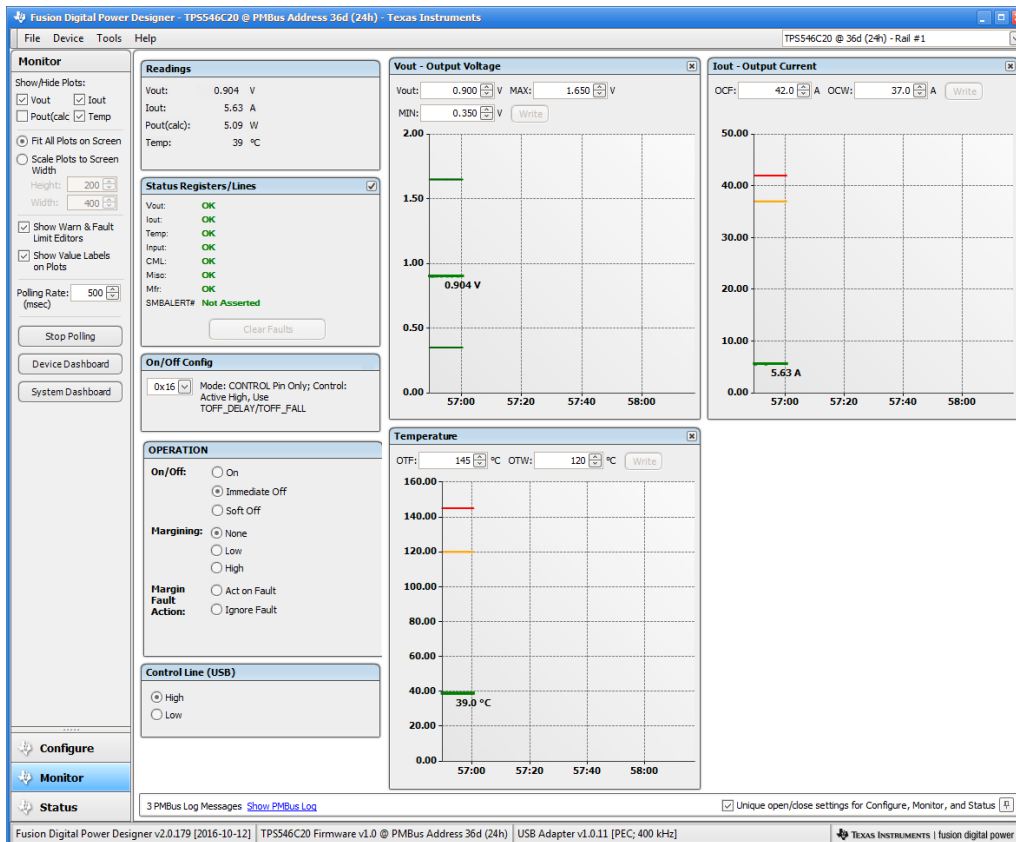


Figure 34. Monitor Screen with 10A total load

Selecting *Status* screen **Figure 35** from lower left corner shows the status of the device .

The figure shows two screenshots of the Fusion Digital Power Designer software interface, specifically the Status screen. The top screenshot shows the status for PMBus Address 36d (24h), and the bottom screenshot shows the status for PMBus Address 37d (25h). Both screenshots display a grid of status registers with their bit values and descriptions. The registers are organized into several categories: STATUS_VOUT, STATUS_IOUT, STATUS_TEMP, STATUS_WORD, STATUS_CML, STATUS_INPUT, STATUS_FANS_1_2, STATUS_FANS_3_4, STATUS_MFR_SPECIFIC, and STATUS_OTHER. A legend at the bottom of each screen indicates the color coding for Fault (red), Warning (yellow), and other states. The bottom screenshot shows the 'Is_Slave' bit in the STATUS_MFR_SPECIFIC register highlighted in green.

STATUS_VOUT

| | | |
|---|-------------------|-----|
| 7 | OVF | 0x1 |
| 6 | OVW | 0x1 |
| 5 | UVW | 0x1 |
| 4 | UVF | 0x1 |
| 3 | VOUT_MAX_MIN Warn | 0x1 |
| 2 | TON MAX Fault | 0x1 |
| 1 | 0 | 0x1 |
| 0 | 0 | 0x1 |

STATUS_IOUT

| | | |
|---|--------------------------------|-----|
| 7 | IOUT OC Fault | 0x1 |
| 6 | IOUT OC Fault with LV Shutdown | 0x1 |
| 5 | IOUT OC Warning | 0x1 |
| 4 | IOUT UC Fault | 0x1 |
| 3 | Current Share Fault | 0x1 |
| 2 | Power Limiting Mode | 0x1 |
| 1 | POUT OP Fault | 0x1 |
| 0 | POUT OP Warning | 0x1 |

STATUS_TEMP

| | | |
|---|------------|-----|
| 7 | OT Fault | 0x1 |
| 6 | OT Warning | 0x1 |
| 5 | UT Fault | 0x1 |
| 4 | UT Warning | 0x1 |
| 3 | Reserved | 0x1 |
| 2 | Reserved | 0x1 |
| 1 | Reserved | 0x1 |
| 0 | Reserved | 0x1 |

STATUS_WORD

| | | |
|----|------------------|-----|
| 15 | VFW | 0x1 |
| 14 | OCFW | 0x1 |
| 13 | INPUT | 0x1 |
| 12 | MFR fault/warn | 0x1 |
| 11 | PGOOD_Z | 0x1 |
| 10 | FANS | 0x1 |
| 9 | OTHER | 0x1 |
| 8 | Unknown | 0x1 |
| 7 | Busy | 0x1 |
| 6 | OFF | 0x1 |
| 5 | OVF | 0x1 |
| 4 | OCF | 0x1 |
| 3 | Vout_MAX_Warning | 0x1 |
| 2 | OTWF | 0x1 |
| 1 | CHL | 0x1 |
| 0 | OTH | 0x1 |

STATUS_CML

| | | |
|---|--------------------------|-----|
| 7 | Invalid Command | 0x1 |
| 6 | Invalid Data | 0x1 |
| 5 | PEC Fault | 0x1 |
| 4 | Memory Fault | 0x1 |
| 3 | Processor Fault | 0x1 |
| 2 | Reserved | 0x1 |
| 1 | Other Comms Fault | 0x1 |
| 0 | Other Memory/Logic Fault | 0x1 |

STATUS_INPUT

| | | |
|---|----------------|-----|
| 7 | Vin OV Fault | 0x1 |
| 6 | Vin OV Warning | 0x1 |
| 5 | Vin UV Warning | 0x1 |
| 4 | Vin UV Fault | 0x1 |
| 3 | Low_VIN | 0x1 |
| 2 | IIN OC Fault | 0x1 |
| 1 | IIN OC Warning | 0x1 |
| 0 | PIN OP Warning | 0x1 |

STATUS_FANS_1_2

| | | |
|---|------------------------|-----|
| 7 | Fan 1 Fault | 0x1 |
| 6 | Fan 2 Fault | 0x1 |
| 5 | Fan 1 Warning | 0x1 |
| 4 | Fan 2 Warning | 0x1 |
| 3 | Fan 1 Speed Overridden | 0x1 |
| 2 | Fan 2 Speed Overridden | 0x1 |
| 1 | Air Flow Fault | 0x1 |
| 0 | Air Flow Warning | 0x1 |

STATUS_FANS_3_4

| | | |
|---|------------------------|-----|
| 7 | Fan 3 Fault | 0x1 |
| 6 | Fan 4 Fault | 0x1 |
| 5 | Fan 3 Warning | 0x1 |
| 4 | Fan 4 Warning | 0x1 |
| 3 | Fan 3 Speed Overridden | 0x1 |
| 2 | Fan 4 Speed Overridden | 0x1 |
| 1 | Reserved | 0x1 |
| 0 | Reserved | 0x1 |

STATUS_MFR_SPECIFIC

| | | |
|---|-----------------------------|-----|
| 7 | Over temperature fault Band | 0x1 |
| 6 | FSH Illegal ZERO state | 0x1 |
| 5 | FSH Illegal MANY ONES state | 0x1 |
| 4 | Invalid PPV1 detection | 0x1 |
| 3 | Invalid PPV0 detection | 0x1 |
| 2 | RESET VOUT | 0x1 |
| 1 | Is_Slave | 0x1 |
| 0 | SYNC_FAULT | 0x1 |

STATUS_OTHER

| | | |
|---|---------------------------------------|-----|
| 7 | Reserved | 0x1 |
| 6 | Reserved | 0x1 |
| 5 | Input A fuse Or circuit breaker fault | 0x1 |
| 4 | Input B fuse or circuit breaker fault | 0x1 |
| 3 | Input A OR-ing device fault | 0x1 |
| 2 | Input B OR-ing device fault | 0x1 |
| 1 | Output OR-ing device fault | 0x1 |
| 0 | Reserved | 0x1 |

Legend: Key: Fault (red), Warning (yellow), See other register (blue), Bit not set (grey), Bit not implemented (grey).

Figure 35. Status Screen

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