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Evaluating the ADE7878 Energy Metering IC

FEATURES

- **Evaluation board designed to be used with accompanying software to implement a fully functional 3-phase energy meter**
- **Easy connection of external transducers via screw terminals**
- **Easy modification of signal conditioning components using PCB sockets**
- **LED indicators on the CF1, CF2, CF3, IRQ0, and IRQ1 logic outputs**
- **Optically isolated metering components and USB-based communication with a PC**
- **External voltage reference option available for on-chip reference evaluation**
- **PC COM port-based firmware updates**

GENERAL DESCRIPTION

The ADE7878 is a high accuracy, 3-phase electrical energy measurement IC with serial interfaces and three flexible pulse outputs. The ADE7878 incorporates seven ADCs, reference circuitry, and all signal processing required to perform total (fundamental and harmonic) active, reactive, and apparent energy measurement, fundamental active and reactive energy measurement, and rms calculations.

This user guide describes the ADE7878 evaluation kit hardware, firmware, and software functionality. The evaluation board contains an ADE7878 and a LPC2368 microcontroller (from NXP Semiconductors). The ADE7878 and its associated metering components are optically isolated from the microcontroller. The microcontroller communicates with the PC using a USB interface. Firmware updates can be loaded using one PC com port and a regular serial cable.

The ADE7878 evaluation board and this user guide, together with the ADE7878 data sheet, provide a complete evaluation platform for the ADE7878.

The evaluation board has been designed so that the ADE7878 can be evaluated in an energy meter. Using appropriate current transducers, the evaluation board can be connected to a test bench or high voltage (240 V rms) test circuit. On-board resistor divider networks provide the attenuation for the line voltages. This user guide describes how the current transducers should be connected for the best performance. The evaluation board requires two external 3.3 V power supplies and the appropriate current transducers.

EVALUATION BOARD CONNECTION DIAGRAM

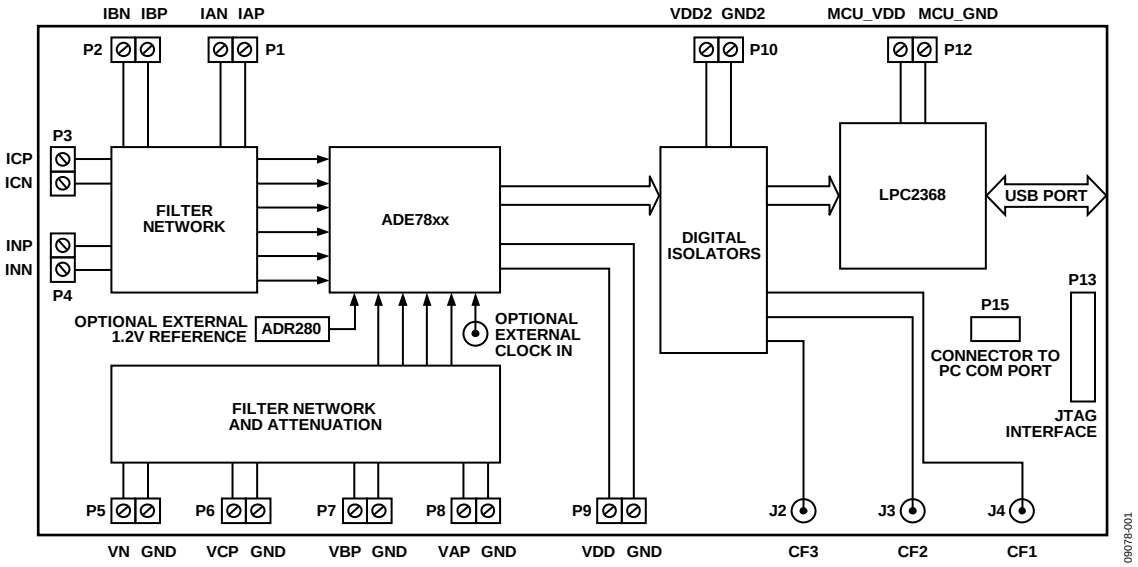

Figure 1.

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REVISION HISTORY

8/10—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The evaluation board has three power domains: one that supplies the microcontroller and one side of the isocouplers, one that supplies the other side of the optocouplers, and one that supplies the ADE7878. The ground of the microcontroller's power domain is connected to the ground of the PC through the USB cable. The ground of the ADE7878 power domain is determined by the ground of the phase voltages, VAP, VBP, VCP, and VN, and must be different from the ground of the microcontroller's power domain.

The microcontroller 3.3 V supply is provided at the P12 connector. The ADE7878 3.3 V supply is provided at the P9 connector. Close jumper JP2 to ensure that the same 3.3 V supply from ADE7878 is also provided at the isocouplers.

ANALOG INPUTS (P1 TO P4 AND P5 TO P8)

Current and voltage signals are connected at the screw terminal, P1 to P4 and P5 to P8, respectively. All analog input signals are filtered using the on-board antialiasing filters before the signals are connected to the ADE7878. The components used on the board are the recommended values to be used with the ADE7878.

Current Sense Inputs (P1, P2, P3, and P4)

The ADE7878 measures three phase currents and the neutral current. Current transformers or Rogowski coils can be used to sense the current but should not be mixed together. The ADE7878 contains different internal PGA gains on phase currents and on the neutral current; therefore, sensors with different ratios can be used. The only requirement is to have the same scale signals at the PGA outputs; otherwise, the mismatch functionality of the ADE7878 is compromised (see the ADE7878 data sheet for more details about neutral current mismatch). Figure 2 shows the structure used for the Phase A current; the sensor outputs are connected to the P1 connector.

The R1 and R2 resistors are the burden resistors and, by default, they are not populated. They can also be disabled using the JP1A and JP2A jumpers. The R9/C9 and R10/C10 RC networks are used in conjunction with Rogowski coils. They can be disabled using the JP3A and JP4A jumpers. The R17/C17 and R18/C18 RC networks are the antialiasing filters. The default corner frequency of these low pass filters is 7.2 kHz (1 kΩ/22 nF). These filters can easily be adjusted by replacing the components on the evaluation board.

All the other current channels (that is, Phase B, Phase C, and the neutral current) have a similar input structure.

Using a Current Transformer as the Current Sensor

Figure 3 shows how a current transformer can be used as a current sensor in one phase of a 3-phase, 4-wire distribution system (Phase A). The other two phases and the neutral current require similar connections.

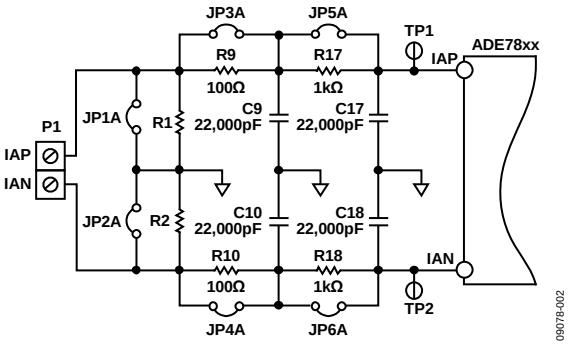


Figure 2. Phase A Current Input Structure on the Evaluation Board

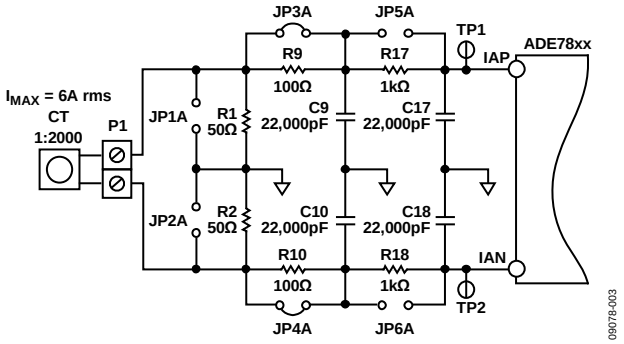


Figure 3. Example of a Current Transformer Connection

The R1 and R2 burden resistors must be defined as functions of the current transformer ratio and maximum current of the system, using the following formula:

$$R1 = R2 = 1/2 \times 0.5/sqrt(2) \times N/I_{FS}$$

where:
$0.5/sqrt(2)$ is the rms value of the full-scale voltage accepted at the ADC input.
N is the input-to-output ratio of the current transformer.
I_{FS} is the maximum rms current to be measured.

The JP1A and JP2A jumpers should be opened if R1 and R2 are used. The antialiasing filters should be enabled by opening the J5A and J6A jumpers (see Figure 3).

The secondary current of the transformer is converted to a voltage by using a burden resistor across the secondary winding outputs. Care should be taken when using a current transformer as the current sensor. If the secondary is left open (that is, no burden is connected), a large voltage may be present at the secondary outputs. This can cause an electric shock hazard and potentially damage electronic components.

Most current transformers introduce a phase shift that the manufacturer indicates in the data sheet. This phase shift can lead to significant energy measurement errors, especially at low power factors. The ADE7878 can correct the phase error using the APHCAL[9:0], BPHCAL[9:0], and CPHCAL[9:0] phase calibration registers as long as the error stays between −6.732° and +1.107° at 50 Hz (see the ADE7878 data sheet for more

details). The software supplied with the ADE7878 evaluation board allows user adjustment of phase calibration registers.

For this particular example, burden resistors of 50 Ω signify an input current of 7.05 A rms at the ADE7878 ADC full-scale input (0.5 V). In addition, the PGA gains for the current channel must be set at 1. For more information about setting PGA gains, see the ADE7878 data sheet. The evaluation software allows the user to configure the current channel gain.

Using a Rogowski Coil as the Current Sensor

Figure 4 shows how a Rogowski coil can be used as a current sensor in one phase of a 3-phase, 4-wire distribution system (Phase A). The other two phases and the neutral current require similar connections. The Rogowski coil does not require any burden resistors; therefore, R1 and R2 should not be populated. The antialiasing filters should be enabled by opening the J5A and J6A jumpers. To account for the high frequency noise introduced by the coil, an additional antialiasing filter must be introduced by opening the JP3A and JP4A jumpers. Then, to compensate for the 20 dB/dec gain introduced by the di/dt sensor, the integrator of the ADE7878 must be enabled by setting Bit 0 (INTEN) of the CONFIG register. The integrator has a −20 dB/dec attenuation and an approximately −90° phase shift and, when combined with the di/dt sensor, results in a magnitude and phase response with a flat gain over the frequency band of interest.

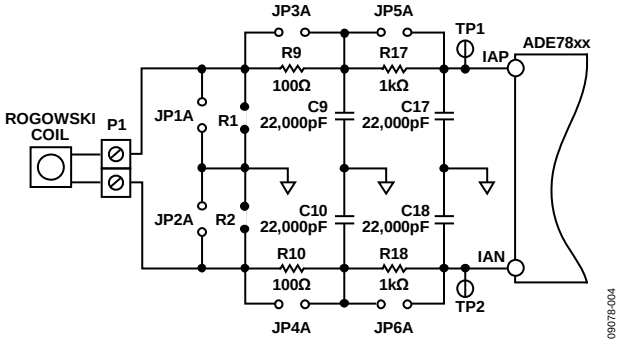


Figure 4. Example of a Rogowski Coil Connection

Voltage Sense Inputs (P5, P6, P7, and P8 Connectors)

The voltage input connections on the ADE7878 evaluation board can be directly connected to the line voltage sources. The line voltages are attenuated using a simple resistor divider network before they are supplied to the ADE7878. The attenuation network on the voltage channels is designed so that the corner frequency (3 dB frequency) of the network matches that of the antialiasing filters in the current channel inputs. This prevents the occurrence of large energy errors at low power factors.

Figure 5 shows a typical connection of the Phase A voltage inputs; the resistor divider is enabled by opening the JP7A jumper. The antialiasing filter on the VN data path is enabled by opening the JP7N jumper. JP8A and JP8N are also opened. The VN analog input is connected to AGND via the R25/C25 antialiasing filter using the JP8N connector.

The attenuation networks can be easily modified by the user to accommodate any input level. However, the value of R32 (1 kΩ), should be modified only together with the corresponding resistors in the current channel (R17 and R18 on the Phase A current data path).

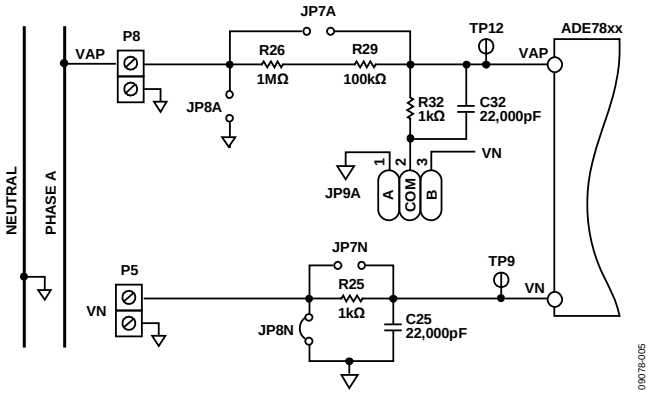


Figure 5. Phase A Voltage Input Structure on the Evaluation Board

The maximum signal level permissible at the VAP, VBP, and VCP pins of the ADE7878 is 0.5 V peak. Although the ADE7878 analog inputs can withstand ±2 V without risk of permanent damage, the signal range should not exceed ±0.5 V with respect to AGND for a specified operation.

Table 1. Recommended Settings for Evaluation Board Connectors

Jumper	Option	Description
JP1	Soldered	Connects AGND to ground. By default, it is soldered.
JP1A, JP1B, JP1C, JP1N,	Open	Connect IAP, IBP, IC, and INP to AGND. By default, they are open.
JP2	Closed	Connects the ADE7878 VDD power supply (VDD_F at the P9 connector) to the power supply of the isocouplers (VDD2 at the P10 connector). By default, it is closed.
JP2A, JP2B, JP2C, JP2N	Open	Connect IAN, IBN, ICN, and INN to AGND. By default, they are open.
JP3	Unsoldered	Connects the pad metal below the ADE7878 to AGND. By default, it is unsoldered.
JP3A, JP3B, JP3C, JP3N	Closed	Disable the phase compensation network in the IAP, IBP, ICP, and INP data path. By default, they are closed.
JP4	Soldered	Connects C3 to DVDD. By default, it is soldered.
JP4A, JP4B, JP4C, JP4N	Closed	Disable the phase compensation network in the IAN, IBN, ICN, and INN data path. By default, they are closed.
JP5	Soldered	Connects C5 to AVDD. By default, it is soldered.
JP5A, JP5B, JP5C, JP5N	Open	Disable the phase antialiasing filter in the IAP, IBP, ICP, and INP data path. By default, they are open.
JP6	Soldered	Connects C41 to the REF pin of the ADE7878. By default, it is soldered.
JP6A, JP6B, JP6C, JP6N	Open	Disable the phase antialiasing filter in the IAN, IBN, ICN, and INN data path. By default, they are open.
JP7	Closed	Enables the supply to the microcontroller. When open, takes out the supply to the microcontroller. By default, it is closed.
JP7A, JP7B, JP7C	Open	Disable the resistor divider in the VAP, VBP, and VCP data path. By default, they are open.
JP7N	Open	Disables the antialiasing filter in the VN data path. By default, it is open.
JP8	Open	Sets the microcontroller in flash memory programming mode. By default, it is open.
JP8A, JP8B, JP8C	Open	Connect VAP, VBP, and VCP to AGND. By default, they are open.
JP8N	Closed	Connects VN to AGND. By default, it is closed.
JP9	Open	When closed, signals the microcontroller to declare all I/O pins as outputs. It is used when another microcontroller is used to manage the ADE7878 through the P38 socket. By default, it is open.
JP9A, JP9B, JP9C	Soldered to Pin 1 (AGND)	Connect the ground of antialiasing filters in the VAP, VB, and VCP data path to AGND or VN. By default, they are soldered to AGND.
JP10	Open	Connects the external voltage reference to ADE7878. By default, it is open.
JP11	Soldered to Pin 1	Connects the CLKIN pin of the ADE7878 to a 16,384 MHz crystal (Pin 1 of JP11) or to an external clock input provided at J1. By default, it is soldered to Pin 1.
JP12	Soldered to Pin 3 (AGND)	Connects DGND (Pin 2 of JP12) of the ADE7878 to ground (Pin 1 of JP12) or to AGND (Pin 3 of JP12).
JP35, JP33	Open	If I^2C communication between the NXP LPC2368 and the ADE7878 is used, these connectors should be closed with 0 Ω resistors, and the JP36 and JP34 connectors should be opened. By default, the SPI is the communication used between the NXP LPC2368 and the ADE7878; therefore, these connectors are open.
JP31, JP37	Open	If HSDC communication is used, these connectors should be closed with 0 Ω resistors, and the JP35 and JP33 connectors should also be closed. By default, the SPI is the communication used between the NXP LPC2368 and the ADE7878; therefore, these connectors are open.
JP36, JP34, JP32, JP38	Closed with 0 Ω resistors	If SPI communication is used between the NXP LPC2368 and the ADE7878, these connectors should be closed and JP35, JP33, JP31, and JP37 should be opened. By default, the SPI is the communication used between the NXP LPC2368 and the ADE7878; therefore, these connectors are closed.

SETTING UP THE EVALUATION BOARD AS AN ENERGY METER

Figure 6 shows a typical setup for the ADE7878 evaluation board. In this example, an energy meter for a 4-wire, 3-phase distribution system is shown. Current transformers are used to sense the phase and neutral currents and are connected as shown in Figure 6. The line voltages are connected directly to the evaluation board as shown. Note that the state of all jumpers must match the states shown in Figure 6, keeping in mind that the board is supplied from two different 3.3 V power supplies, one for the ADE7878 domain, VDD, and one for the NXP LPC2368 domain, MCU_VDD. Because the two domains are isolated to ensure that there is no electrical connection between the high voltage test circuit and the control circuit, the power supplies should have floating voltage outputs.

The evaluation board is connected to the PC using a regular USB cable supplied with the board. When the evaluation board is powered up and connected to the PC, the enumeration process begins and the PC recognizes new hardware and asks to install the appropriate driver. The drive can be found in the VirCOM_Driver_XP folder of the CD. After the driver is installed, the supplied evaluation software can be launched. The next section describes the ADE7878 evaluation software in detail and how it can be installed and uninstalled.

Activating Serial Communication Between the ADE7878 and the NXP LPC2368

The ADE7878 evaluation board is supplied with communication between the ADE7878 and the NXP LPC2368 that is set through the SPI ports. The JP32, JP34, JP36, and JP38 jumpers are closed using 0 Ω resistors, and the JP31, JP33, JP35, and JP37 jumpers are open. The SPI port should be chosen as the active port in the ADE7878 control panel.

Communication between the ADE7878 and the NXP LPC2368 is also possible using the I²C ports. To accomplish this, the JP31, JP33, JP35, and JP37 jumpers should be closed using 0 Ω resistors, and the JP32, JP34, JP36, and JP38 jumpers should be open. In this case, the I²C port should be chosen as the active port in the ADE7878 control panel (see Table 2).

Table 2. Jumper State to Activate SPI or I²C Communication

Active Communication	Jumpers Closed with 0 Ω Resistors	Jumpers Open
SPI (Default)	JP32, JP34, JP36, JP38	JP31, JP33, JP35, JP37
I²C	JP31, JP33, JP35, JP37	JP32, JP34, JP36, JP38

Using the Evaluation Board with Another Microcontroller

It is possible to manage the ADE7878 mounted on the evaluation board with a different microcontroller mounted on another board. The ADE7878 can be connected to this second board through one of two connectors: P11 or P38. P11 is placed on the same power domain as the ADE7878. P38 is placed on the power domain of the NXP LPC2368 and communicates with the ADE7878 through the isocouplers. If P11 is used, the power domain of the NXP LPC2368 should not be supplied at P12. If P38 is used, a conflict may arise with the NXP LPC2368 I/O ports. The following two options are provided to deal with this situation:

- One option is to keep the NXP LPC2368 running and close JP9. This tells the NXP LPC2368 to set all of its I/Os high to allow the other microcontroller to communicate with the ADE7878. After JP9 is closed, the S2 reset button should be pressed low to force the NXP LPC2368 to reset. This is necessary because the state of JP9 is checked inside the NXP LPC2368 program only once after reset.
- The other option is to cut the power supply of the NXP LPC2368 by disconnecting JP7.

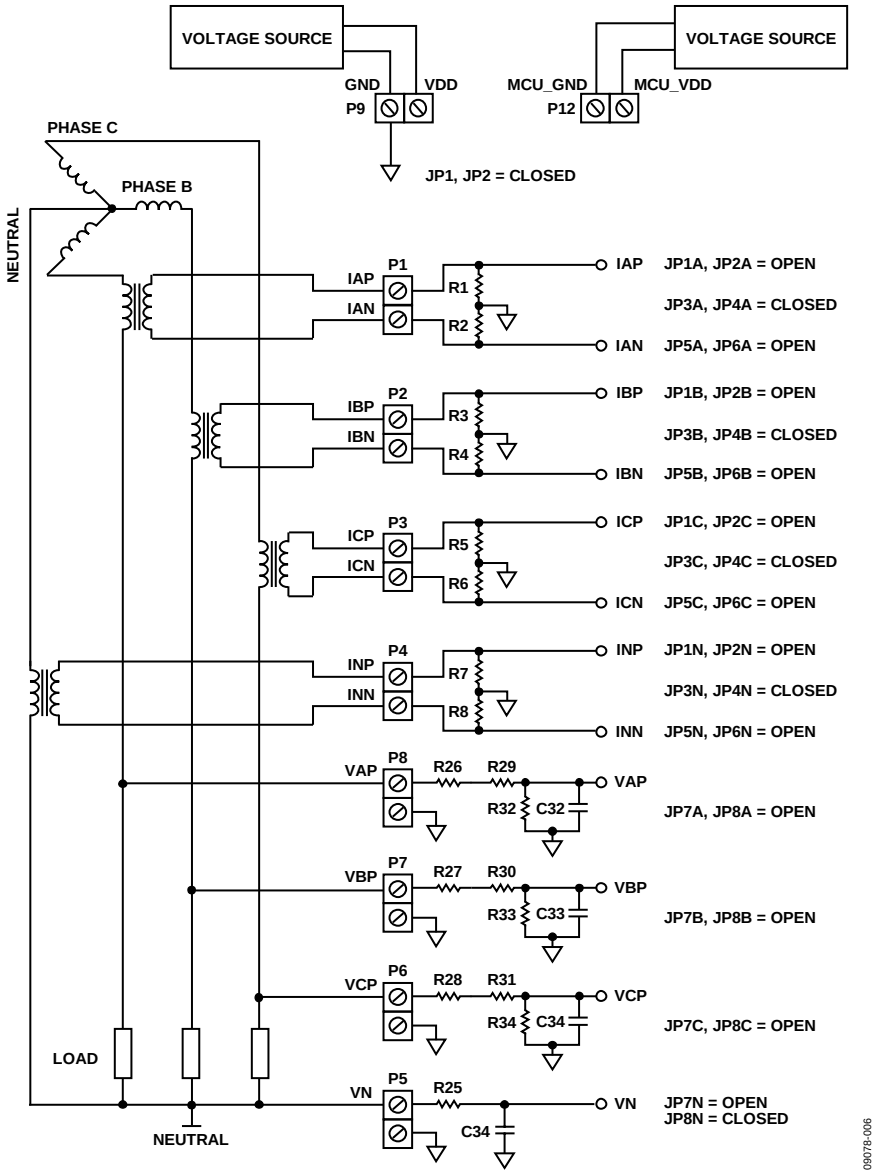


Figure 6. Typical Setup for the ADE7878 Evaluation Board

EVALUATION BOARD SOFTWARE

The ADE7878 evaluation board is supported by Windows® based software that allows the user to access all the functionality of the ADE7878. The software communicates with the NXP LPC2368 microcontroller using the USB as a virtual COM port. The NXP LPC2368 communicates with the ADE7878 to process the requests that are sent from the PC.

INSTALLING AND UNINSTALLING THE ADE7878 SOFTWARE

The ADE7878 software is supplied on one CD-ROM. It contains two projects: one that represents the NXP LPC2368 project and one LabVIEW™ based program that runs on the PC. The NXP LPC2368 project is already loaded into the processor, but the LabVIEW based program must be installed.

1. To install the ADE7878 software, place the CD-ROM in the CD-ROM reader and double-click **LabView_project\installation_files\setup.exe**. This launches the setup program that automatically installs all the software components, including the uninstall program, and creates the required directories.
2. To launch the software, go to the **Start/Programs/ ADE7878 Eval Software** menu and click **ADE7878 Eval Software**.

Both the ADE7878 evaluation software program and the NI run-time engine are easily uninstalled by using the **Add/ Remove Programs** option in the control panel.

1. Before installing a new version of the ADE7878 evaluation software, first uninstall the previous version.
2. Select the **Add/Remove Programs** option in the Windows control panel.
3. Select the program to uninstall and click the **Add/Remove** button.

FRONT PANEL

When the software is launched, the **Front Panel** is opened. This panel contains three areas: the main menu at the left, the sub-menu at the right, and a box that displays the name of the communication port used by the PC to connect to the evaluation port, also at the right (see Figure 7).

The COM port used to connect the PC with the evaluation board must be selected first. The program displays a list of the active COM ports, allowing you to select the right one. To learn what COM port is used by the evaluation board, launch the Windows **Device Manager** (the **devmgmt.msc** file) in the **Run** window on the Windows **Start** menu. By default, the program offers the option of searching for the COM port.

Serial communication between the microcontroller and the ADE7878 is introduced using a switch. By default, the SPI port is used. Note that the active serial port must first be set in the hardware. See the Activating Serial Communication Between the ADE7878 and the NXP LPC2368 section for details on how to set it up.

The main menu has only one choice, other than **Exit**, enabled, **Find COM Port**. Clicking it starts a process in which the PC tries to connect to the evaluation board using the port indicated in the **Start** menu. It uses the echo function of the communication protocol (see the Managing the Communication Protocol Between the Microcontroller and the ADE7878 section). It displays the port that matches the protocol and then sets it to 115,200 baud, eight data bits, no parity, no flow control, one stop bit.

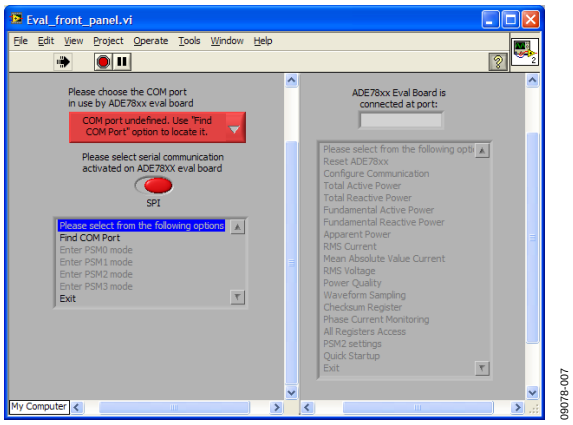


Figure 7. Front Panel of ADE7878 Software

If the evaluation board is not connected, the port is displayed as **XXXXX**. In this case, the evaluation software is still accessible, but no communication can be executed. In both cases, whether the search for the COM port is successful or not, the cursor is positioned back at **Please select from the following options** in the main menu, **Find COM Port** is grayed out, and the next main menu options are enabled (see Figure 8). These options allow you to command the ADE7878 in either the PSM0 or PSM3 power mode. The other power modes, PSM1 and PSM2, are not available because initializations have to be made in PSM0 before the ADE7878 can be used in one of these other modes.

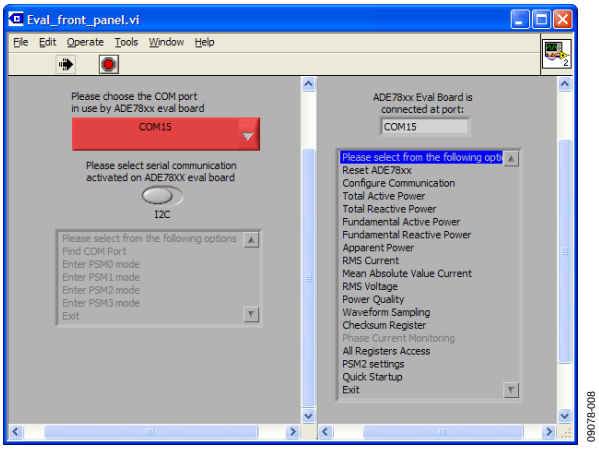


Figure 8. Front Panel After the COM Port Is Identified

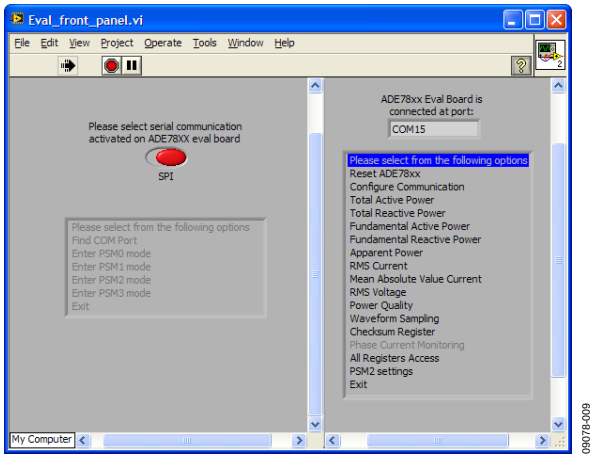


Figure 9. Front Panel After the ADE7878 Enters PSM0 Mode

PSM0 MODE—NORMAL POWER MODE

Enter PSM0 Mode

When the evaluation board is powered up, the ADE7878 is in PSM3 sleep mode. When **Enter PSM0 mode** is selected, the microcontroller manipulates the PM0 and PM1 pins of the ADE7878 to switch it into PSM0 mode. It waits 50 ms for the circuit to power up and, if SPI communication is activated on the board, it executes three SPI write operations to Address 0xEBFF of the ADE7878 to activate the SPI port.

If the operation has been correctly executed or I²C communication is used, the message **Configuring LPC2368 – ADE7878 communication was successful** is displayed, and you must click **OK** to continue. The only error that may occur during this operation is communication related; if this happens, the following message is displayed: **Configuring LPC2368 – ADE7878 communication was not successful. Please check the communication between the PC and ADE7878 evaluation board and between LPC2368 and ADE78xx**.

Bit 1 (I2C_LOCK) of the CONFIG2[7:0] register is now set to 1 to lock in the serial port choice. Then the DICOEFF register is initialized with 0xFF8000, and the DSP of the ADE7878 is started when the software program writes **RUN = 0x1**. At the end of this process, the entire main menu is grayed out, and the submenu is enabled. You can now manage all functionality of the ADE7878 in PSM0 mode. To switch the ADE7878 to another power mode, click the **Exit** button on the submenu. The state of the **Front Panel** is shown in Figure 9.

Reset ADE7878

When **Reset ADE78xx** is selected on the **Front Panel**, the RESET pin of the ADE7878 is kept low for 20 ms and then is set high. If the operation is correctly executed, the message **ADE7878 was reset successfully** is displayed, and you must click **OK** to continue. The only error that may occur during this operation is communication related; if this happens, the following message is displayed: **The communication between PC and ADE7878 evaluation board or between LPC2368 and ADE78xx did not function correctly. There is no guarantee the reset of ADE7878 has been performed.**

Configure Communication

When **Configure Communication** is selected on the **Front Panel**, the panel shown in Figure 10 is opened. This panel is useful if an ADE7878 reset has been performed and the SPI is no longer the active serial port. Select the SPI port by clicking the **I2C/SPI Selector** button and then click **OK** to update the selection and lock the port. If the port selection is successful, the message, **Configuring LPC2368 – ADE7878 communication was successful,** is displayed, and you must click **OK** to continue. If a communication error occurs, the message, **Configuring LPC2368 – ADE7878 communication was not successful. Please check the communication between the PC and ADE7878 evaluation boar**d, is displayed.

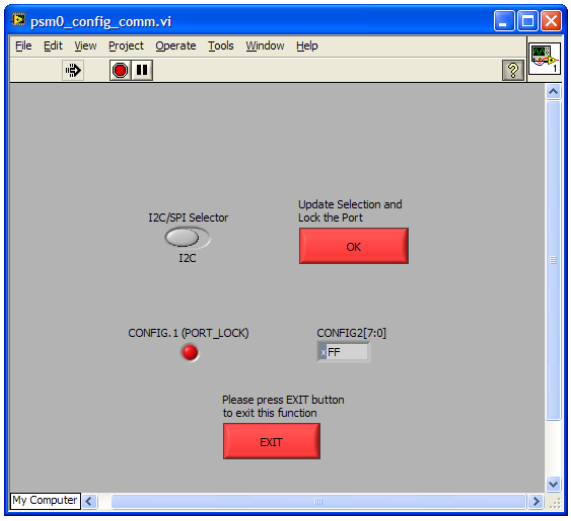


Figure 10. Configure Communication Panel

The CONFIG2[7:0] register is written with Bit 1 (I2C_LOCK) set to 1 so that you do not need to remember to set it once the communication is set. The contents of CONFIG2[7:0] are then read back and displayed with Bit 1 (I2C_LOCK).

To close the panel, click the **Exit** button; the cursor is positioned at **Please select from the following options** in the submenu of the **Front Panel**.

Total Active Power

When **Total Active Power** is selected on the **Front Panel**, the panel shown in Figure 11 is opened. The screen has an upper half and a lower half: the lower half shows the total active power data path of one phase, and the upper half shows bits, registers, and commands necessary to power management.

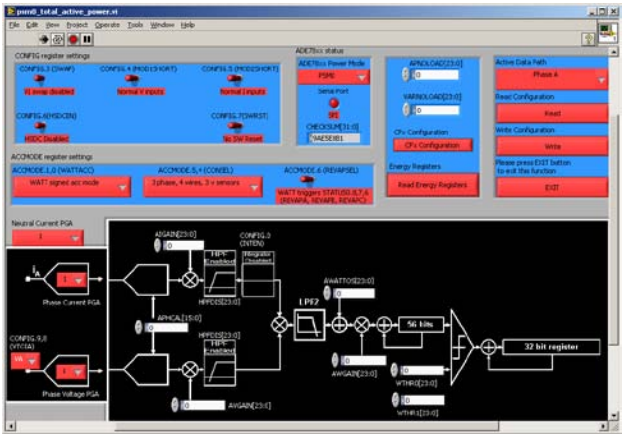


Figure 11. Total Active Power Panel

The **Active Data Path** button manages which data path is shown in the bottom half. Some registers or bits, like the WTHR0[23:0] register or Bit 0 (INTEN) of the CONFIG[15:0] register, are common to all data paths, independent of the phase shown. When these registers are updated, all the values in all data paths are updated. The HPFDIS[23:0] register is included twice in the data path, but only the register value from the current data path is written into the ADE7878. All the other instances take this value directly.

1. Click the **Read Configuration** button to cause all registers that manage the total active power to be read and displayed. Registers from the inactive data paths are also read and updated.
2. Click the **Write Configuration** button to cause all registers that manage the total active power to be written into the ADE7878. Registers from the inactive data paths are also written. The **ADE78xx status** box shows the power mode that the ADE7878 is in (it should always be PSM0 in this window), the active serial port (it should always be SPI), and the CHECKSUM[31:0] register. After every read and write operation, the CHECKSUM[31:0] register is read and its contents displayed.
3. Click the **CFx Configuration** button to open a new panel (see Figure 12). This panel gives access to all bits and registers that configure the CF1, CF2, and CF3 outputs of the ADE7878. The **Read Setup** and **Write Setup** buttons update and display the CF1, CF2, and CF3 output values.

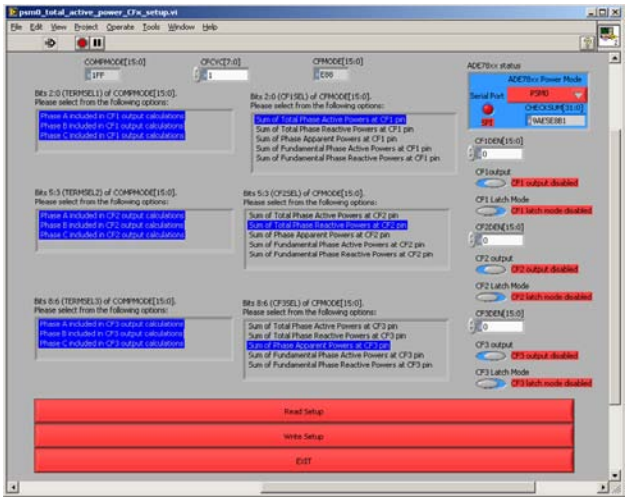


Figure 12. CFx Configuration Panel

Like the **Total Active Power** panel, the CHECKSUM[31:0] register is read back whenever a read or write operation is executed in the **CFx Configuration** panel. To select more than one option for a TERMSELx bit in the COMPMODE [15:0] register, press the **CTRL** key while clicking the options you want.

Clicking the **Exit** button closes the panel and redisplays the **Total Active Power** panel. When the **Read Energy Registers** button in the **Total Active Power** panel is clicked, a new panel is opened (see Figure 13). This panel gives access to bits and registers that configure the energy accumulation. The **Read Setup** and **Write Setup** buttons update and display the bit and register values.

The CHECKSUM[31:0] register is read back whenever a read or write operation is executed in the **Read Energy Registers** panel. Clicking the **Read all energy registers** button causes all energy registers to be read immediately, without regard to the modes in which they function.

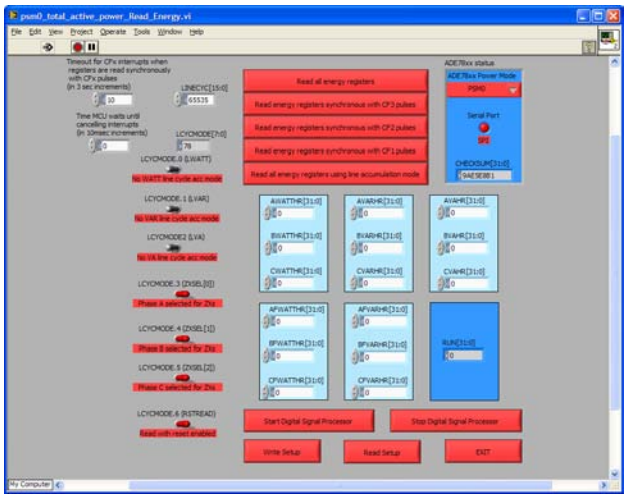


Figure 13. Read Energy Registers Panel

The panel also gives the choice of reading the energy registers synchronous to CFx interrupts (pulses) or using line cycle accumulation mode. When the **Read energy registers synchronous with CF1 pulses** button is clicked, the following happens:

1. The STATUS0[31:0] register is read and then written back to so that all nonzero interrupt flag bits are cancelled.
2. Bit 14 (CF1) in the MASK0[31:0] register is set to 1, and the interrupt protocol is started (see the Managing the Communication Protocol Between the Microcontroller and the ADE7878 section for protocol details).
3. The microcontroller then waits until the $\overline{\text{IRQ0}}$ pin goes low. If the wait is longer than the timeout you indicate in 3 sec increments, the following error message is displayed: **No CF1 pulse was generated. Verify all the settings before attempting to read energy registers in this mode!**
4. When the $\overline{\text{IRQ0}}$ pin goes low, the STATUS0[31:0] register is read and written back to cancel Bit 14 (CF1); then the energy registers involved in the CF1 signal are read and their contents are displayed. A timer in 10 ms increments can be used to measure the reaction time after the $\overline{\text{IRQ0}}$ pin goes low.
5. The operation is repeated until the button is clicked again.

The process is similar when the other CF2, CF3, and line accumulation (**Read Energy Registers** panel) buttons are clicked.

It is recommended to always use a timeout when dealing with interrupts. By default, the timeout is set to 10 (indicating a 30 sec timeout), and the timer is set to 0 (indicating that the STATUSx[31:0] and energy registers are read immediately after the $\overline{\text{IRQ0}}$ pin goes low).

When clicked on the **Front Panel**, the **Total Reactive Power**, **Fundamental Active Power**, and **Fundamental Reactive Power** buttons open panels that are very similar to the **Total Active Power** panel. These panels are shown in Figure 14, Figure 15, and Figure 16.

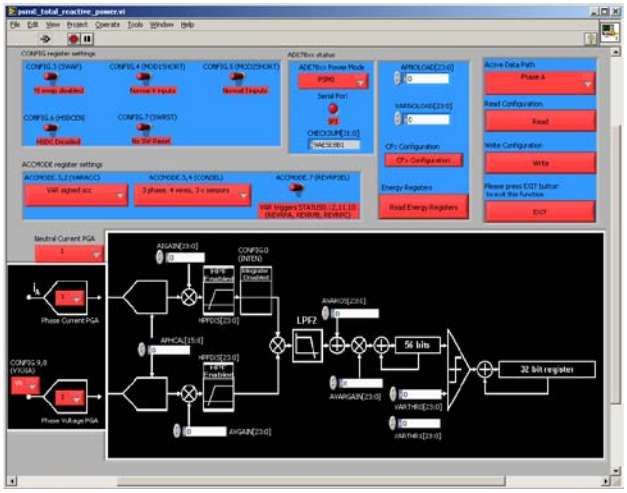


Figure 14. Total Reactive Power Panel

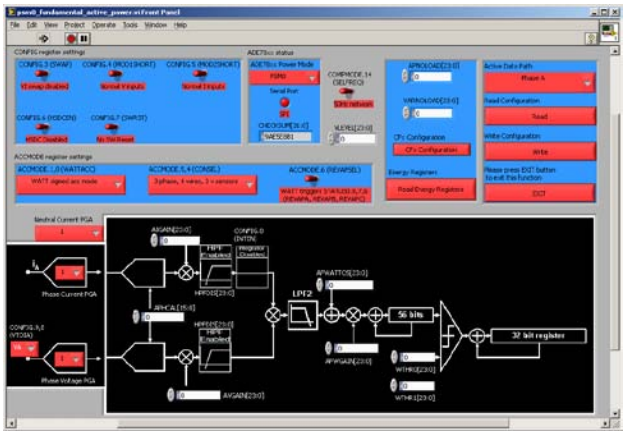


Figure 15. Fundamental Active Power Panel

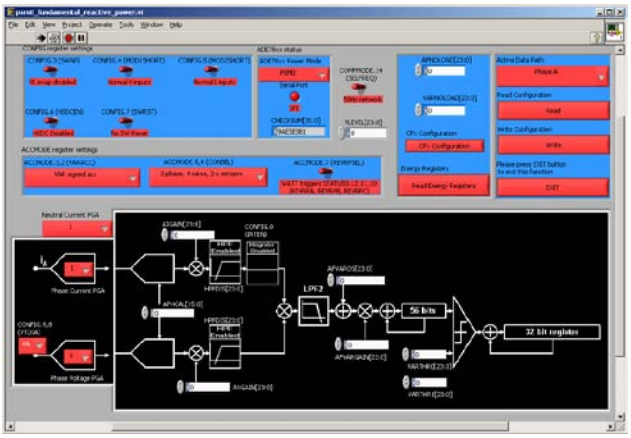


Figure 16. Fundamental Reactive Power Panel

Apparent Power

When **Apparent Power** is selected on the **Front Panel**, a new panel is opened (see Figure 17). Similar to the other panels that deal with power measurement, this panel is divided into two parts: the lower half shows the apparent power data path of one phase and the ADE7878 status; the upper half shows the bits, registers, and commands necessary to power management.

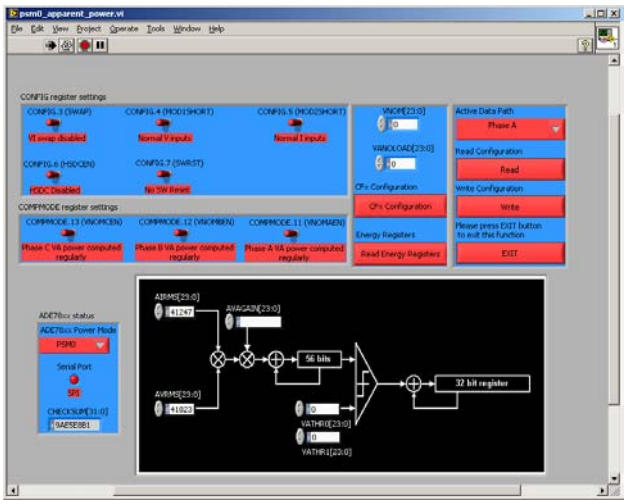


Figure 17. Apparent Power Panel

Current RMS

When **RMS Current** is selected on the **Front Panel**, a new panel is opened (see Figure 18). All data paths of all phases are available.

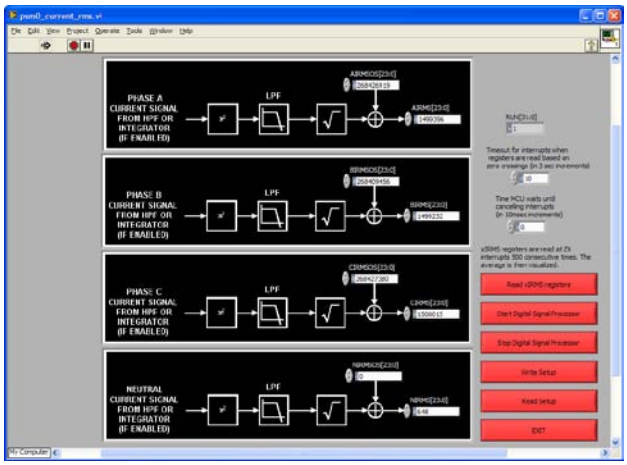


Figure 18. Current RMS panel

Clicking the **Read Setup** button causes a read of all registers shown in the panel. Clicking the **Write Setup** button causes writes to the xIRMSOS[23:0] registers.

You can use the **Start Digital Signal Processor** and **Stop Digital Signal Processor** buttons to manage the Run[15:0] register and the **Read xIRMS registers** button, which uses the ZXIA, ZXIB, and ZXIC interrupts at the $\overline{\text{IRQ1}}$ pin, to read the xIRMS[23:0]registers 500 consecutive times and then compute and display their average. If no interrupt occurs for the time indicated by the timeout (in 3 sec increments), the following message is displayed: **No ZXIA, ZXIB or ZXIC interrupt was generated. Verify at least one sinusoidal signal is provided between IAP-IAN, IBP-IBN or ICP-ICN pins**. A delay can be introduced (in 10 ms increments) between the time the $\overline{\text{IRQ1}}$ pin goes low and the moment the xIRMS registers are read. The operation is repeated until the button is clicked again.

Mean Absolute Value Current

When **Mean Absolute Value Current** is selected on the **Front Panel**, a new panel is opened (see Figure 19). When the **Read xIMAV registers** button is clicked, the xIMAV[19:0] registers are read 10 consecutive times, and their average is computed and displayed. After this operation, the button is returned to high automatically. The ADE7878 status is also displayed.

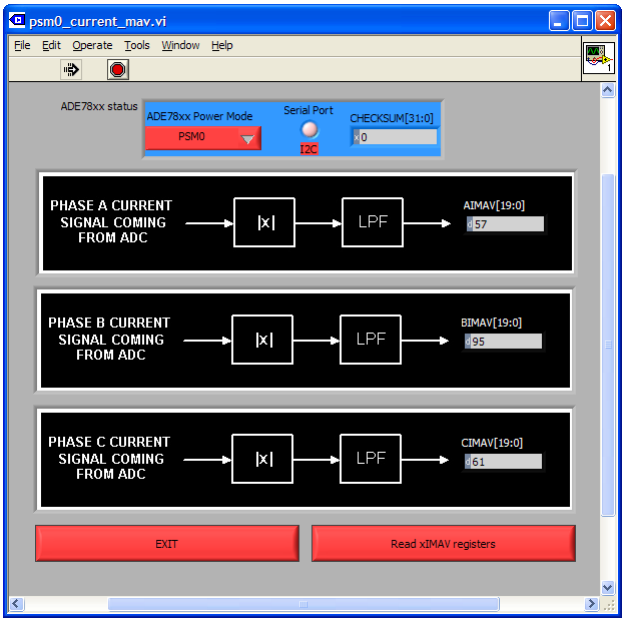


Figure 19. Mean Absolute Value Current Panel

Voltage RMS

When **RMS Voltage** is selected on the **Front Panel**, the **Voltage RMS** panel is opened (see Figure 20). This panel is very similar to the **Current RMS** panel. Clicking the **Read Setup** button executes a read of the xVRMSOS[23:0] and xVRMS[23:0] registers.

Clicking **Write Setup** writes the xVRMSOS[23:0] registers into the ADE7878. The **Start Digital Signal Processor** and **Stop Digital Signal Processor** buttons manage the Run[15:0] register.

When the **Read xVRMS registers** button is clicked, the xVRMS[23:0] registers are read 500 consecutive times and the average is displayed. The operation is repeated until the button is clicked again. Note that the ZXVA, ZXVB, and ZXVC zero-crossing interrupts are not used in this case because they are disabled when the voltages go below 10% of full scale. This allows rms voltage registers to be read even when the phase voltages are very low.

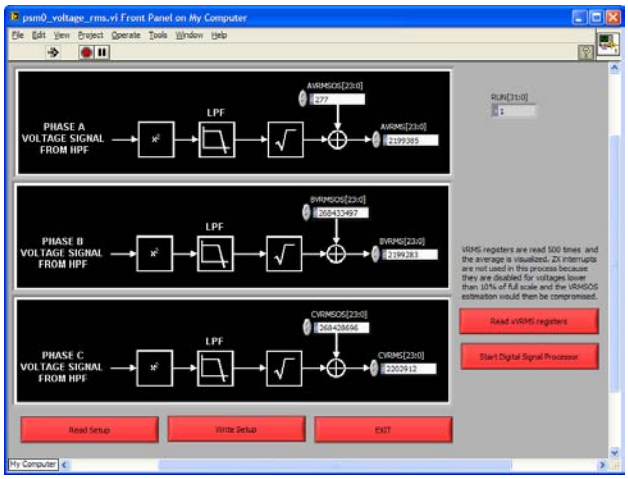


Figure 20. Voltage RMS Panel

Power Quality

The **Power Quality** panel is accessible from the **Front Panel** and is divided into two parts (see Figure 21). The lower part displays registers that manage the power quality measurement functions for the **Active Measurement** button in the upper part of the panel. The upper part also displays the ADE7878 status and the buttons that manage the measurements.

When the **READ CONFIGURATION** button is clicked, all power quality registers (MASK1[31:0], STATUS1[31:0], PERIOD[15:0], MMODE[7:0], ISUM[27:0], OVLVL[23:0], OILVL[23:0], PHSTATUS[15:0], IPEAK[31:0], VPEAK[31:0], SAGLVL[23:0], SAGCYC[7:0], ANGLE0[15:0], ANGLE1[15:0], ANGLE2[15:0], COMPMODE[15:0], CHECKSUM[31:0], and PEAKCYC[7:0]) are read, and the ones belonging to the active panel are displayed. Based on the PERIOD[15:0] register, the line frequency is computed and displayed in the lower part of the panel, in **Zero Crossing Measurements**. Based on the ANGLEx[15:0] registers, cos(ANGLEx) is computed and displayed in the **Time Intervals Between Phases** panel that is accessible from the **Active Measurement Zero Crossing** dropdown box (see Figure 21).

When the **WRITE CONFIGURATION** button is clicked, MMODE[7:0], OVLVL[23:0], OILVL[23:0], SAGLVL[23:0], SAGCYC[7:0], COMPMODE[15:0], and PEAKCYC[7:0] are written into the ADE7878, and CHECKSUM[31:0] is read back and displayed in the CHECKSUM[31:0] box at the top of the upper part of the panel.

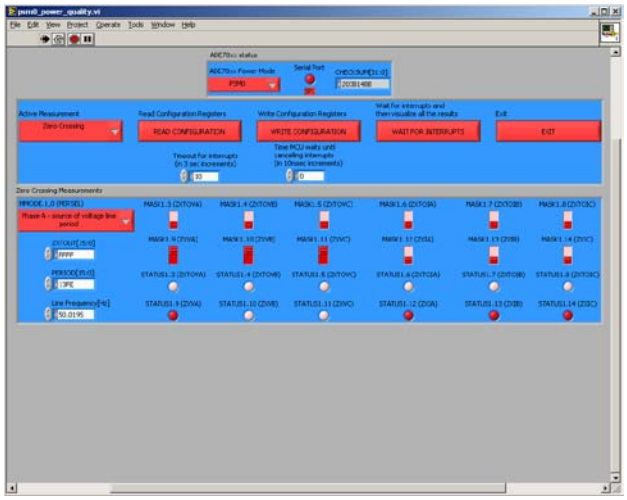


Figure 21. Power Quality Zero-Crossing Measurements Panel

When the **WAIT FOR INTERRUPTS** button is clicked, the interrupts that you have enabled in the MASK1[31:0] register are monitored. When the $\overline{\text{IRQ1}}$ pin goes low, the STATUS1[31:0] register is read and its bits are displayed. The ISUM[27:0], PHSTATUS[15:0], IPEAK[31:0], VPEAK[31:0], ANGLE0[15:0], ANGLE1[15:0], and ANGLE2[15:0] registers are also read and displayed. A timeout should be introduced in 3 sec increments to ensure that the program does not wait indefinitely for interrupts. A timer (in 10 ms increments) is provided to allow reading of the registers with a delay from the moment the interrupt is triggered.

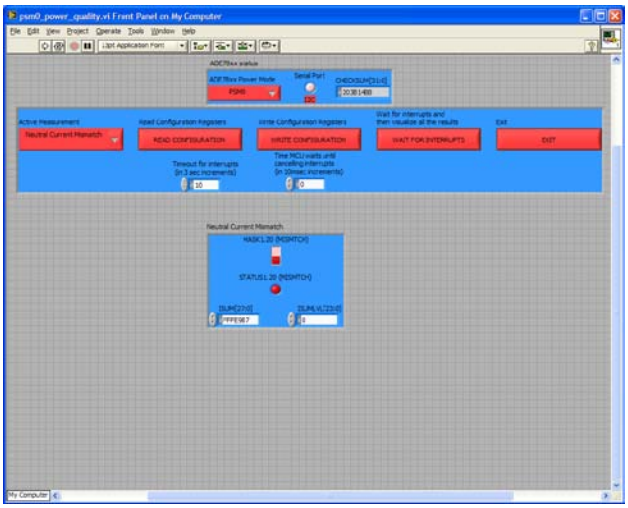
The **Active Measurement Zero Crossing** button gives access to the **Zero Crossing**, **Neutral Current Mismatch**, **Overvoltage and Overcurrent Measurement**, **Peak Detection**, and **Time Intervals Between Phases** panels (see Figure 21 through Figure 25).

The line frequency is computed using the PERIOD[15:0] register, based on the following formula:

$$f = \frac{256{,}000}{Period}[Hz]$$

The cosine of the ANGLE0[15:0], ANGLE1[15:0], and ANGLE2[15:0] measurements is computed using the following formula:

$$cos(ANGLEx) = cos\left(\frac{ANGLEx \times 360 \times f}{256{,}000}\right)$$

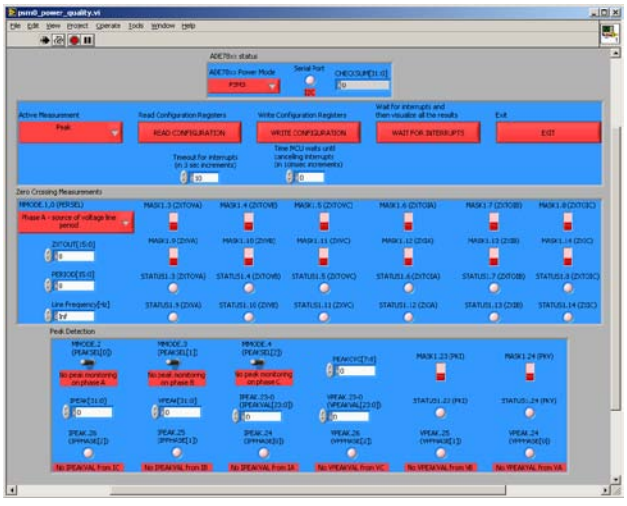


09078-022

Figure 22. Neutral Current Mismatch Panel

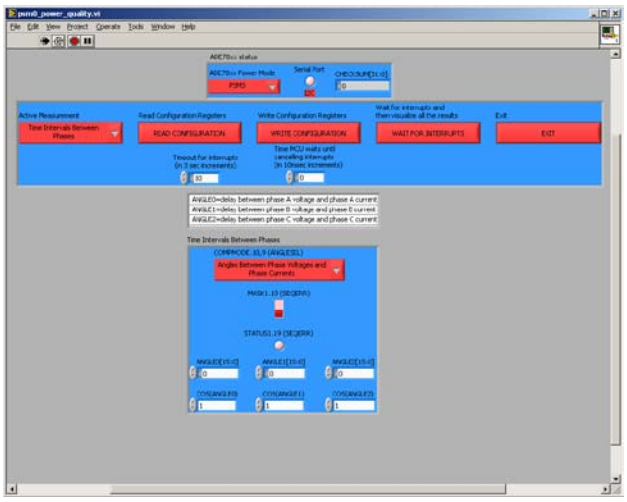
09078-023

Figure 23. Overvoltage and Overcurrent Measurements Panel



09078-024

Figure 24. Peak Detection Panel

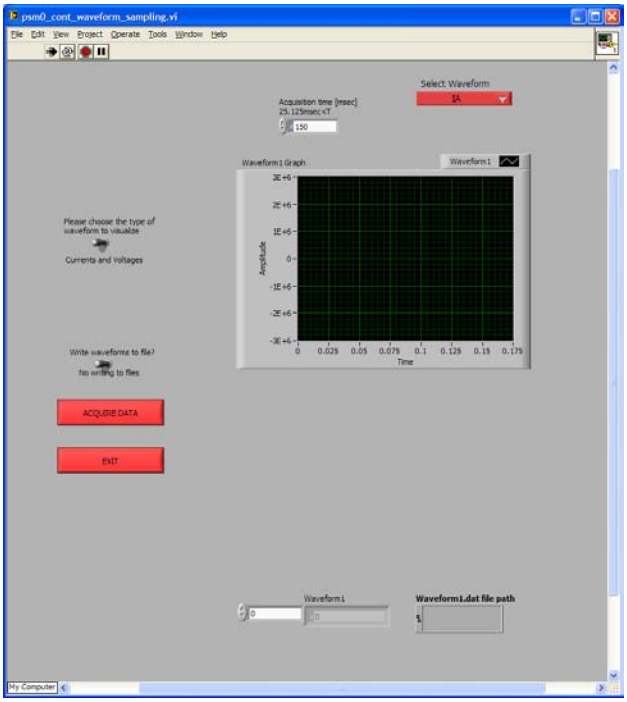


09078-025

Figure 25. Time Intervals Between Phases Panel

Waveform Sampling

The **Waveform Sampling** panel (see Figure 26) is accessible from the **Front Panel** and uses the HSDC port to acquire data from the ADE7878 and display it. It can be accessed only if the communication between the ADE7878 and the NXP LPC2368 is through the I²C. See the Activating Serial Communication Between the ADE7878 and the NXP LPC2368 section for details on how to set I²C communication on the ADE7878 evaluation board.



09078-026

Figure 26. Waveform Sampling Panel

The HSDC transmits data to the NXP LPC2368 at 4 MHz because this is the maximum speed at which the slave SPI of the NXP LPC2368 can receive data. The panel contains some switches that must be set before acquiring data.

- One switch chooses the quantities that are displayed: phase currents and voltages or phase powers. For every set of quantities, only one can be acquired at a time. This choice is made using the **Select Waveform** button.
- A second switch allows acquired data to be stored in files for further use. This switch is set with the **ACQUIRE DATA** button.
- The acquisition time should also be set before an acquisition is ordered. By default, this time is 150 ms. It is unlimited for phase currents and voltages and for phase powers. The NXP LPC2368 executes in real time three tasks using the ping pong buffer method: continuously receiving data from HSDC, storing the data into its USB memory, and sending the data to the PC. Transmitting seven phase currents and voltages at 4 MHz takes 103.25 µs (which is less than 125 µs); therefore, the HSDC update rate is 8 kHz (HSDC_CFG = 0x0F). Transmitting nine phase powers takes 72 µs (again, less than 125 µs); therefore, the HSDC update rate is also 8 kHz (HSDC_CGF = 0x11).

To start the acquisition, click the **ACQUIRE DATA** button. The data is displayed on one plot. If you click the **Write waveforms to file?/No writing to files** switch to enable the writing of waveforms to a file, the program asks for the name and location of the files before storing the waveform.

Checksum Register

The **Checksum Register** panel is accessible from the **Front Panel** and gives access to all ADE7878 registers that are used to compute the CHECKSUM[31:0] register (see Figure 27). You can read/write the values of these registers by clicking the **Read** and **Write** buttons. The LabView program estimates the value of the CHECKSUM[31:0] register and displays it whenever one of the registers is changed. When the **Read** button is pressed, the registers are read and the CHECKSUM[31:0] register is read and its values displayed. This allows you to compare the value of the CHECKSUM[31:0] register estimated by LabView with the value read from the ADE7878. The values should always be identical.

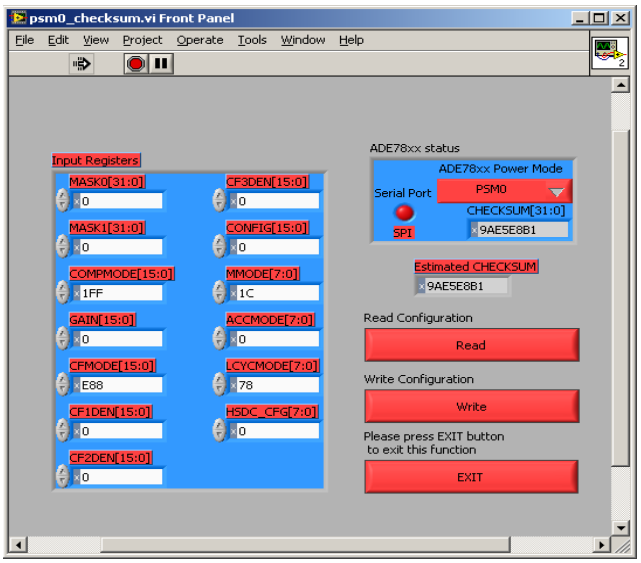


Figure 27. Checksum Register Panel

All Registers Access

The **All Registers Access** panel is accessible from the **Front Panel** and gives read/write access to all ADE7878 registers. Because there are many, the panel can scroll up and down and has multiple read, write, and exit buttons (see Figure 28 and Figure 29). The registers are listed in columns in alphabetical order, starting at the upper left. The panel also allows you to save all control registers into a data file by clicking the **Save All Regs into a file** button. By clicking the **Load All Regs from a file** button, you can load all control registers from a data file. Then, by clicking the **Write All Regs** button, you can load these values into the ADE7878. The order in which the registers are stored into a file is shown in the Control Registers Data File section.

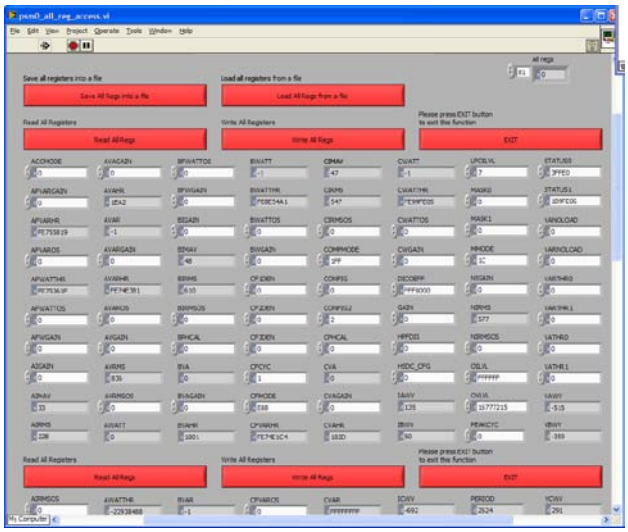


Figure 28. Panel Giving Access to All ADE7878 Registers (1)

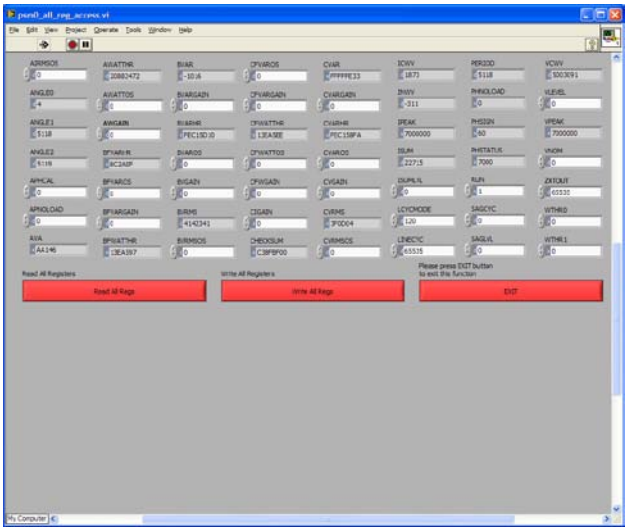


Figure 29. Panel Giving Access to All ADE7878 Registers (2)

Quick Startup

The **Quick Startup** panel is accessible from the **Front Panel** and can be used to rapidly initialize a 3-phase meter (see Figure 30).

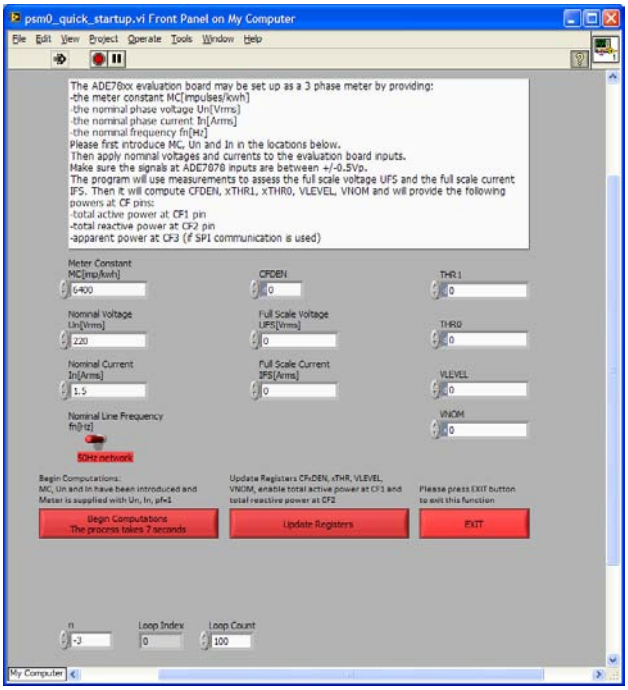


Figure 30. Panel Used to Quickly Set Up the 3-Phase Meter

The meter constant (MC, in impulses/kWh), the nominal voltage (Un, in V rms units), the nominal current (In, in A rms units), and the nominal line frequency (fn, in either 50 Hz or 60 Hz) must be introduced in the panel controls. Then phase voltages and phase currents must be provided through the relative sensors.

Clicking the **Begin Computations** button starts the program that reads rms voltages and currents and calculates the full-scale voltage and currents used to further initialize the meter. This process takes 7 sec as the program reads the rms voltages 100 times and the rms currents 100 times and then averages them (this is because the PC reads the rms values directly and cannot synchronize the readings with the zero crossings).

The program then computes the full-scale voltages and currents and the constants that are important for setting up the ADE7878: nominal values (n), CFDEN, WTHR1, VARTHR1, VATHR1 and WTHR0, VARTHR0, and VATHR0.

At this point, you can overwrite these values. You can also click the **Update Registers** button to cause the program to do the following:

- Initialize the CFxDEN and xTHR registers
- Enable the CF1 pin to provide a signal proportional to the total active power, the CF2 pin to provide a signal proportional to the total reactive power, and the CF3 pin to provide a signal proportional to the apparent power.

Throughout the program, it is assumed that PGA gains are 1 (for simplicity) and that the Rogowski coil integrators are disabled. You can enter and modify the PGAs and enable the integrators before executing this quick startup if necessary.

At this point, the evaluation board is set up as a 3-phase meter, and calibration can be executed. To store the register initializations, click the **Save All Regs into a file** button in the **All Registers Access** panel. After the board is powered down and then powered up again, the registers can be loaded into the ADE7878 by simply loading back the content of the data file. To do this, click the **Load All Regs from a file** button in the **All Registers Access** panel.

PSM2 Settings

The **PSM2 Settings** panel, which is accessible from the **Front Panel**, gives access to the LPOILVL[7:0] register that is used to access PSM2 low power mode (see Figure 31). You can manipulate its LPOIL[2:0] and LPLINE[4:0] bits. The value shown in the LPOILVL[7:0] register is composed from these bits and then displayed. Note that you cannot write a value into the register by writing a value in the LPOILVL[7:0] register box.

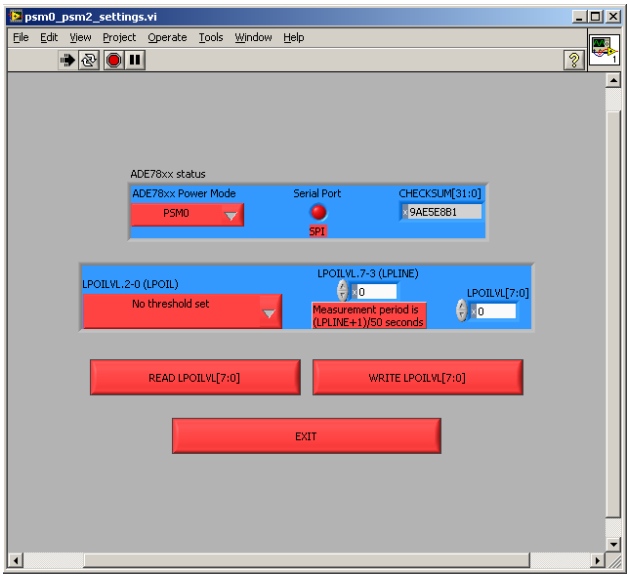


Figure 31. PSM2 Settings Panel

PSM1 MODE

Enter PSM1 Mode

When **Enter PSM1 mode** is selected on the **Front Panel**, the microcontroller manipulates the PM0 and PM1 pins of the ADE7878 to switch the ADE7878 into PSM1 reduced power mode. Then, the submenu allows access only to the **Mean Absolute Value Current** function because this is the only ADE7878 functionality available in this reduced power mode (see Figure 32).

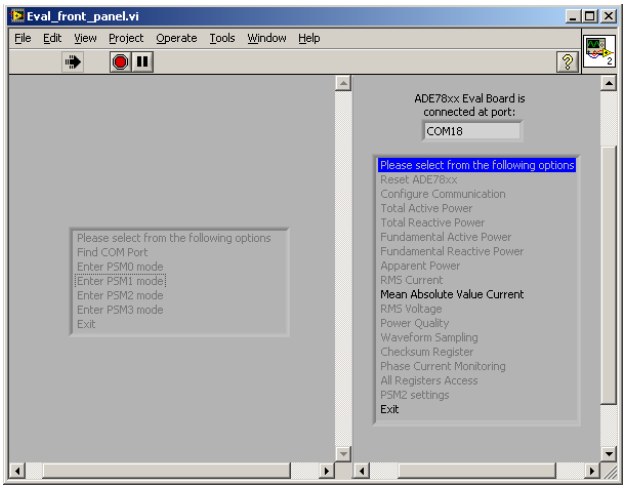


Figure 32. Front Panel After the ADE7878 Enters PSM1 Mode

Mean Absolute Value Current in PSM1 Mode

The **Mean Absolute Value Current** panel, which is accessible from the **Front Panel** when **Enter PSM1 mode** is selected, is very similar to the panel accessible in PSM0 mode (see the Mean Absolute Value Current section for details). The only difference is that **ADE7878 status** does not show the CHECKSUM[31:0] register because it is not available in PSM1 mode (see Figure 33)

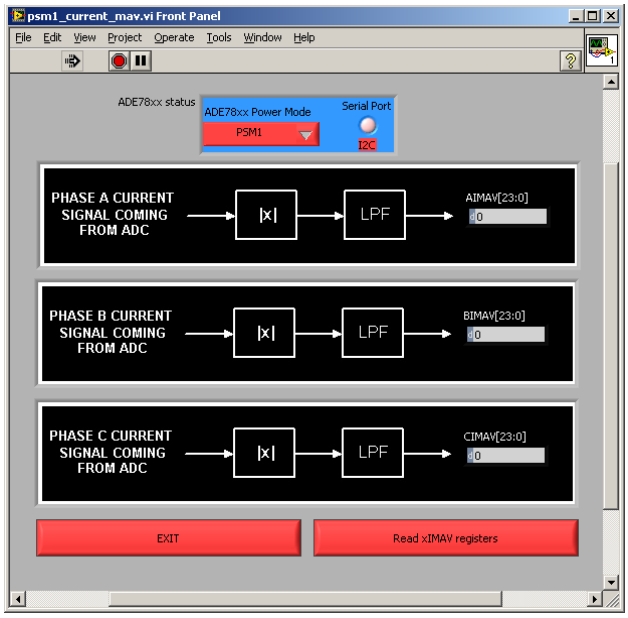


Figure 33. Mean Absolute Value Currents Panel in PSM1 Mode

PSM2 MODE

Enter PSM2 Mode

When **Enter PSM2 mode** is selected on the **Front Panel**, the microcontroller manipulates the PM0 and PM1 pins of the ADE7878 to switch the ADE7878 into PSM2 low power mode. Then the submenu allows access only to the **Phase Current Monitoring** function because this is the only ADE7878 functionality available in this low power mode.

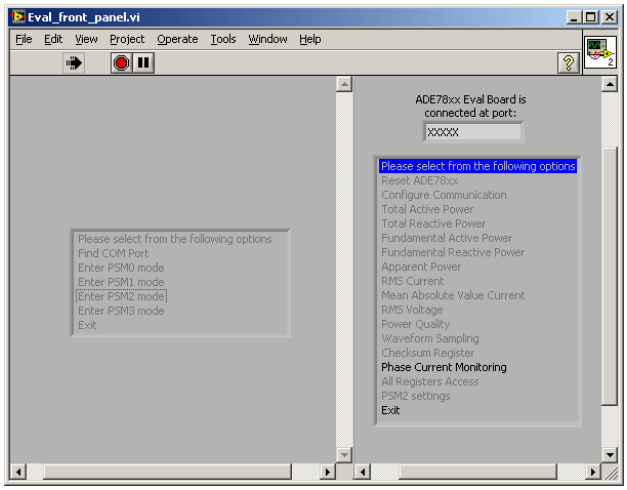


Figure 34. Front Panel After the ADE7878 Enters PSM2 Mode

Phase Current Monitoring

The **Phase Current Monitoring** panel is accessible from the **Front Panel** when **Enter PSM2 mode** is selected; it allows you to display the state of the IRQ0and IRQ1 pins because, in PSM2 low power mode, the ADE7878 compares the phase currents against a threshold determined by the LPOILVL[7:0] register (see Figure 35). Clicking the **READ STATUS OF IRQ0 AND IRQ1 PINS** button reads the status of these pins and displays and interprets the status.

This operation is managed by the LPOILVL[7:0] register and can be modified only in PSM0 mode. The panel offers this option by switching the ADE7878 into PSM0 mode and then back to PSM2 mode when one of the **READ LPOILVL/WRITE LPOILVL** buttons is clicked. To avoid toggling both the PM0 and PM1 pins at the same time during this switch, the ADE7878 is set to PSM3 when changing modes.

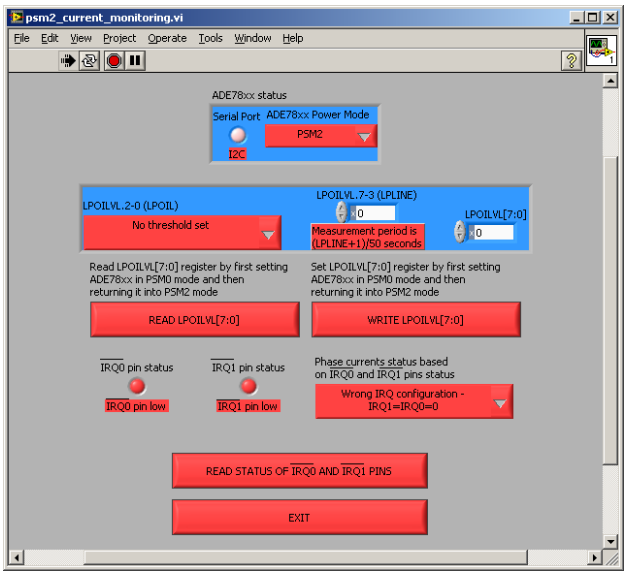


Figure 35. Panel Managing Current Monitoring in PSM2 Mode

PSM3 MODE

Enter PSM3 Mode

In PSM3 sleep mode, most of the internal circuits of the ADE7878 are turned off. Therefore, no submenu is activated while in this mode. You can click the **Enter PSM0 mode**, **Enter PSM1 mode**, or **Enter PSM2** mode button to set the ADE7878 to one of these power modes.

MANAGING THE COMMUNICATION PROTOCOL BETWEEN THE MICROCONTROLLER AND THE ADE7878

In this section, the protocol commands are listed that have been implemented to manage the ADE7878 from the PC using the microcontroller.

The microcontroller is a pure slave during the communication process. It receives a command from the PC, executes the command, and sends an answer to the PC. The PC should wait for the answer before sending a new command to the microcontroller.

Table 3. Echo Command—Message from the PC to the Microcontroller

Byte	Description
0	A = 0x41
1	N = number of bytes transmitted after this byte
2	Data Byte N – 1 (MSB)
3	Data Byte N – 2
4	Data Byte N – 3
…	…
N	Data Byte 1
N + 1	Data Byte 0 (LSB)

Table 4. Echo Command—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52
1	A = 0x41
2	N = number of bytes transmitted after this byte
3	Data byte N – 1 (MSB)
4	Data byte N – 2
…	…
N + 1	Data Byte 1
N + 2	Data Byte 0 (LB)

Table 5. Power Mode Select—Message from the PC to the Microcontroller

Byte	Description
0	B = 0x42, change PSM mode
1	N = 1
2	Data Byte 0: 0x00 = PSM0 0x01 = PSM1 0x02 = PSM2 0x03 = PSM3

Table 6. Power Mode Select—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52
1	~ = 0x7E, to acknowledge that the operation was successful

Table 7. Reset—Message from the PC to the Microcontroller

Byte	Description
0	C = 0x43, toggle the $\overline{\text{RESET}}$ pin and keep it low for at least 10 ms
1	N = 1
2	Data Byte 0: this byte can have any value

Table 8. Reset—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52
1	~ = 0x7E, to acknowledge that the operation was successful

Table 9. I²C/SPI Select (Configure Communication)—Message from the PC to the Microcontroller

Byte	Description
0	D = 0x44, select I²C and SPI and initialize them; then set CONFIG2[7:0] = 0x2 to lock in the port choice. When I²C is selected, also enable SSP0 of the LPC2368 (used for HSDC).
1	N = 1.
2	Data Byte 0: 0x00 = I²C, 0x01 = SPI.

Table 10. I²C/SPI Select (Configure Communication)—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52
1	~ = 0x7E, to acknowledge that the operation was successful

Table 11. Data Write—Message from the PC to the Microcontroller

Byte	Description
0	E = 0x45.
1	N = number of bytes transmitted after this byte. N can be 1 + 2, 2 + 2, 4 + 2, or 6 + 2.
2	MSB of the address.
3	LSB of the address.
4	Data Byte N – 3 (MSN).
5	Data Byte N – 4.
6	Data Byte N – 5.
…	…
N + 2	Data Byte 1.
N + 3	Data Byte 0 (LSB).

Table 12. Data Write—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52
1	~ = 0x7E, to acknowledge that the operation was successful

Table 13. Data Read—Message from the PC to the Microcontroller

Byte	Description
0	F = 0x46.
1	N = number of bytes transmitted after this byte; N = 3.
2	MSB of the address.
3	LSB of the address.
4	M = number of bytes to be read from the address above. M can be 1, 2, 4, or 6.

Table 14. Data Read—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52.
1	MSB of the address.
2	LSB of the address.
3	Byte 5, Byte 3, Byte 1, or Byte 0 (MSB) read at the location indicated by the address. The location may contain 6, 4, 2, or 1 byte. The content is transmitted MSB first.
4	Byte 4, Byte 2, or Byte 0.
5	Byte 3, Byte 1.
6	Byte 2, Byte 0.
7	Byte 1.
8	Byte 0.

Table 15. Interrupt Setup—Message from the PC to the Microcontroller

Byte	Description
0	J = 0x4A.
1	N = 8, number of bytes transmitted after this byte.
2	MSB of the MASK1[31:0] or MASK0[31:0] register.
3	LSB of the MASK1[31:0] or MASK0[31:0] register.
4	Byte 3 of the desired value of the MASK0[31:0] or MASK1[31:0] register.
5	Byte 2.
6	Byte 1.
7	Byte 0.
8	Time out byte: time the MCU must wait for the interrupt to be triggered. It is measured in 3 sec increments. Time out byte (TOB) = 0 means that timeout is disabled.
9	IRQ timer: time the MCU leaves the $\overline{IRQx}$ pin low before writing back to clear the interrupt flag. It is measured in 10 ms increments. Timer = 0 means that timeout is disabled.

Table 16. Interrupt Setup—Message from the Microcontroller to the PC

Byte	Description
0	R = 0x52.
1	Byte 3 of the STATUS0[31:0] or STATUS1[31:0] register. If the program waited for TOB × 3 sec and the interrupt was not triggered, then Byte 3 = Byte 2 = Byte 1 = Byte 0 = 0xFF.
2	Byte 2 of the STATUS0[31:0] or STATUS1[31:0] register.
3	Byte 1 of the STATUS0[31:0] or STATUS1[31:0] register.
4	Byte 0 of the STATUS0[31:0] or STATUS1[31:0] register.

The microcontroller executes the following operations once the interrupt setup command is received:

1. Reads the STATUS0[31:0] or STATUS1[31:0] register (depending on the address received from the PC) and, if it shows an interrupt already triggered (one of its bits is equal to 1), it erases the interrupt by writing it back.
2. Writes to the MASK0[31:0] or MASK1[31:0] register with the value received from the PC.
3. Waits for the interrupt to be triggered. If the wait is more than the timeout specified in the command, 0xFFFFFFFF is sent back.
4. If the interrupt is triggered, the STATUS0[31:0] or STATUS1[31:0] register is read and then written back to clear it. The value read at this point is the value sent back to the PC so that you can see the source of the interrupts.
5. Sends back the answer.

Table 17. Interrupt Pins Status—Message from the PC to the Microcontroller

Byte	Description
0	H = 0x48.
1	N = 1, number of bytes transmitted after this byte.
2	Any byte. This value is not used by the program but it is used in the communication because N must not be equal to 0.

Table 18. Interrupt Pins Status—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52.
1	A number representing the status of the $\overline{IRQ0}$ and $\overline{IRQ1}$ pins. 0: $\overline{IRQ0}$ = low, $\overline{IRQ1}$ = low 1: $\overline{IRQ0}$ = low, $\overline{IRQ1}$ = high. 2: $\overline{IRQ0}$ = high, $\overline{IRQ1}$ = low. 3: $\overline{IRQ0}$ = high, $\overline{IRQ1}$ = high. The reason for the $\overline{IRQ0}$ and $\overline{IRQ1}$ order is that on the microcontroller IO port, $\overline{IRQ0}$= P0.1 and $\overline{IRQ1}$ = P0.0.

ACQUIRING HSDC DATA CONTINUOUSLY

This function acquires data from the HSDC continuously for a defined time period and for up to two variables. The microcontroller sends data in packages of 4 kB.

Table 19 describes the protocol when two instantaneous phase currents or voltages are acquired.

Table 19. Acquire HSDC Data Continuously—Message from the PC to the Microcontroller If Phase Currents and Voltages Are Acquired

Byte	Description
0	G = 0x47.
1	N = number of bytes transmitted after this byte. N = 32.
2	0: corresponds to Byte 3 of IA. Because this byte is only a sign extension of Byte 2, it is not sent back by the microcontroller.
3	Increment_IA_Byte2. If IA is to be acquired, Byte 3, Byte 4, and Byte 5 are 1. Otherwise, they are 0.
4	Increment_IA_Byte1.
5	Increment_IA_Byte2.
6	0.
7	Increment_VA_Byte2. If VA is to be acquired, Byte 7, Byte 8, and Byte 9 are 1. Otherwise, they are 0.
8	Increment_VA_Byte1.
9	Increment_VA_Byte0.
10	0.
11	Increment_IB_Byte2. If IB is to be acquired, Byte 11, Byte 12, and Byte 13 are 1. Otherwise, they are 0.
12	Increment_IB_Byte1.
13	Increment_IB_Byte0.
14	0.
15	Increment_VB_Byte2. If VB is to be acquired, Byte 15, Byte 16, and Byte 17 are 1. Otherwise, they are 0.
16	Increment_VB_Byte1.
17	Increment_VB_Byte0.
18	0.
19	Increment_IC_Byte2. If IC is to be acquired, Byte 19, Byte 20, and Byte 21 are 1. Otherwise, they are 0.
20	Increment_IC_Byte1.
21	Increment_IC_Byte0.
22	0.
23	Increment_VC_Byte2. If VC is to be acquired, Byte 23, Byte 24, and Byte 25 are 1. Otherwise, they are 0.
24	Increment_VC_Byte1.
25	Increment_VC_Byte0.
26	0.
27	Increment_IN_Byte2. If IN is to be acquired, Byte 27, Byte 28, and Byte 29 are 1. Otherwise, they are 0.
28	Increment_IN_Byte1.
29	Increment_IN_Byte0.
30	Byte 1 of M. M is a 16-bit number. The number of 32-bit samples acquired by the microcontroller is $(2 \times M + 1) \times 67$ per channel.
31	Byte 0 of M.

If two of the phase powers are to be acquired, the protocol changes (see Table 20).

Table 20. Acquire HSDC Data Continuously—Message from the PC to the Microcontroller If Phase Powers Are Acquired

Byte	Description
0	G = 0x47
1	N = number of bytes transmitted after this byte. N = 38.
2	0: corresponds to Byte 3 of AVA. Because this byte is only a sign extension of Byte 2, it is not sent back by the microcontroller.
3	Increment_AVA_Byte2. If AVA is to be acquired, Byte 3, Byte 4, and Byte 5 are 1. Otherwise, they are 0.
4	Increment_AVA_Byte1.
5	Increment_AVA_Byte2.
6	0.
7	Increment_BVA_Byte2. If BVA is to be acquired, Byte 7, Byte 8, and Byte 9 are 1. Otherwise, they are 0.
8	Increment_BVA_Byte1.
9	Increment_BVA_Byte0.
10	0.
11	Increment_CVA_Byte2. If CVA is to be acquired, Byte 11, Byte 12, and Byte 13 are 1. Otherwise, they are 0.
12	Increment_CVA_Byte1.
13	Increment_CVA_Byte0.
14	0.
15	Increment_AWATT_Byte2. If AWATT is to be acquired, Byte 15, Byte 16, and Byte 17 are 1. Otherwise, they are 0.
16	Increment_AWATT_Byte1.
17	Increment_AWATT_Byte0.
18	0.
19	Increment_BWATT_Byte2. If BWATT is to be acquired, then Byte 19, Byte 20, and Byte 21 are 1. Otherwise, they are 0.
20	Increment_BWATT_Byte1.
21	Increment_BWATT_Byte0.
22	0.
23	Increment_CWATT_Byte2. If CWATT is to be acquired, Byte 23, Byte 24, and Byte 25 are 1. Otherwise, they are 0.
24	Increment_CWATT_Byte1.
25	Increment_CWATT_Byte0.
26	0.
27	Increment_AVAR_Byte2. If AVAR is to be acquired, Byte 27, Byte 28, and Byte 29 are 1. Otherwise, they are 0.
28	Increment_AVAR_Byte1.
29	Increment_AVAR_Byte0.
30	0.
31	Increment_BVAR_Byte2. If BVAR is to be acquired, then Byte 31, Byte 32, and Byte 33 are 1. Otherwise, they are 0.
32	Increment_BVAR_Byte1.
33	Increment_BVAR_Byte0.
34	0.
35	Increment_CVAR_Byte2. If CVAR is to be acquired, Byte 35, Byte 36, and Byte 37 are 1. Otherwise, they are 0.

Byte	Description
36	Increment_CVAR_Byte1.
37	Increment_CVAR_Byte0.
38	Byte 1 of M. M is a 16-bit number. The number of 32-bit samples acquired by the microcontroller is (2 × M + 1) × 67 per channel.
39	Byte 0 of M.

After receiving the command, the microcontroller enables the HSDC port and acquires 67 × 7 × 4 = 1876 bytes into BUFFER0. As soon as BUFFER0 is filled, data is acquired in BUFFER1 (equal in size to BUFFER0), while 2 × 3 × 67 = 402 bytes (134 24-bit words) from BUFFER0 are transmitted to the PC. As soon as BUFFER1 is filled, data is acquired into BUFFER0 while 402 bytes from BUFFER1 are transmitted to the PC. Only the less significant 24 bits of every 32-bit instantaneous value are sent to the PC to decrease the size of the buffer sent to the PC. The most significant eight bits are only an extension of a 24-bit signed word; therefore, no information is lost. The protocol used by the microcontroller to send data to the PC is shown in Table 21.

Table 21. Acquire HSDC Data Continuously—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52
1	Byte 2 (MSB) of Word 1
2	Byte 1 of Word 1
3	Byte 0 (LSB) of Word 1
4	Byte 2 (MSB) of Word 2
5	Byte 1 (MSB) of Word 2
…	...
402	Byte 0 (LSB) of Word 134

STARTING THE ADE7878 DSP

This function orders the microcontroller to start the DSP. The microcontroller writes to the run register with 0x1.

Table 22. Start ADE7878 DSP—Message from the PC to the Microcontroller

Byte	Description
0	N = 0x4E
1	N = number of bytes transmitted after this byte; N = 1
2	Any byte

Table 23. Start ADE7878 DSP—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52
1	~ = 0x7E, to acknowledge that the operation was successful

STOPPING THE ADE7878 DSP

This function orders the microcontroller to stop the DSP. The microcontroller writes to the run register with 0x0.

Table 24. Stop ADE7878 DSP—Message from the PC to the Microcontroller

Byte	Description
0	O = 0x4F
1	N = number of bytes transmitted after this byte; N = 1
2	Any byte

Table 25. Stop ADE7878 DSP—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52
1	~ = 0x7E to acknowledge that the operation was successful

UPGRADING MICROCONTROLLER FIRMWARE

Although the evaluation board is supplied with the microcontroller firmware already installed, the ADE7878 evaluation software CD provides the NXP LPC2368 microcontroller project developed under the IAR embedded workbench environment for ARM. Users in possession of this tool can modify the project at will and can download it using an IAR J-link debugger. As an alternative, the executable can be downloaded using a program called Flash Magic, available on the evaluation software CD or at the following website: http://www.flashmagictool.com/.

Flash Magic uses the PC COM port to download the microcontroller firmware. The procedure for using Flash Magic is as follows:

1. Plug a serial cable into connector P15 of the ADE7878 evaluation board and into a PC COM port. As an alternative, use the ADE8052Z-DWDL1 ADE downloader from Analog Devices, Inc., together with a USB cable.
2. Launch the **Device Manager** under Windows XP by writing **devmgmt.msc** into the **Start/Run** box. This helps to identify which COM port is used by the serial cable.
3. Plug the USB2UART board into the P15 connector of the ADE7878 evaluation board with the VDD pin of the USB2UART aligned at Pin 1 of P15.
4. Connect Jumper JP8. The P2.10/$\overline{\text{EINT0}}$ pin of the microcontroller is now connected to ground.
5. Supply the board with two 3.3 V supplies at the P10 and P12 connectors.
6. Press and release the reset button, S2, on the ADE7878 evaluation board.
7. Launch Flash Magic and do the following:
   a. Select a COM port (COMx as seen in the **Device Manager**).
   b. Set the baud rate to 115,200.
   c. Select the NXP LPC2368 device.
   d. Set the interface to none (ISP).
   e. Set the DOscillator frequency (MHz) to 12.0.
   f. Select **Erase all Flash + Code Rd Block**.
   g. Choose **ADE7878_Eval_Board.hex** from the **\Debug\Exe** project folder.
   h. Select **Verify after programming**.

   The Flash Magic settings are shown in Figure 36.

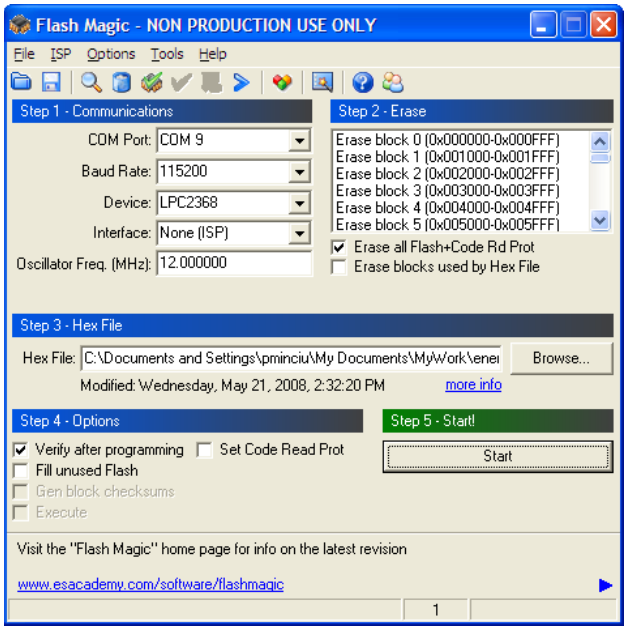


Figure 36. Flash Magic Settings

8. Click **Start** to begin the download process.
9. After the process finishes, extract the JP8 jumper.
10. Reset the ADE7878 evaluation board by pressing and releasing the S2 reset button.

At this point, the program should be functional, and a USB cable can be connected to the board. When the PC recognizes the evaluation board and asks for a driver, point it to the project **\VirCOM_Driver_XP** folder. The **ADE7878_eval_board_vircomport.inf** file is the driver.

CONTROL REGISTERS DATA FILE

Table 26 shows the order in which the control registers of the ADE7878 are stored into a data file when you click the **Save All Regs into a file** button in the **All Registers Access** panel.

Table 26. Control Register Data File Content

Line Number	Register
1	AIGAIN
2	AVGAIN
3	BIGAIN
4	BVGAIN
5	CIGAIN
6	CVGAIN
7	NIGAIN
8	AIRMSOS
9	AVRMSOS
10	BIRMSOS
11	BVRMSOS
12	CIRMSOS
13	CVRMSOS
14	NIRMSOS
15	AVAGAIN
16	BVAGAIN
17	CVAGAIN
18	AWGAIN
19	AWATTOS
20	BWGAIN
21	BWATTOS
22	CWGAIN
23	CWATTOS
24	AVARGAIN
25	AVAROS
26	BVARGAIN
27	BVAROS
28	CVARGAIN
29	CVAROS
30	AFWGAIN
31	AFWATTOS
32	BFWGAIN
33	BFWATTOS
34	CFWGAIN
35	CFWATTOS
36	AFVARGAIN
37	AFVAROS
38	BFVARGAIN
39	BFVAROS
40	CFVARGAIN
41	CFVAROS
42	VATHR1
43	VATHR0
44	WTHR1
45	WTHR0
46	VARTHR1
47	VARTHR0
48	VANOLOAD
49	APNOLOAD
50	VARNOLOAD
51	VLEVEL
52	DICOEFF
53	HPFDIS
54	ISUMLVL
55	RUN
56	OILVL
57	OVLVL
58	SAGLVL
59	MASK0
60	MASK1
61	VNOM
62	LINECYC
63	ZXTOUT
64	COMPMODE
65	Gain
66	CFMODE
67	CF1DEN
68	CF2DEN
69	CF3DEN
70	APHCAL
71	BPHCAL
72	CPHCAL
73	CONFIG
74	MMODE
75	ACCMODE
76	LCYCMODE
77	PEAKCYC
78	SAGCYC
79	CFCYC
80	HSDC_CFG
81	LPOILVL
82	CONFIG2

EVALUATION BOARD SCHEMATICS AND LAYOUT

SCHEMATIC

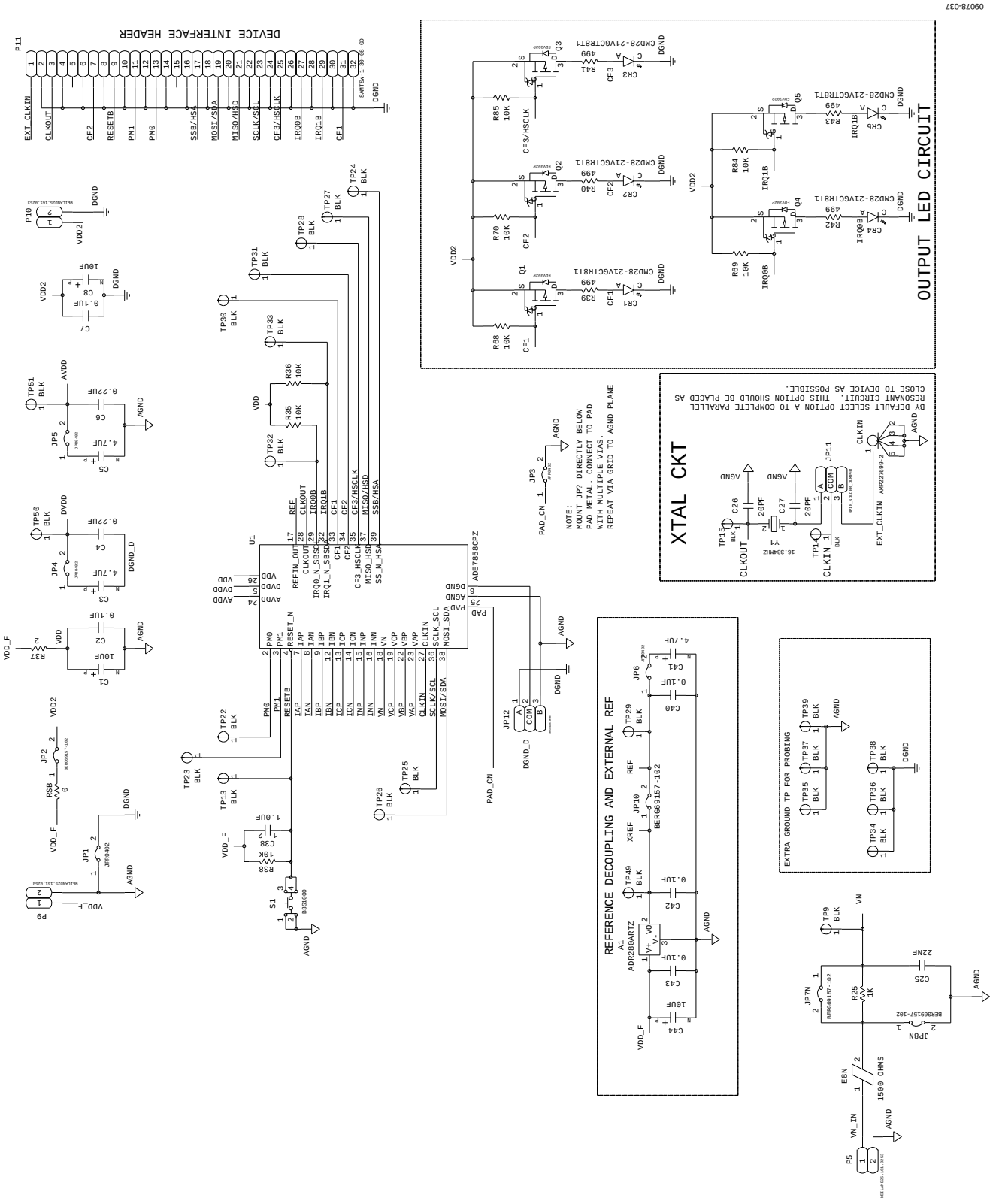


Figure 37.

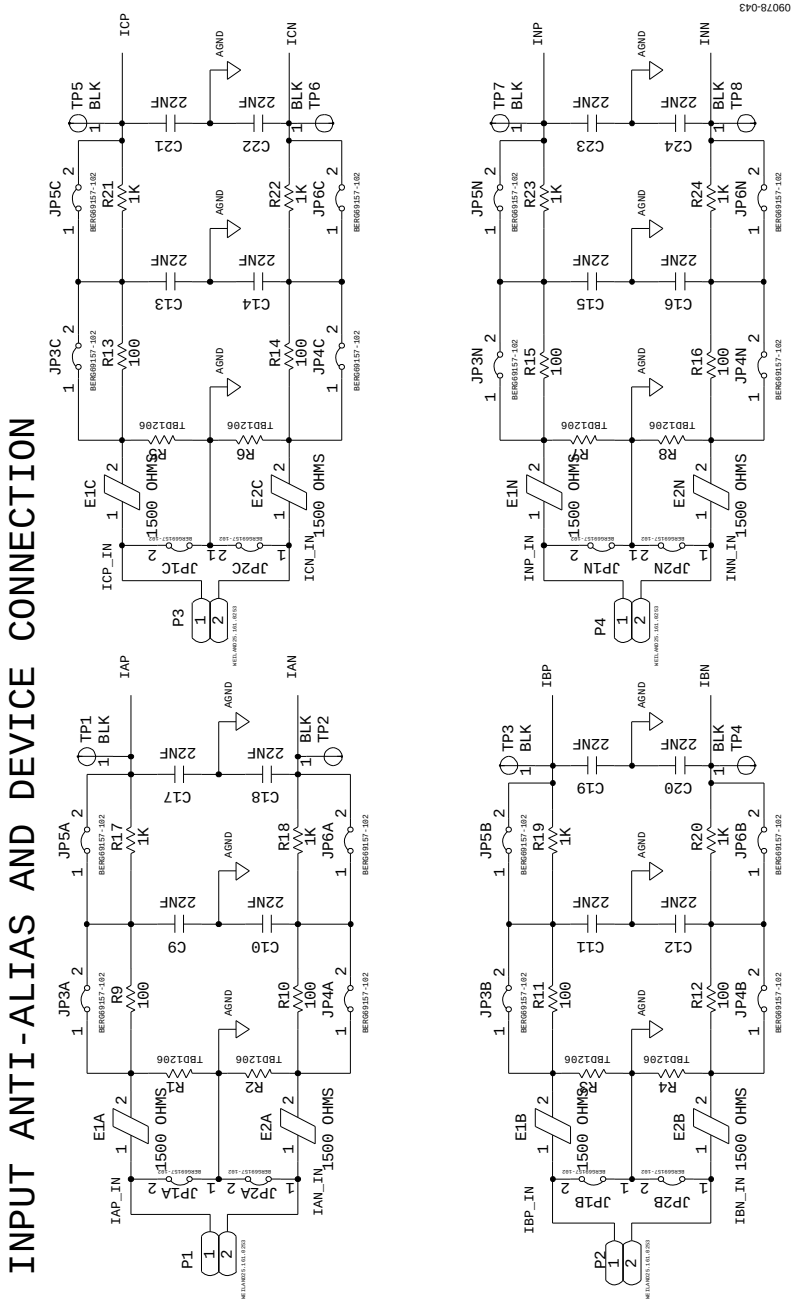

INPUT ANTI-ALIAS AND DEVICE CONNECTION
09078-043
IAP
IAN
ICP
ICN
IBP
IBN
INP
INN
AGND
1500 OHMS
22NF
1K
100
TBD1206
BERG69157-102
P1
P2
P3
P4

Figure 38.

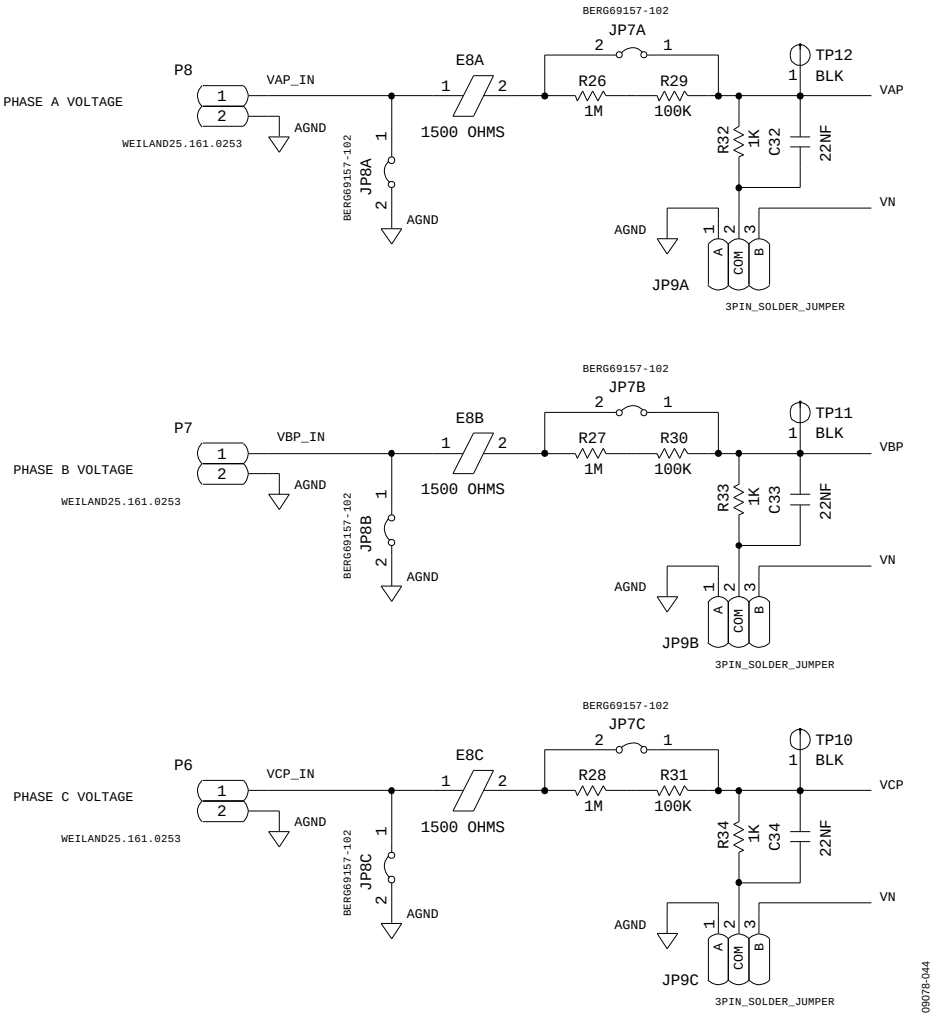

BERG69157-102
JP7A
P8
VAP_IN
E8A
TP12
BLK
PHASE A VOLTAGE
R26
1M
R29
100K
VAP
AGND
WEILAND25.161.0253
1500 OHMS
R32
1K
C32
22NF
BERG69157-102
JP8A
VN
AGND
JP9A
3PIN_SOLDER_JUMPER
BERG69157-102
JP7B
P7
VBP_IN
E8B
TP11
BLK
PHASE B VOLTAGE
R27
1M
R30
100K
VBP
AGND
WEILAND25.161.0253
1500 OHMS
R33
1K
C33
22NF
BERG69157-102
JP8B
VN
AGND
JP9B
3PIN_SOLDER_JUMPER
BERG69157-102
JP7C
P6
VCP_IN
E8C
TP10
BLK
PHASE C VOLTAGE
R28
1M
R31
100K
VCP
AGND
WEILAND25.161.0253
1500 OHMS
R34
1K
C34
22NF
BERG69157-102
JP8C
VN
AGND
JP9C
3PIN_SOLDER_JUMPER
09078-044

Figure 39.

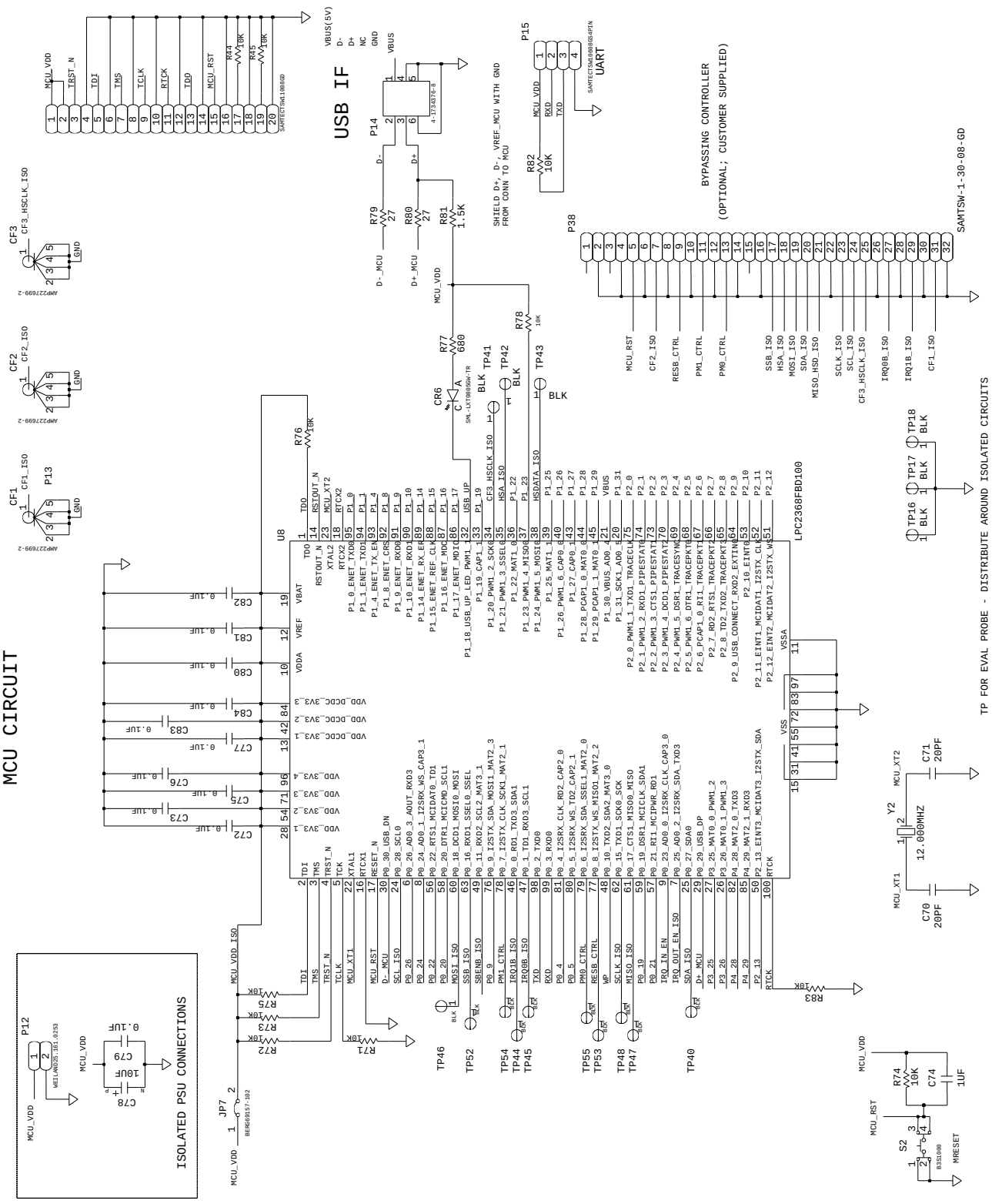

MCU CIRCUIT
ISOLATED PSU CONNECTIONS
USB IF
BYPASSING CONTROLLER
(OPTIONAL; CUSTOMER SUPPLIED)
TP FOR EVAL PROBE - DISTRIBUTE AROUND ISOLATED CIRCUITS
LPC2368FBD100
SAMTSW-1-30-08-GD
UART
MCU_VDD
MCU_VDD_ISO
MCU_RST
MCU_XT1
MCU_XT2
12.000MHZ
MRESET
VBUS(5V)
D-
D+
NC
GND
VBUS
SHIELD D+, D-, VREF_MCU WITH GND
FROM CONN TO MCU
CF1_ISO
CF2_ISO
CF3_HSCLK_ISO
MCU_RST
RESB_CTRL
PM1_CTRL
PM0_CTRL
SSB_ISO
HSA_ISO
MOSI_ISO
SDA_ISO
MISO_HSD_ISO
SCLK_ISO
SCL_ISO
IRQ0B_ISO
IRQ1B_ISO
CF1_ISO
ISOLATED PSU CONNECTIONS

Figure 40.

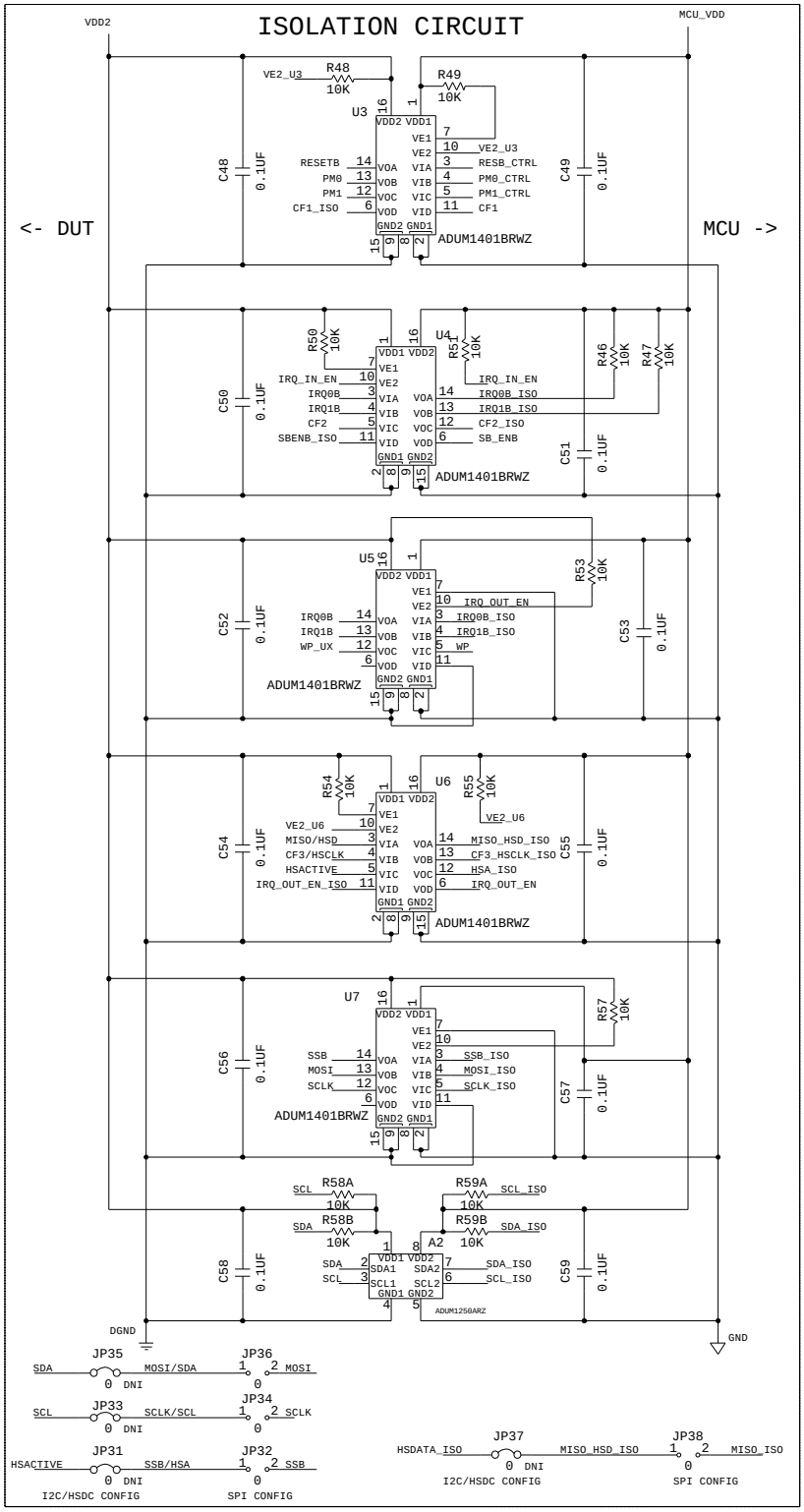

ISOLATION CIRCUIT
VDD2
MCU_VDD
<- DUT
MCU ->
U3
U4
U5
U6
U7
ADUM1401BRWZ
ADUM1250ARZ
R48
R49
R50
R51
R53
R54
R55
R57
R58A
R58B
R59A
R59B
10K
C48
C49
C50
C51
C52
C53
C54
C55
C56
C57
C58
C59
0.1UF
VE2_U3
RESETB
PM0
PM1
CF1_ISO
RESB_CTRL
PM0_CTRL
PM1_CTRL
CF1
IRQ_IN_EN
IRQ0B
IRQ1B
CF2
SBENB_ISO
IRQ0B_ISO
IRQ1B_ISO
CF2_ISO
SB_ENB
IRQ_OUT_EN
WP_UX
WP
VE2_U6
MISO/HSD
CF3/HSCLK
HSACTIVE
IRQ_OUT_EN_ISO
MISO_HSD_ISO
CF3_HSCLK_ISO
HSA_ISO
SSB
MOSI
SCLK
SSB_ISO
MOSI_ISO
SCLK_ISO
SCL
SDA
SCL_ISO
SDA_ISO
A2
DGND
GND
JP35
JP36
JP33
JP34
JP31
JP32
JP37
JP38
SDA
MOSI/SDA
MOSI
SCL
SCLK/SCL
SCLK
HSACTIVE
SSB/HSA
SSB
HSDATA_ISO
MISO_HSD_ISO
MISO_ISO
DNI
I2C/HSDC CONFIG
SPI CONFIG
09078-045

Figure 41.

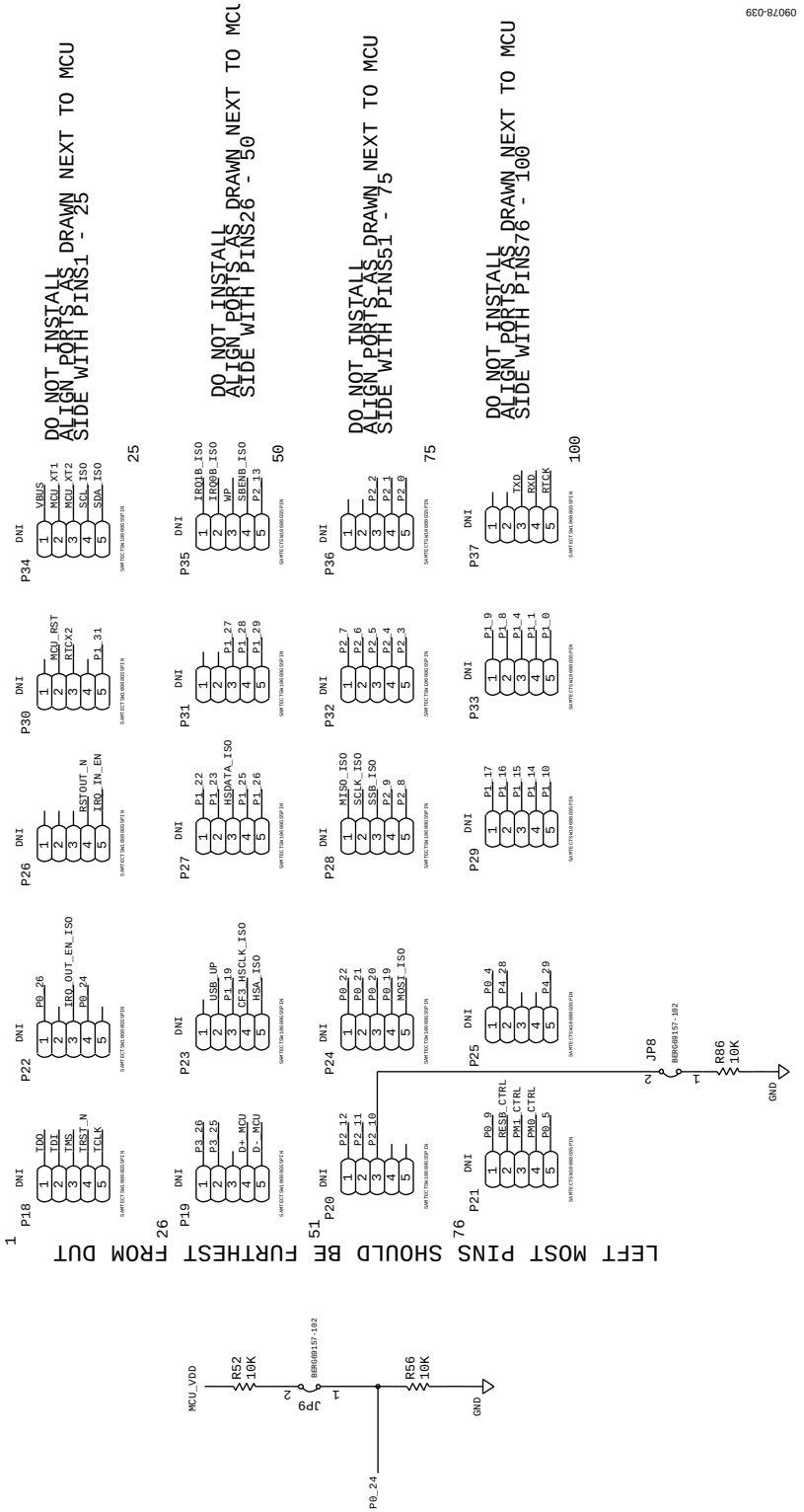

09078-039
DO NOT INSTALL
ALIGN PORTS AS DRAWN NEXT TO MCU
SIDE WITH PINS1 - 25
DO NOT INSTALL
ALIGN PORTS AS DRAWN NEXT TO MCU
SIDE WITH PINS26 - 50
DO NOT INSTALL
ALIGN PORTS AS DRAWN NEXT TO MCU
SIDE WITH PINS51 - 75
DO NOT INSTALL
ALIGN PORTS AS DRAWN NEXT TO MCU
SIDE WITH PINS76 - 100
LEFT MOST PINS SHOULD BE FURTHEST FROM DUT
P18
P19
P20
P21
P22
P23
P24
P25
P26
P27
P28
P29
P30
P31
P32
P33
P34
P35
P36
P37
JP8
BERG69157-102
R86
10K
GND
MCU_VDD
R52
10K
JP9
R56
10K
P0_24

Figure 42.

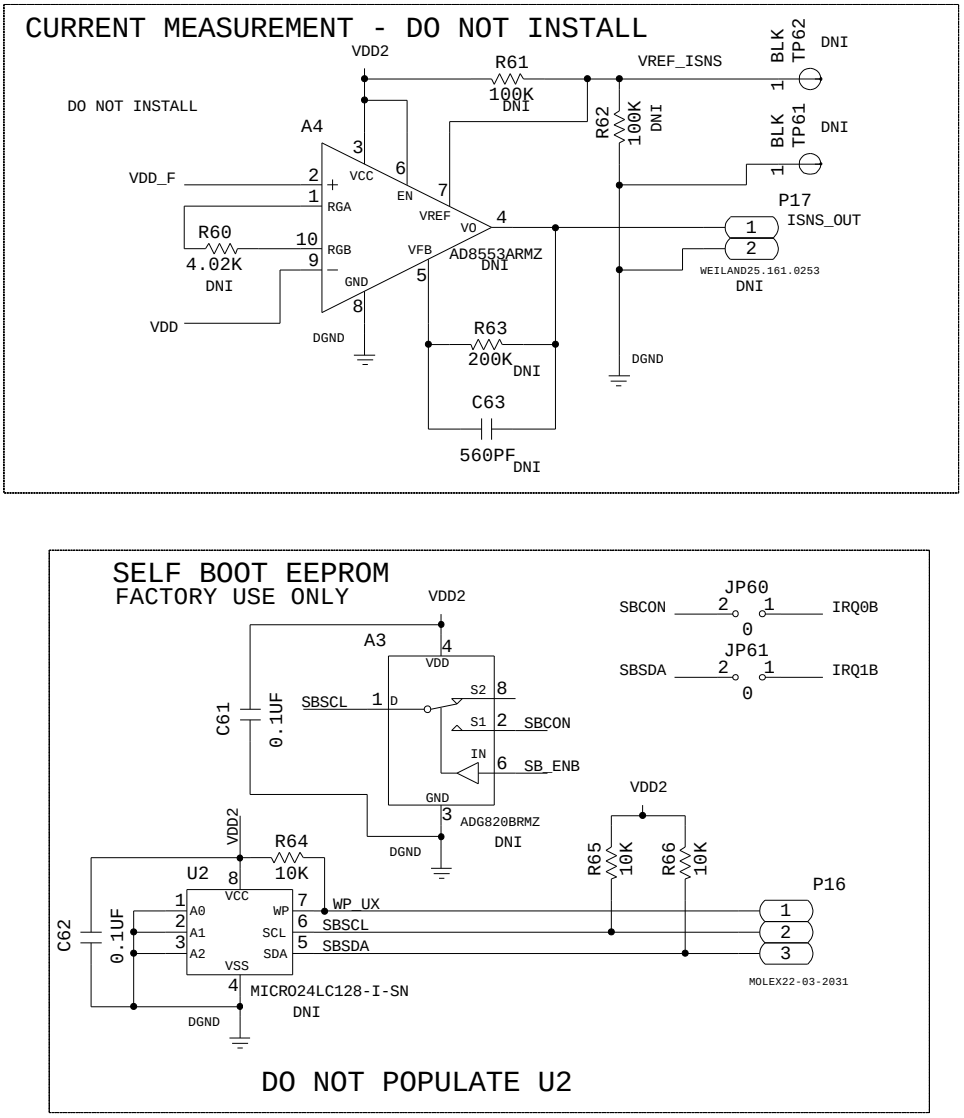

CURRENT MEASUREMENT - DO NOT INSTALL
DO NOT INSTALL
VDD2
R61
100K
DNI
VREF_ISNS
BLK TP62
DNI
R62
100K
DNI
BLK TP61
DNI
A4
VDD_F
VCC
EN
VREF
VO
RGA
RGB
VFB
GND
AD8553ARMZ
DNI
R60
4.02K
DNI
P17
ISNS_OUT
WEILAND25.161.0253
DNI
VDD
DGND
R63
200K
DNI
C63
560PF
DNI
DGND
SELF BOOT EEPROM
FACTORY USE ONLY
VDD2
A3
VDD
C61
0.1UF
SBSCL
S2
S1
SBCON
IN
SB_ENB
GND
ADG820BRMZ
DNI
DGND
JP60
SBCON
IRQ0B
JP61
SBSDA
IRQ1B
R65
10K
R66
10K
R64
10K
U2
VCC
A0
A1
A2
VSS
WP
SCL
SDA
WP_UX
SBSCL
SBSDA
P16
MOLEX22-03-2031
C62
0.1UF
MICRO24LC128-I-SN
DNI
DO NOT POPULATE U2
09078-046

Figure 43.

LAYOUT

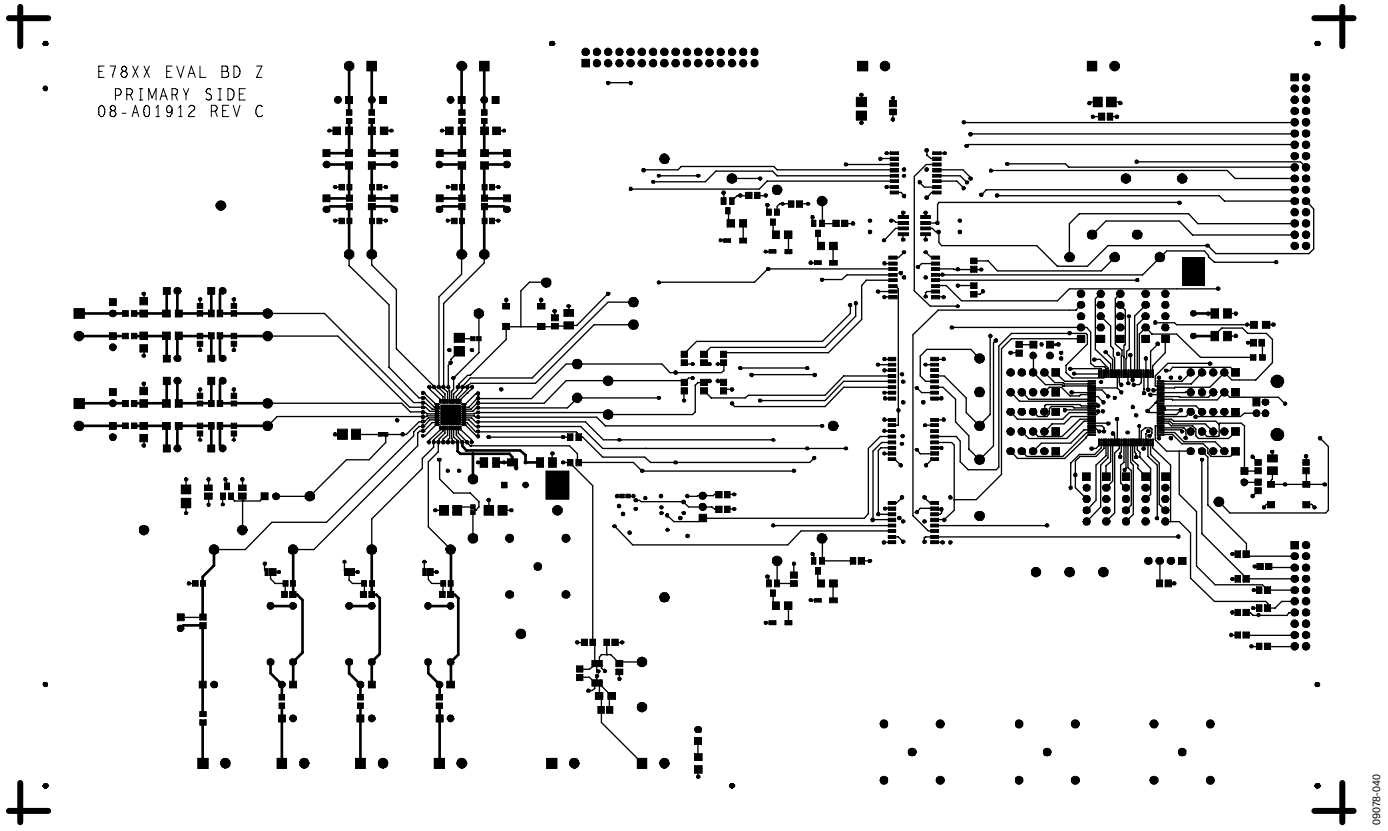


Figure 44.

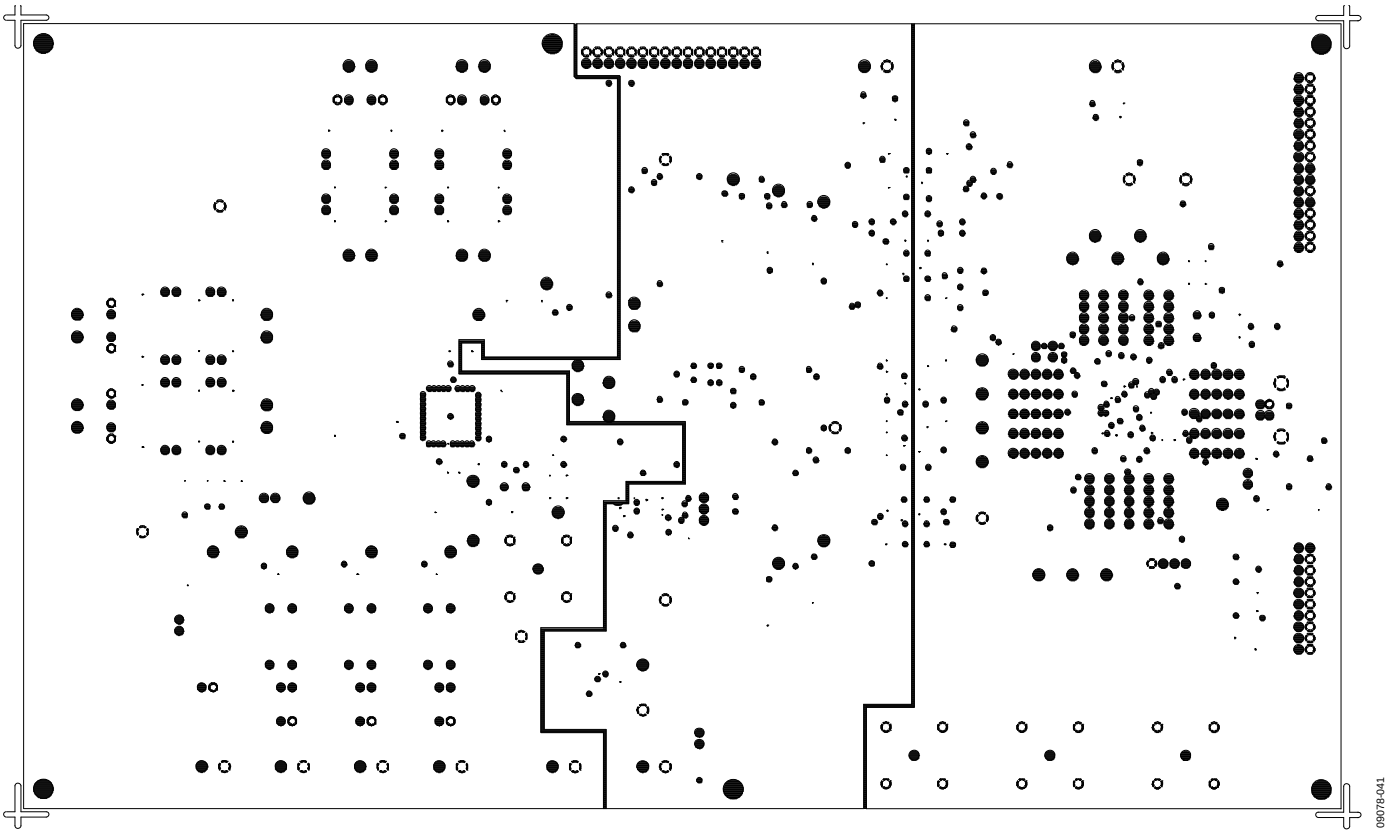


Figure 45.

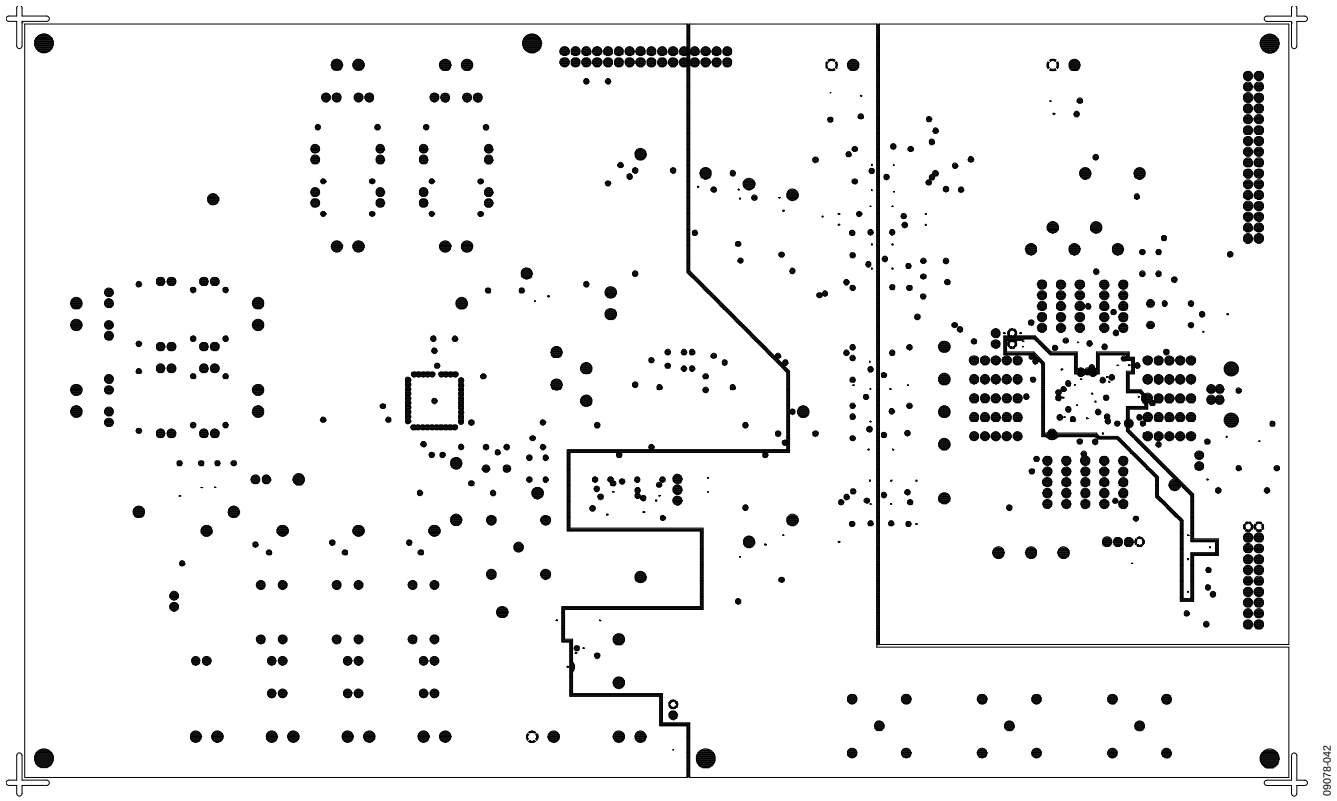


Figure 46.

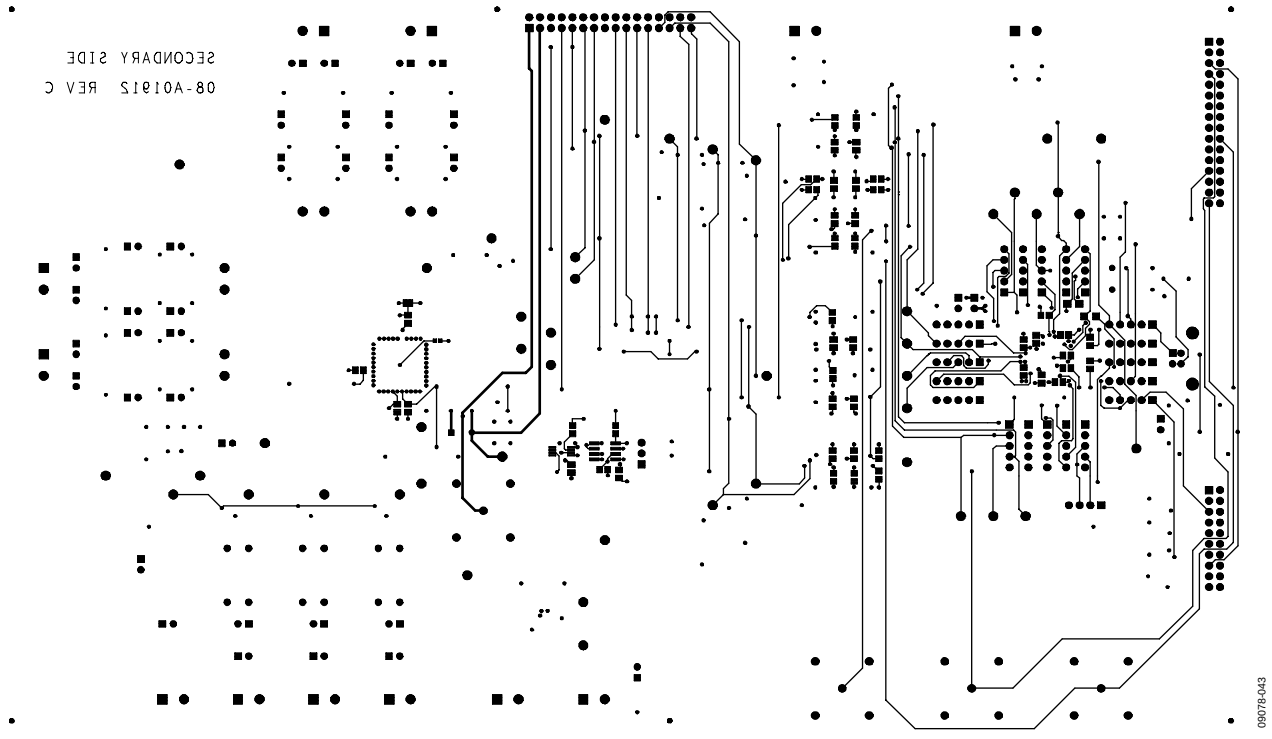


Figure 47.

ORDERING INFORMATION

BILL OF MATERIALS

Table 27.

Qty	Designator	Description	Manufacturer/Part Number
1	A1	IC-ADI, 1.2 V, ultralow power, high PSRR voltage reference	Analog Devices, Inc./ADR280ARTZ
1	A2	IC swappable dual isolator	Analog Devices, Inc./ADUM1250ARZ
4	C1, C8, C44, C78	Capacitor, tantalum, 10 µF	AVX
20	C9 to C25, C32 to C34	Capacitor, ceramic, 22 nF	AVX
30	C2, C7, C40, C42, C43, C48 to C59, C61, C62, C72, C73, C75 to C77, C79 to C84	Capacitor, chip, X7R 0805, 0.1 µF	Murata
4	C26, C27, C70, C71	Capacitor, mono, ceramic, C0G, 0402, 20 pF	Murata
3	C3, C5, C41	Capacitor, tantalum, 4.7 µF	AVX
2	C38, C74	Capacitor, ceramic chip, 1206, X7R, 1.0 µF	Taiyo Yuden
2	C4, C6	Capacitor, ceramic, X7R, 0.22 µF	Phycomp (Yageo)
4	CF1 to CF3, CLKIN	Connector, PCB coax, BNC, ST	AMP (Tyco)/227699-2
5	CR1 to CR5	Diode, LED, green, SMD	Chicago Mini Lamp (CML Innovative Technologies)/CMD28-21VGCTR8T1
1	CR6	LED, green, surface mount	LUMEX/SML-LXT0805GW-TR
12	E1A, E1B, E1C, E1N, E2A, E2B, E2C, E2N, E8A, E8B, E8C, E8N	Inductor, chip, ferrite bead, 0805, 1500 Ω	Murata
37	JP2, JP7 to JP10, JP1A to JP8A, JP1B to JP8B, JP1C to JP8C, JP1N to JP8N	Connector, PCB Berg jumper, ST, male 2-pin	Berg/69157-102
5	JP11, JP12, JP9A, JP9B, JP9C	3-pin solder jumper	N/A
6	JP32, JP34, JP36, JP38, JP60, JP61	Resistor jumper, SMD 0805 (open), 0 Ω	Panasonic
11	P1 to P10, P12	Connector, PCB TERM, black, 2-pin, ST	WeilandD/25.161.0253
2	P11, P38	Connector, PCB, header, SHRD, ST, male 32-pin	Samtec/TSW-1-30-08-G-D
1	P13	Connector, PCB, Berg, header, ST, male 20-pin	Samtec/TSW-110-08-G-D
1	P14	Connector, PCB, USB, Type B, R/A, through hole	AMP (Tyco)/4-1734376-8
1	P15	Connector, PCB, Berg, header, ST, male 4-pin	Samtec/TSW106-08-G-S
1	P16	Connector, PCB straight header 3-pin	Molex/22-03-2031
5	Q1 to Q5	Trans digital FET P channel	Fairchild/FDV302P
8	R1 to R8	Do not install (TBD_R1206)	N/A
8	R9 to R16	Resistor, PREC, thick film chip, R1206, 100 Ω	Panasonic
12	R17 to R25, R32 to R34	Resistor, PREC, thick film chip, R0805, 1 kΩ	Panasonic
3	R26 to R28	Resistor, MF, RN55, 1 M	Vishay-Dale
3	R29 to R31	Resistor, MF, RN5, 100 kΩ	Vishay-Dale
39	R35, R36, R38, R44 to R57, R64 to R66, R68 to R76, R78, R82 to R86, R58A, R58B, R59A, R59B	Resistor PREC thick film chip, R0805, 10 kΩ	Panasonic
1	R37	Resistor, film, SMD 0805, 2 Ω	Panasonic
5	R39 to R43	Resistor, PREC, thick film chip, R1206, 499	Panasonic
1	R77	Resistor, film, SMD, 0805, 680 Ω	Multicomp
2	R79, R80	Resistor, film, SMD, 1206, 27 Ω	Yageo-Phycomp
1	R81	Resistor, PREC, thick film chip, R1206, 1.5 kΩ	Panasonic
1	RSB	Resistor, jumper, SMD, 1206 (open), 0	Panasonic
2	S1, S2	SW SM mechanical key switch	Omron/B3S1000
52	TP1 to TP18, TP22 to TP55	Connector, PCB, test point, black	Components Corporation
1	U1	IC-ADI, polyphase, multifunction, energy metering IC	Analog Devices, Inc./ADE7878CPZ
5	U3 to U7	IC-ADI quad channel digital isolator	Analog Devices, Inc./ADum1401BRWZ
1	U8	IC ARM7, MCU, flash, 512 kΩ, 100 LQFP	NXP/LPC2368FBD100

Qty	Designator	Description	Manufacturer/Part Number
1	Y1	IC crystal, 16.384 MHz	Valpey Fisher Corporation
1	Y2	IC crystal quartz, 12.000 MHz	ECS
1	A3	IC-ADI 1.8 V to 5.5 V 2:1 MUX/SPDT switches	Analog Devices, Inc./ADG820BRMZ
1	A4	IC-ADI 1.8 V to 5 V auto-zero in amp with shutdown	Analog Devices, Inc./AD8553ARMZ
1	C63	Capacitor, ceramic, NP0, 560 pF	Phycomp (Yageo)
4	JP31, JP33, JP35, JP37	Resistor, jumper, SMD, 0805 (SHRT), 0	Panasonic
1	P17	Connector, PCB, TERM, black, 2-pin, ST	Weiland/25.161.0253
20	P18 to P37	Connector, PCB, Berg, header, ST, male 5-pin	Samtec/TSW106-08-G-S
1	R60	Resistor, PREC, thick film chip, R0805, 4.02 kΩ	Panasonic
2	R61, R62	Resistor, PREC, thick film chip, R0805, 100 kΩ	Panasonic
1	R63	Resistor, PREC, thick film chip, R1206, 200 kΩ	Panasonic
2	TP61, TP62	Connector, PCB test point, black	Components Corporation
1	U2	IC, serial EEPROM, 128 kΩ, 2.5 V	Microchip/24LC128-I-SN

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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