FDMS86300DC

POWERTRENCH® MOSFET, N-Channel, DUAL COOL® 56

80 V, 110 A, 3.1 mΩ

General Description

This N−Channel MOSFET is produced using Fairchild Semiconductor's advanced POWERTRENCH® process that incorporates Shielded Gate technology. Advancements in both silicon and DUAL COOL® package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction−to−Ambient thermal resistance.

Features

- DUAL COOL Top Side Cooling PQFN package
- Max $r_{DS(on)}$ = 3.1 mΩ at V_{GS} = 10 V, I_D = 24 A
- Max $r_{DS(on)}$ = 4.0 mΩ at V_{GS} = 8 V, I_D = 21 A
- High performance technology for extremely low $r_{DS(on)}$
- 100% UIL Tested
- RoHS Compliant

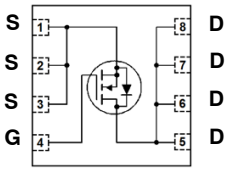
Typical Applications

- Synchronous Rectifier for DC/DC Converters
- Telecom Secondary Side Rectification
- High End Server/Workstation Vcore Low Side

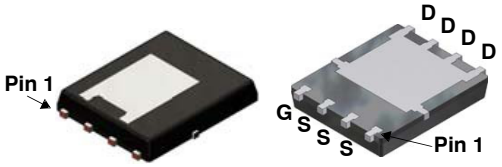
ON Semiconductor®

www.onsemi.com

ELECTRICAL CONNECTION



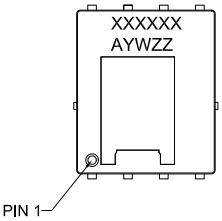
N-Channel MOSFET



Top **Bottom**

DFN8 5.1x6.15
(Dual Cool 56)
CASE 506EG

MARKING DIAGRAM



XXXXXX	= Device Code
A	= Assy Location
Y	= Year Code
WW	= Work Week Code
ZZ	= Assy Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

© Semiconductor Components Industries, LLC, 2013

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Shipping†
86300	FDMS86300DC	UDFN8	13”	12 mm	3000 Units/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter				Ratings	Units
V_{DS}	Drain to Source Voltage				80	V
V_{GS}	Gate to Source Voltage				±20	V
I_D	Drain Current	–Continuous	T_C = 25°C		110	A
		–Continuous	T_A = 25°C	(Note 1a)	24	
		–Pulsed		(Note 2)	260	
E_{AS}	Single Pulse Avalanche Energy			(Note 3)	240	mJ
P_D	Power Dissipation		T_C = 25°C		125	W
	Power Dissipation		T_A = 25°C	(Note 1a)	3.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range				–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		45		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.5	3.3	4.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		–11		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 24 A		2.6	3.1	mΩ
		V_{GS} = 8 V, I_D = 21 A		3.1	4.0	
		V_{GS} = 10 V, I_D = 24 A, T_J = 125°C		4.1	5.0	
g_{FS}	Forward Transconductance	V_{DD} = 10 V, I_D = 24 A		79		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		5265	7005	pF
C_{OSS}	Output Capacitance			929	1235	pF
C_{RSS}	Reverse Transfer Capacitance			21	50	pF
R_G	Gate Resistance		0.1	1.2	2.6	Ω

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
SWITCHING CHARACTERISTICS						
$td_{(ON)}$	Turn – On Delay Time	V_{DD} = 40 V, I_D = 24 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		29	47	ns
t_r	Rise Time			25	44	ns
$t_{D(OFF)}$	Turn – Off Delay Time			35	57	ns
t_f	Fall Time			9	18	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 40 V, I_D = 24 A		72	101	nC
	Total Gate Charge	V_{GS} = 0 V to 8 V, V_{DD} = 40 V, I_D = 24 A		59	84	nC
Q_{gs}	Gate to Source Gate Charge			26		nC
Q_{gd}	Gate to Drain "Miller" Charge			14		nC
DRAIN–SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.7 A (Note 2)		0.72	1.2	V
		V_{GS} = 0 V, I_S = 24 A (Note 2)		0.80	1.3	
I_S	Source to Drain Diode Forward Voltage	T_C = 25°C			75	V
					150	
t_{rr}	Reverse Recovery Time	I_F = 24 A, di/dt = 100 A/μs		56	88	ns
Q_{rr}	Reverse Recovery Charge			42	67	nC

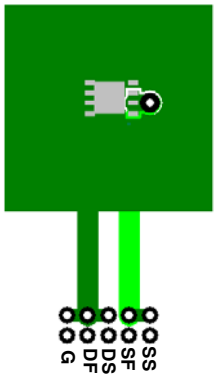
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

THERMAL CHARACTERISTICS

Symbol	Parameter		Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	2.3	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	1.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1c)	27	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1e)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1f)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1h)	61	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	11	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1l)	13	

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a FR−4 board using a specified pad of 2 oz copper as shown below. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 38°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 81°C/W when mounted on a minimum pad of 2 oz copper.

c) Still air, 20.9×10.4×12.7 mm Aluminum Heat Sink, 1 in^2 pad of 2 oz copper

d) Still air, 20.9×10.4×12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper

e) Still air, 45.2×41.4×11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, 1 in^2 pad of 2 oz copper

f) Still air, 45.2×41.4×11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, minimum pad of 2 oz copper

g) .200FPM Airflow, No Heat Sink, 1 in^2 pad of 2 oz copper

h) .200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper

i) .200FPM Airflow, 20.9×10.4×12.7 mm Aluminum Heat Sink, 1 in^2 pad of 2 oz copper

j) .200FPM Airflow, 20.9×10.4×12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper

k) .200FPM Airflow, 45.2×41.4×11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, 1 in^2 pad of 2 oz copper

l) .200FPM Airflow, 45.2×41.4×11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C; N−ch: L = 0.3 mH, I_{AS} = 40 A, V_{DD} = 72 V, V_{GS} = 10 V.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

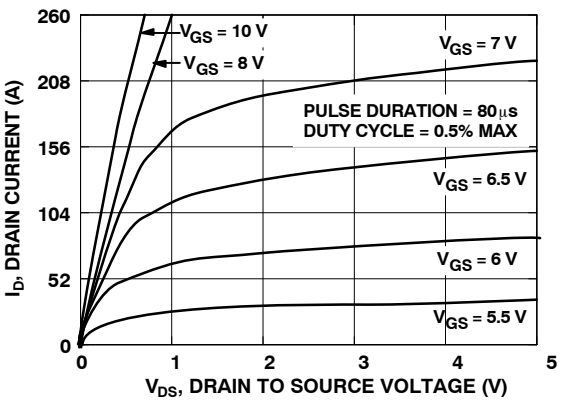


Figure 1. On Region Characteristics

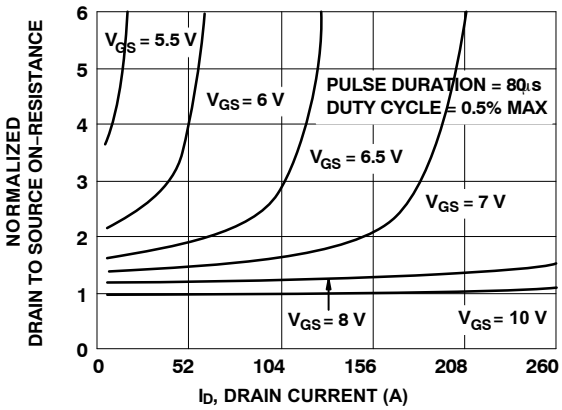


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

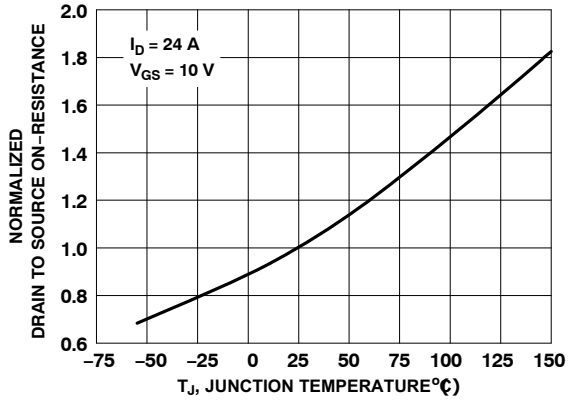


Figure 3. Normalized On Resistance vs. Junction Temperature

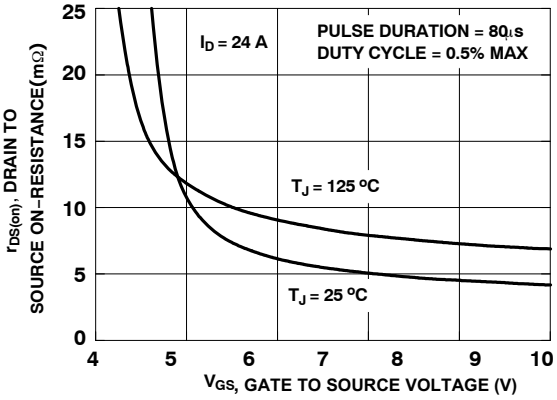


Figure 4. On-Resistance vs. Gate to Source Voltage

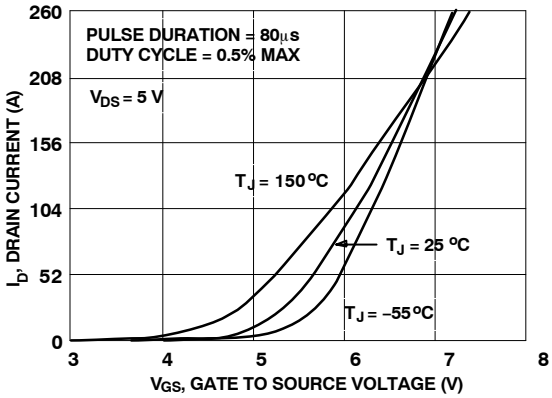


Figure 5. Transfer Characteristics

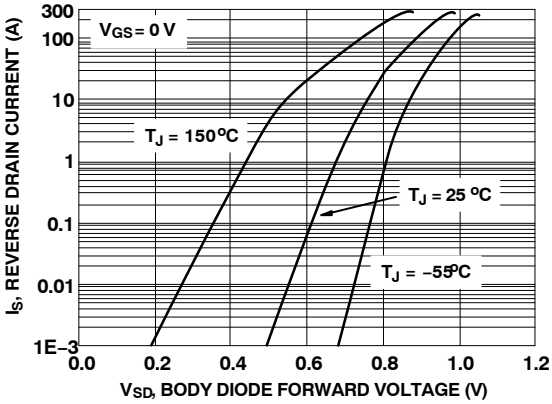


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

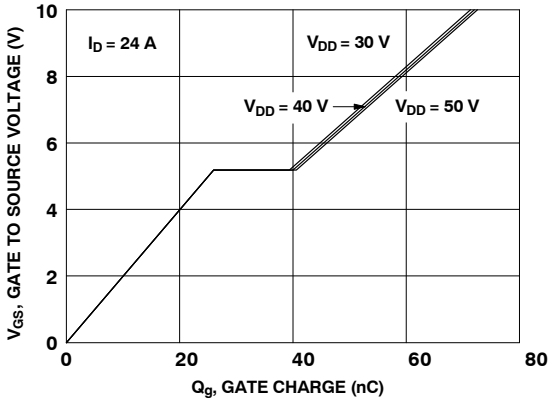


Figure 7. Gate Charge Characteristics

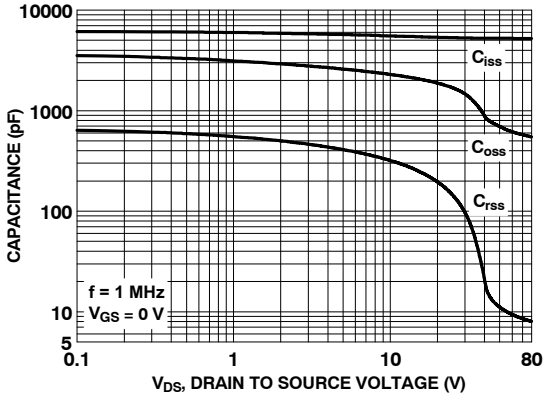


Figure 8. Capacitance vs. Drain to Source Voltage

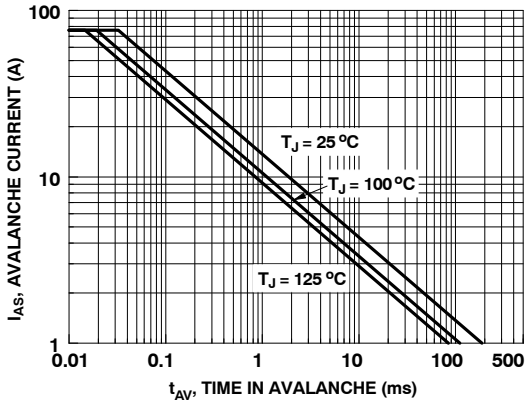


Figure 9. Unclamped Inductive Switching Capability

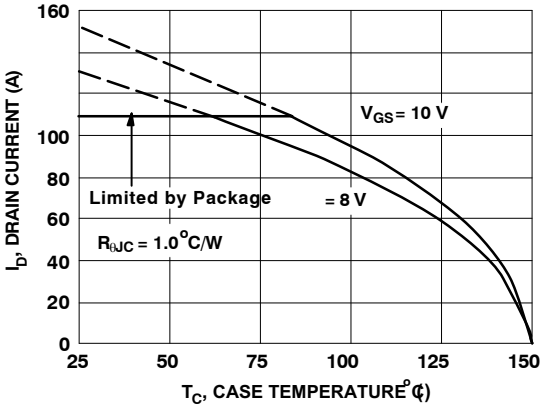


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

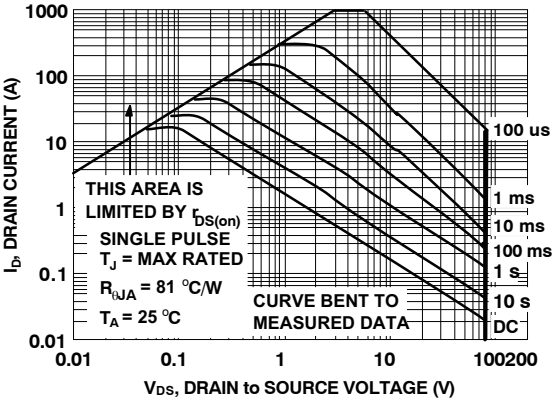


Figure 11. Forward Bias Safe Operating Area

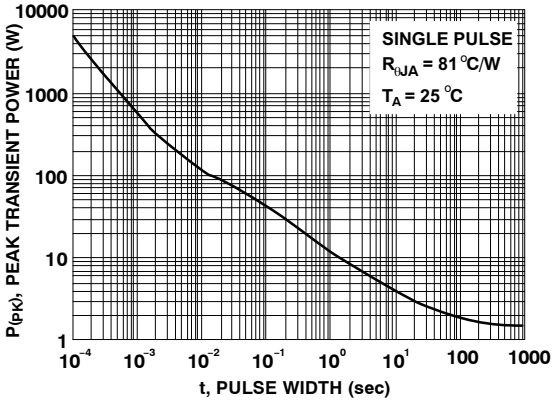


Figure 12. Single Pulse Maximum Power Dissipation

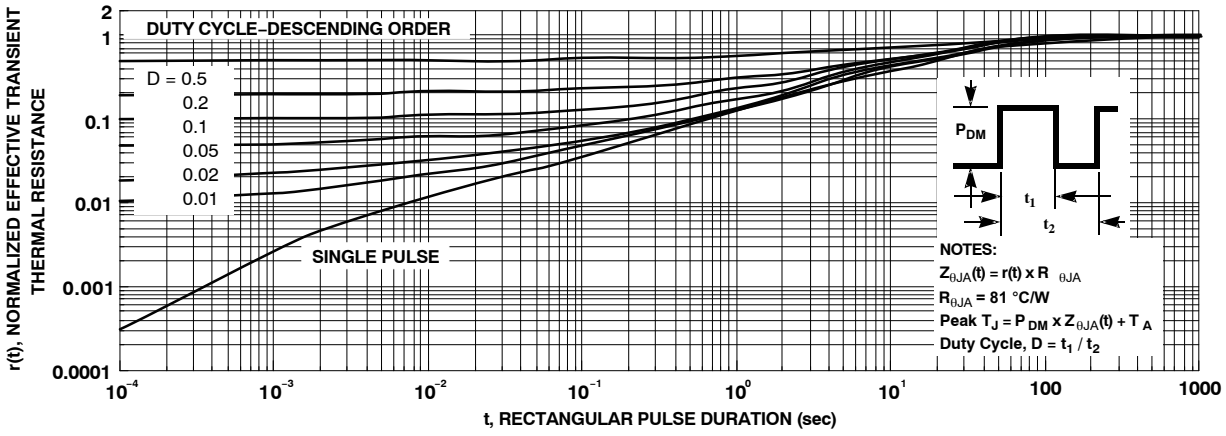
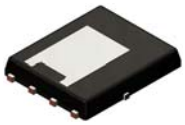


Figure 13. Junction–to–Case Transient Thermal Response Curve

POWERTRENCH and DUAL COOL are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

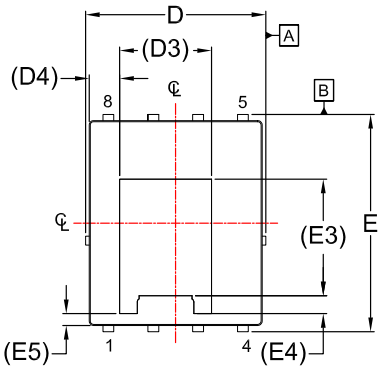
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

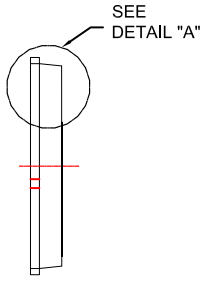


DFN8 5.1x6.15, 1.27P
CASE 506EG
ISSUE A

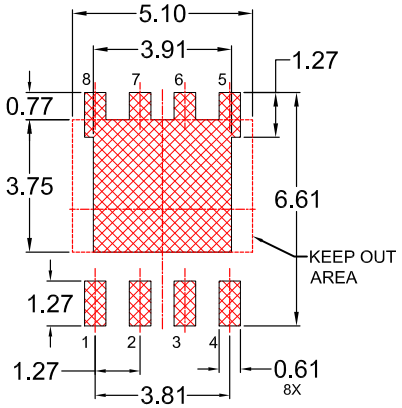
DATE 18 JUL 2018



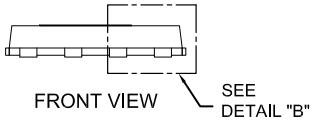
TOP VIEW

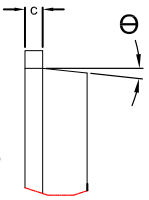


SIDE VIEW

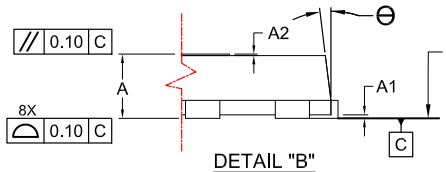


LAND PATTERN
RECOMMENDATION



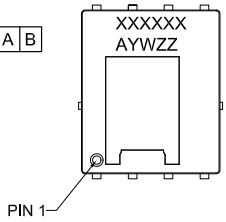


DETAIL "A"
SCALE: 2:1



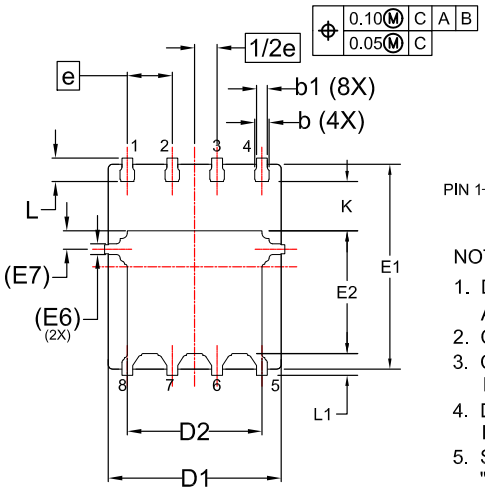
DETAIL "B"
SCALE: 2:1

GENERIC MARKING DIAGRAM



XXXXXX = DEVICE CODE
A = ASSY LOCATION
Y = YEAR CODE
W = WORK WEEK CODE
ZZ = ASSY LOT CODE

*THIS INFORMATION IS GENERIC. PLEASE REFER TO DEVICE DATA SHEET FOR ACTUAL PART MARKING.



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
Θ	0°	--	12°

DOCUMENT NUMBER:	**98AON84257G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DFN8 5.1x6.15, 1.27P**	**PAGE 1 OF 1**

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2018

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊