NBSG16

2.5 V/3.3 V SiGe Differential Receiver/Driver with RSECL* Outputs

*Reduced Swing ECL

ON Semiconductor®

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QFN−16
MN SUFFIX
CASE 485G

Description

The NBSG16 is a differential receiver/driver targeted for high frequency applications. The device is functionally equivalent to the EP16 and LVEP16 devices with much higher bandwidth and lower EMI capabilities.

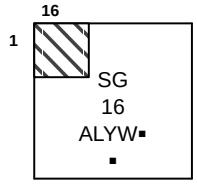
Inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), HSTL, LVTTL, LVCMOS, CML, or LVDS. Outputs are RSECL (Reduced Swing ECL), 400 mV.

The V_{BB} and V_{MM} pins are internally generated voltage supplies available to this device only. The V_{BB} is used as a reference voltage for single-ended NECL or PECL inputs and the V_{MM} pin is used as a reference voltage for LVCMOS inputs. For all single-ended input conditions, the unused complementary differential input is connected to V_{BB} or V_{MM} as a switching reference voltage. V_{BB} or V_{MM} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{MM} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} and V_{MM} outputs should be left open.

Features

- Maximum Input Clock Frequency > 12 GHz Typical
- Maximum Input Data Rate > 12 Gb/s Typical
- 120 ps Typical Propagation Delay
- 40 ps Typical Rise and Fall Times
- RSPECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- RSNECL Output with RSNECL or NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −3.465 V
- RSECL Output Level (400 mV Peak-to-Peak Output), Differential Output Only
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, and LVEL Devices
- V_{BB} and V_{MM} Reference Voltage Output
- These are Pb-Free Devices

MARKING DIAGRAMS*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

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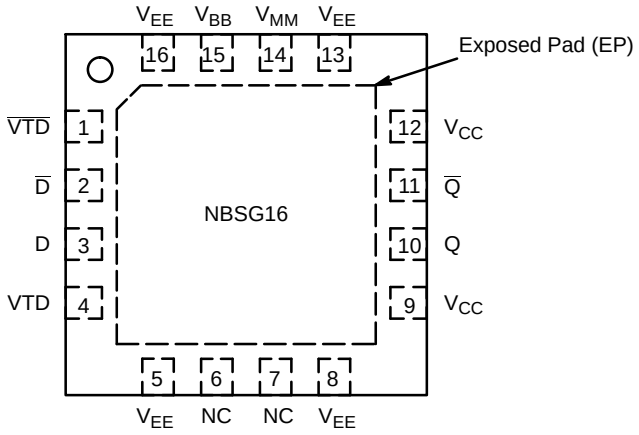


Figure 1. QFN−16 Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	$\overline{VTD}$	−	Internal 50 Ω Termination Pin. See Table 2.
2	$\overline{D}$	ECL, CML, LVCMOS, LVDS, LVTTL Input	Inverted Differential Input. Internal 75 kΩ to V_{EE} and 36.5 kΩ to V_{CC}.
3	D	ECL, CML, LVCMOS, LVDS, LVTTL Input	Noninverted differential input. Internal 75 kΩ to V_{EE}
4	VTD	−	Internal 50 Ω Termination Pin. See Table 2.
5, 8, 13, 16	V_{EE}	−	Negative Supply Voltage
6,7	NC	−	No Connect
9, 12	V_{CC}	−	Positive Supply Voltage
10	Q	RSECL Output	Noninverted Differential Output. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V
11	$\overline{Q}$	RSECL Output	Inverted Differential Output. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V
14	V_{MM}	−	LVCMOS Reference Voltage Output. $(V_{CC} - V_{EE})/2$
15	V_{BB}	−	ECL Reference Voltage Output
−	EP	−	The Exposed Pad (EP) on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die but may be electrically and thermally connected to V_{EE} on the PC board.

1. All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation. The thermally exposed pad on package bottom (see case drawing) must be attached to a heat-sinking conduit.
2. In the differential configuration when the input termination pins (VTD, $\overline{VTD}$) are connected to a common termination voltage, and if no signal is applied then the device will be susceptible to self-oscillation.

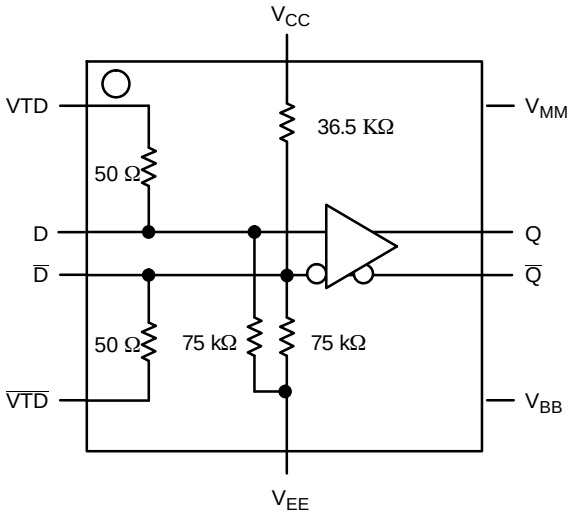


Figure 2. Logic Diagram

Table 2. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTD and $\overline{VTD}$ to V_{CC}
LVDS	Connect VTD and $\overline{VTD}$ together
AC−COUPLED	Bias VTD and $\overline{VTD}$ Inputs within (V_{IHCMR}) Common Mode Range
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL	The external voltage should be applied to the unused complementary differential input. Nominal voltage is 1.5 V for LVTTL.
LVCMOS	V_{MM} should be connected to the unused complementary differential input.

Table 3. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor (D, $\overline{D}$)		75 kΩ
Internal Input Pullup Resistor ($\overline{D}$)		36.5 kΩ
ESD Protection	Human Body Model Machine Model	> 2 kV > 100 V
Moisture Sensitivity (Note 3)	Pb-Free	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		167
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		−3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.6 −3.6	V V
V_{INPP}	Differential Input Voltage $\lvert D - \overline{D} \rvert$	$V_{CC} - V_{EE} \ge 2.8$ V $V_{CC} - V_{EE} < 2.8$ V		2.8 $\lvert V_{CC} - V_{EE} \rvert$	V
I_{out}	Output Current	Continuous Surge		25 50	mA
I_{BB}	V_{BB} Sink/Source			1	mA
I_{MM}	V_{MM} Sink/Source			1	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 4)	0 lfpm 500 lfpm		41.6 35.2	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	2S2P (Note 4)		4.0	°C/W
T_{sol}	Wave Solder Pb-Free			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT
(V_{CC} = 2.5 V; V_{EE} = 0 V) (Note 5)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
POWER SUPPLY CURRENT											
I_{EE}	Negative Power Supply Current	17	23	29	17	23	29	17	23	29	mA
RSPECL OUTPUTS (Note 6)											
V_{OH}	Output HIGH Voltage	1450	1530	1575	1525	1565	1600	1550	1590	1625	mV
V_{OUTPP}	Output Voltage Amplitude	350	410	525	350	410	525	350	410	525	mV
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 5 & 7) (Note 7)											
V_{IH}	Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{IL}	Input LOW Voltage	0		V_{IH} − 150	0		V_{IH} − 150	0		V_{IH} − 150	mV
V_{th}	Input Threshold Voltage Range (Note 8)	950		V_{CC} − 75	950		V_{CC} − 75	950		V_{CC} − 75	mV
V_{ISE}	Single-Ended Input Voltage ($V_{IH} - V_{IL}$)	150		2600	150		2600	150		260	mV
V_{BB}	PECL Output Voltage Reference	1080	1140	1200	1080	1140	1200	1080	1140	1200	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 6 & 8) (Note 9)											
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	0		V_{IHD} − 75	0		V_{IHD} − 75	0		V_{IHD} − 75	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 10) (Figure 9)	1200		2500	1200		2500	1200		2500	mV
I_{IH}	Input HIGH Current (@V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@V_{IL})		25	50		25	50		25	50	μA
LVCMOS CONTROL PIN											
V_{MM}	CMOS Output Voltage Reference V_{CC}/2	1100	1250	1400	1100	1250	1400	1100	1250	1400	mV
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with V_{CC}.
6. All loading with 50 Ω to V_{CC} − 2.0 V.
7. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously.
8. V_{th} is applied to the complementary input when operating in single-ended mode. $V_{th} = (V_{IH} - V_{IL}) / 2$.
9. V_{IHD}, V_{ILD}, V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.
10. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT
(V_{CC} = 3.3 V; V_{EE} = 0 V) (Note 11)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
POWER SUPPLY CURRENT											
I_{EE}	Negative Power Supply Current	17	23	29	17	23	29	17	23	29	mA
RSPECL OUTPUTS (Note 12)											
V_{OH}	Output HIGH Voltage	2250	2330	2375	2325	2365	2400	2350	2390	2425	mV
V_{OUTPP}	Output Voltage Amplitude	350	410	525	350	410	525	350	410	525	mV
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 5 & 7) (Note 13)											
V_{IH}	Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{IL}	Input LOW Voltage	0		V_{IH} − 150	0		V_{IH} − 150	0		V_{IH} − 150	mV
V_{th}	Input Threshold Voltage Range (Note 14)	950		V_{CC} − 75	950		V_{CC} − 75	950		V_{CC} − 75	mV
V_{ISE}	Single-Ended Input Voltage ($V_{IH} - V_{IL}$)	150		2600	150		2600	150		260	mV
V_{BB}	PECL Output Voltage Reference	1880	1940	2000	1880	1940	2000	1880	1940	2000	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 6 & 8) (Note 15)											
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	0		V_{IHD} − 75	0		V_{IHD} − 75	0		V_{IHD} − 75	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 16) (Figure 9)	1200		3300	1200		3300	1200		3300	mV
I_{IH}	Input HIGH Current (@V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@V_{IL})		25	50		25	50		25	50	μA
LVCMOS CONTROL PIN											
V_{MM}	CMOS Output Voltage Reference V_{CC}/2	1500	1650	1800	1500	1650	1800	1500	1650	1800	mV
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Input and output parameters vary 1:1 with V_{CC}.
12. All loading with 50 Ω to V_{CC} − 2.0 V.
13. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously.
14. V_{th} is applied to the complementary input when operating in single-ended mode. $V_{th} = (V_{IH} - V_{IL}) / 2$.
15. V_{IHD}, V_{ILD}, V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.
16. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. DC CHARACTERISTICS, NECL or RSNECL INPUT WITH NECL OUTPUT
(V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V) (Note 17)

		−40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
POWER SUPPLY CURRENT											
I_{EE}	Negative Power Supply Current	17	23	29	17	23	29	17	23	29	mA
RSPECL OUTPUTS (Note 18)											
V_{OH}	Output HIGH Voltage	−1050	−970	−925	−975	−935	−900	−950	−910	−875	mV
V_{OUTPP}	Output Voltage Amplitude	350	410	525	350	410	525	350	410	525	mV
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 5 & 7) (Note 19)											
V_{IH}	Input HIGH Voltage	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	mV
V_{IL}	Input LOW Voltage	V_{EE}		V_{IH} − 150	V_{EE}		V_{IH} − 150	V_{EE}		V_{IH} − 150	mV
V_{th}	Input Threshold Voltage Range (Note 20)	V_{EE} + 950		V_{CC} − 75	V_{EE} + 950		V_{CC} − 75	V_{EE} + 950		V_{CC} − 75	mV
V_{ISE}	Single-Ended Input Voltage (V_{IH} – V_{IL})	150		2600	150		2600	150		260	mV
V_{BB}	NECL Output Voltage Reference	−1420	−1360	−1300	−1420	−1360	−1300	−1420	−1360	−1300	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 6 & 8) (Note 21)											
V_{IHD}	Differential Input HIGH Voltage	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		V_{IHD} − 75	V_{EE}		V_{IHD} − 75	V_{EE}		V_{IHD} − 75	mV
V_{ID}	Differential Input Voltage (V_{IHD} – V_{ILD})	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 22) (Figure 9)	V_{EE} + 1200		0	V_{EE} + 1200		0	V_{EE} + 1200		0	mV
I_{IH}	Input HIGH Current (@V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@V_{IL})		25	50		25	50		25	50	μA
LVCMOS CONTROL PIN (Note 23)											
V_{MM}	CMOS Output Voltage Reference V_{CC}/2	V_{MM} − 150	V_{MM}	V_{MM} + 150	V_{MM} − 150	V_{MM}	V_{MM} + 150	V_{MM} − 150	V_{MM}	V_{MM} + 150	mV
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

17. Input and output parameters vary 1:1 with V_{CC}.
18. All loading with 50 Ω to V_{CC} − 2.0 V.
19. V_{th}, V_{IH}, $V_{IL,}$ and V_{ISE} parameters must be complied with simultaneously.
20. V_{th} is applied to the complementary input when operating in single-ended mode. V_{th} = (V_{IH} − V_{IL}) / 2.
21. V_{IHD}, $V_{ILD,}$ V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.
22. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
23. V_{MM} typical = $|V_{CC} - V_{EE}|/2 + V_{EE} = V_{MMT}$

Table 8. AC CHARACTERISTICS

(V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V)

		−40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Input Clock Frequency (See Figure 3. f_{max}/JITTER) (Note 24)	10.7	12		10.7	12		10.7	12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	90	110	130	100	120	140	95	125	145	ps
t_{SKEW}	Duty Cycle Skew (Note 25)		3	15		3	15		3	15	ps
t_{JITTER}	RMS Random Clock Jitter f_{in} < 10 GHz Peak−to−Peak Data Dependent Jitter f_{in} < 10 Gb/s		0.2 8	2		0.2 8	2		0.2 8	2	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 26)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times @ 1 GHz Q, $\overline{Q}$ (20% − 80%)	20	30	50	20	30	50	20	30	50	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

24. Measured using a 400 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V. Input edge rates 40 ps (20% − 80%).
25. See Figure 10. $t_{skew} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform.
26. $V_{INPP(max)}$ cannot exceed $V_{CC} - V_{EE}$

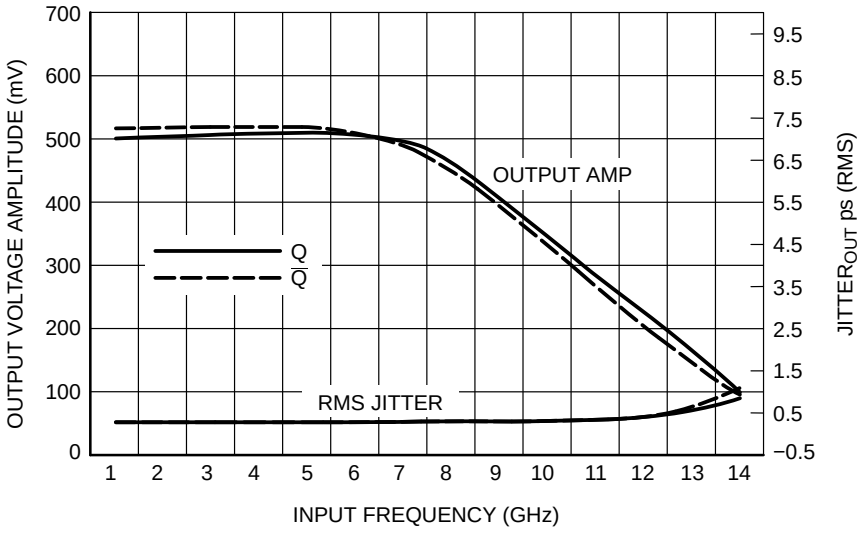
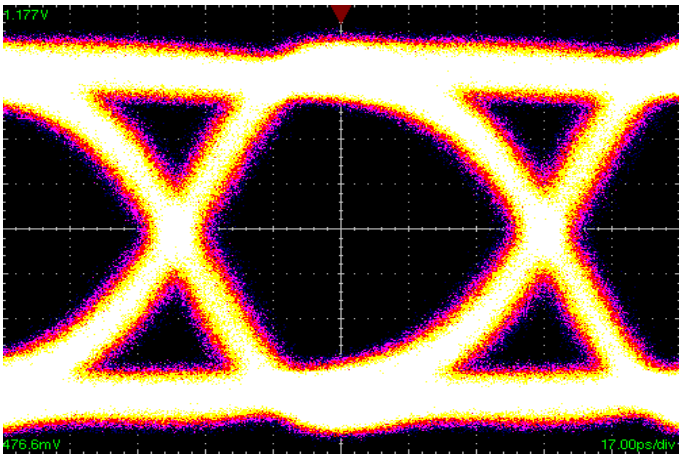


Figure 3. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)



X = 17ps/Div Y = 70 mV/Div

Figure 4. 10.709 Gb/s Diagram (3.0 V, 25°C)

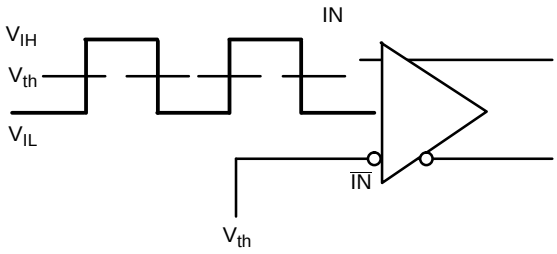


Figure 5. Differential Input Driven Single-Ended

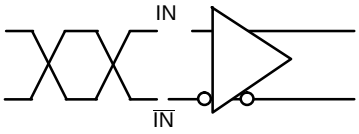


Figure 6. Differential Inputs Driven Differentially

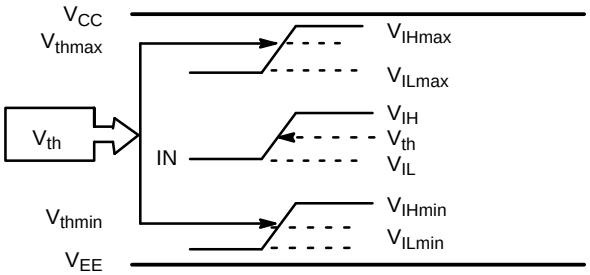


Figure 7. V_{th} Diagram

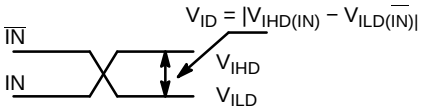


Figure 8. Differential Inputs Driven Differentially

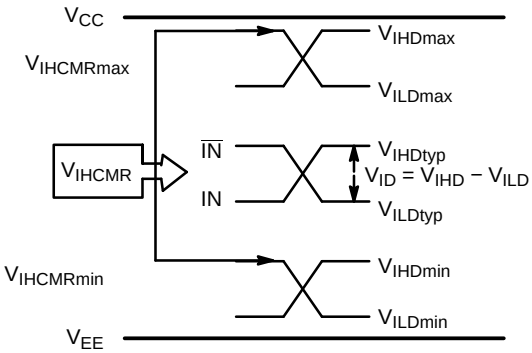


Figure 9. V_{IHCMR} Diagram

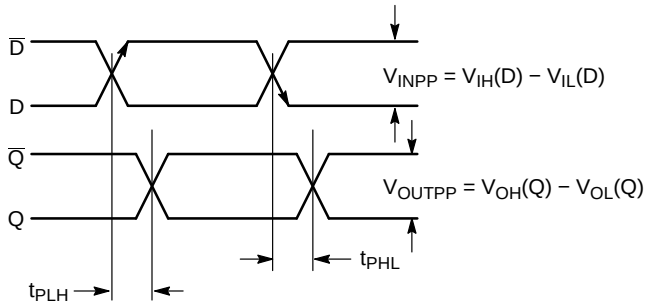


Figure 10. AC Reference Measurement

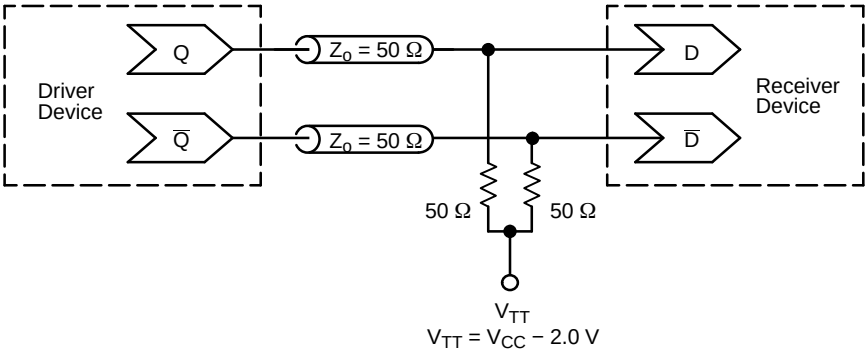


Figure 11. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

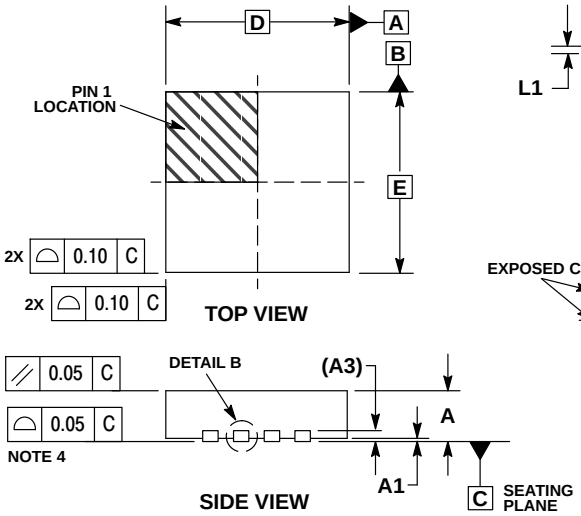
ORDERING INFORMATION

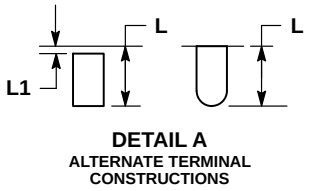
Device	Package	Shipping†
NBSG16MNG	QFN-16 (Pb-Free / Halide-Free)	123 Units / Tube
NBSG16MNR2G	QFN-16 (Pb-Free / Halide-Free)	3000 / Tape & Reel
NBSG16MNHTBG	QFN-16 (Pb-Free / Halide-Free)	100 / Tape & Reel

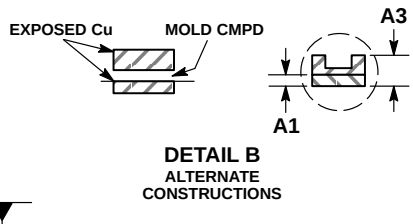
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

QFN16 3x3, 0.5P
CASE 485G
ISSUE F

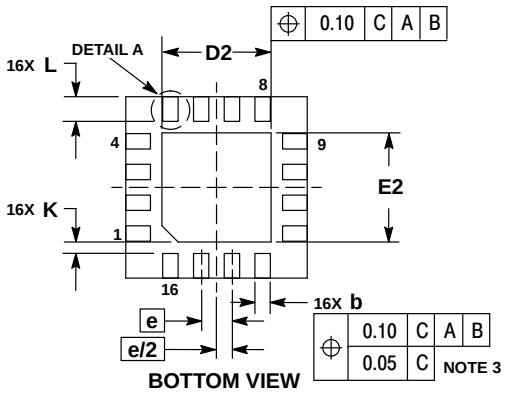




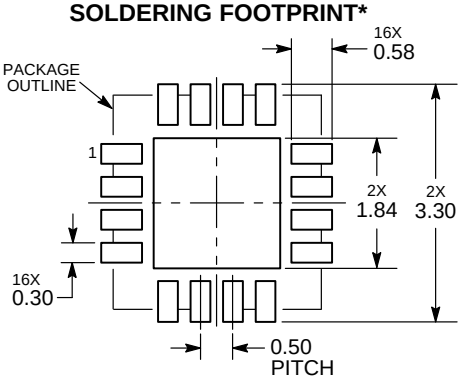


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.18	0.24	0.30
D		3.00 BSC	
D2	1.65	1.75	1.85
E		3.00 BSC	
E2	1.65	1.75	1.85
e		0.50 BSC	
K		0.18 TYP	
L	0.30	0.40	0.50
L1	0.00	0.08	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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