Pseudo Differential, 555 kSPS 12-Bit ADC in an 8-Lead SOT-23

AD7453

FEATURES

Specified for V_{DD} of 2.7 V to 5.25 V
Low power at max throughput rate:
3.3 mW max at 555 kSPS with V_{DD} = 3 V
7.25 mW max at 555 kSPS with V_{DD} = 5 V
Pseudo differential analog input
Wide input bandwidth:
70 dB SINAD at 100 kHz input frequency
Flexible power/serial clock speed management
No pipeline delays
High speed serial interface:
SPI®/QSPI™/MICROWIRE™/DSP compatible
Power-down mode: 1 µA max
8-lead SOT-23 package

APPLICATIONS

Transducer interface
Battery-powered systems
Data acquisition systems
Portable instrumentation

GENERAL DESCRIPTION

The AD7453[1] is a 12-bit, high speed, low power, successive approximation (SAR) analog-to-digital converter that features a pseudo differential analog input. This part operates from a single 2.7 V to 5.25 V power supply and features throughput rates up to 555 kSPS.

The part contains a low noise, wide bandwidth, differential track-and-hold amplifier (T/H) that can handle input frequencies up to 3.5 MHz. The reference voltage for the AD7453 is applied externally to the V_{REF} pin and can range from 100 mV to V_{DD}, depending on the power supply and what suits the application.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the device to interface with microprocessors or DSPs. The input signals are sampled on the falling edge of $\overline{CS}$; the conversion is also initiated at this point.

The SAR architecture of this part ensures that there are no pipeline delays. The AD7453 uses advanced design techniques to achieve very low power dissipation.

FUNCTIONAL BLOCK DIAGRAM

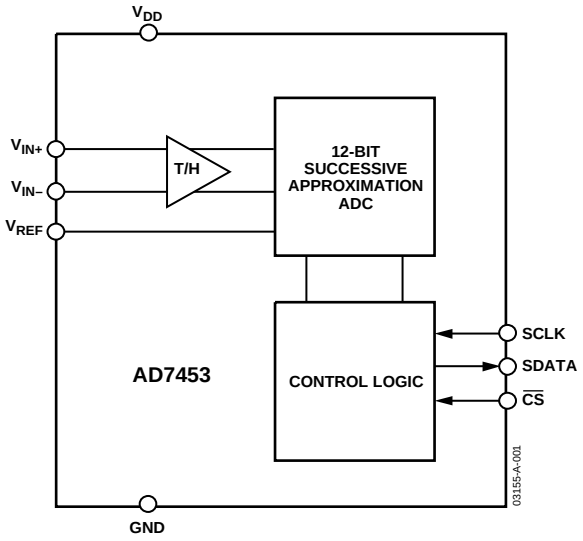


Figure 1.

PRODUCT HIGHLIGHTS

1. Operation with 2.7 V to 5.25 V Power Supplies.
2. High Throughput with Low Power Consumption. With a 3 V supply, the AD7453 offers 3.3 mW max power consumption for a 555 kSPS throughput rate.
3. Pseudo Differential Analog Input.
4. Flexible Power/Serial Clock Speed Management. The conversion rate is determined by the serial clock, allowing the power to be reduced as the conversion time is reduced through the serial clock speed increase. This part also features a shutdown mode to maximize power efficiency at lower throughput rates.
5. Variable Voltage Reference Input.
6. No Pipeline Delay.
7. Accurate control of the sampling instant via a $\overline{CS}$ input and once-off conversion control.
8. ENOB > 10 bits Typically with 500 mV Reference.

[1]Protected by U.S. Patent Number 6,681,332.

Rev. B
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REVISION HISTORY

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SPECIFICATIONS

V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 10 MHz, f_S = 555 kSPS, V_{REF} = 2.5 V, F_{IN} = 100 kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted

Table 1.

Parameter	Test Conditions/Comments	A Version[1]	B Version[1]	Unit
DYNAMIC PERFORMANCE	f_{IN} = 100 kHz			
Signal to Noise Ratio (SNR)[2]	V_{DD} = 2.7 V to 5.25 V	70	70	dB min
Signal to (Noise + Distortion) (SINAD)[2]	V_{DD} = 2.7 V to 3.6 V	69	69	dB min
	V_{DD} = 4.75 V to 5.25 V	70	70	dB min
Total Harmonic Distortion (THD)[2]	V_{DD} = 2.7 V to 3.6 V; –78 dB typ	–73	–73	dB max
	V_{DD} = 4.75 V to 5.25 V; –80 dB typ	–75	–75	dB max
Peak Harmonic or Spurious Noise[2]	V_{DD} = 2.7 V to 3.6 V; –80 dB typ	–73	–73	dB max
	V_{DD} = 4.75 V to 5.25 V; –82 dB typ	–75	–75	dB max
Intermodulation Distortion (IMD)[2]	fa = 90 kHz; fb = 110 kHz			
Second-Order Terms		–80	–80	dB typ
Third-Order Terms		–80	–80	dB typ
Aperture Delay[2]		5	5	ns typ
Aperture Jitter[2]		50	50	ps typ
Full-Power Bandwidth[2, 3]	@ –3 dB	20	20	MHz typ
	@ –0.1 dB	2.5	2.5	MHz typ
DC ACCURACY				
Resolution		12	12	Bits
Integral Nonlinearity (INL)[2]		±1.5	±1	LSB max
Differential Nonlinearity (DNL)[2]	Guaranteed no missed codes to 12 bits	±0.95	±0.95	LSB max
Offset Error[2]		±3.5	±3.5	LSB max
Gain Error[2]		±3	±3	LSB max
ANALOG INPUT				
Full-Scale Input Span	V_{IN+} – V_{IN-}	V_{REF}	V_{REF}	V
Absolute Input Voltage				
V_{IN+}		V_{REF}	V_{REF}	V
V_{IN-}[4]	V_{DD} = 2.7 V to 3.6 V	–0.1 to +0.4	–0.1 to +0.4	V
	V_{DD} = 4.75 V to 5.25 V	–0.1 to +1.5	–0.1 to +1.5	V
DC Leakage Current		±1	±1	µA max
Input Capacitance	When in track/hold	30/10	30/10	pF typ
REFERENCE INPUT				
V_{REF} Input Voltage	± 1% tolerance for specified performance	2.5[5]	2.5[5]	V
DC Leakage Current		±1	±1	µA max
V_{REF} Input Capacitance	When in track/hold	10/30	10/30	pF typ
LOGIC INPUTS				
Input High Voltage, V_{INH}		2.4	2.4	V min
Input Low Voltage, V_{INL}		0.8	0.8	V max
Input Current, I_{IN}	Typically 10 nA, V_{IN} = 0 V or V_{DD}	±1	±1	µA max
Input Capacitance, C_{IN}[6]		10	10	pF max
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DD} = 4.75 V to 5.25 V, I_{SOURCE} = 200 µA	2.8	2.8	V min
	V_{DD} = 2.7 V to 3.6 V, I_{SOURCE} = 200 µA	2.4	2.4	V min
Output Low Voltage, V_{OL}	I_{SINK} = 200 µA	0.4	0.4	V max
Floating-State Leakage Current		±1	±1	µA max
Floating-State Output Capacitance[6]		10	10	pF max
Output Coding		Straight (natural) binary		

Parameter	Test Conditions/Comments	A Version[1]	B Version[1]	Unit
CONVERSION RATE				
Conversion Time	1.6 µs with a 10 MHz SCLK	16	16	SCLK cycles
Track-and-Hold Acquisition Time[2]	Sine wave input	250	250	ns max
	Full-scale step input	290	290	ns max
Throughput Rate		555	555	kSPS max
POWER REQUIREMENTS				
V_{DD}		2.7/5.25	2.7/5.25	V min/max
I_{DD}[7, 8]				
Normal Mode (Static)	SCLK on or off	0.5	0.5	mA typ
Normal Mode (Operational)	V_{DD} = 4.75 V to 5.25 V	1.5	1.5	mA max
	V_{DD}= 2.7 V to 3.6 V	1.2	1.2	mA max
Full Power-Down Mode	SCLK on or off	1	1	µA max
Power Dissipation				
Normal Mode (Operational)	V_{DD} = 5 V; 1.55 mW typ for 100 kSPS[7]	7.25	7.25	mW max
	V_{DD} = 3 V; 0.64 mW typ for 100 kSPS[7]	3.3	3.3	mW max
Full Power-Down Mode	V_{DD} = 5 V; SCLK on or off	5	5	µW max
	V_{DD} = 3 V; SCLK on or off	3	3	µW max

[1] Temperature ranges as follows: A, B versions: –40°C to +85°C.
[2] See Terminology section.
[3] Analog inputs with slew rates exceeding 27 V/µs (full-scale input sine wave > 3.5 MHz) within the acquisition time may cause an incorrect result to be returned by the converter.
[4] A small dc input is applied to V_{IN-} to provide a pseudo ground for V_{IN+}.
[5] The AD7453 is functional with a reference input in the range 100 mV to V_{DD}.
[6] Guaranteed by characterization.
[7] See Power vs. Throughput Rate section.
[8] Measured with a full-scale dc input.

TIMING SPECIFICATIONS

Guaranteed by characterization. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

See Figure 2 and the Serial Interface section.

V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 10 MHz, f_S = 555 kSPS, V_{REF} = 2.5 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCLK}[1]	10	kHz min	
	10	MHz max	
$t_{CONVERT}$	16 × t_{SCLK}		t_{SCLK} = 1/f_{SCLK}
	1.6	µs max	
t_{QUIET}	60	ns min	Minimum quiet time between the end of a serial read and the next falling edge of $\overline{CS}$
t_1	10	ns min	Minimum $\overline{CS}$ pulse width
t_2	10	ns min	$\overline{CS}$ falling edge to SCLK falling edge setup time
t_3[2]	20	ns max	Delay from $\overline{CS}$ falling edge until SDATA three-state disabled
t_4[2]	40	ns max	Data access time after SCLK falling edge
t_5	0.4 t_{SCLK}	ns min	SCLK high pulse width
t_6	0.4 t_{SCLK}	ns min	SCLK low pulse width
t_7	10	ns min	SCLK edge to data valid hold time
t_8[3]	10	ns min	SCLK falling edge to SDATA three-state enabled
	35	ns max	SCLK falling edge to SDATA three-state enabled
$t_{POWER-UP}$ [4]	1	µs max	Power-up time from full power-down

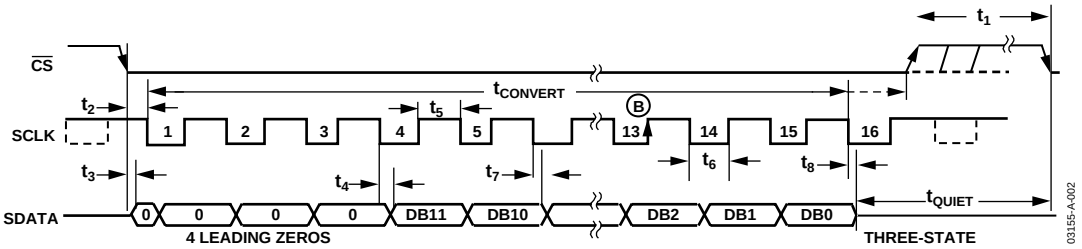


Figure 2. AD7453 Serial Interface Timing Diagram

[1] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[2] Measured with the load circuit of Figure 3 and defined as the time required for the output to cross 0.8 V or 2.4 V with V_{DD} = 5 V, and the time required for an output to cross 0.4 V or 2.0 V for V_{DD} = 3 V.
[3] t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.
[4] See Power-Up Time section.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	–0.3 V to +7 V
V_{IN+} to GND	–0.3 V to V_{DD} + 0.3 V
V_{IN-} to GND	–0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	–0.3 V to +7 V
Digital Output Voltage to GND	–0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	–0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial (A, B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +85°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	211.5°C/W (SOT-23)
θ_{JC} Thermal Impedance	91.99°C/W (SOT-23)
Lead Temperature, Soldering	
Vapor Phase (60 secs)	215°C
Infrared (15 secs)	220°C
ESD	1 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1] Transient currents of up to 100 mA will not cause SCR latch-up.

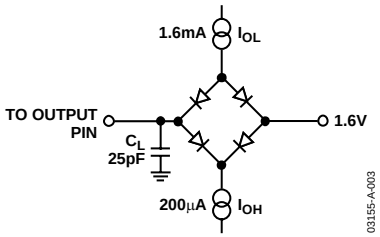


Figure 3. Load Circuit for Digital Output Timing Specifications

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

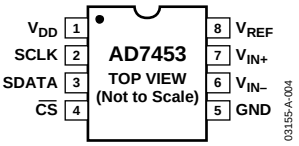


Figure 4. Pin Function Descriptions

Table 4. Pin Function Descriptions

Mnemonic	Function
V_{REF}	Reference Input for the AD7453. An external reference in the range 100 mV to V_{DD} must be applied to this input. The specified reference input is 2.5 V. This pin should be decoupled to GND with a capacitor of at least 0.1 µF.
V_{IN+}	Noninverting Analog Input.
V_{IN-}	Inverting Input. This pin sets the ground reference point for the V_{IN+} input. Connect to ground or to a dc offset to provide a pseudo ground.
GND	Analog Ground. Ground reference point for all circuitry on the AD7453. All analog input signals and any external reference signal should be referred to this GND voltage.
$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating a conversion on the AD7453 and framing the serial data transfer.
SDATA	Serial Data. Logic output. The conversion result from the AD7453 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream of the AD7453 consists of four leading zeros followed by the 12 bits of conversion data that are provided MSB first. The output coding is straight (natural) binary.
SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the conversion process.
V_{DD}	Power Supply Input. V_{DD} is 2.7 V to 5.25 V. This supply should be decoupled to GND with a 0.1 µF capacitor and a 10 µF tantalum capacitor.

TERMINOLOGY

Signal-to-(Noise + Distortion) Ratio

The measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02N + 1.76)\ \text{dB}$$

Thus, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion (THD)

Total harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7453, it is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second to the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at the sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7453 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dB.

Aperture Delay

The amount of time from the leading edge of the sampling clock until the ADC actually takes the sample.

Aperture Jitter

The sample-to-sample variation in the effective point in time at which the actual sample is taken.

Full Power Bandwidth

The full power bandwidth of an ADC is the input frequency at which the amplitude of the reconstructed fundamental is reduced by 0.1 dB or 3 dB for a full-scale input.

Integral Nonlinearity (INL)

The maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)

The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

The deviation of the first code transition (000...000 to 000...001) from the ideal (i.e., AGND + 1 LSB)

Gain Error

This is the deviation of the last code transition (111...110 to 111...111) from the ideal (i.e., VREF − 1 LSB), after the offset error has been adjusted out.

Track-and-Hold Acquisition Time

The minimum time required for the track and hold amplifier to remain in track mode for its output to reach and settle to within 0.5 LSB of the applied input signal.

Power Supply Rejection Ratio (PSRR)

The ratio of the power in the ADC output at full-scale frequency, *f*, to the power of a 100 mV p-p sine wave applied to the ADC V_{DD} supply of frequency f_S. The frequency of this input varies from 1 kHz to 1 MHz.

$$PSRR(\text{dB}) = 10\log(Pf/Pf_S)$$

Pf is the power at frequency *f* in the ADC output; *Pfs* is the power at frequency f_S in the ADC output.

AD7453–TYPICAL PERFORMANCE CHARACTERISTICS

Default Conditions: T_A = 25°C, f_S = 555 kSPS, f_{SCLK} = 10 MHz, V_{DD} = 2.7 V to 5.25 V, V_{REF} = 2.5 V, unless otherwise noted.

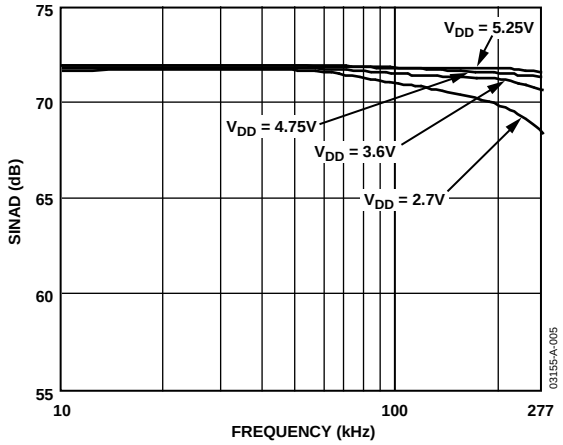


Figure 5. SINAD vs. Analog Input Frequency for Various Supply Voltages

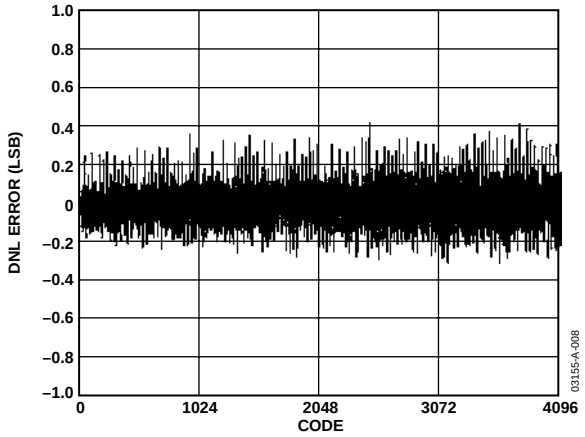


Figure 8. Typical DNL for the AD7453 for V_{DD} = 5 V

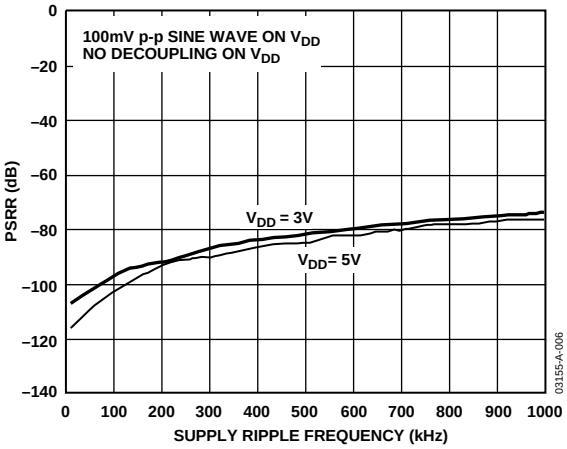


Figure 6. PSRR vs. Supply Ripple Frequency without Supply Decoupling

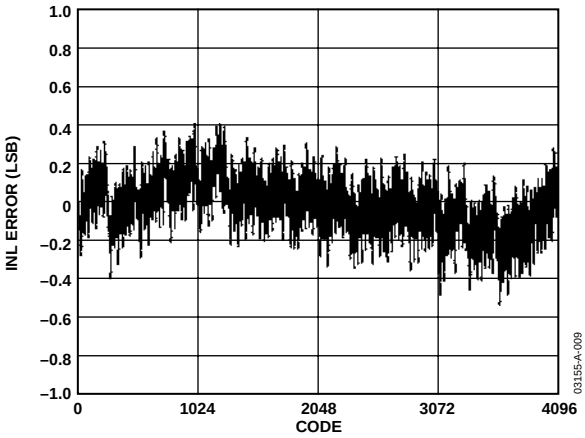


Figure 9. Typical INL for the AD7453 for V_{DD} = 5 V

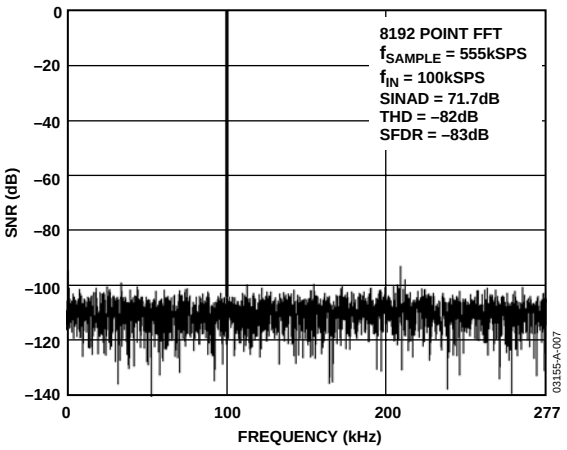


Figure 7. Dynamic Performance for V_{DD} = 5 V

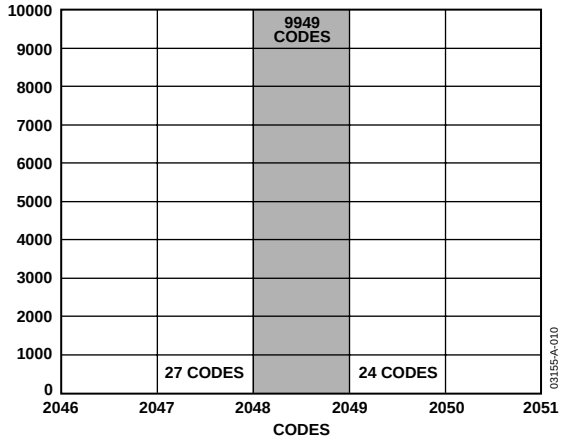


Figure 10. Histogram of 10,000 Conversions of a DC Input

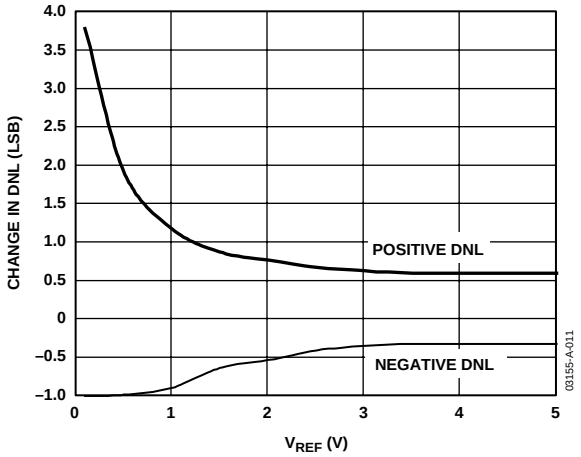


Figure 11. Change in DNL vs. V_{REF} for V_{DD} = 5 V

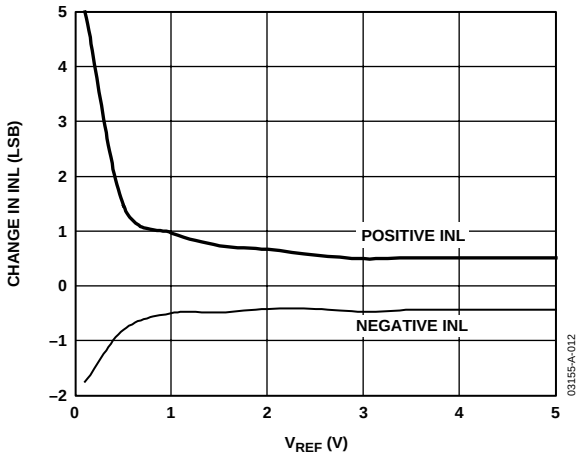


Figure 12. Change in INL vs. V_{REF} for V_{DD} = 5 V

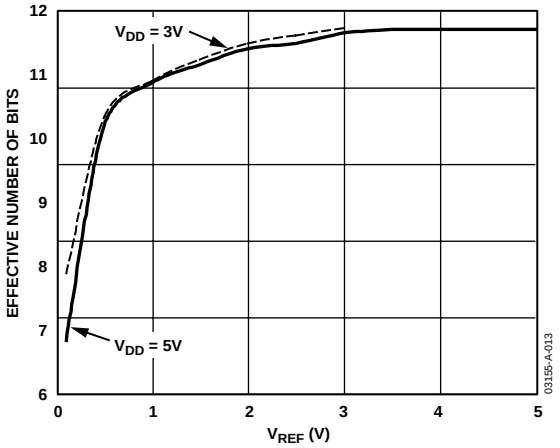


Figure 13. ENOB vs. V_{REF} for V_{DD} = 3 V and 5 V

CIRCUIT INFORMATION

The AD7453 is a 12-bit, low power, single-supply, successive approximation analog-to-digital converter (ADC) with a pseudo differential analog input. It operates with a single 2.7 V to 5.25 V power supply and is capable of throughput rates up to 555 kSPS when supplied with a 10 MHz SCLK. It requires an external reference to be applied to the V_{REF} pin.

The AD7453 has an on-chip differential track-and-hold amplifier, a successive approximation (SAR) ADC, and a serial interface, housed in an 8-lead SOT-23 package. The serial clock input accesses data from the part and provides the clock source for the successive approximation ADC. The AD7453 features a power-down option for reduced power consumption between conversions. The power-down feature is implemented across the standard serial interface, as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7453 is a successive approximation ADC based around two capacitive DACs. Figure 14 and Figure 15 show simplified schematics of the ADC in the acquisition and conversion phase, respectively. The ADC is comprised of control logic, an SAR, and two capacitive DACs. In Figure 14 (acquisition phase), SW3 is closed and SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.

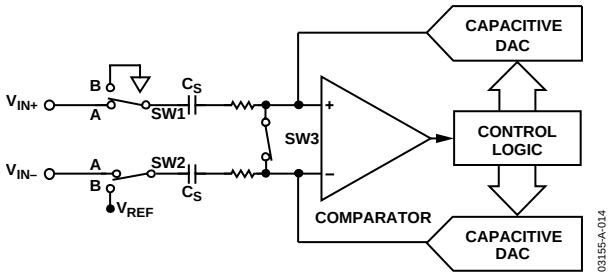


Figure 14. ADC Acquisition Phase

When the ADC starts a conversion (Figure 15), SW3 opens and SW1 and SW2 move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC's output code. The output impedances of the sources driving the V_{IN+} and V_{IN-} pins must be matched; otherwise the two inputs have different settling times, resulting in errors.

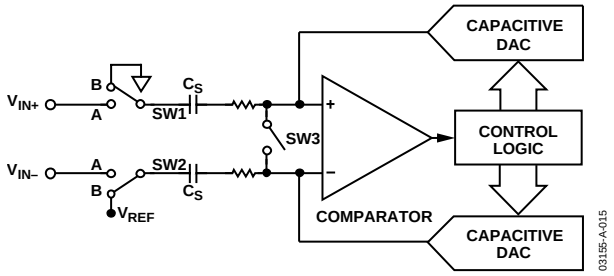


Figure 15. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding for the AD7453 is straight (natural) binary. The designed code transitions occur at successive LSB values (i.e., 1 LSB, 2 LSB, and so on). The LSB size is $V_{REF}/4096$. The ideal transfer characteristic of the AD7453 is shown in Figure 16.

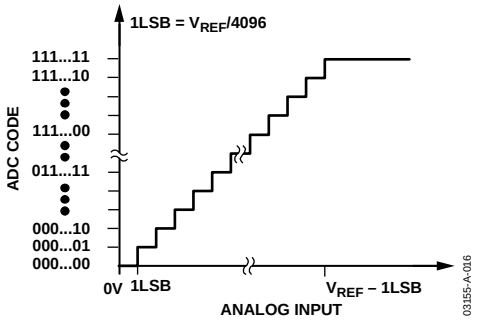


Figure 16. Ideal Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 17 shows a typical connection diagram for the AD7453. In this setup, the GND pin is connected to the analog ground plane of the system. The V_{REF} pin is connected to the AD780, a 2.5 V decoupled reference source. The signal source is connected to the V_{IN+} analog input via a unity gain buffer. A dc voltage is connected to the V_{IN-} pin to provide a pseudo ground for the V_{IN+} input. The V_{DD} pin should be decoupled to AGND with a 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor. The reference pin should be decoupled to AGND with a capacitor of at least 0.1 µF. The conversion result is output in a 16-bit word with four leading zeros followed by the MSB of the 12-bit result.

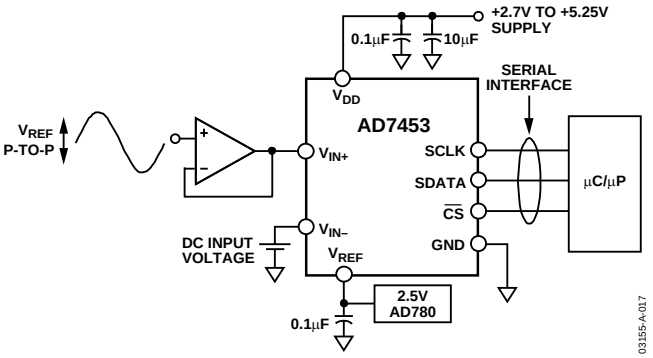


Figure 17. Typical Connection Diagram

THE ANALOG INPUT

The AD7453 has a pseudo differential analog input. The V_{IN+} input is coupled to the signal source and must have an amplitude of V_{REF} p-p to make use of the full dynamic range of the part. A dc input is applied to V_{IN-}. The voltage applied to this input provides an offset from ground or a pseudo ground for the V_{IN+} input. The main benefit of pseudo differential inputs is that they separate the analog input signal ground from the ADC's ground, allowing dc common-mode voltages to be cancelled.

Because the ADC operates from a single supply, it is necessary to level shift ground-based bipolar signals to comply with the input requirements. An op amp (for example, the AD8021) can be configured to rescale and level shift a ground-based (bipolar) signal so that it is compatible with the input range of the AD7453. See Figure 18.

When a conversion takes place, the pseudo ground corresponds to 0 and the maximum analog input corresponds to 4096.

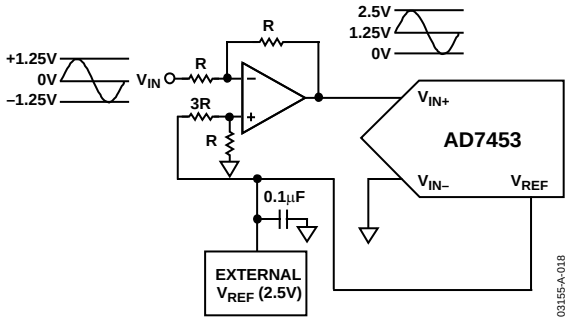


Figure 18. Op Amp Configuration to Level Shift a Bipolar Input Signal

Analog Input Structure

Figure 19 shows the equivalent circuit of the analog input structure of the AD7453. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. This causes these diodes to become forward biased and to start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part. The capacitors, C1 in Figure 19, are typically 4 pF and can be attributed primarily to pin capacitance. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 100 Ω. The capacitors C2 are the ADC's sampling capacitors, and have a typical capacitance of 16 pF.

For ac applications, removing high frequency components from the analog input signal through the use of an RC low-pass filter on the relevant analog input pins is recommended. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC, which may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

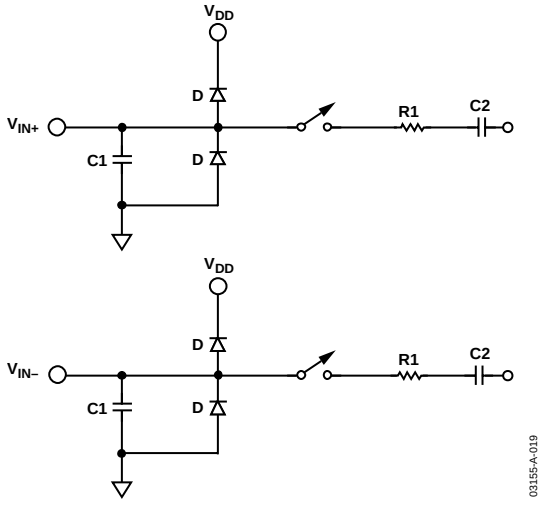


Figure 19. Equivalent Analog Input Circuit.
Conversion Phase—Switches Open; Track Phase—Switches Closed

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases and performance degrades. Figure 20 shows a graph of the THD versus analog input signal frequency for different source impedances.

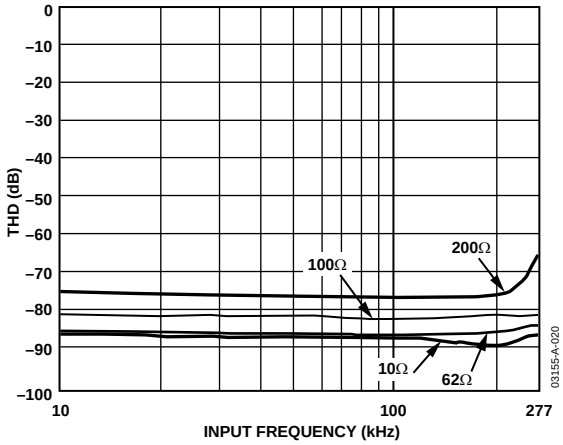


Figure 20. THD vs. Analog Input Frequency for Various Source Impedances

Figure 21 shows a graph of THD versus analog input frequency for various supply voltages while sampling at 555 kSPS with an SCLK of 10 MHz. In this case, the source impedance is 10 Ω.

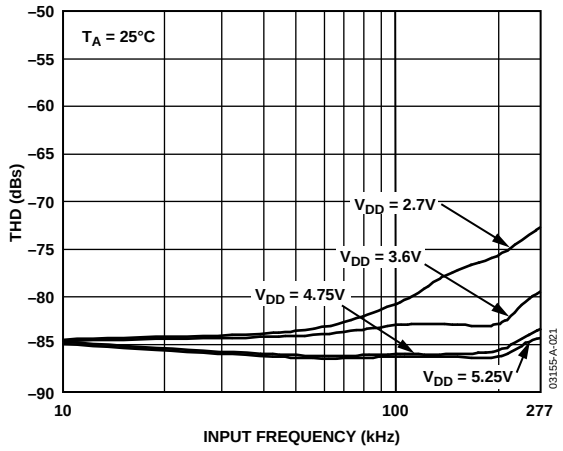


Figure 21. THD vs. Analog Input Frequency for Various Supply Voltages

DIGITAL INPUTS

The digital inputs applied to the AD7453 are not limited by the maximum ratings that limit the analog inputs. Instead, the digital inputs applied, i.e., $\overline{CS}$ and SCLK, can go to 7 V and are not restricted by the V_{DD} + 0.3 V limits as on the analog input.

The main advantage of the inputs not being restricted to the V_{DD} + 0.3 V limit is that power supply sequencing issues are avoided. If $\overline{CS}$ or SCLK are applied before V_{DD}, there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V were applied prior to V_{DD}.

REFERENCE

An external source is required to supply the reference to the AD7453. This reference input can range from 100 mV to V_{DD}. The specified reference is 2.5 V for the 2.7 V to 5.25 V power supply range. The reference input chosen for an application should never be greater than the power supply. Errors in the reference source result in gain errors in the AD7453 transfer function. A capacitor of at least 0.1 µF should be placed on the V_{REF} pin. Suitable reference sources for the AD7453 include the AD780 and the ADR421. Figure 22 shows a typical connection diagram for the V_{REF} pin.

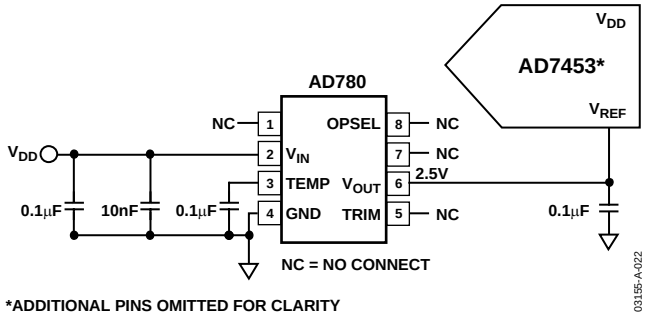


Figure 22. Typical V_{REF} Connection Diagram for V_{DD} = 5 V

SERIAL INTERFACE

Figure 2 shows a detailed timing diagram of the serial interface of the AD7453. The serial clock provides the conversion clock and controls the transfer of data from the device during conversion. $\overline{CS}$ initiates the conversion process and frames the data transfer. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode and takes the bus out of three-state. The analog input is sampled and the conversion is initiated at this point. The conversion requires 16 SCLK cycles to complete.

Once 13 SCLK falling edges have occurred, the track-and-hold goes back into track mode on the next SCLK rising edge, as shown at Point B in Figure 2. On the 16th SCLK falling edge, the SDATA line goes back into three-state.

If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion is terminated and the SDATA line goes back into three-state.

The conversion result from the AD7453 is provided on the SDATA output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream of the AD7453 consists of four leading zeros, followed by 12 bits of conversion data, provided MSB first. The output coding is straight (natural) binary.

Sixteen serial clock cycles are required to perform a conversion and to access data from the AD7453. $\overline{CS}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out on the subsequent SCLK falling edges, beginning with the second leading zero. Thus the first falling clock edge on the serial clock provides the second leading zero. The final bit in the data transfer is valid on the 16th falling edge, having been clocked out on the previous (15th) falling edge. Once the conversion is complete and the data has been accessed after the 16 clock cycles, it is important to ensure that, before the next conversion is initiated, enough time is left to meet the acquisition and quiet time specifications. See Timing Example 1.

In applications with a slower SCLK, it may be possible to read in data on each SCLK rising edge, i.e., the first rising edge of SCLK after the $\overline{CS}$ falling edge would have the leading zero provided, and the 15th SCLK edge would have DB0 provided.

Timing Example 1

Having F_{SCLK} = 10 MHz and a throughput rate of 555 kSPS gives a cycle time of

$$1/Throughput = 1/555{,}000 = 1.8\ \mu s$$

A cycle consists of

$$t_2 + 12.5(1/F_{SCLK}) + t_{ACQ} = 1.8\ \mu s$$

Therefore if t_2 = 10 ns,

$$10\ ns + 12.5(1/10\ MHz) + t_{ACQ} = 1.8\ \mu s$$

$$t_{ACQ} = 540\ ns$$

This 540 ns satisfies the requirement of 290 ns for t_{ACQ}. From Figure 23, t_{ACQ} comprises

$$2.5(1/F_{SCLK}) + t_8 + t_{QUIET}$$

where t_8 = 35 ns. This allows a value of 255 ns for t_{QUIET}, satisfying the minimum requirement of 60 ns.

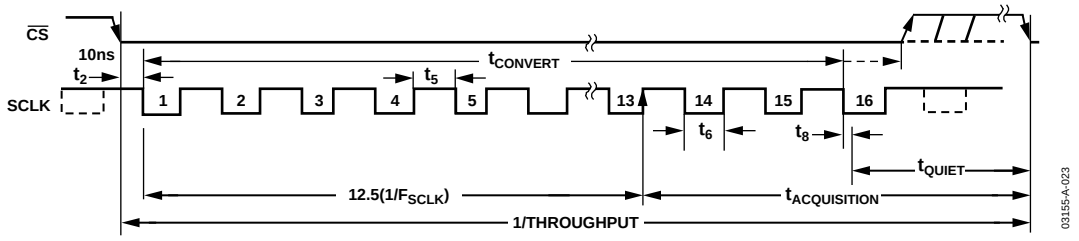


Figure 23. Serial Interface Timing Example

MODES OF OPERATION

The mode of operation of the AD7453 is selected by controlling the logic state of the $\overline{CS}$ signal during a conversion. There are two possible modes of operation, normal mode and power-down mode. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated determines whether the AD7453 enters power-down mode. Similarly, if already in power-down, $\overline{CS}$ controls whether the device returns to normal operation or remains in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/ throughput rate ratio for differing application requirements.

NORMAL MODE

This mode is intended for fastest throughput rate performance. The user does not have to worry about any power-up times with the AD7453 remaining fully powered up all the time. Figure 24 shows the general diagram of the operation of the AD7453 in this mode. The conversion is initiated on the falling edge of $\overline{CS}$, as described in the Serial Interface section. To ensure that the part remains fully powered up, $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$.

If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge but before the 16th SCLK falling edge, the part remains powered up but the conversion is terminated and SDATA goes back into three-state. Sixteen serial clock cycles are required to complete the conversion and access the complete conversion result. $\overline{CS}$ may idle high until the next conversion, or may idle low until some time prior to the next conversion. Once a data transfer is complete, i.e., when SDATA has returned to three-state, another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by again bringing $\overline{CS}$ low.

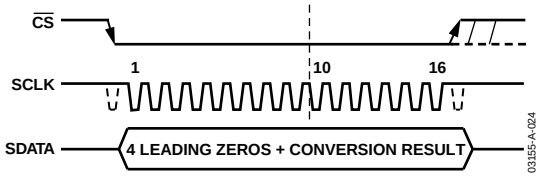


Figure 24. Normal Mode Operation

POWER-DOWN MODE

This mode is intended for use in applications where slower throughput rates are required—the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate and the ADC is then powered down for a relatively long duration between these bursts of several conversions. When the AD7453 is in power-down mode, all analog circuitry is powered down. For the AD7453 to enter power-down mode, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK, as shown in Figure 25.

Once $\overline{CS}$ has been brought high in this window of SCLKs, the part enters power-down, the conversion that was initiated by the falling edge of $\overline{CS}$ is terminated, and SDATA goes back into three-state. The time from the rising edge of $\overline{CS}$ to SDATA three-state enabled is never greater than t_8 (see the Timing Specifications). If $\overline{CS}$ is brought high before the second SCLK falling edge, the part remains in normal mode and does not power down. This avoids accidental power-down due to glitches on the $\overline{CS}$ line.

To exit this mode of operation and power up the AD7453 again, a dummy conversion is performed. On the falling edge of $\overline{CS}$, the device begins to power up, and continues to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The device is fully powered up after 1 µs has elapsed and, as shown in Figure 26, valid data results from the next conversion.

If $\overline{CS}$ is brought high before the 10th falling edge of SCLK, the AD7453 again goes back into power-down. This avoids accidental power-up due to glitches on the $\overline{CS}$ line or an inadvertent burst of eight SCLK cycles while $\overline{CS}$ is low. So although the device may begin to power up on the falling edge of $\overline{CS}$, it again powers down on the rising edge of $\overline{CS}$ as long as it occurs before the 10th SCLK falling edge.

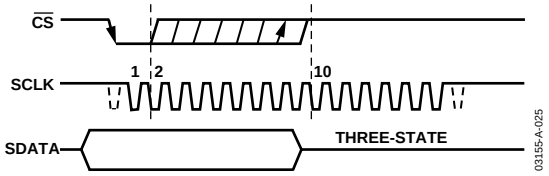


Figure 25. Entering Power-Down Mode

POWER-UP TIME

The power-up time of the AD7453 is typically 1 μs, which means that with any frequency of SCLK up to 10 MHz, one dummy cycle is always sufficient to allow the device to power up. Once the dummy cycle is complete, the ADC is fully powered up and the input signal is acquired properly. The quiet time, t_{QUIET}, must still be allowed—from the point at which the bus goes back into three-state after the dummy conversion to the next falling edge of $\overline{CS}$.

When running at the maximum throughput rate of 555 kSPS, the AD7453 powers up and acquires a signal within ±0.5 LSB in one dummy cycle. When powering up from power-down mode with a dummy cycle, as in Figure 26, the track and-hold, which was in hold mode while the part was powered down, returns to track mode after the first SCLK edge the part receives after the falling edge of $\overline{CS}$. This is shown as Point A in Figure 26.

Although at any SCLK frequency one dummy cycle is sufficient to power up the device and acquire V_{IN}, it does not necessarily mean that a full dummy cycle of 16 SCLKs must always elapse to power up the device and acquire V_{IN} fully; 1 μs is sufficient to power up the device and acquire the input signal.

For example, if a 5 MHz SCLK frequency is applied to the ADC, the cycle time is 3.2 μs (i.e., 1/(5 MHz) × 16). In one dummy cycle, 3.2 μs, the part is powered up and V_{IN} is acquired fully. However after 1 μs with a 5 MHz SCLK, only five SCLK cycles have elapsed. At this stage, the ADC is fully powered up and the signal acquired. So in this case, $\overline{CS}$ can be brought high after the 10th SCLK falling edge and brought low again after a time, t_{QUIET}, to initiate the conversion.

When power supplies are first applied to the AD7453, the ADC may either power up in the power-down mode or normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure that the part is fully powered up before attempting a valid conversion. Likewise, if the user wants the part to power up in power-down mode, the dummy cycle may be used to ensure the device is in power-down mode by executing a cycle such as that shown in Figure 25. Once supplies are applied to the AD7453, the power-up time is the same as that when powering up from power-down mode. It takes approximately 1 μs to power up fully if the part powers up in normal mode. It is not necessary to wait 1 μs before executing a dummy cycle to ensure the desired mode of operation. Instead, the dummy cycle can occur directly after power is supplied to the ADC. If the first valid conversion is then performed directly after the dummy conversion, care must be taken to ensure that adequate acquisition time has been allowed.

As mentioned earlier, when powering up from the power-down mode, the part returns to track mode upon the first SCLK edge applied after the falling edge of $\overline{CS}$. However, when the ADC powers up initially after supplies are applied, the track-and-hold is already in track mode. This means (assuming one has the facility to monitor the ADC supply current) that if the ADC powers up in the desired mode of operation and thus a dummy cycle is not required to change the mode, then a dummy cycle is not required to place the track-and-hold into track.

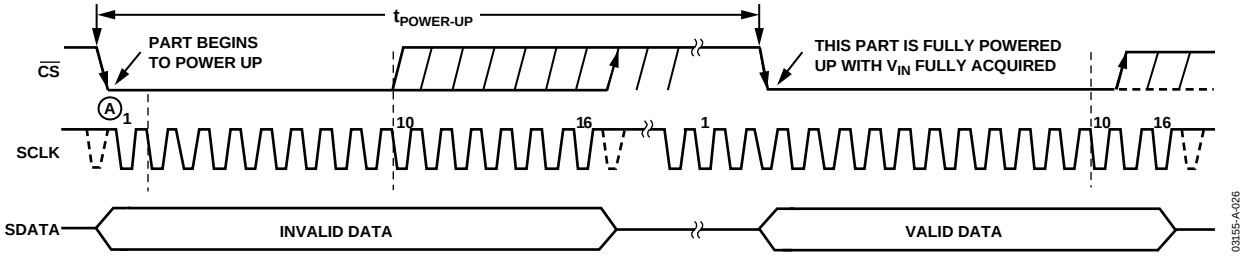


Figure 26. Exiting Power-Down Mode

POWER VS. THROUGHPUT RATE

By using the power-down mode on the AD7453 when not converting, the average power consumption of the ADC decreases at lower throughput rates. Figure 27 shows how, as the throughput rate is reduced, the device remains in its power-down state longer and the average power consumption reduces accordingly. For example, if the AD7453 is operated in continuous sampling mode with a throughput rate of 100 kSPS and a 10 MHz SCLK, and the device is placed in the power-down mode between conversions, then the power consumption is calculated as follows:

Power dissipation during normal operation = 7.25 mW *max* (*for* V_{DD} = 5 V).

If the power-up time is one dummy cycle (1.06 µs if $\overline{CS}$ is brought high after the 10th SCLK falling edge in the cycle and then brought low after the quiet time) and the remaining conversion time is another cycle (1.6 µs), then the AD7453 can be said to dissipate 7.25 mW for 2.66 µs* during each conversion cycle.

If the throughput rate = 100 kSPS, then the cycle time = 10 µs and the average power dissipated during each cycle is

$$(2.66/10) \times 7.25 \text{ mW} = 1.92 \text{ mW}$$

For the same scenario, if V_{DD} = 3 V, the power dissipation during normal operation is 3.3 mW max. The AD7453 can now be said to dissipate 3.3 mW for 2.66 µs* during each conversion cycle.

The average power dissipated during each cycle with a throughput rate of 100 kSPS is therefore

$$(2.66/10) \times 3.3 \text{ mW} = 0.88 \text{ mW}$$

This is how the power numbers in Figure 27 are calculated.

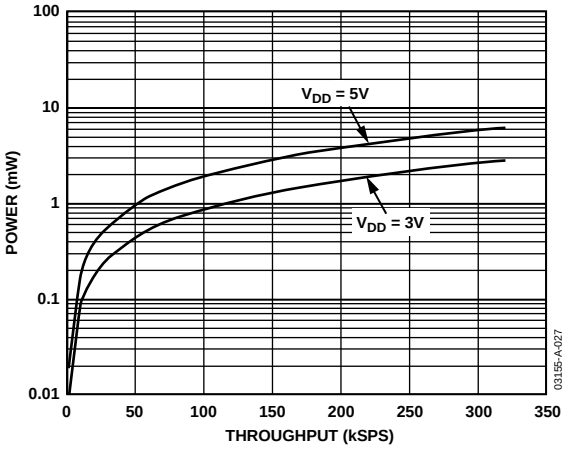


Figure 27. Power vs. Throughput Rate for Power-Down Mode

*This figure assumes a very short time to enter power-down mode. This increases as the burst of clocks used to enter power down mode is increased.

For throughput rates above 320 kSPS, the serial clock frequency should be reduced for optimum power performance.

MICROPROCESSOR AND DSP INTERFACING

The serial interface on the AD7453 allows the part to be connected directly to a range of different microprocessors. This section explains how to interface the AD7453 with some of the more common microcontroller and DSP serial interface protocols.

AD7453 to ADSP-21xx

The ADSP-21xx family of DSPs are interfaced directly to the AD7453 without any glue logic required.

The SPORT control register should be set up as follows:

TFSW = RFSW = 1	Alternate Framing
INVRFS = INVTFS = 1	Active Low Frame Signal
DTYPE = 00	Right Justify Data
SLEN = 1111	16-Bit Data-Words
ISCLK = 1	Internal Serial Clock
TFSR = RFSR = 1	Frame Every Word
IRFS = 0	
ITFS = 1	

To implement power-down mode, SLEN should be set to 1001 to issue an 8-bit SCLK burst.

The connection diagram is shown in Figure 28. The ADSP-21xx has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in alternate framing mode and the SPORT control register is set up as described. The frame synchronization signal generated on the TFS is tied to $\overline{CS}$, and, as with all signal processing applications, equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC, and, under certain conditions, equidistant sampling may not be achieved.

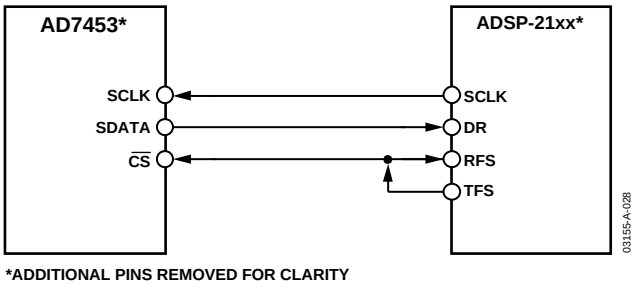


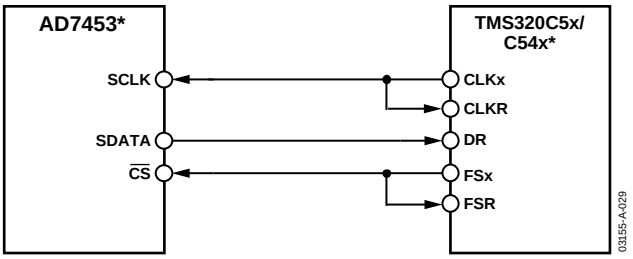
Figure 28. Interfacing to the ADSP-21xx

The timer registers, for example, are loaded with a value that provides an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and thus the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given, (i.e., AX0 = TX0), the state of the SCLK is checked. The DSP waits until the SCLK has gone high, low, and high again before transmission starts. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, then the data may be transmitted or it may wait until the next clock edge.

For example, the ADSP-2111 has a master clock frequency of 16 MHz. If the SCLKDIV register is loaded with the value 3, an SCLK of 2 MHz is obtained and eight master clock periods elapse for every SCLK period. If the timer registers are loaded with the value 803, then 100.5 SCLKs occur between interrupts and subsequently between transmit instructions. This situation results in nonequidistant sampling as the transmit instruction is occurring on an SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N, equidistant sampling is implemented by the DSP.

AD7453 to TMS320C5x/C54x

The serial interface on the TMS320C5x/C54x uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7453. The $\overline{CS}$ input allows easy interfacing between the TMS320C5x/C54x and the AD7453 without any glue logic required. The serial port of the TMS320C5x/C54x is set up to operate in burst mode with internal CLKx (Tx serial clock) and FSx (Tx frame sync). The serial port control register (SPC) must have the following setup: FO = 0, FSM = 1, MCM = 1 and TXM = 1. The format bit, FO, may be set to 1 to set the word length to eight bits in order to implement the power-down mode on the AD7453. The connection diagram is shown in Figure 29. For signal processing applications, it is imperative that the frame synchronization signal from the TMS320C5x/C54x provide equidistant sampling.

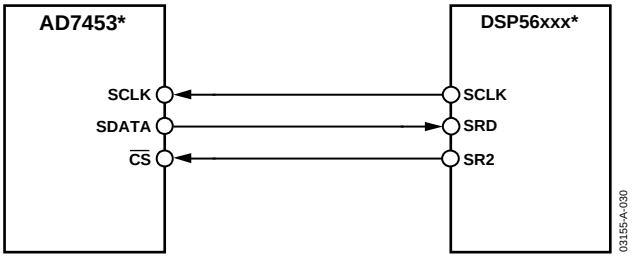


*ADDITIONAL PINS REMOVED FOR CLARITY

Figure 29. Interfacing to the TMS320C5x/C54x

AD7453 to DSP56xxx

The connection diagram in Figure 30 shows how the AD7453 can be connected to the SSI (synchronous serial interface) of the DSP56xxx family of DSPs from Motorola. The SSI is operated in synchronous mode (SYN bit in CRB = 1) with internally generated 1-bit clock period frame sync for both Tx and Rx (Bit FSL1 = 1 and Bit FSL0 = 0 in CRB). Set the word length to 16 by setting Bits WL1 = 1 and WL0 = 0 in CRA. To implement the power-down mode on the AD7453, the word length can be changed to eight bits by setting Bits WL1 = 0 and WL0 = 0 in CRA. For signal processing applications, it is imperative that the frame synchronization signal from the DSP56xxx provide equidistant sampling.



*ADDITIONAL PINS REMOVED FOR CLARITY

Figure 30. Interfacing to the DSP56xxx

APPLICATION HINTS

Grounding and Layout

The printed circuit board that houses the AD7453 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should be joined in only one place, and the connection should be a star ground point established as close to the GND pin on the AD7453 as possible.

Avoid running digital lines under the device as this couples noise onto the die. The analog ground plane should be allowed to run under the AD7453 to avoid noise coupling. The power supply lines to the AD7453 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board.

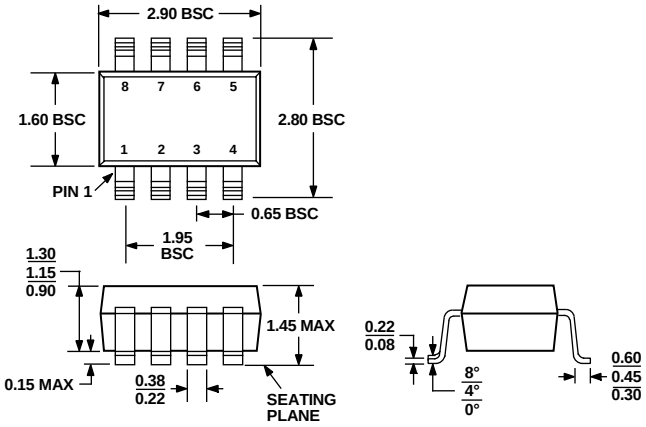
In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side. Good decoupling is also important. All analog supplies should be decoupled with 10 µF tantalum capacitors in parallel with 0.1 µF capacitors to GND. To achieve the best from these decoupling components, they must be placed as close as possible to the device.

EVALUATING THE AD7453'S PERFORMANCE

The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the evaluation board controller. The evaluation board controller can be used in conjunction with the AD7453 evaluation board, as well as many other Analog Devices evaluation boards ending with the CB designator, to demonstrate/evaluate the ac and dc performance of the AD7453.

The software allows the user to perform ac (Fast Fourier Transform) and dc (histogram of codes) tests on the AD7453. For more information, see the AD7453 application note that accompanies the evaluation kit.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178BA

Figure 31. 8-Lead Small Outline Transistor Package [SOT-23]
(RT-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)[1]	Package Description	Package Option	Branding
AD7453ART-REEL7	–40°C to +85°C	±1.5	8-Lead SOT-23	RT-8	C0C
AD7453BRT-R2	–40°C to +85°C	±1	8-Lead SOT-23	RT-8	C09
AD7453BRT-REEL7	–40°C to +85°C	±1	8-Lead SOT-23	RT-8	C09
EVAL-AD7453CB[2]			Evaluation Board		
EVAL-CONTROL BRD2[3]			Controller Board		

[1] Linearity error here refers to integral nonlinearity error.
[2] This can be used as a standalone evaluation board or in conjunction with the evaluation board controller for evaluation/demonstration purposes.
[3] The evaluation board controller is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designator. For a complete Evaluation Kit, you will need to order the ADC evaluation board, i.e., EVAL-AD7453CB, the EVAL-CONTROL BRD2, and a 12 V ac transformer. See the AD7453 application note that accompanies the evaluation kit for more information.

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