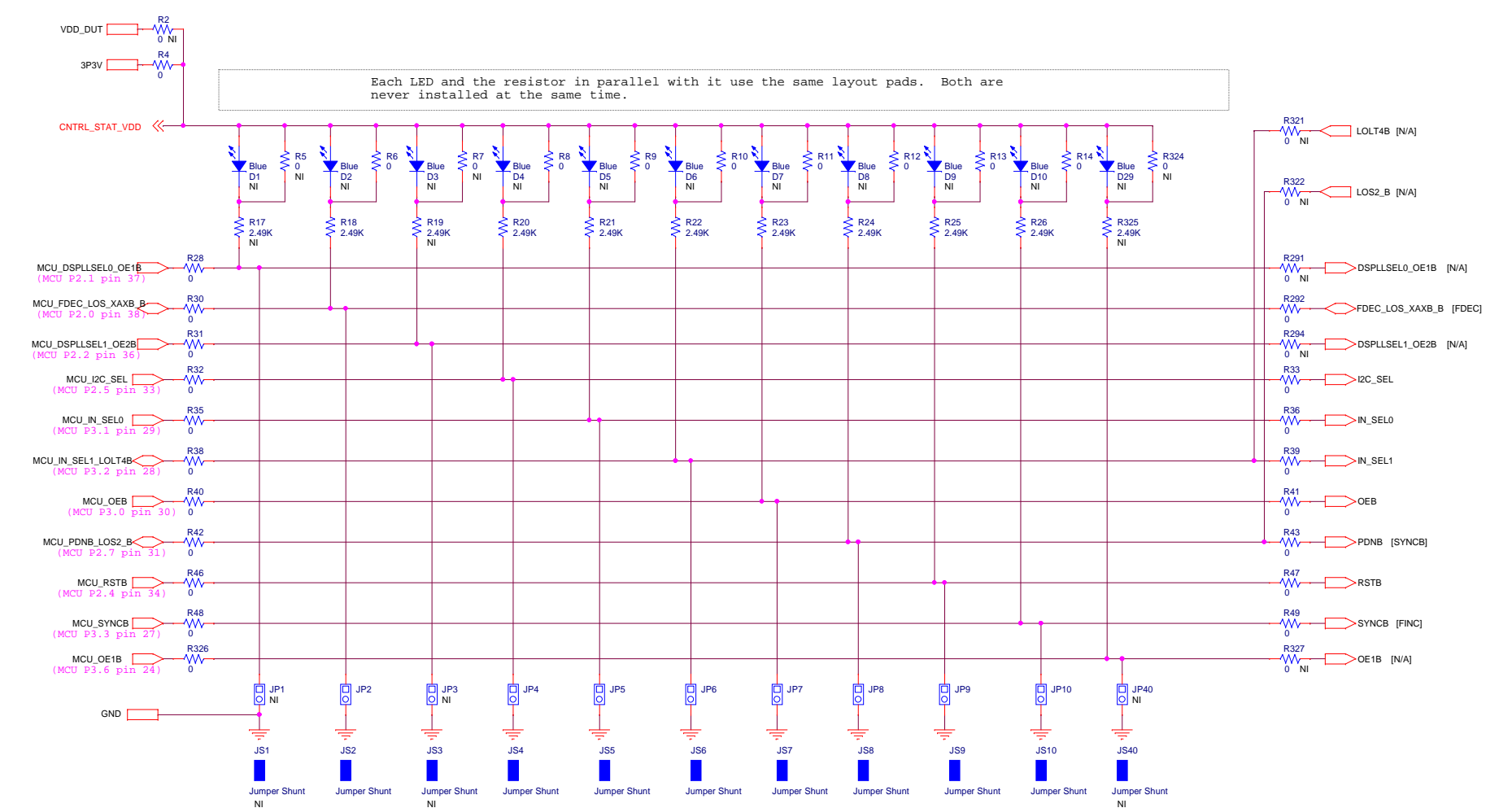





REVISION CONTROL

Rev 1.0 - July 1, 2014, Initial Board Release

# CONTROL PINS CONNECTIONS



Note:  
1. If the net name differs from the DUT pin name, the corresponding DUT pin name is enclosed in brackets. [DUT Pin Name]  
2. "N/A" in brackets indicates that the function is not used for the DUT. [N/A]



400 W Cesar Chavez  
Austin, TX 78701

Title

CONTROL PINS\_P1

Size

B

Document Number

SIS341-EB

Date

Tuesday, May 20, 2014

Sheet

3

of

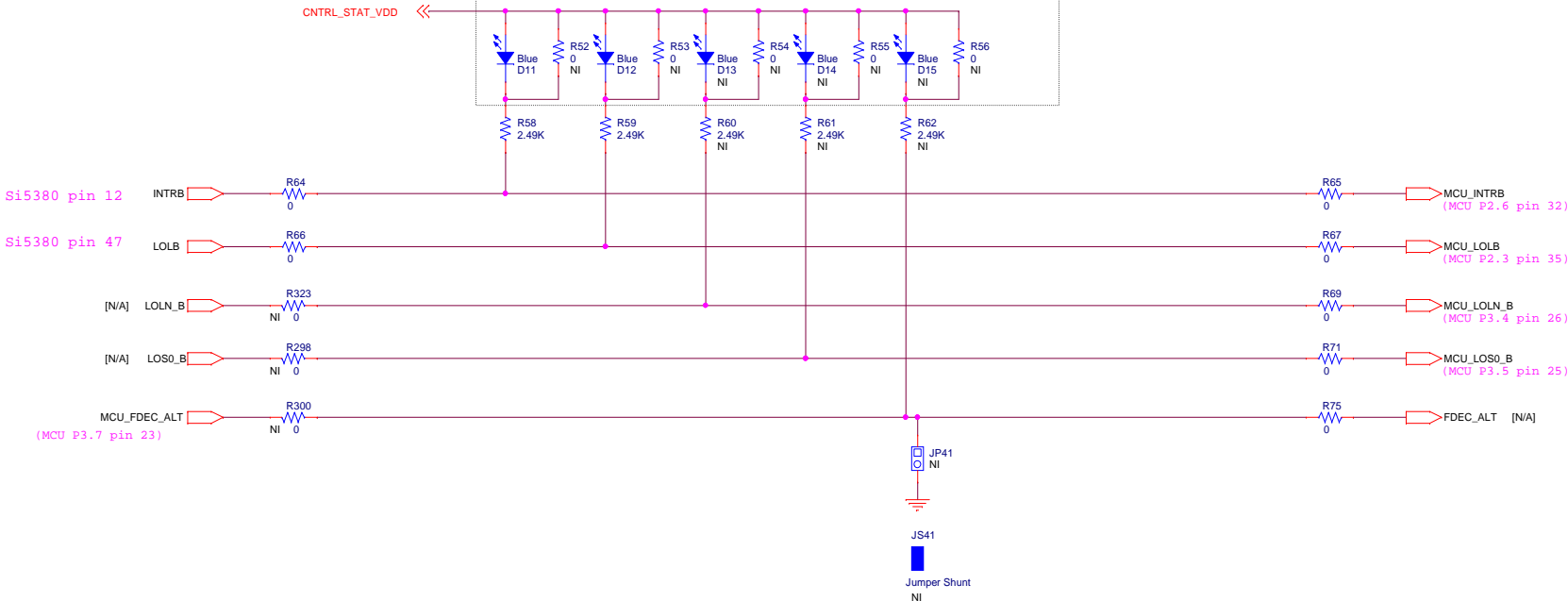
44

Rev

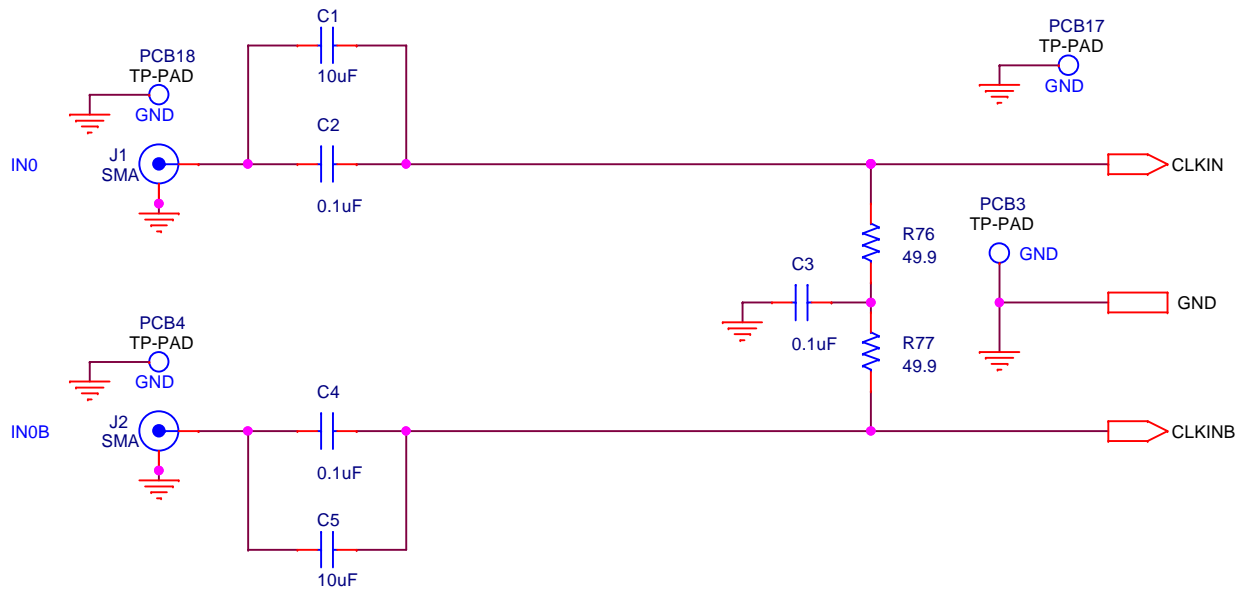
1.0

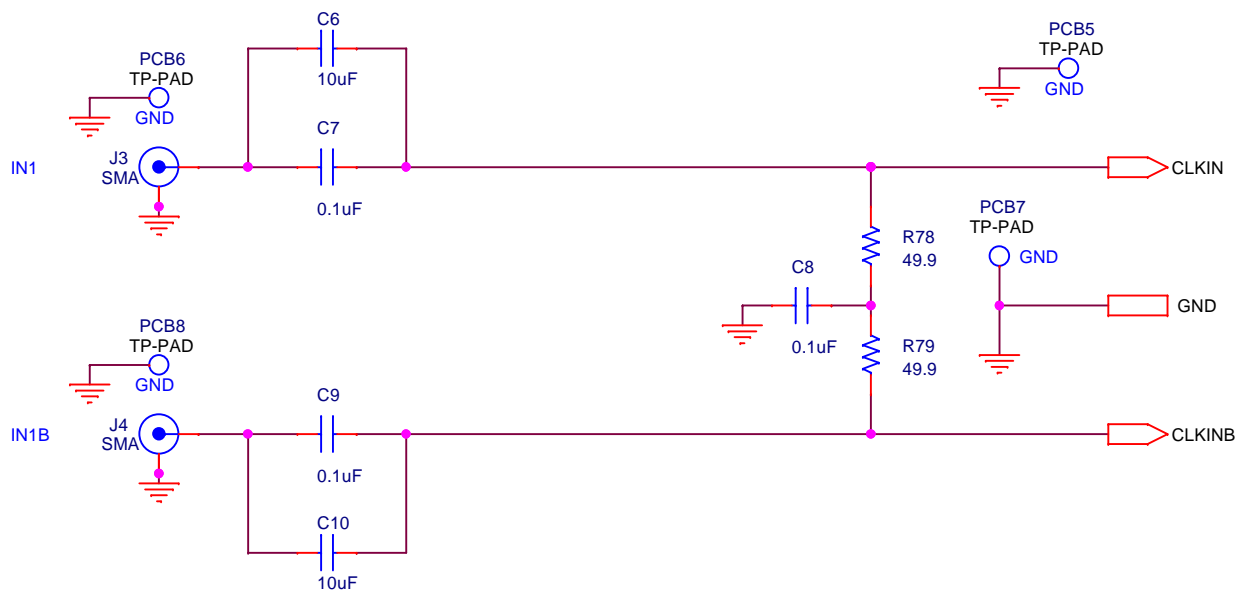
# CONTROL PINS CONNECTIONS


Each LED and the resistor in parallel with it use the same layout pads.  
Both are never installed at the same time.

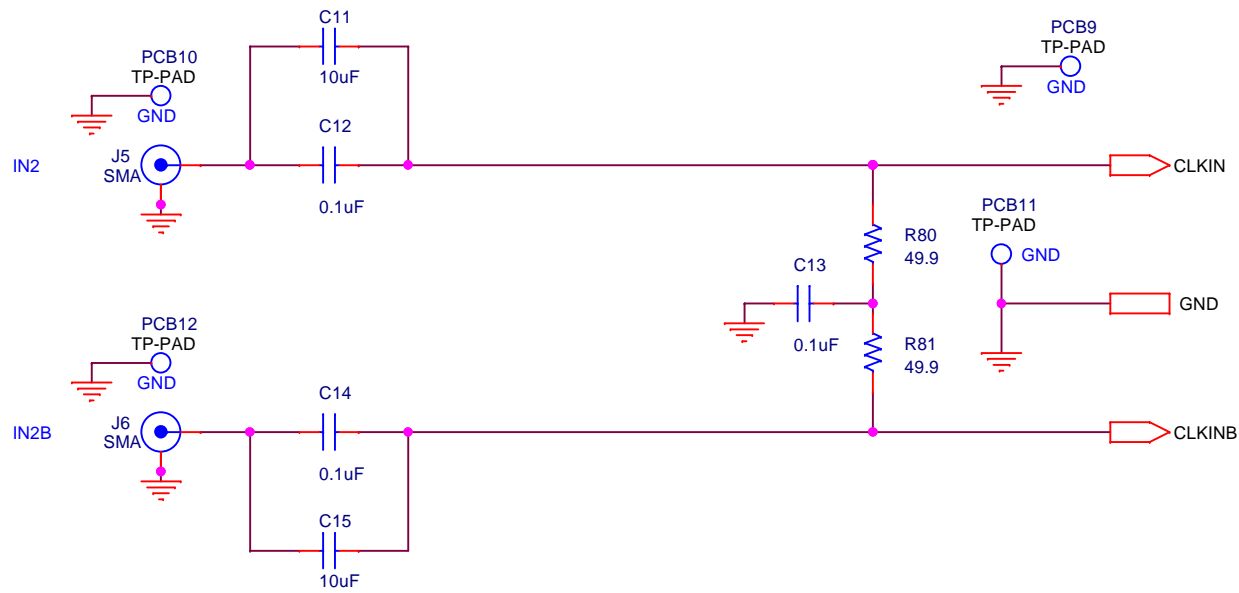


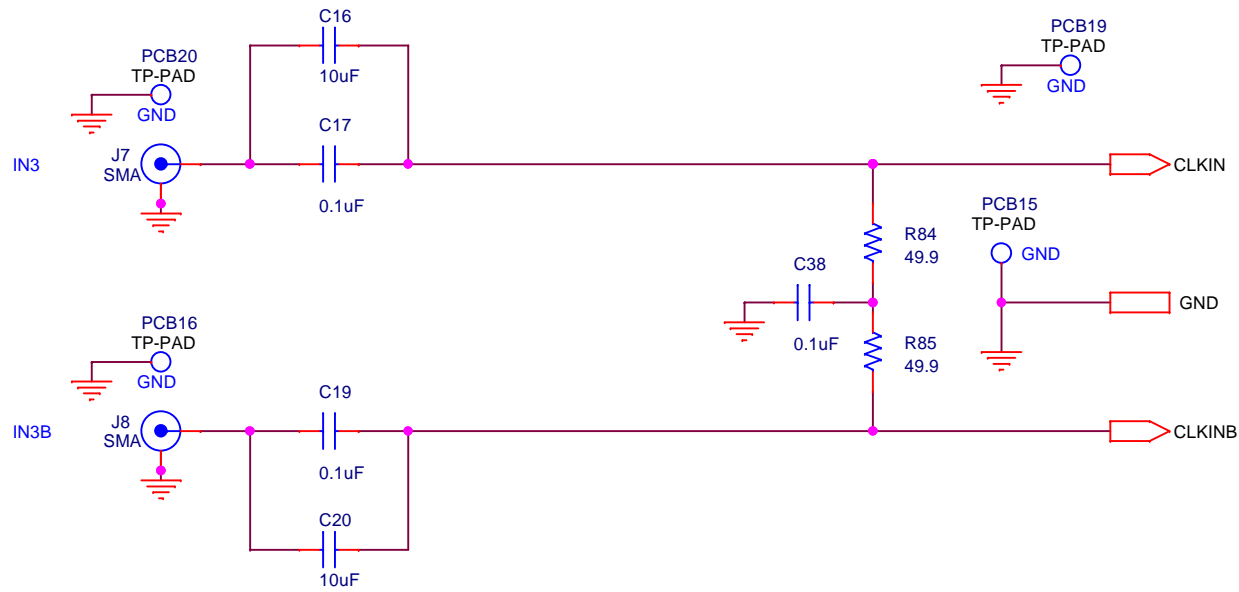
Note:  
1. "N/A" in brackets indicates that the function is not used for the DUT. [N/A]





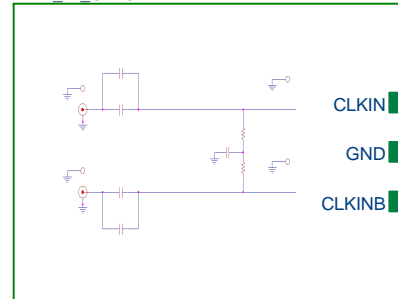
 <b>SILICON LABS</b>		400 W Cesar Chavez Austin, TX 78701	
Title DIFF_INPUT_CLK			
Size A	Document Number SI5341-EB		Rev 1.0
Date: Tuesday, May 20, 2014		Sheet 6	of 44







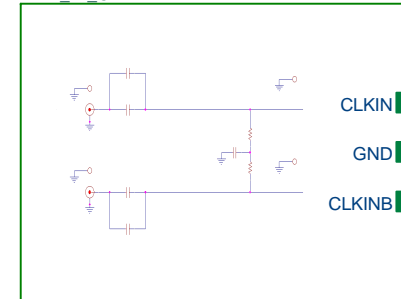
DIFF\_IN\_CLK0



CLKIN → CLKIN0  
 GND → GND  
 CLKINB → CLKIN0B

DIFF\_INPUT\_CLK

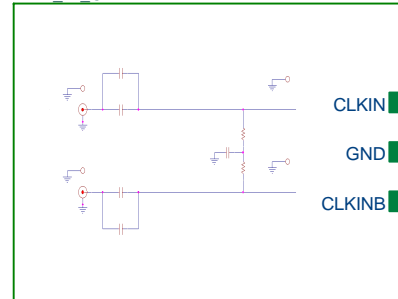
DIFF\_IN\_CLK2



CLKIN → CLKIN2  
 GND → GND  
 CLKINB → CLKIN2B

DIFF\_INPUT\_CLK

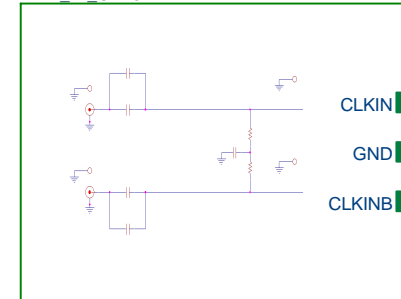
DIFF\_IN\_CLK1



CLKIN → CLKIN1  
 GND → GND  
 CLKINB → CLKIN1B

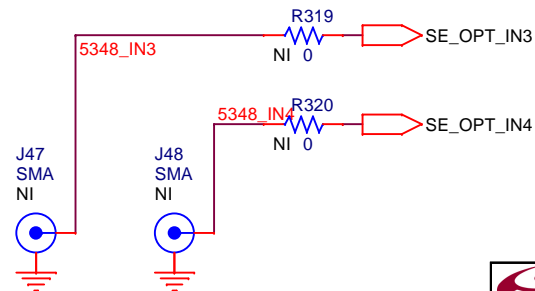
DIFF\_INPUT\_CLK

DIFF\_IN\_CLK3




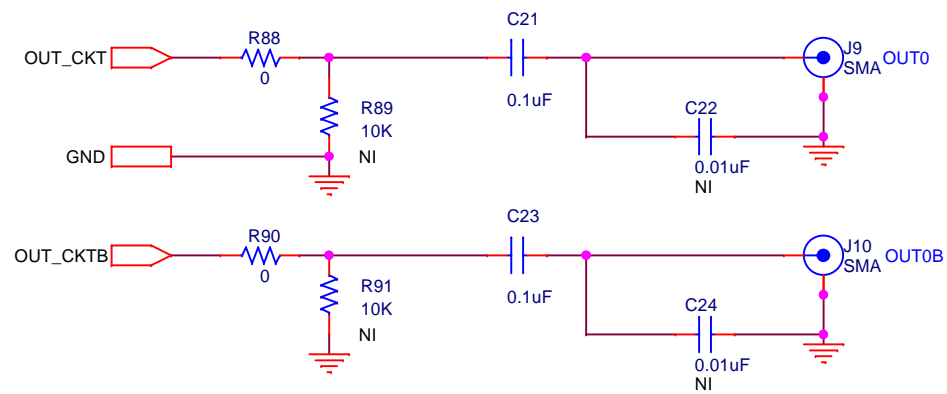
CLKIN → CLKIN3  
 GND → GND  
 CLKINB → CLKIN3B


DIFF\_INPUT\_CLK

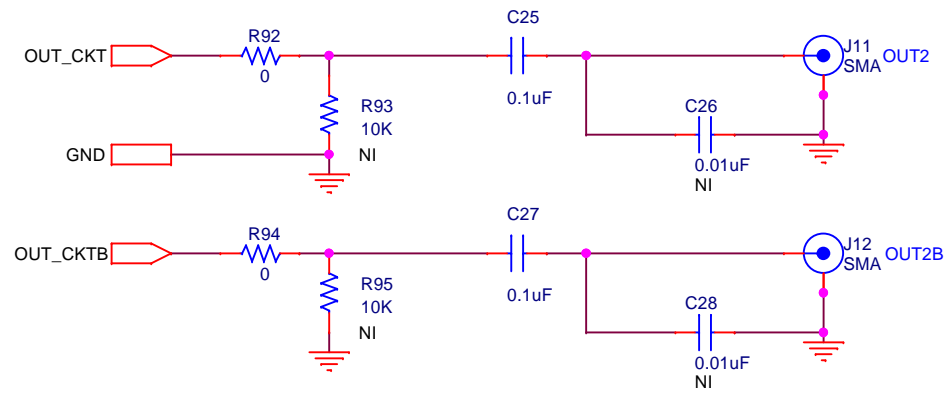



Single-ended clocks only.

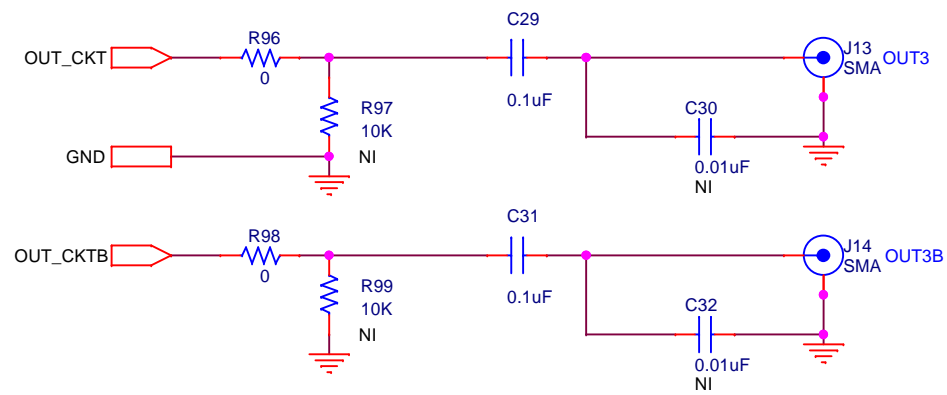
		400 W Cesar Chavez Austin, TX 78701	
Title		DIFF_INPUT_CLOCKS_4	
Size A	Document Number SI5341-EB		Rev 1.0
Date:	Tuesday, May 20, 2014	Sheet	9 of 44




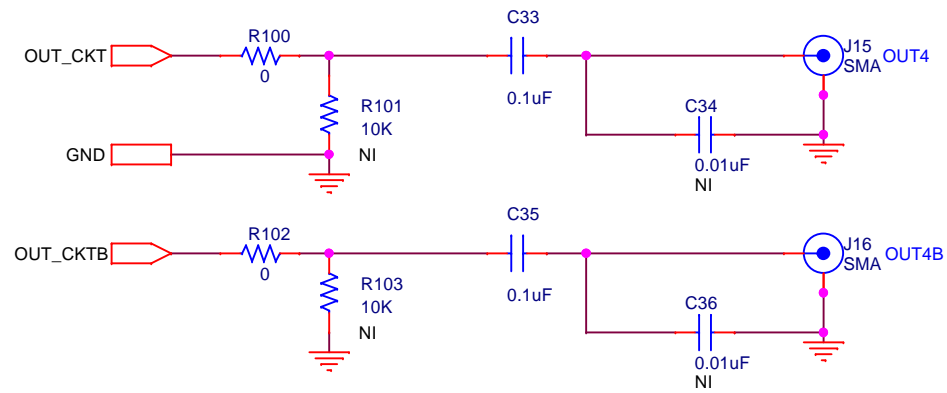
		400 W Cesar Chavez Austin, TX 78701	
Title		DIFF_OUTPUT_CLK	
Size A	Document Number SI5341-EB		Rev 1.0
Date: Tuesday, May 20, 2014		Sheet 10	of 44




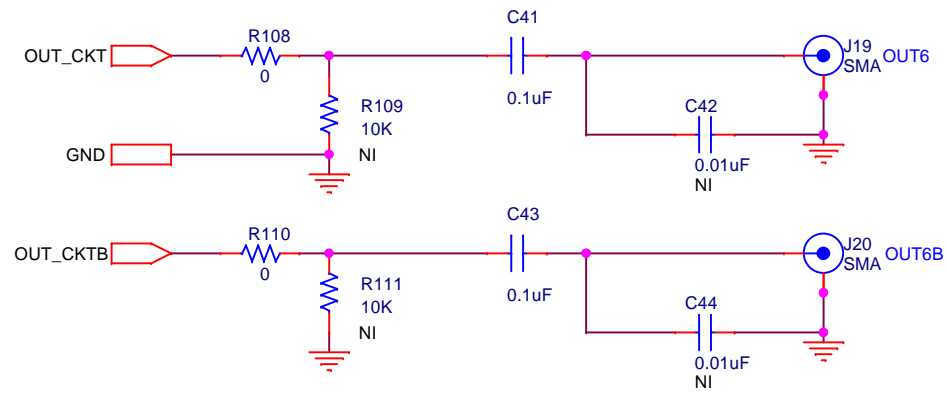
 400 W Cesar Chavez Austin, TX 78701		Rev 1.0
Size A	Document Number SI5341-EB	
Date: Tuesday, May 20, 2014		Sheet 11 of 44




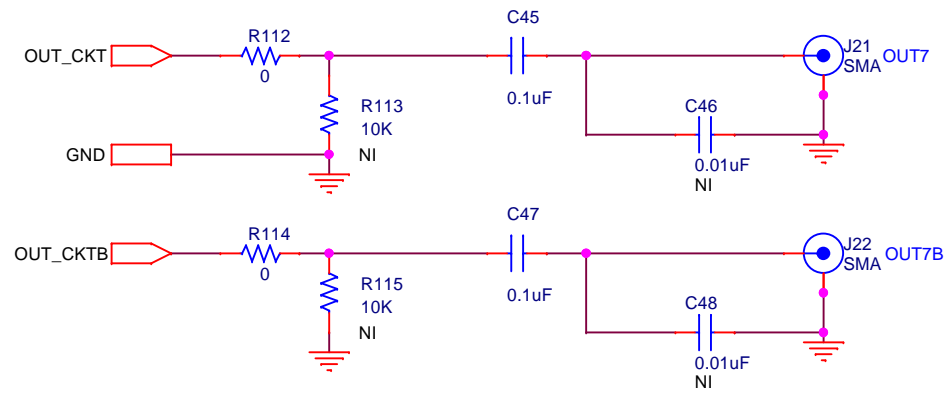
 400 W Cesar Chavez Austin, TX 78701		Title DIFF_OUTPUT_CLK
Size A	Document Number SI5341-EB	Rev 1.0
Date: Tuesday, May 20, 2014		Sheet 12 of 44




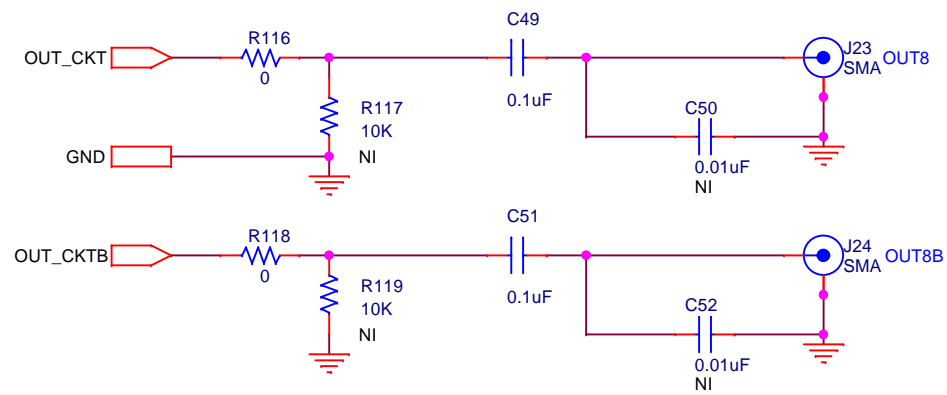
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SILICON LABS		Title	
		DIFF_OUTPUT_CLK	
Size A	Document Number SI5341-EB		Rev 1.0
Date: Tuesday, May 20, 2014		Sheet	13 of 44




		400 W Cesar Chavez Austin, TX 78701	
SILICON LABS		Title	
		DIFF_OUTPUT_CLK	
Size A	Document Number SI5341-EB		Rev 1.0
Date: Tuesday, May 20, 2014		Sheet	14 of 44

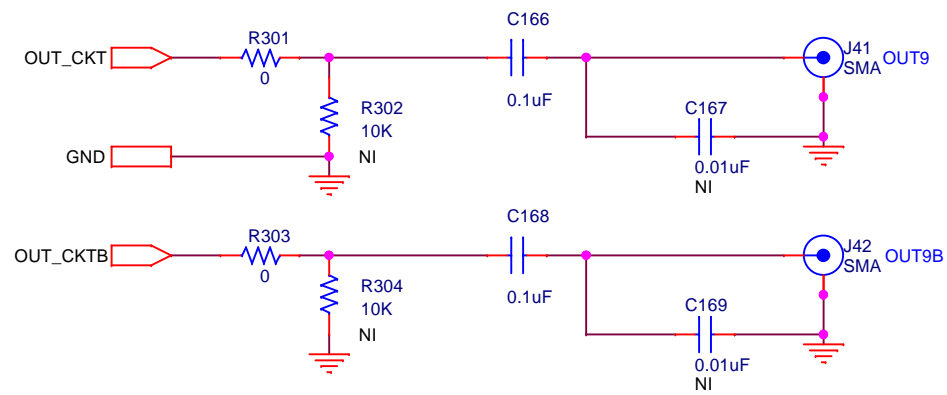



 400 W Cesar Chavez Austin, TX 78701			
		Title	
		DIFF_OUTPUT_CLK	
Size A	Document Number SI5341-EB		Rev 1.0
Date:		Tuesday, May 20, 2014	Sheet 15 of 44



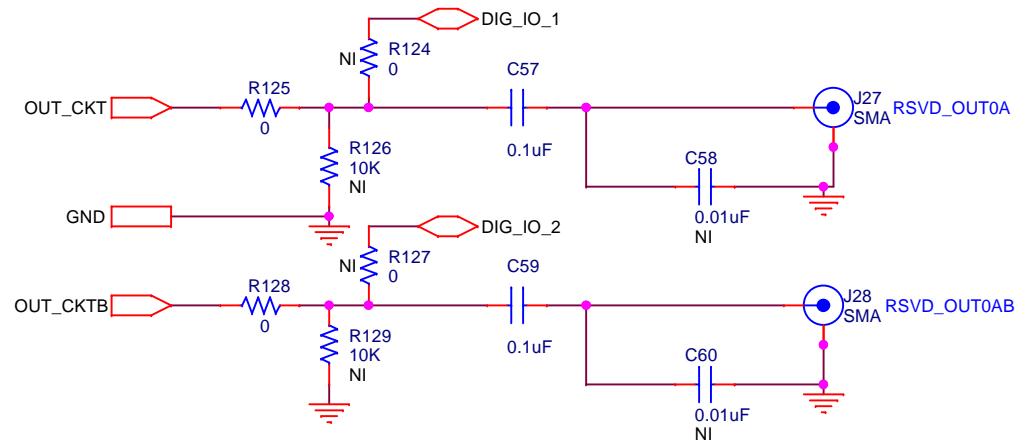
		400 W Cesar Chavez Austin, TX 78701	
Title		DIFF_OUTPUT_CLK	
Size A	Document Number SI5341-EB		Rev 1.0
Date:	Tuesday, May 20, 2014	Sheet	16 of 44






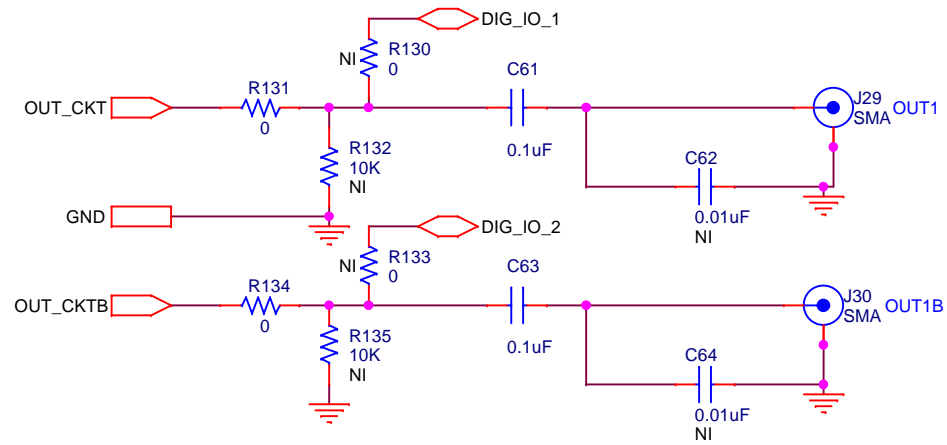
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SILICON LABS		Title	
		DIFF_OUTPUT_CLK	
Size A	Document Number SI5341-EB		Rev 1.0
Date: Tuesday, May 20, 2014		Sheet	17 of 44


# DIFF\_OUTPUT\_CLK\_DIG\_IO



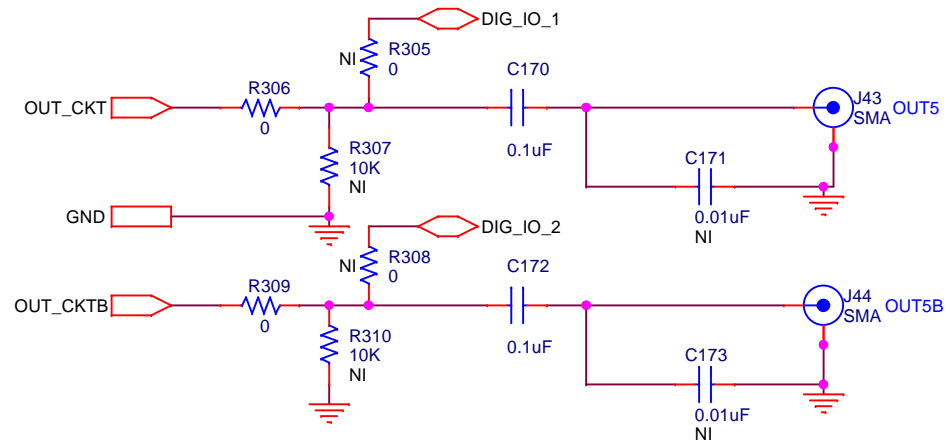
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SILICON LABS		Title	
		DIFF_OUTPUT_CLK_DIG_IO	
Size A	Document Number SI5341-EB		Rev 1.0
Date: Tuesday, May 20, 2014		Sheet	18 of 44


# DIFF\_OUTPUT\_CLK\_DIG\_IO



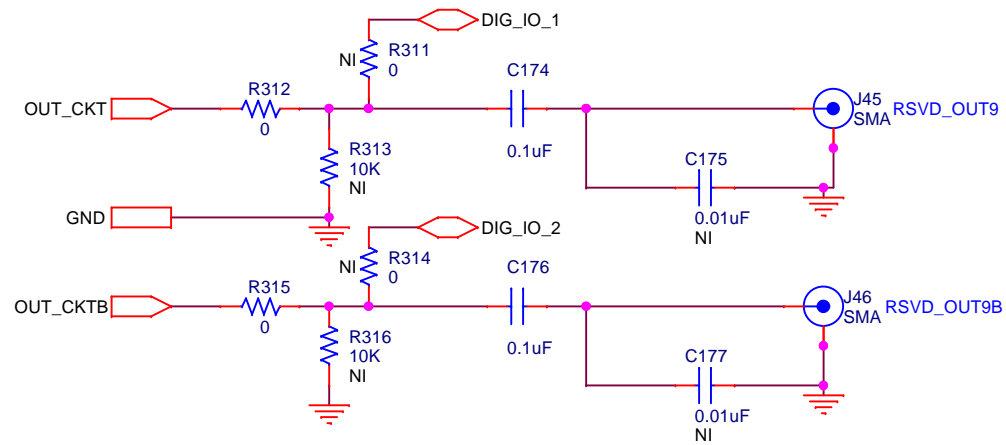
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SILICON LABS		Title	
		DIFF_OUTPUT_CLK_DIG_IO	
Size	Document Number		Rev
A	SI5341-EB		1.0
Date:		Tuesday, May 20, 2014	Sheet 19 of 44


# DIFF\_OUTPUT\_CLK\_DIG\_IO

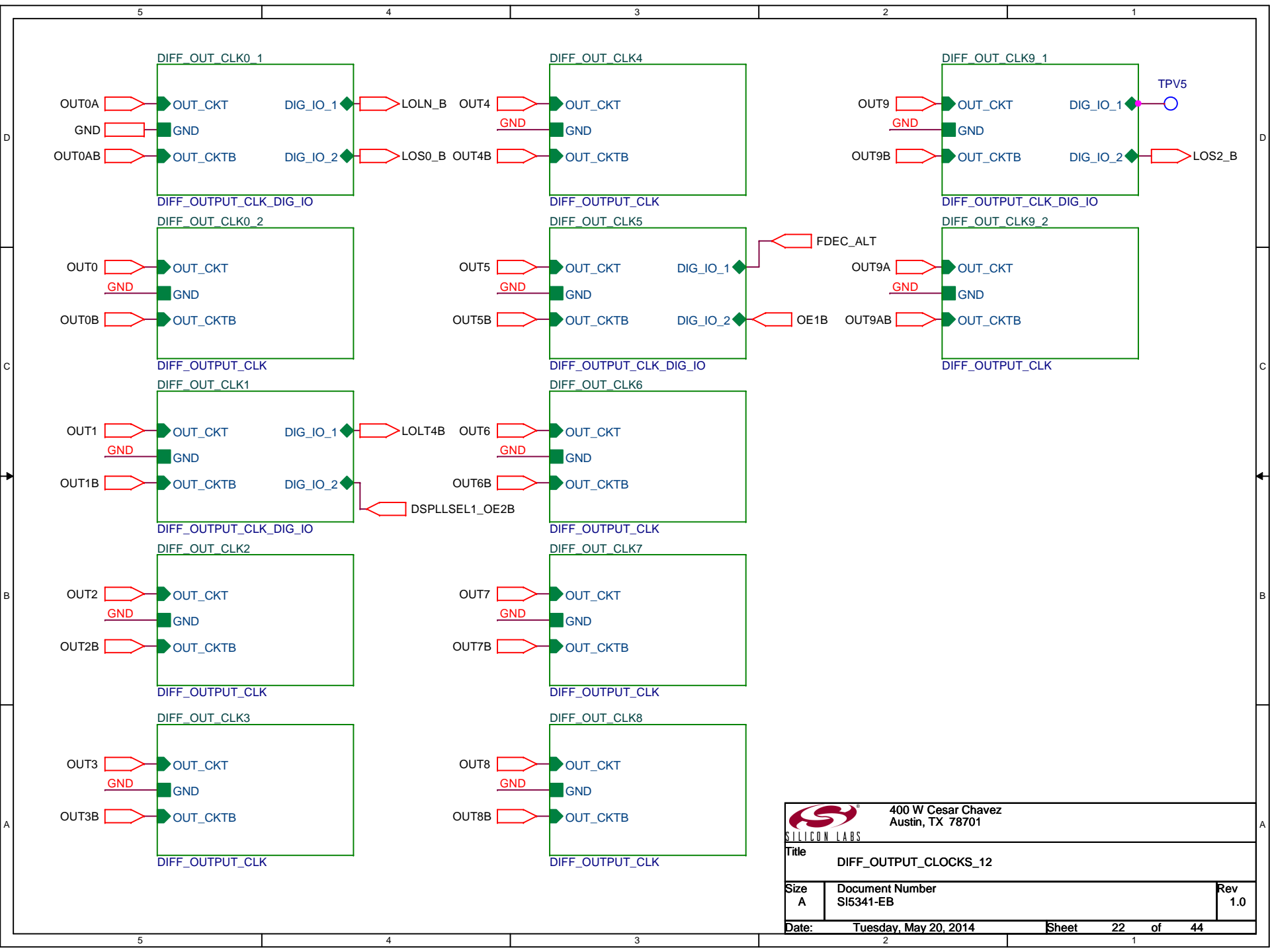


		400 W Cesar Chavez Austin, TX 78701	
Title			
DIFF_OUTPUT_CLK_DIG_IO			
Size A	Document Number SI5341-EB		Rev 1.0
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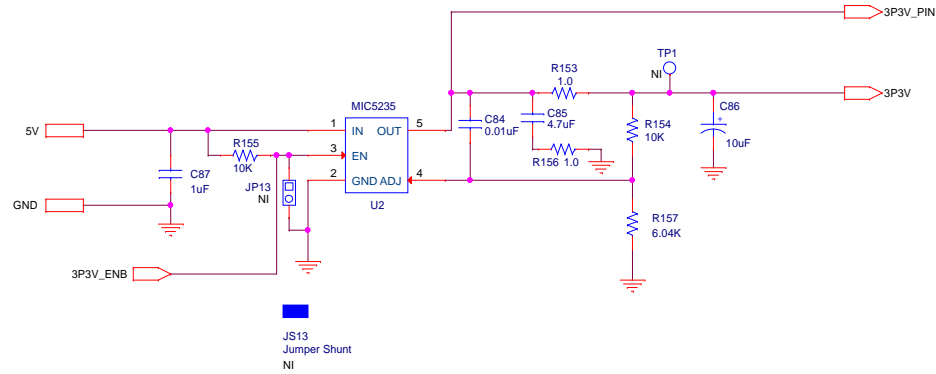
# DIFF\_OUTPUT\_CLK\_DIG\_IO



		400 W Cesar Chavez Austin, TX 78701	
SILICON LABS		Title	
		DIFF_OUTPUT_CLK_DIG_IO	
Size A	Document Number SI5341-EB		Rev 1.0
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# Fixed 3.3V 150 mA Voltage Regulator



3P3V\_DUT (In Schematic)  
VDDA DUT (Board Silkscreen)



400 W Cesar Chavez  
Austin, TX 78701

Title  
VDD\_REG\_MIC5235

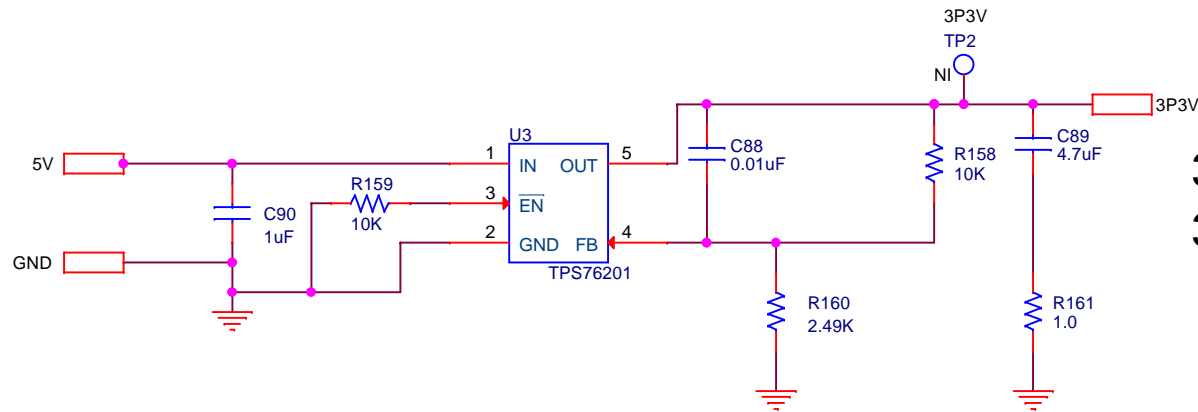
Size  
B Document Number  
SIS341-EB

Rev  
1.0


Date: Tuesday, May 20, 2014

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# Fixed 3.3V 100 mA Voltage Regulator (Enabled, no current measurement supported.)

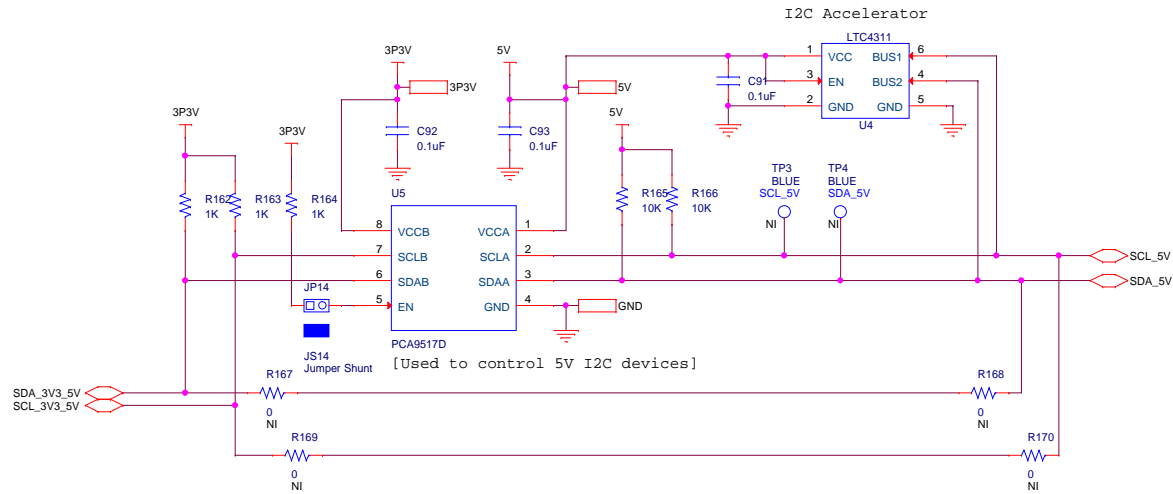


3P3V (In Schematic)  
3P3V (Board Silkscreen)

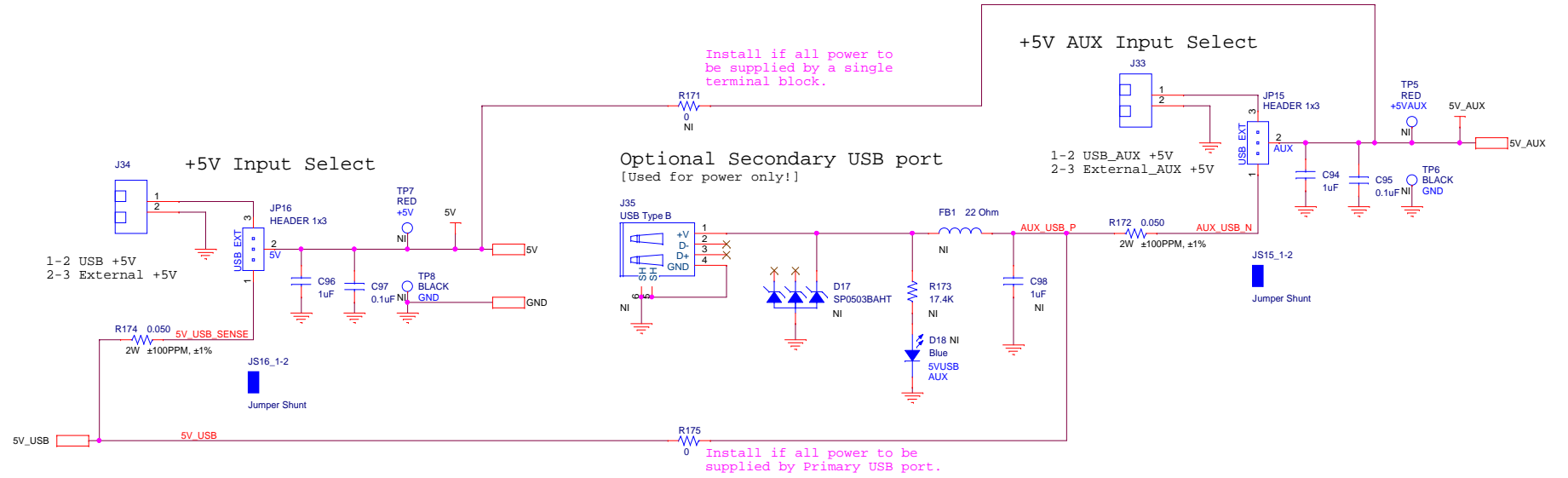
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Title		FIXED_3V3_REG_TPS76201_EN_NO_IM	
Size A	Document Number SI5341-EB	<Variant Name>	Rev 1.0
Date:	Tuesday, May 20, 2014	Sheet	24 of 44



I2C LEVEL TRANSLATORS



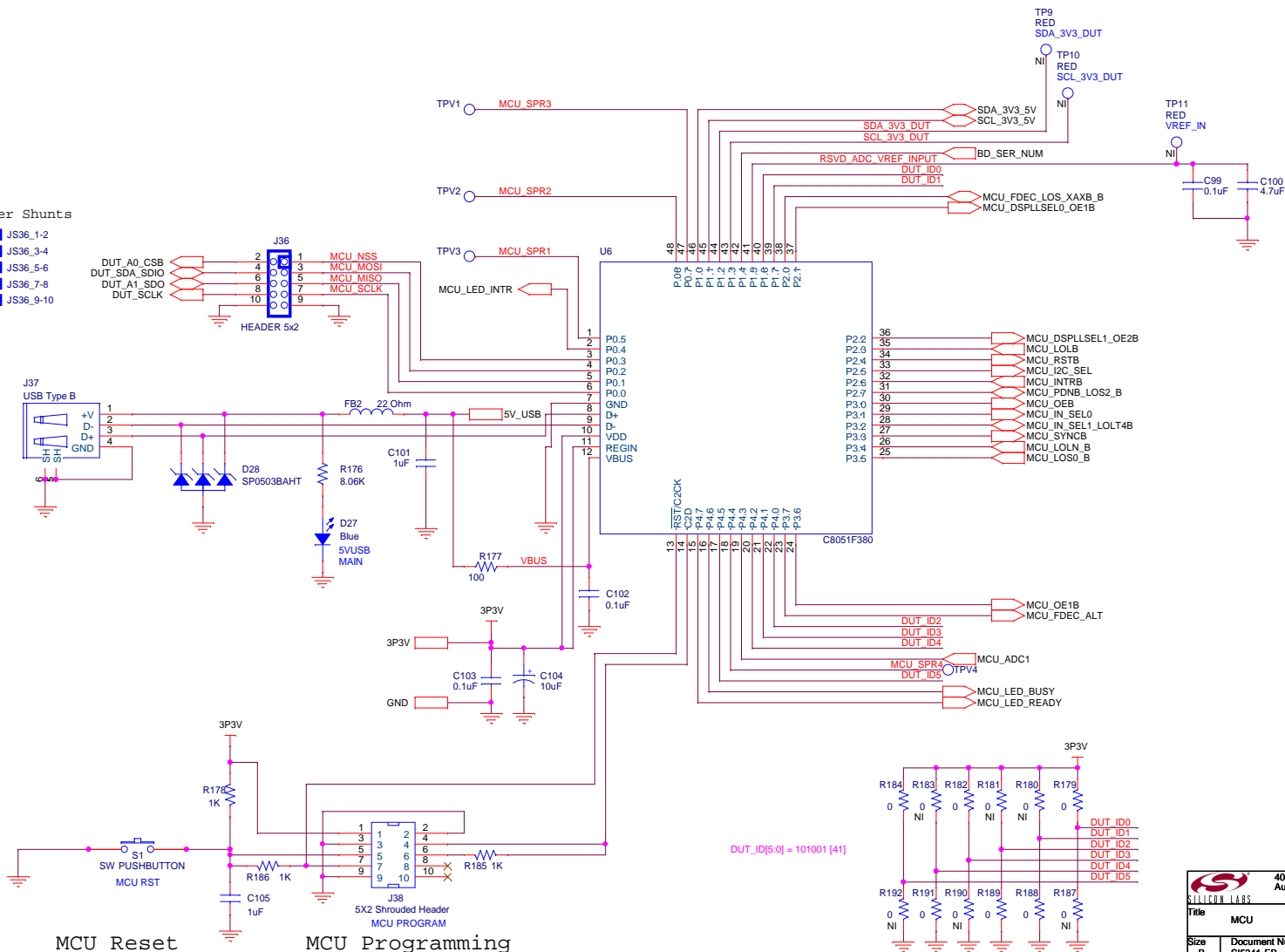
MAIN POWER INPUT SELECTS  
EXTERNAL OR USB



# 8051 MCU

## Jumper Shunts

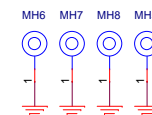
- JS36\_1-2
- JS36\_3-4
- JS36\_5-6
- JS36\_7-8
- JS36\_9-10



## Mounting Holes, Screws, and Standoffs

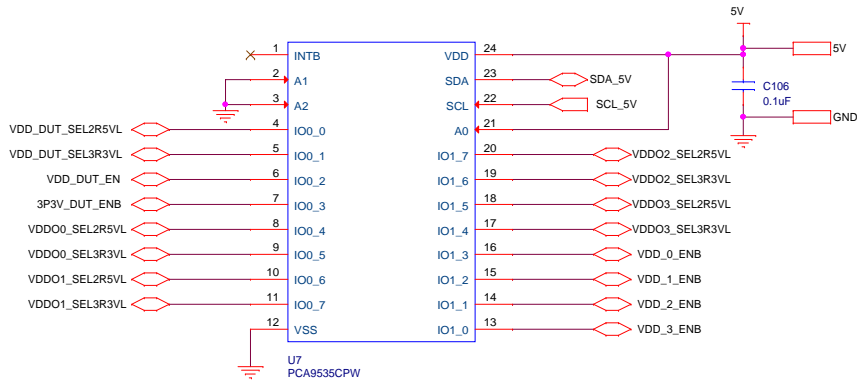


## Mounting Holes

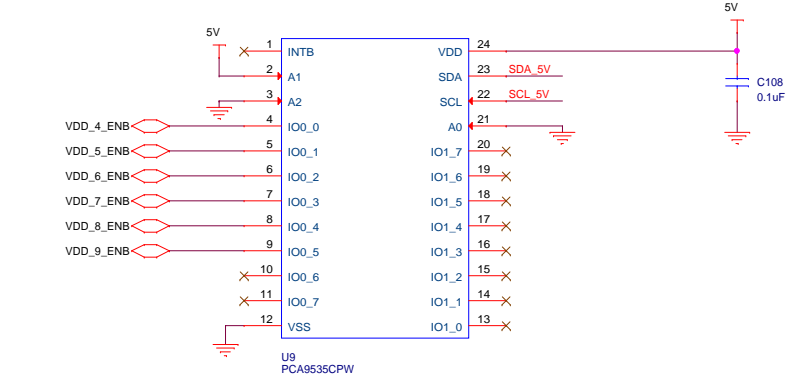


		400 W Cesar Chavez Austin, TX 78701	
Title		MCU	
Size	Document Number	Rev	
B	SIS341-EB	1.0	
Date:	Monday, June 09, 2014	Sheet	27 of 44

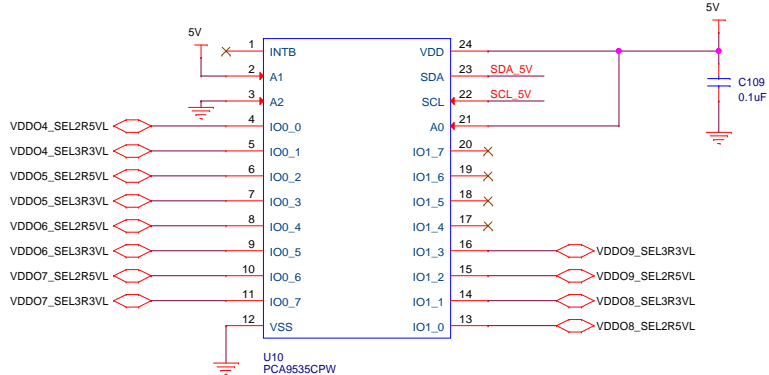
PERIPHERALS



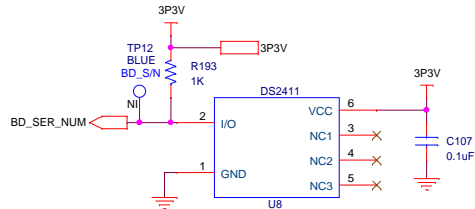
I2C VDD ENABLES/SELECTS FOR REGULATORS  
I2C address: 0100001



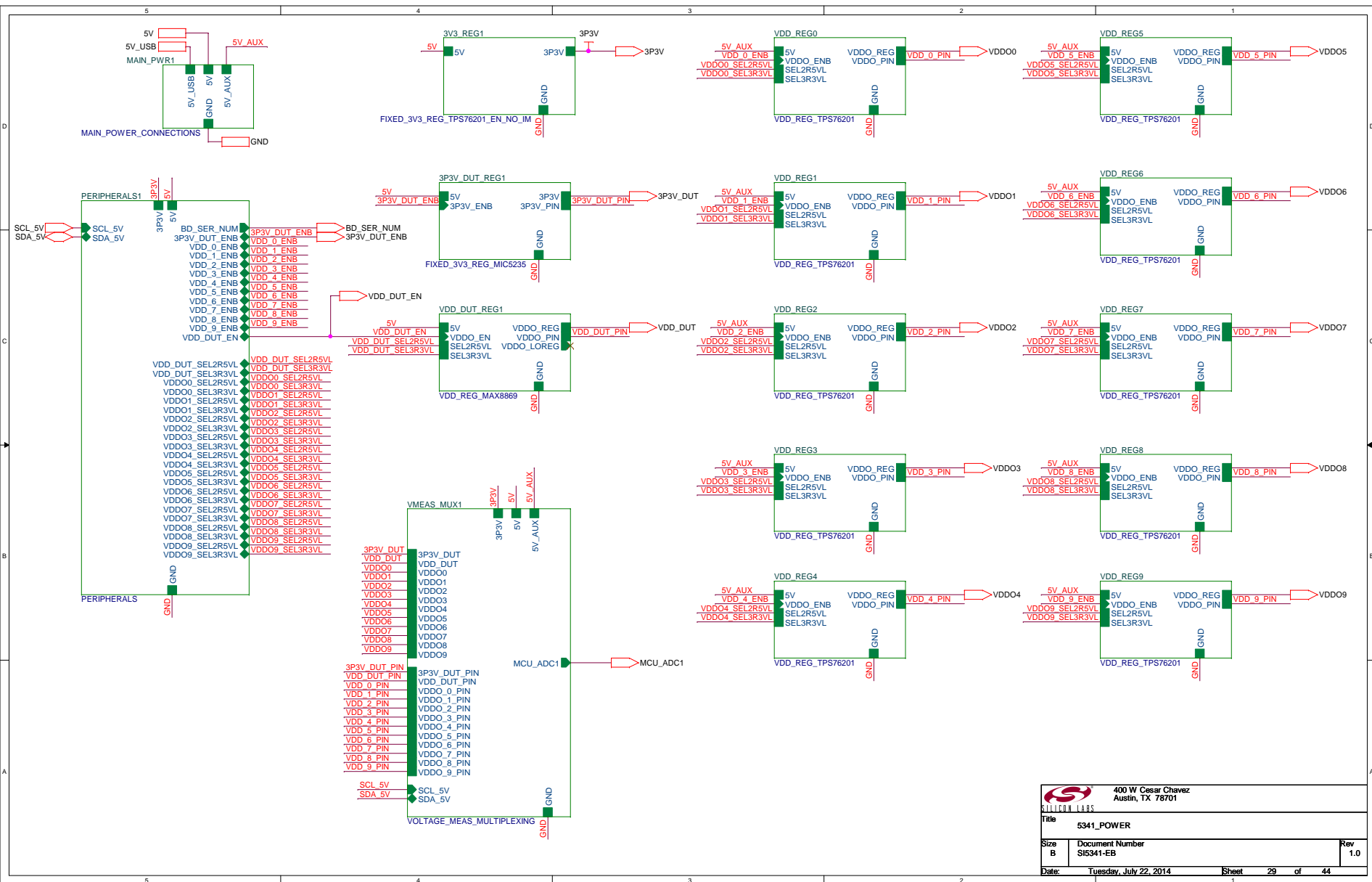
I2C VDD ENABLES/SELECTS FOR REGULATORS  
I2C address: 0100010



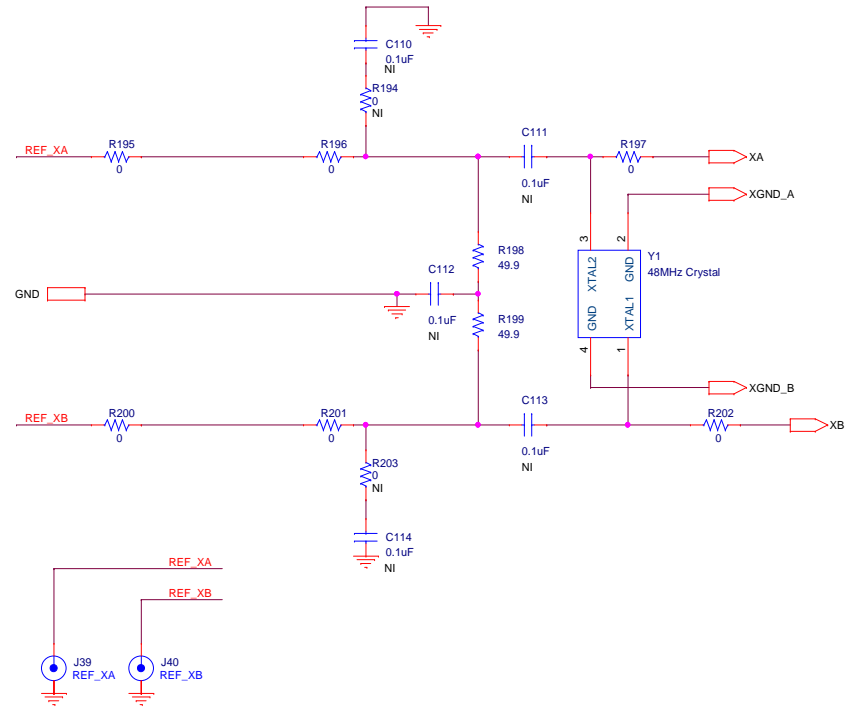
I2C VDD ENABLES/SELECTS FOR REGULATORS  
I2C address: 0100011



Board Serial Number

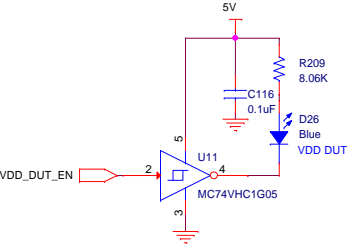
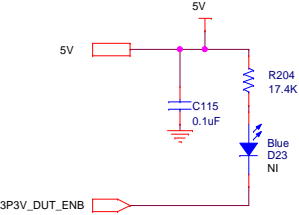
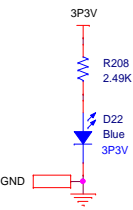
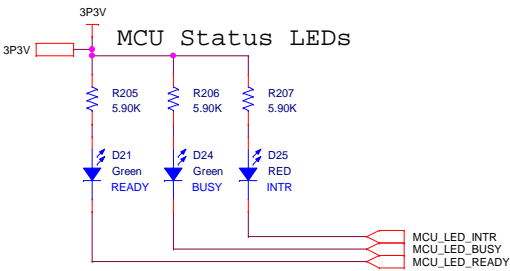


# REFERENCE INPUT CONNECTIONS





LEDS - SUPPLIES & STATUS



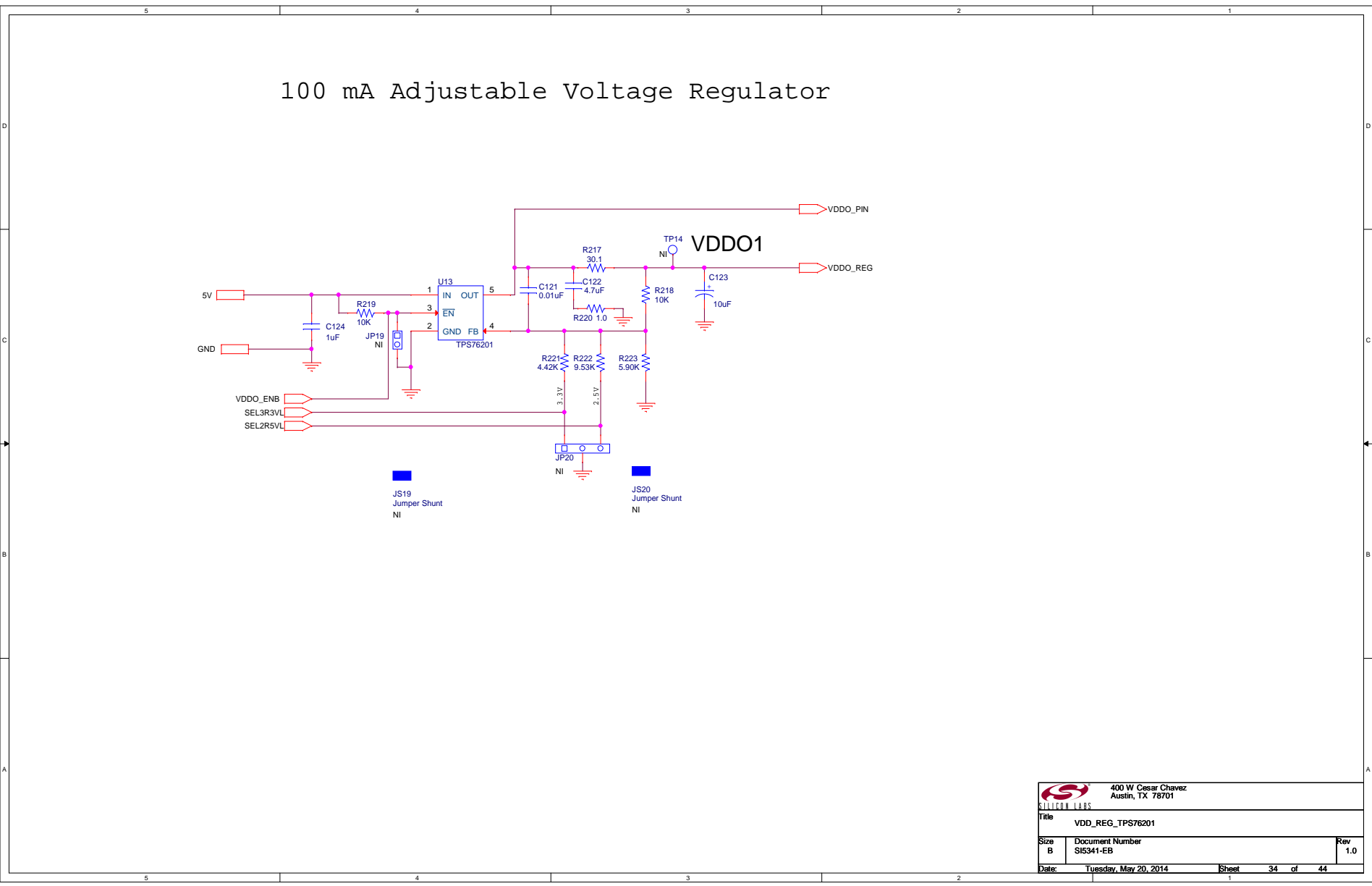


The schematic diagram illustrates the VDDO0 power supply circuit. It features a 5V input source connected to a 1uF capacitor (C120) and a 10K resistor (R212). The output of this network is connected to the IN pin of the TPS76201 op-amp (U12). The op-amp is configured as a voltage follower, with its output connected to its FB pin. The output of the op-amp is connected to a 30.1 ohm resistor (R210), a 0.01uF capacitor (C117), and a 4.7uF capacitor (C118). The output is also connected to a 10K resistor (R211) and a 10uF capacitor (C119). The output voltage is labeled VDDO0 and VDDO\_REG. The circuit also includes a 3.3V regulator (U13) and a 2.5V regulator (U14) with their respective resistors and capacitors. A jumper shunt JP18 is used for the 2.5V regulator output.

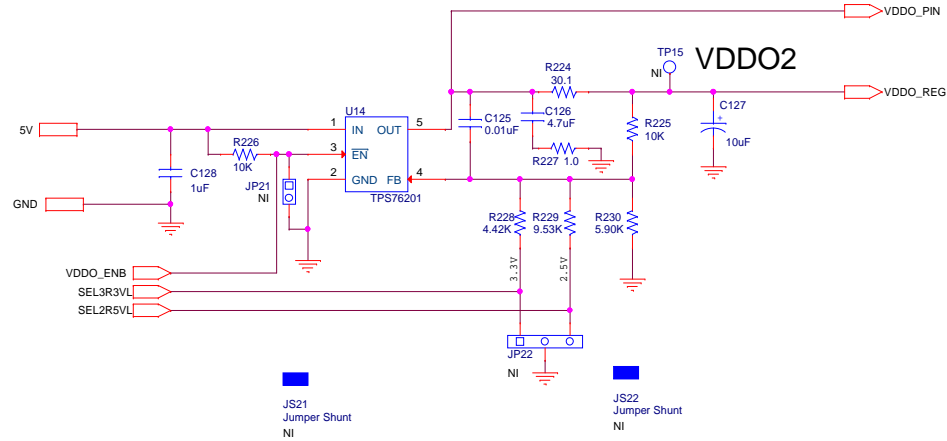
# 100 mA Adjustable Voltage Regulator

The schematic diagram illustrates a 100 mA Adjustable Voltage Regulator circuit. The circuit is powered by a 5V input and ground. The input is connected to the IN pin of the TPS76201 (U13). The EN pin is connected to the 5V input through a 10K resistor (R219). The FB pin is connected to ground. The output of the regulator is connected to the VDDO1 and VDDO\_REG pins. The output is filtered by a 10uF capacitor (C123). The feedback network consists of resistors R217 (30.1K), R218 (10K), R220 (1.0K), R221 (4.42K), R222 (9.53K), and R223 (5.90K). The output is also filtered by a 0.01uF capacitor (C121) and a 4.7uF capacitor (C122). The circuit includes two jumper shunts, JS19 and JS20, and a test point, TP14.

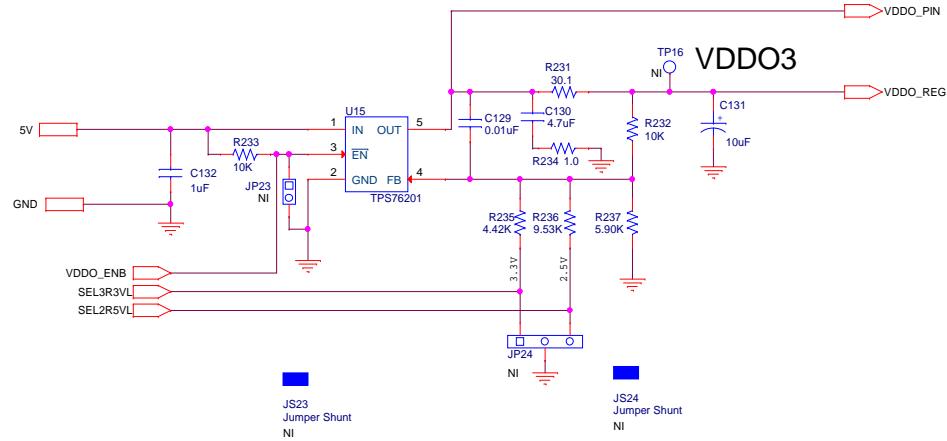
SILICON LABS		400 W Cesar Chavez Austin, TX 78701	
Title: VDD_REG_TPS76201			
Size: B	Document Number: SIS341-EB		Rev: 1.0
Date: Tuesday, May 20, 2014	Sheet: 1	34 of 44	



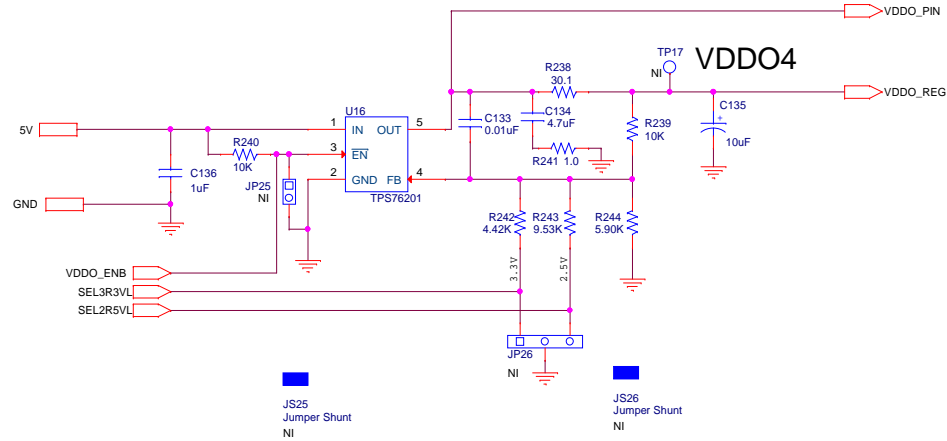
# 100 mA Adjustable Voltage Regulator



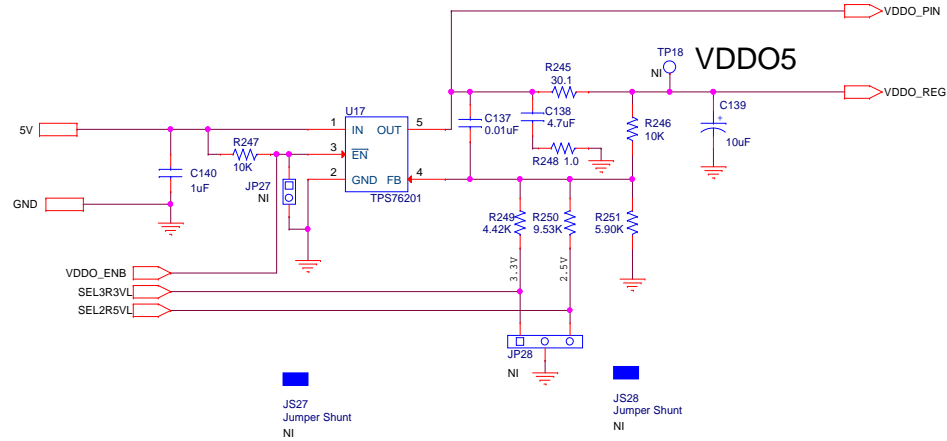
# 100 mA Adjustable Voltage Regulator



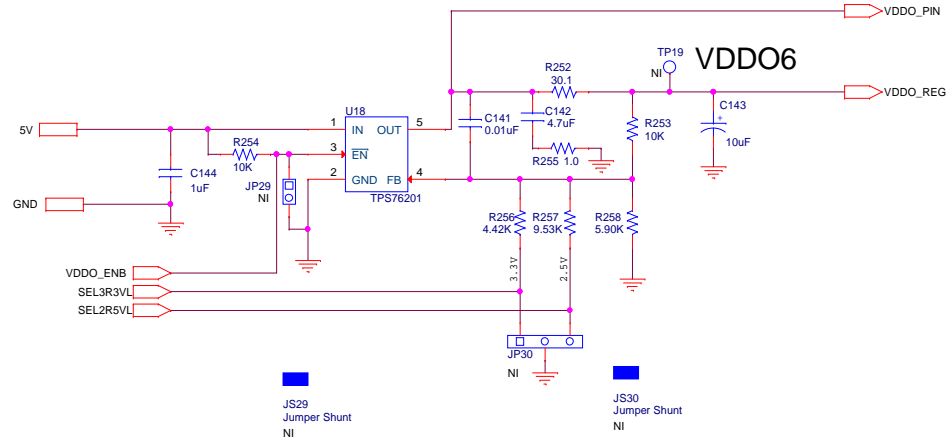
# 100 mA Adjustable Voltage Regulator



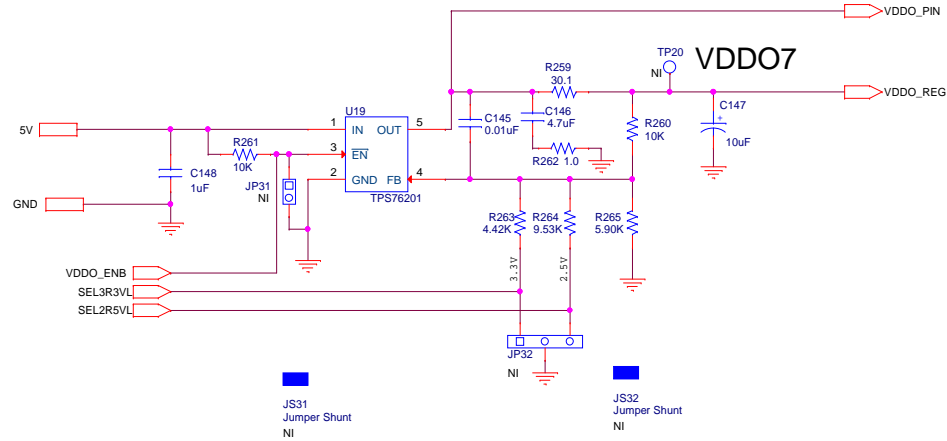
# 100 mA Adjustable Voltage Regulator



# 100 mA Adjustable Voltage Regulator

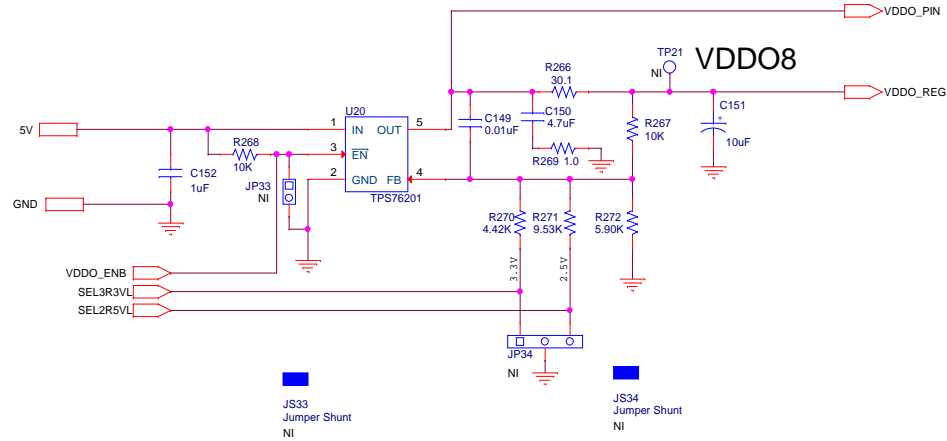


# 100 mA Adjustable Voltage Regulator





# 100 mA Adjustable Voltage Regulator







# VOLTAGE MEASUREMENT MULTIPLEXING

