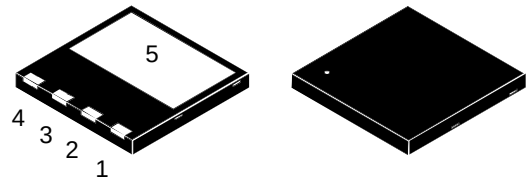
STL38N65M5

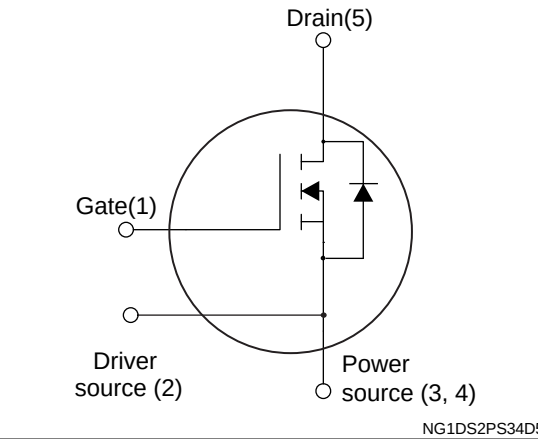
N-channel 650 V, 0.090 Ω typ., 22.5 A MDmesh™ M5 Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data



PowerFLAT™ 8x8 HV

Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D
STL38N65M5	710 V	0.105 Ω	22.5 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL38N65M5	38N65M5	PowerFLAT™ 8x8 HV	Tape and reel

This is information on a product in full production.

www.st.com

Contents

1 Electrical ratings 3
2 Electrical characteristics 4
2.1 Electrical characteristics (curves) 6
3 Test circuits 9
4 Package information 10
4.1 PowerFLAT™ 8x8 HV package information 11
4.2 PowerFLAT™ 8x8 HV packing information 13
5 Revision history 15

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	± 25	V
I_D(1)	Drain current (continuous) at T_C = 25 °C	22.5	A
I_D(1)	Drain current (continuous) at T_C = 100 °C	16	A
I_{DM}(1)(2)	Drain current (pulsed)	90	A
I_D(3)	Drain current (continuous) at T_{pcb} = 25 °C	3.5	A
I_D(3)	Drain current (continuous) at T_{pcb} = 100 °C	2.2	A
P_{TOT}(3)	Total dissipation at T_{pcb} = 25 °C	2.8	W
P_{TOT}(1)	Total dissipation at T_C = 25 °C	150	W
I_{AR}	Avalanche current, repetitive or notrepetitive (pulse width limited by Tj max)	7	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	660	mJ
dv/dt(4)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	

Notes:

(1)The value is rated according to $R_{thj\text{-}case}$.

(2)Pulse width limited by safe operating area.

(3)When mounted on FR-4 board of 1 inch² , 2oz Cu.

(4)I_{SD} ≤ 22.5 A, di/dt ≤ 400 A/µs; $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 400 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.83	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb max	45	°C/W

Notes:

(1)When mounted on FR-4 board of 1 inch², 2oz Cu.

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage Drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 12.5 A		0.090	0.105	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 100 V, f = 1 MHz, V_{GS} = 0 V	-	3000	-	pF
C_{oss}	Output capacitance		-	74	-	pF
C_{rss}	Reverse transfer capacitance		-	5.8	-	pF
$C_{o(er)}$(1)	Equivalent output capacitance energy related	V_{DS} = 0 to 80% $V_{(BR)DSS}$, V_{GS} = 0 V	-	70	-	pF
$C_{o(tr)}$(2)	Equivalent output capacitance time related		-	244	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz	-	2.4	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 15 A, V_{GS} = 10 V (see *Figure 16: "Gate charge test circuit"*)	-	71	-	nC
Q_{gs}	Gate-source charge		-	18	-	nC
Q_{gd}	Gate-drain charge		-	30	-	nC

Notes:

(1)$C_{o(er)}$ is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

(2)$C_{o(tr)}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	V_{DD} = 400 V, I_D = 20 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 17: " Test circuit for inductive load switching and diode recovery times"*and *Figure 20: "Switching time waveform"*)	-	66	-	ns
$t_{r(V)}$	Voltage rise time		-	9	-	ns
$t_{f(i)}$	Crossing fall time		-	9	-	ns
$t_{C(off)}$	Crossing time		-	13	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} *(1)*	Source-drain current		-		22.5	A
I_{SDM} *(1),(2)*	Source-drain current (pulsed)		-		90	A
V_{SD} *(3)*	Forward on voltage	V_{GS} = 0 V, I_{SD} = 22.5 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 22.5 A, di/dt = 100 A/µs, V_{DD} = 100 V (see *Figure 17: " Test circuit for inductive load switching and diode recovery times"*)	-	354		ns
Q_{rr}	Reverse recovery charge		-	6		µC
I_{RRM}	Reverse recovery current		-	34		A
t_{rr}	Reverse recovery time	I_{SD} = 22.5 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 150 °C (see *Figure 17: " Test circuit for inductive load switching and diode recovery times"*)	-	428		ns
Q_{rr}	Reverse recovery charge		-	8		µC
I_{RRM}	Reverse recovery current		-	38		A

Notes:

(1)The value is rated according to $R_{thj\text{-}case}$ and limited by package.

(2)Pulse width is limited by safe operating area

(3)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

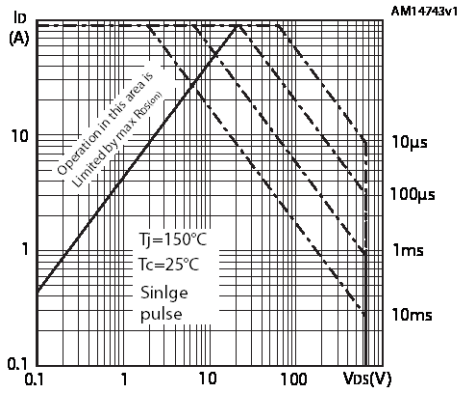


Figure 3: Thermal impedance

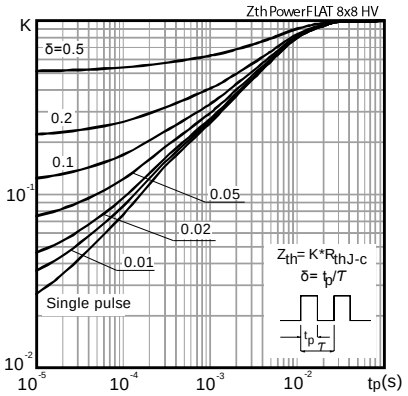


Figure 4: Output characteristics

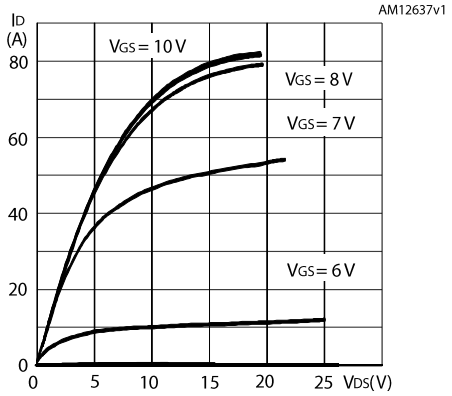


Figure 5: Transfer characteristics

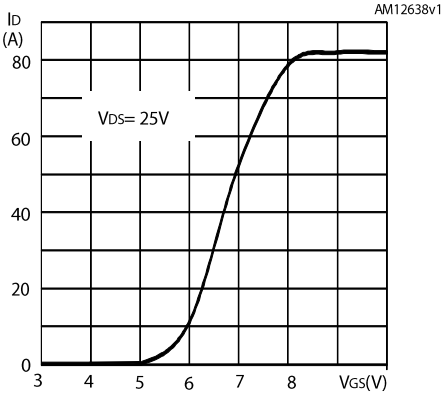


Figure 6: Gate charge vs gate-source voltage

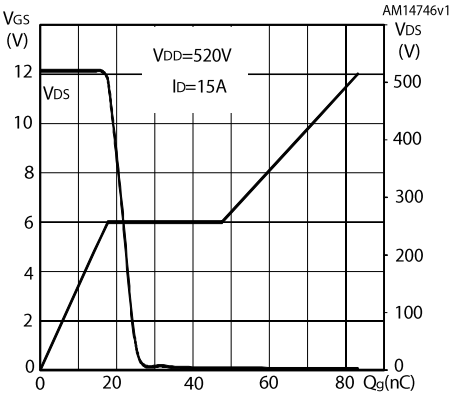


Figure 7: Static drain-source on-resistance

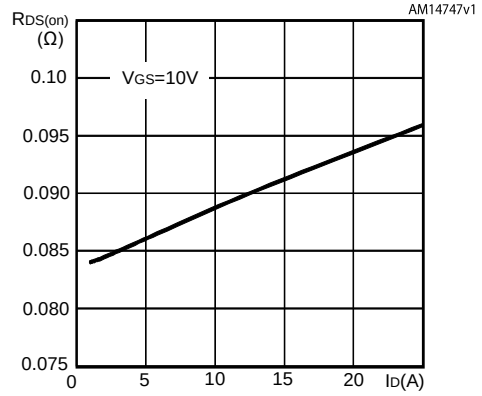


Figure 8: Capacitance variations

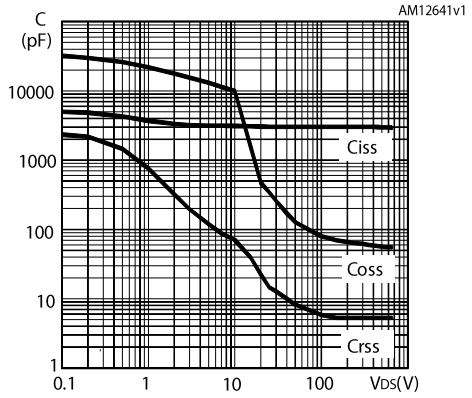


Figure 9: Normalized gate threshold voltage vs temperature

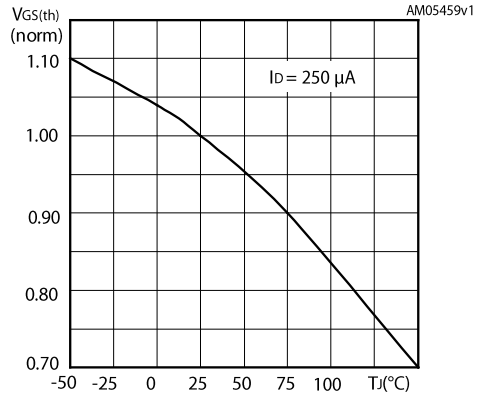


Figure 10: Normalized on-resistance vs temperature

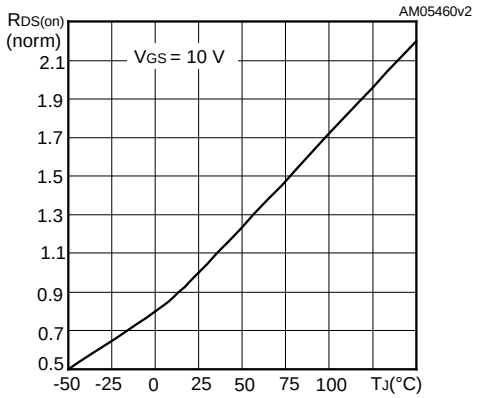


Figure 11: Normalized V(BR)DSS vs temperature

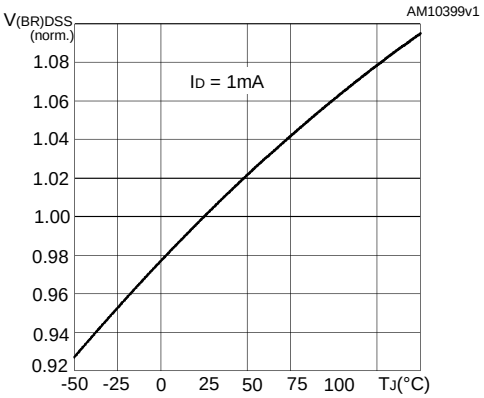


Figure 12: Output capacitance stored energy

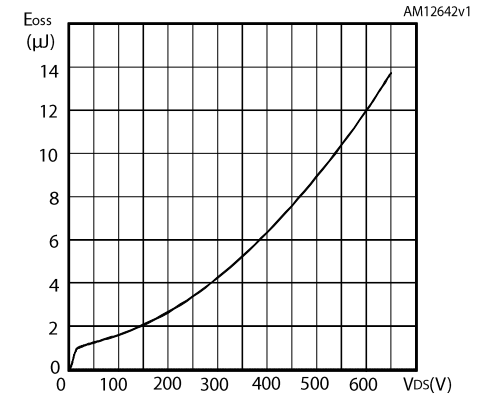


Figure 13: Source-drain diode forward characteristics

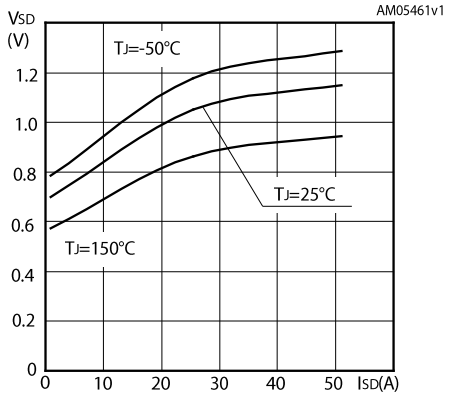
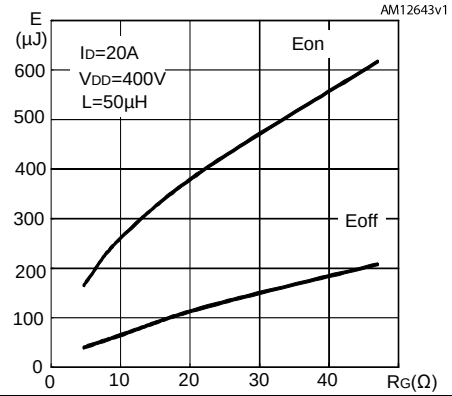


Figure 14: Switching losses vs gate resistance



The previous figure E_{on} includes reverse recovery of a SiC diode.

3 Test circuits

Figure 15: Switching times test circuit for resistive load

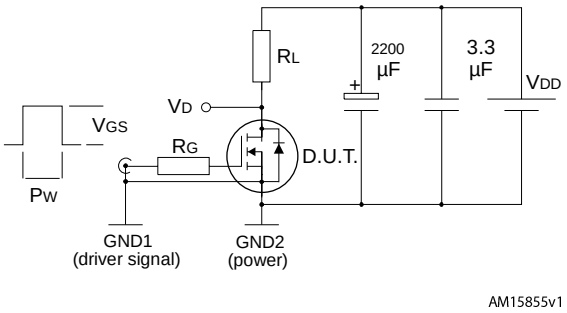


Figure 16: Gate charge test circuit

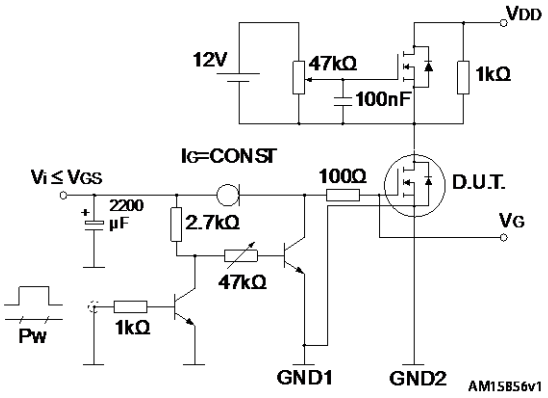


Figure 17: Test circuit for inductive load switching and diode recovery times

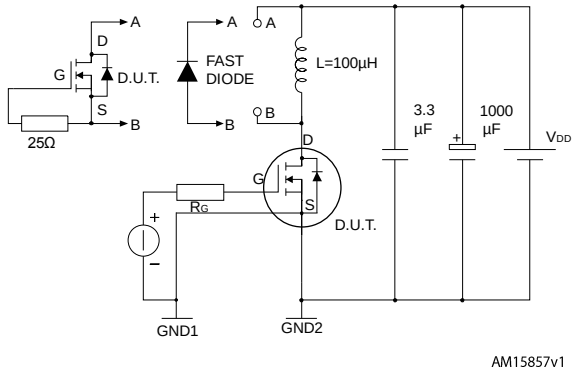


Figure 18: Unclamped inductive load test circuit

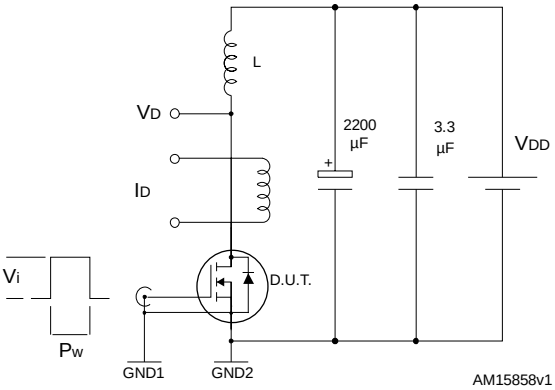


Figure 19: Unclamped inductive waveform

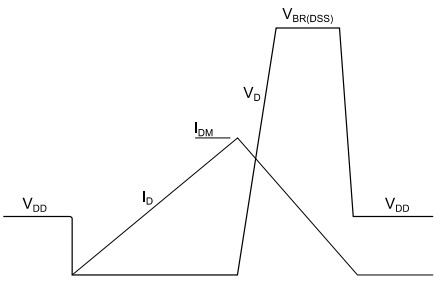
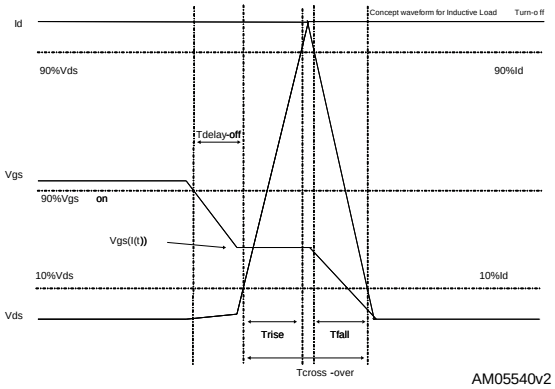


Figure 20: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 8x8 HV package information

Figure 21: PowerFLAT™ 8x8 HV drawing

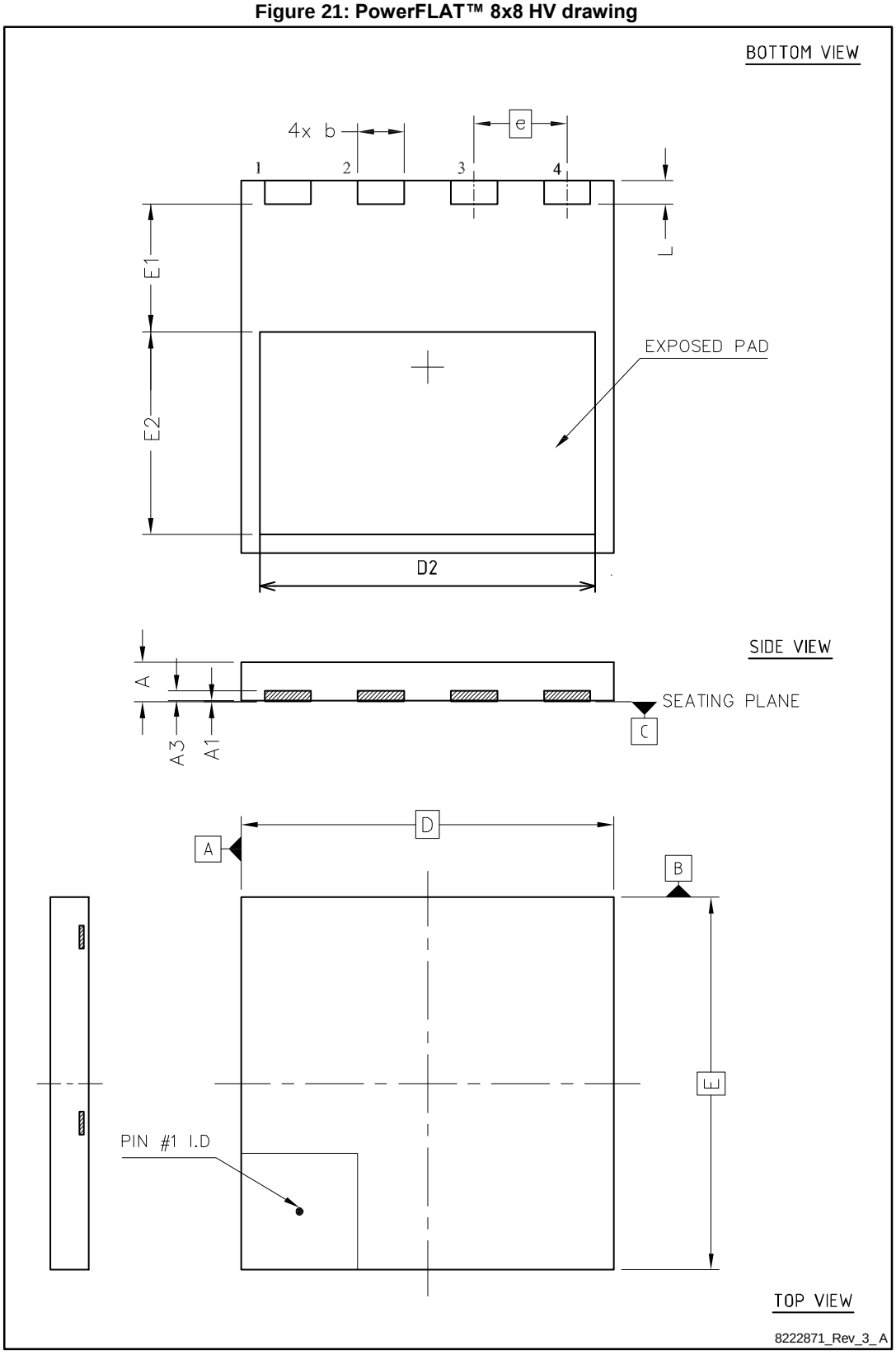
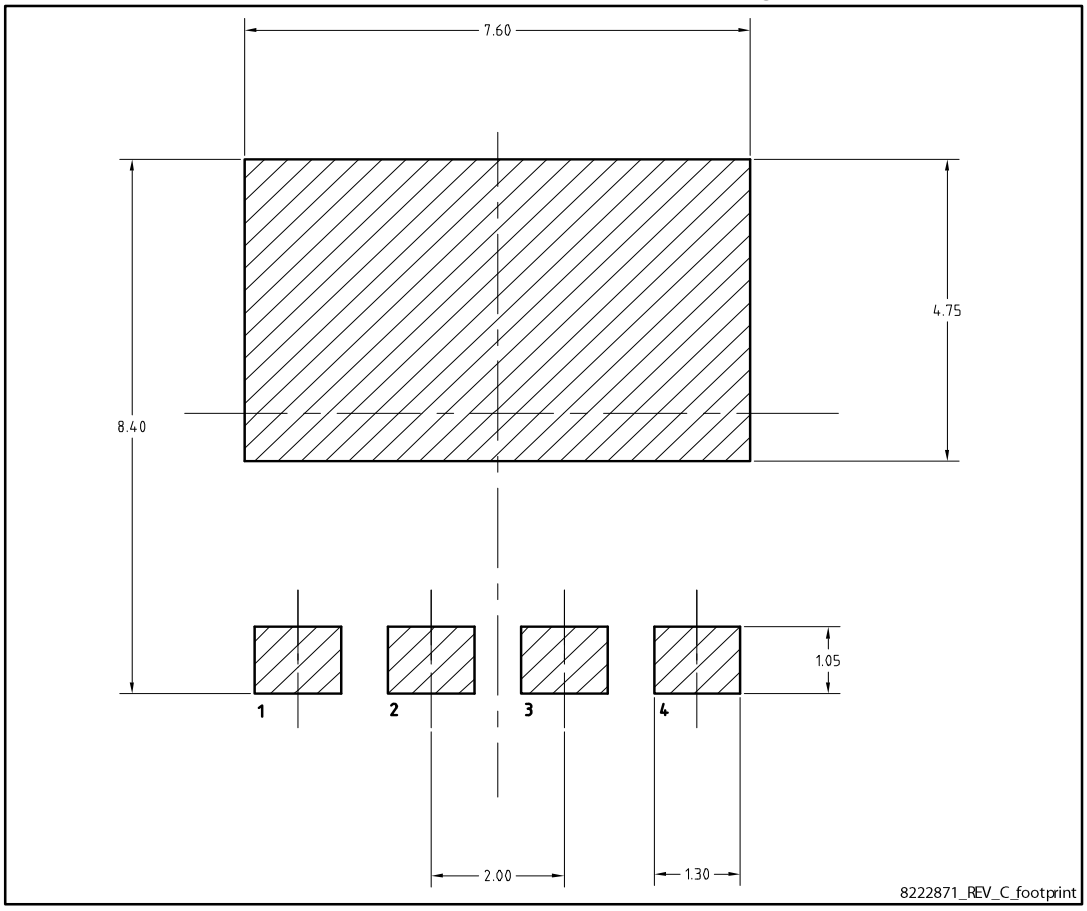


Table 8: PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00	
L	0.40	0.50	0.60

Figure 22: PowerFLAT™ 8x8 HV drawing



All the dimensions are in millimeters.

4.2 PowerFLAT™ 8x8 HV packing information

Figure 23: PowerFLAT™ 8x8 HV tape

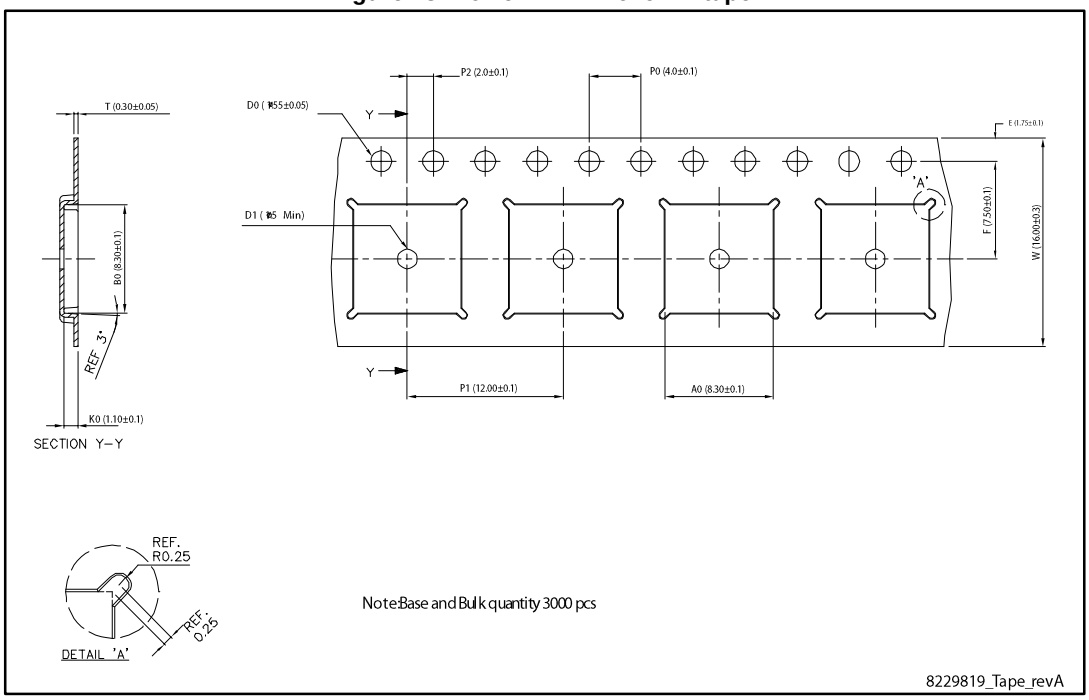


Figure 24: PowerFLAT™ 8x8 HV package orientation in carrier tape

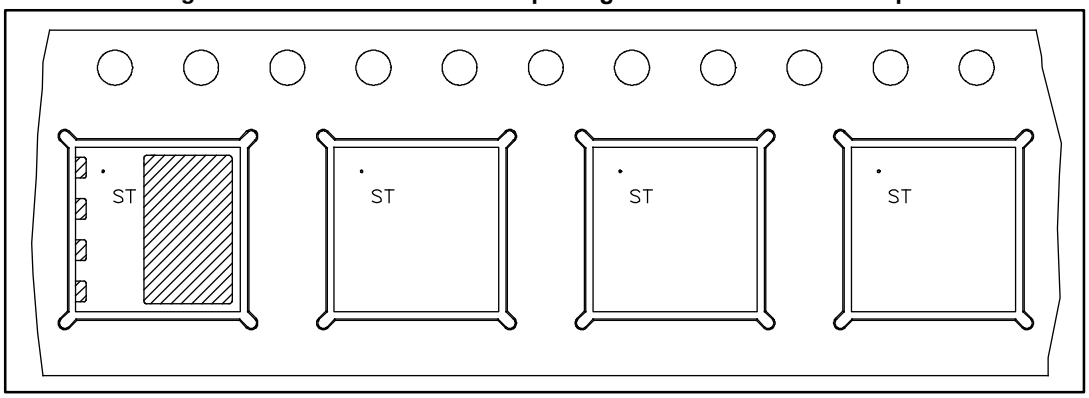
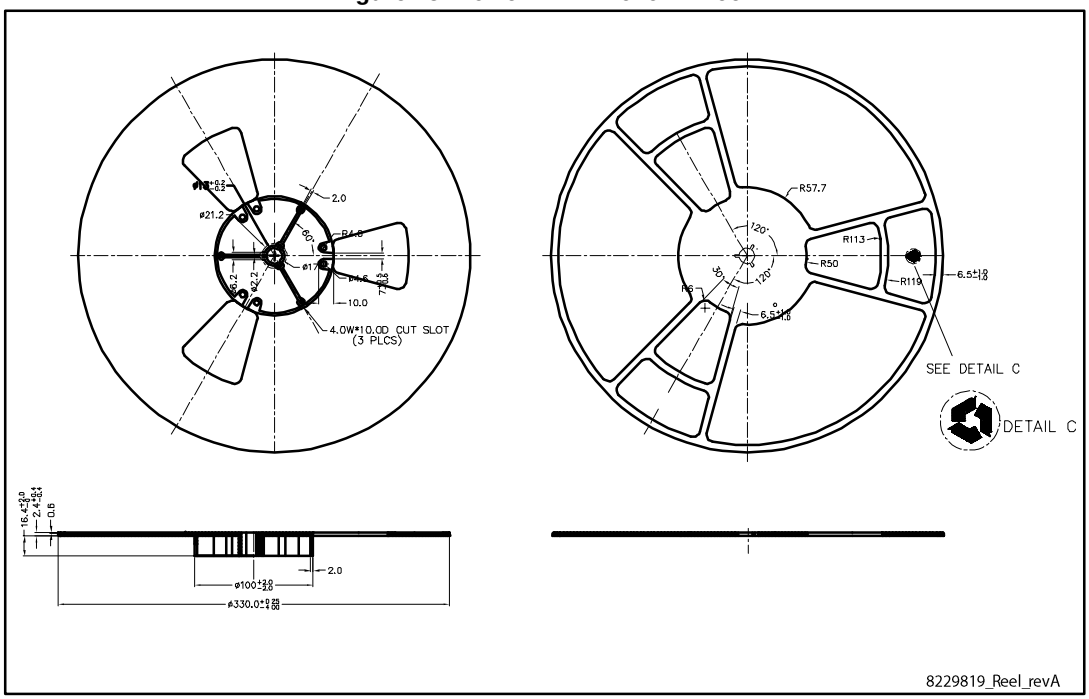


Figure 25: PowerFLAT™ 8x8 HV reel



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
17-Jan-2013	1	First release.
27-Aug-2015	2	Updated title, features, internal schematic and description on cover page. Document status promoted from preliminary to production data. Updated package information. Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved