

Using Configurable Active Delay Elements in CDCF5801 Feedback Loop

H. Jungert, S. Tambouris, K. Mustafa

Clock Drivers

ABSTRACT

This document describes a specific failure mode and a workaround when using the CDCF5801 to align two input clocks where the output clock, CLKOUT is being fed back to the phase-aligner of the CDCF5801 using a configurable active delay element (e.g., Microcontroller, ASIC, FPGA, DSP) as illustrated in figure 1. The observed operation of the failure mode is that the DLYCTRL input of the CDCF5801 locks with a 180 degree phase shift to the LEADLAG input. In the intended operational mode the DLYCTRL input and LEADLAG input are adjusted such that both inputs are aligned with 0 degree.

1 Active Delay Element in Feedback Path

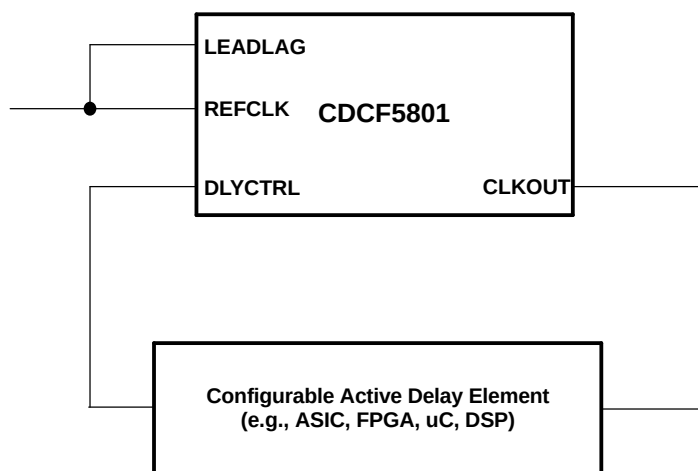


Figure 1. Active Delay Element in Feedback Path

2 Preconditions to Cause a 180 Degree False Lock Between REFCLK and CLKOUT

1. Feedback loop is not closed at power up. The configurable active delay element does not yet act as a buffer, i.e. there is no constant delay between CLKOUT signal and DLYCTRL signal.
2. The PLL internal to the CDCF5801 has achieved lock on REFCLK signal prior to closing the feedback loop

3. A precise 180 degree (± 2 degrees) phase shift exists between LEADLAG and DLYCTRL at closure of feedback loop.
4. The DLYCTRL input has not seen any CLK cycles before closing the feedback loop.

3 Workaround to Avoid 180 Degree False Lock

CDCF5801 PLL/Phase lock needs to be re-initialized as follows:

The external feedback loop must be stable (i.e. the active delay element has been completely initialized and acts as a constant delay buffer) at the time when PWRDNB is asserted high. Subsequently, the CDCF5801-internal PLL begins its lock-in behavior and DLYCTRL and LEADLAG input are aligned to a 0 degree phase relationship.

The following diagram outlines the recommended operation/ordering of events.

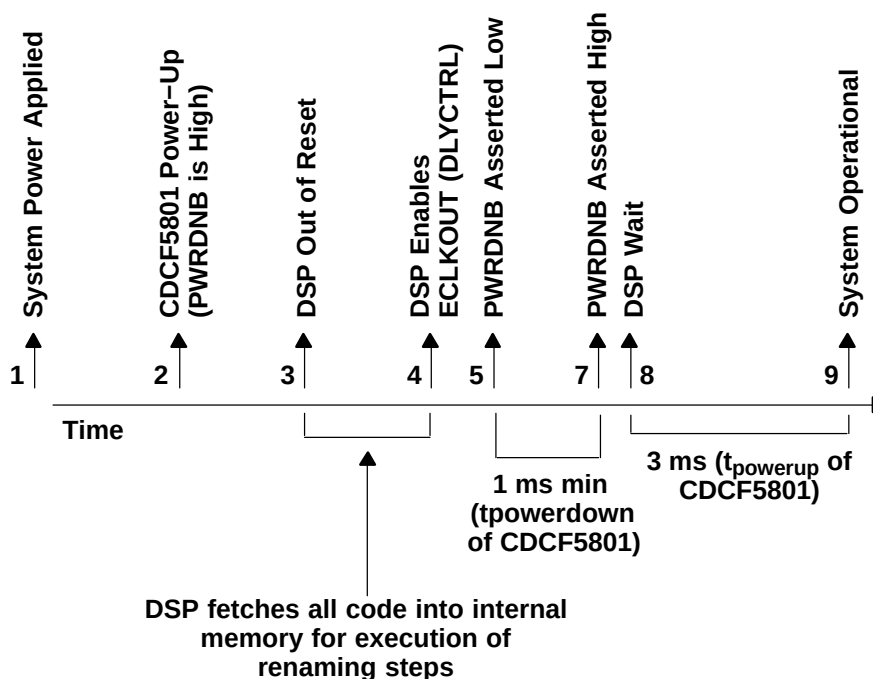


Figure 2. Workaround Timing in When a DSP is Used

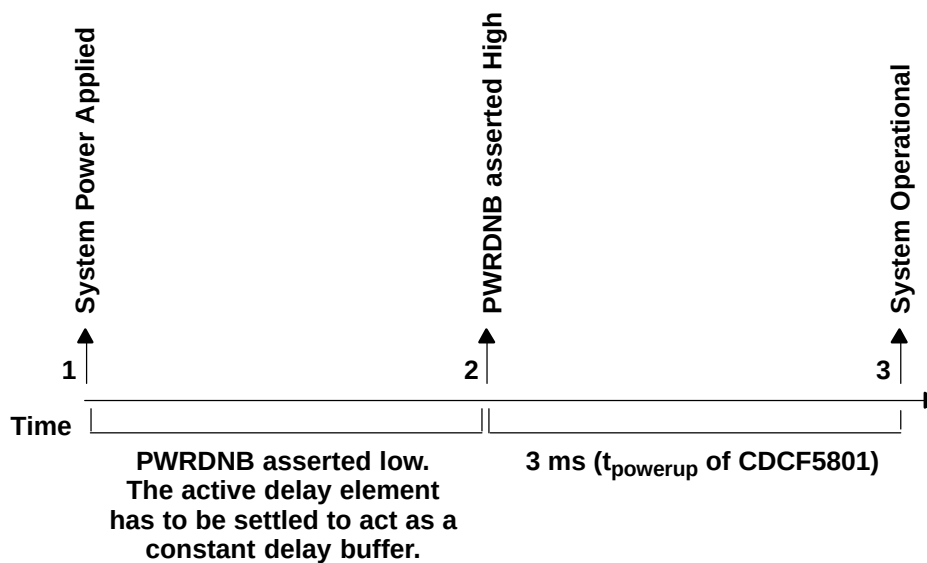


Figure 3. Workaround Timing for Gneral Use other than DSP

4 Reference

- How to Use the CDCF5801 for Phase Alignment/Adjustment Application Note ([SCAA070](#))

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