

MOSFET - Power, Single P-Channel, WDFN6 -20 V

Product Preview

NTLJS7D2P02P8Z

Features

- Small Footprint (4 mm²) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- These Devices are Pb-Free, Halogen-Free/BFR-Free and are RoHS Compliant

Applications

- Battery Management
- Protection
- Power Load Switch

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	-20	V
Gate-to-Source Voltage			V_{GS}	± 8.0	V
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	-13.1	A
		$T_A = 85^{\circ}\text{C}$		-9.5	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		$T_A = 25^{\circ}\text{C}$	P_D	2.40	W
Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	-7.9	A
		$T_A = 85^{\circ}\text{C}$		-5.7	
Power Dissipation $R_{\theta JA}$ (Notes 2, 3)		$T_A = 25^{\circ}\text{C}$	P_D	0.86	W
Pulsed Drain Current	$T_A = 25^{\circ}\text{C}$, $t_p = 10\ \mu\text{s}$		I_{DM}	52	A
Operating Junction and Storage Temperature Range			T_J , T_{stg}	-55 to +150	$^{\circ}\text{C}$
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	52	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	145	

1. Surface-mounted on FR4 board using 1 in² pad size, 2 oz. Cu pad.
2. Surface-mounted on FR4 board using minimum pad size, 2 oz. Cu pad.
3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro-mechanical application board design. $R_{\theta CA}$ is determined by the user's board design.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

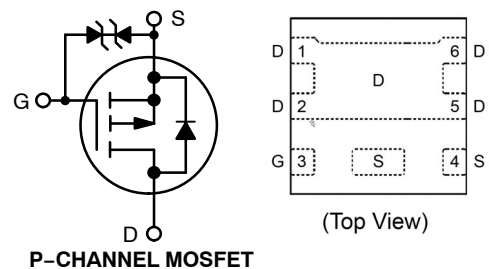
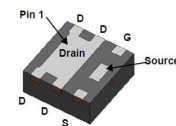


ON Semiconductor®

www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
-20 V	9 m Ω @ -4.5 V	-13.1 A
	11 m Ω @ -2.5 V	

ELECTRICAL CONNECTION



WDFN6 (2.05x2.05)
CASE 483AV

MARKING DIAGRAM



YW = Date Code
ZZ = Assembly Lot Code
A = Assembly Site Code
7D2 = Specific Device Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 4 of this data sheet.

NTLJS7D2P02P8Z

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
-----------	--------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 μA	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = -250 μA, ref to 25°C		14.4		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = -16 V	T _J = 25°C		-1	μA
			T _J = 125°C		-10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8.0 V			±10	μA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	-0.4		-1.5	V
Threshold Temperature Coefficient	V _{GS} /T _J	I _D = -250 μA, ref to 25°C		-3.3		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -10 A		7.1	9.0	mΩ
		V _{GS} = -2.5 V, I _D = -5 A		9.1	11	
Forward Transconductance	g _{FS}	V _{DS} = -5 V, I _D = -10 A		59		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = -10 V, f = 1.0 MHz		2790		pF
Output Capacitance	C _{oss}			412		
Reverse Transfer Capacitance	C _{rss}			369		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -10 A		26.7		nC
Threshold Gate Charge	Q _{G(TH)}			1.4		nC
Gate-to-Source Charge	Q _{GS}			3.7		
Gate-to-Drain Charge	Q _{GD}			6.7		

SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 5)

Turn-On Delay Time	t _{d(on)}	V _{GS} = -4.5 V, V _{DD} = -15 V, I _D = -10 A, R _G = 6 Ω		9.3		ns
Rise Time	t _r			25.1		
Turn-Off Delay Time	t _{d(off)}			224		
Fall Time	t _f			130		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = -10 A	T _J = 25°C		0.74	1.2	V
			T _J = 125°C		0.65		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = -100 A/μs, I _S = -10 A			20		ns
Reverse Recovery Charge	Q _{RR}				5.4		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

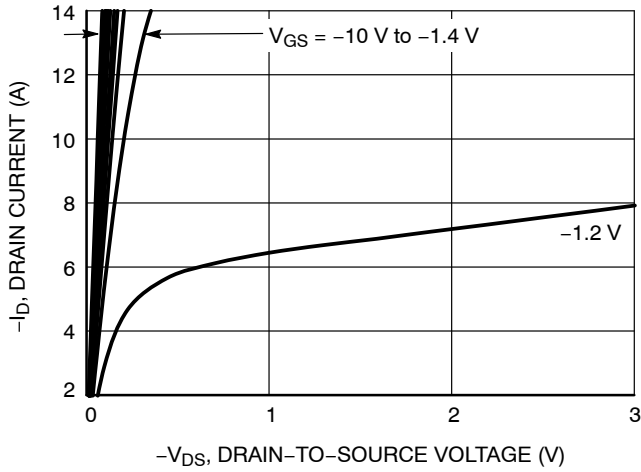


Figure 1. On-Region Characteristics

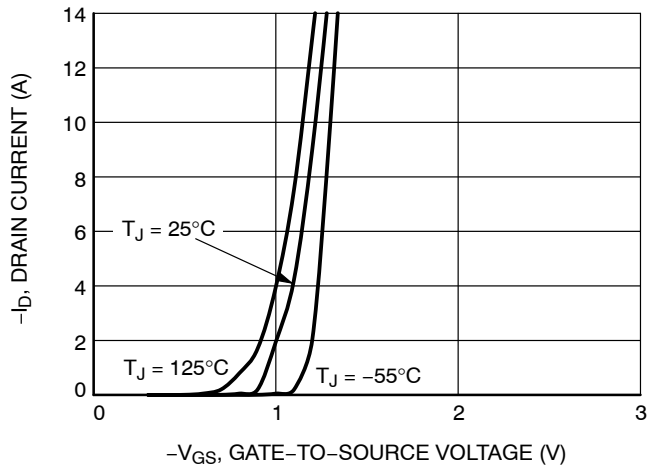


Figure 2. Transfer Characteristics

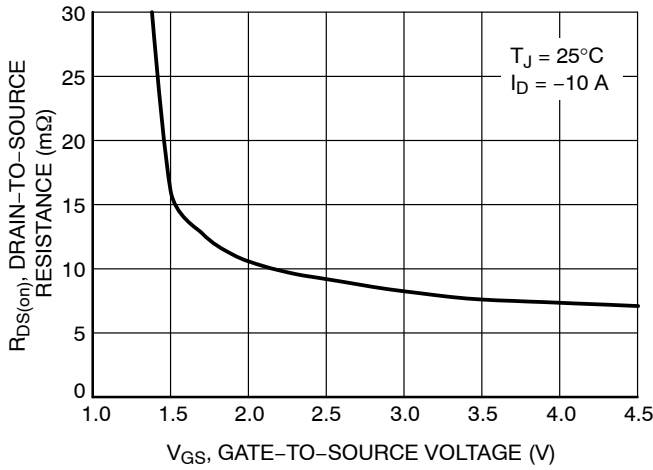


Figure 3. On-Resistance vs. Gate-to-Source Voltage (V)

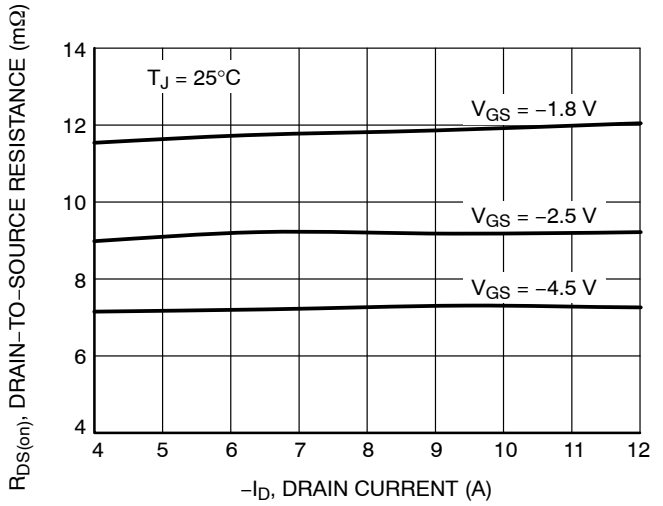


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

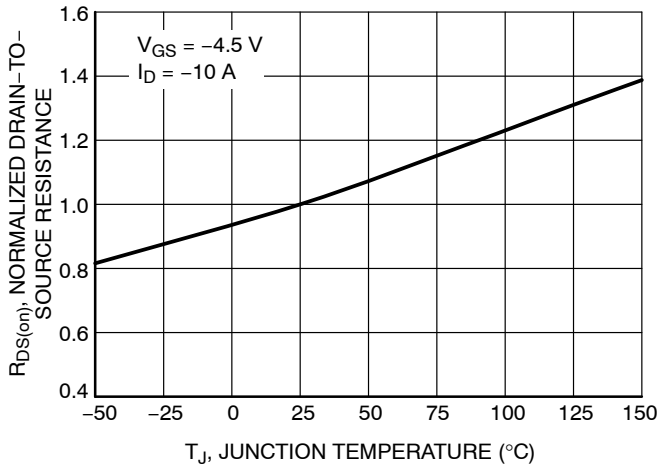


Figure 5. On-Resistance Variation with Temperature

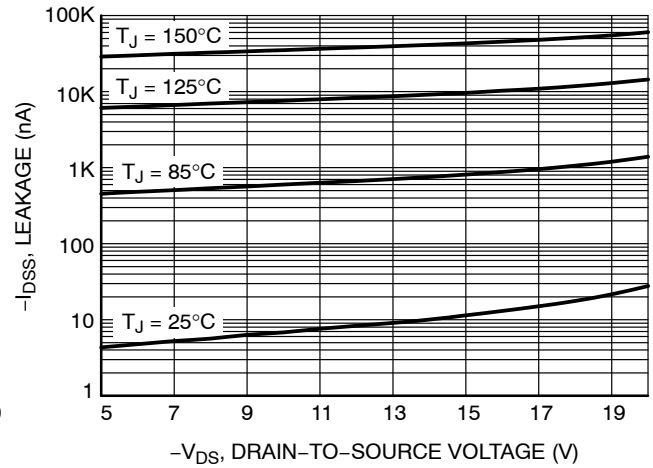


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

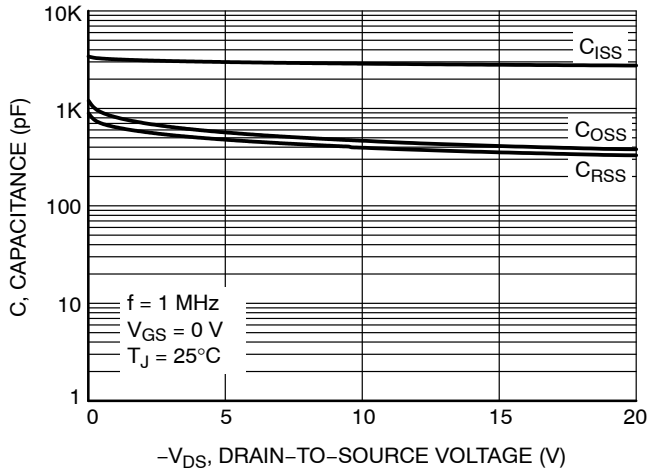


Figure 7. Capacitance Variation

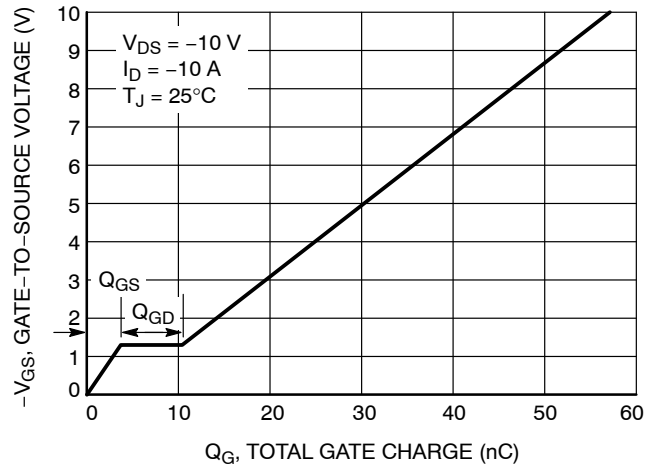


Figure 8. Gate-to-Source vs. Total Charge

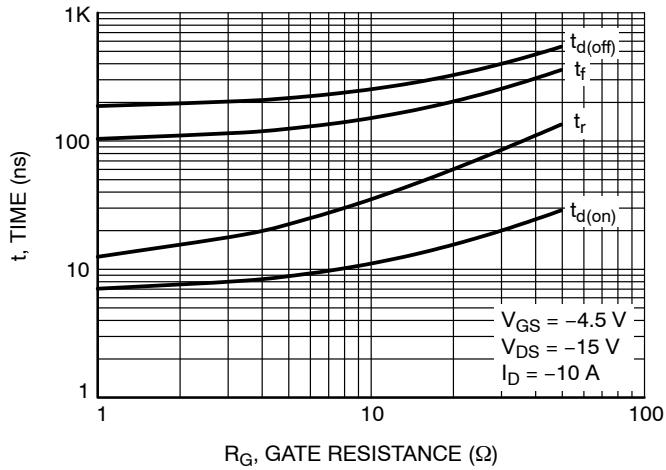


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

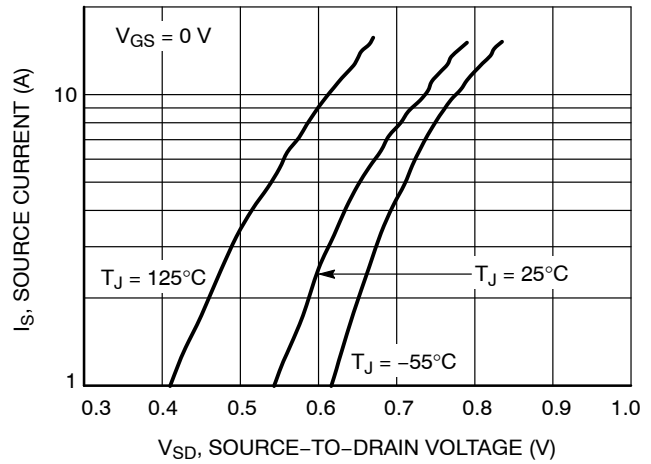


Figure 10. Diode Forward Voltage vs. Current

DEVICE ORDERING INFORMATION

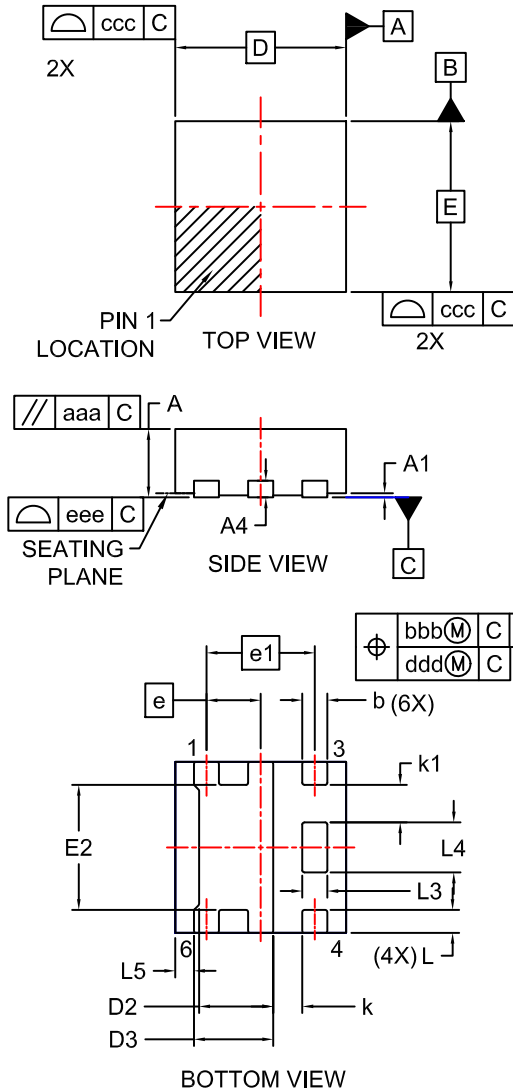
Device	Package	Shipping†
NTLJS7D2P02P8ZTAG	WDFN6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

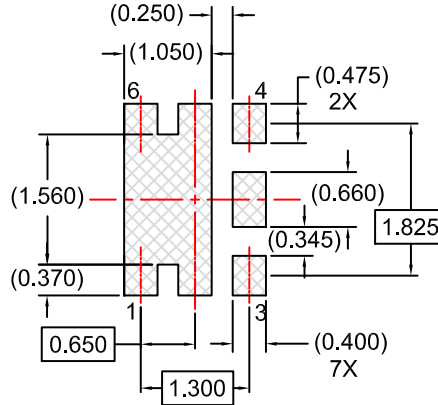
NTLJS7D2P02P8Z

PACKAGE DIMENSIONS

WDFN6 2.05X2.05, 0.65P
CASE 483AV
ISSUE A



LAND PATTERN RECOMMENDATION



NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.60	0.70	0.80
A1	0.00	-	0.05
A4	(0.20)		
b	0.25	0.30	0.35
D	1.95	2.05	2.15
D2	0.84	0.89	0.94
D3	(0.95)		
E	1.95	2.05	2.15
E2	1.45	1.50	1.55
e	0.65 BSC		
e1	1.30 BSC		
k	(0.35)		
k1	(0.45)		
L	0.18	0.28	0.38
L3	0.25	0.30	0.35
L4	0.55	0.60	0.65
L5	(0.23)		
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		
eee	0.05		

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative