16-Bit, 4-Channel, CCD/CMOS Sensor Analog Front-End with Timing Generator

Check for Samples: VSP5610, VSP5611, VSP5612

FEATURES

- **Four-Channel CCD/CMOS Signal: 2-Channel, 3-Channel, and 4-Channel Selectable**
- **Power Supply: 3.3 V Only, Typ (Built-in LDO, 3.3 V to 1.8 V)**
- **Maximum Conversion Rate:**
  - **VSP5610: 35 MSPS**
  - **VSP5611: 50 MSPS**
  - **VSP5612: 70 MSPS**
- **16-Bit Resolution**
- **CDS/SH Selectable**
- **Maximum Input Signal Range: 2.0 V**
- **Analog and Digital Hybrid Gain:**
  - **Analog Gain: 0.5 V/V to 3.5 V/V in 3/64-V/V Steps**
  - **Digital Gain: 1 V/V to 2 V/V in 1/256-V/V Steps**
- **Offset Correction DAC: ±250 mV, 8-Bit**
- **Standard LVDS/CMOS Selectable Output:**
  - **LVDS:**
    - **Data Channel: 2-Channel, 3-Channel**
    - **Clock Channel: 1-Channel**
    - **8-Bit/7-Bit Serializer Selectable**
  - **CMOS: 4 Bits × 4, 8 Bits × 2**
- **Timing Generator:**
  - **Fast Transfer Clock: Eight Signals**
  - **Slow Transfer Clock: Six Signals**
- **Timing Adjustment Resolution: t_{MCLK}/48**
- **Input Clamp/Input Reference Level Internal/External Selectable**
- **Reference DAC: 0.5 V, 1.1 V, 1.5 V, 2 V**
- **SPI™: Three-Wire Serial**
- **GPIO: Four-Port**

APPLICATIONS

- **Copiers**
- **Facsimile Machines**
- **Scanners**

DESCRIPTION

The VSP5610/11/12 are high-speed, high-performance, 16-bit analog-to-digital-converters (ADCs) that have four independent sampling circuit channels for multi-output charge-coupled device (CCD) and complementary metal oxide semiconductor (CMOS) line sensors. Pixel data from the sensor are sampled by the sample/hold (SH) or correlated double sampler (CDS) circuit, and are then converted to digital data by an ADC. Data output is selectable in low-voltage differential signaling (LVDS) or CMOS modes.

The VSP5610/11/12 include a programmable gain to support the pixel level inflection caused by luminance. The integrated digital-to-analog-converter (DAC) can be used to adjust the offset level for the analog input signal. Furthermore, the timing generator (TG) is integrated in these devices for the control of sensor operation.

The VSP5610/11/12 use 1.65 V to 1.95 V for the core voltage and 3.0 V to 3.6 V for I/Os. The core voltage is supplied by a built-in low-dropout regulator (LDO).

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
VSP5610	QFN-56	RSH	0°C to +85°C	VSP5610	VSP5610RSHR	Tape and Reel
VSP5611	QFN-56	RSH	0°C to +85°C	VSP5611	VSP5611RSHR	Tape and Reel
VSP5612	QFN-56	RSH	0°C to +85°C	VSP5612	VSP5612RSHR	Tape and Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	VSP5610, VSP5611, VSP5612	UNIT
Supply voltage: VDD, DVDD_IO, LVDD	4.0	V
Supply voltage difference: VDD, DVDD_IO, LVDD	±0.6	V
Ground voltage difference: VSS, DVSS, LVSS	±0.1	V
Digital voltage input	–0.3 to DVDD_IO + 0.3	V
Analog voltage input	–0.3 to VDD + 0.3	V
Digital input current	±10	mA
Analog input current	±10	mA
Ambient temperature under bias	–40 to +125	°C
Storage temperature	–55 to +150	°C
Junction temperature	+150	°C
Package temperature (IR reflow, peak)	+260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
LDO and analog I/O power-supply voltage	VDD	3.0	3.3	3.6	V
Digital power-supply voltage	DVDD_IO	3.0	3.3	3.6	V
LVDS/CMOS power-supply voltage	LVDD	3.0	3.3	3.6	V
Supply voltage difference	VDD, DVDD_IO, LVDD	–0.3		0.3	V
Digital input logic family			Low-voltage CMOS		
Master clock frequency (MCLK)	VSP5610	1		11.66	MHz
	VSP5611	1		16.66	MHz
	VSP5612	1		23.33	MHz
Serial I/O clock frequency (SCLK)				10	MHz
Operating free-air temperature		0		+85	°C

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ELECTRICAL CHARACTERISTICS: VSP5610

All specifications at T_A = +25°C, supply voltage = +3.3 V, conversion rate = 8.75 MHz, and four-channel mode, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP5610 MIN	VSP5610 TYP	VSP5610 MAX	UNIT
ANALOG INPUT						
Allowable input voltage			0		VDD	V
Full-scale range		Gain = 1 V/V		1		V_{PP}
Input capacitor				5		pF
DIGITAL INPUT						
Positive-going threshold	V_{T+}				DVDD_IO × 0.7	V
Negative-going threshold	V_{T-}		DVDD_IO × 0.3			V
Hysteresis ($V_{T+} – V_{T-}$)	ΔV_T		DVDD_IO × 0.13			V
Input current	I_{IN}				±1	µA
Input capacitor				5		pF
DIGITAL OUTPUT						
High-level output voltage	V_{OH}	I_{OH} = –2 mA	DVDD_IO – 0.45			V
		I_{OH} = –4 mA	DVDD_IO – 0.50			V
		I_{OH} = –8 mA	DVDD_IO – 0.50			V
Low-level output voltage	V_{OL}	I_{OL} = 2 mA			0.35	V
		I_{OL} = 4 mA			0.50	V
		I_{OL} = 8 mA			0.65	V
TG output timing skew		XP1, XP2, XP3, XP4	–1		1	ns
		Other signals	–2		2	ns
CMOS data output bit rate					80	MHz
LVDS DRIVER (TA, TB, TC, TCLK)						
Differential steady-state output voltage adjustment range	$\lvert V_{OD}\rvert$	R_L = 100 Ω	300	350	400	mV
Differential steady-state output adjustment step	$\lvert V_{OD}\rvert$			3		Steps
Differential steady-state output voltage tolerance	$\lvert V_{OD}\rvert$		–30		30	%
Change in the steady-state differential output voltage magnitude between opposite binary states	$\Delta\lvert V_{OD}\rvert$				35	mV
Steady-state common-mode output voltage	$V_{OC(SS)}$	R_L = 100 Ω	1.125		1.375	V
Peak-to-peak common-mode output voltage	$V_{OC(PP)}$			80	150	mV
Short-circuit output current	I_{OS}	V_O = 0 V (V_O = TA, TB, TC, TCLK)		–6	±24	mA
Hi-Z output current	I_{OZ}	V_O = 0 V to LVDD (V_O = TA, TB, TC, TCLK)			±10	µA
Transition time, differential output voltage	t_{LR}/t_{LF}			0.75	1.5	ns
TCLK clock rate			8		35	MHz
LVDS RECEIVER (RCLK)						
Positive-going differential input threshold voltage	V_{IT+}				100	mV
Negative-going differential input threshold voltage	V_{IT-}		–100			mV
RCLK clock rate			1		11.66	MHz

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ELECTRICAL CHARACTERISTICS: VSP5610 (continued)

All specifications at T_A = +25°C, supply voltage = +3.3 V, conversion rate = 8.75 MHz, and four-channel mode, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP5610			UNIT
			MIN	TYP	MAX	
POWER SUPPLY						
LDO and analog I/O supply voltage	VDD		3.0	3.3	3.6	V
Digital I/O supply voltage	DVDD_IO		3.0	3.3	3.6	V
LVDS/CMOS supply voltage	LVDD		3.0	3.3	3.6	V
LDO and analog I/O current	VDD			74.9		mA
Digital I/O current	DVDD_IO	Load = 10 pF		3.8		mA
CMOS current	LVDD			10		mA
LVDS current	LVDD	Three-pair data, one-pair clock		24		mA
Power consumption		LVDS, three-pair		339		mW
		CMOS output		317		mW
		Standby mode (MCLK = 0 MHz)		15		mW
TEMPERATURE RANGE						
Operation temperature	T_A		0		+85	°C
Thermal resistor (junction-to-air)	θ_{JA}	PCB (50 mm × 50 mm, four-layer), 0 lfm airflow		29		°C/W
Thermal resistor (junction-to-case)	θ_{JC}			24		°C/W
DLL, PLL						
MCLK input frequency	f_{MCLK}		1		11.66	MHz
MCLK modulated frequency		MCLK > 5 MHz			35	kHz
MCLK modulated amplitude			–3.5		0	%
DLL tap number				48		Taps
Maximum DLL and PLL lock-up time		MCLK = 1 MHz		10		ms
TRANSFER CHARACTERISTICS						
Channels			2		4	Channels
Resolution				16		Bits
Conversion rate		LVDS, two- and three-channel mode	1		11.66	MHz/Ch
		LVDS, four-channel mode	1		8.75	MHz/Ch
		CMOS 8-bit × 2, two-channel mode	1		11.66	MHz/Ch
		CMOS 4-bit × 4, two-channel mode	1		10	MHz/Ch
		CMOS 8-bit × 2, three-channel mode	1		11.66	MHz/Ch
		CMOS 4-bit × 4, three-channel mode	1		6.7	MHz/Ch
		CMOS 8-bit × 2, four-channel mode	1		8.75	MHz/Ch
		CMOS 4-bit × 4, four-channel mode	1		5	MHz/Ch
Maximum differential nonlinearity		Gain = 1 V/V, 12-bit		±0.5		LSB
Maximum integral nonlinearity		Gain = 1 V/V, 12-bit		±2		LSB
No missing codes				Specified		
Signal-to-noise ratio	SNR	Gain = 1 V/V	72(1)	76		dB
Analog channel crosstalk		Gain = 1 V/V, 12-bit, full-scale step		±3		LSB
Total absolute gain error			–10		10	%

(1) Specified by design.

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ELECTRICAL CHARACTERISTICS: VSP5610 (continued)

All specifications at T_A = +25°C, supply voltage = +3.3 V, conversion rate = 8.75 MHz, and four-channel mode, unless otherwise noted.

PARAMETER	TEST CONDITIONS	VSP5610 MIN	VSP5610 TYP	VSP5610 MAX	UNIT
ANALOG PROGRAMMABLE GAIN (APG)					
Gain range APG_x		0.5		3.5	V/V
Gain step			63		Steps
Gain relative error	Basis gain = 1 V/V	–10		10	%
Gain monotonicity	Only APG_x		Specified		
DIGITAL PROGRAMMABLE GAIN (DPG)					
Gain range DPG_x		1.0		2.0	V/V
Gain step			255		Steps
Gain monotonicity	Only DPG_x		Specified		
AIN REFERENCE LEVEL (REF_AIN)					
Internal DAC output V_{RINT}	Setting code = 2		0.5		V
	Setting code = 3		1.1		V
	Setting code = 0 (default)		1.5		V
	Setting code = 1		2.0		V
Internal DAC output tolerance V_{RINT}		–10		10	%
Internal DAC output temperature drift V_{RINT}	T_A = 0°C to +85°C(2)	–2		2	%
External reference range V_{REXT}		0.5		VDD – 0.9	V
INPUT CLAMP					
Clamp level V_{CLP}	Internal reference level clamp		V_{RINT}		V
	External reference level clamp		V_{REXT}		V
	Fixed level clamp		2.2		V
Clamp-on resistance R_{CLP}			500		Ω
OFFSET DAC					
Resolution			8		Bits
Output range			±250		mV
Setting tolerance		–10		10	%
Temperature drift	T_A = 0°C to +85°C(2)	–2		2	%

(2) Specified by design.

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ELECTRICAL CHARACTERISTICS: VSP5611

All specifications at T_A = +25°C, supply voltage = +3.3 V, conversion rate = 12.5 MHz, and four-channel mode, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP5611 MIN	VSP5611 TYP	VSP5611 MAX	UNIT
ANALOG INPUT						
Allowable input voltage			0		VDD	V
Full-scale range		Gain = 1 V/V		1		V_{PP}
Input capacitor				5		pF
DIGITAL INPUT						
Positive-going threshold	V_{T+}				DVDD_IO × 0.7	V
Negative-going threshold	V_{T-}		DVDD_IO × 0.3			V
Hysteresis ($V_{T+} – V_{T-}$)	ΔV_T		DVDD_IO × 0.13			V
Input current	I_{IN}				±1	µA
Input capacitor				5		pF
DIGITAL OUTPUT						
High-level output voltage	V_{OH}	I_{OH} = –2 mA	DVDD_IO – 0.45			V
		I_{OH} = –4 mA	DVDD_IO – 0.50			V
		I_{OH} = –8 mA	DVDD_IO – 0.50			V
Low-level output voltage	V_{OL}	I_{OL} = 2 mA			0.35	V
		I_{OL} = 4 mA			0.50	V
		I_{OL} = 8 mA			0.65	V
TG output timing skew		XP1, XP2, XP3, XP4	–1		1	ns
		Other signals	–2		2	ns
CMOS data output bit rate					80	MHz
LVDS DRIVER (TA, TB, TC, TCLK)						
Differential steady-state output voltage adjustment range	$\lvert V_{OD} \rvert$	R_L = 100 Ω	300	350	400	mV
Differential steady-state output adjustment step	$\lvert V_{OD} \rvert$			3		Steps
Differential steady-state output voltage tolerance	$\lvert V_{OD} \rvert$		–30		30	%
Change in the steady-state differential output voltage magnitude between opposite binary states	$\Delta\lvert V_{OD} \rvert$				35	mV
Steady-state common-mode output voltage	$V_{OC(SS)}$	R_L = 100 Ω	1.125		1.375	V
Peak-to-peak common-mode output voltage	$V_{OC(PP)}$			80	150	mV
Short-circuit output current	I_{OS}	V_O = 0 V (V_O = TA, TB, TC, TCLK)		–6	±24	mA
Hi-Z output current	I_{OZ}	V_O = 0 V to LVDD (V_O = TA, TB, TC, TCLK)			±10	µA
Transition time, differential output voltage	t_{LR}/t_{LF}			0.75	1.5	ns
TCLK clock rate			8		50	MHz
LVDS RECEIVER (RCLK)						
Positive-going differential input threshold voltage	V_{IT+}				100	mV
Negative-going differential input threshold voltage	V_{IT-}		–100			mV
RCLK clock rate			1		16.66	MHz

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ELECTRICAL CHARACTERISTICS: VSP5611 (continued)

All specifications at T_A = +25°C, supply voltage = +3.3 V, conversion rate = 12.5 MHz, and four-channel mode, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP5611			UNIT
			MIN	TYP	MAX	
POWER SUPPLY						
LDO and analog I/O supply voltage	VDD		3.0	3.3	3.6	V
Digital I/O supply voltage	DVDD_IO		3.0	3.3	3.6	V
LVDS/CMOS supply voltage	LVDD		3.0	3.3	3.6	V
LDO and analog I/O current	VDD			99.6		mA
Digital I/O current	DVDD_IO	Load = 10 pF		5.4		mA
CMOS current	LVDD			10		mA
LVDS current	LVDD	Three-pair data, one-pair clock		24		mA
Power consumption		LVDS, three-pair		426		mW
		CMOS output		398		mW
		Standby mode (MCLK = 0 MHz)		15		mW
TEMPERATURE RANGE						
Operation temperature	T_A		0		+85	°C
Thermal resistor (junction-to-air)	θ_{JA}	PCB (50 mm × 50 mm, four-layer), 0 lfm airflow		29		°C/W
Thermal resistor (junction-to-case)	θ_{JC}			24		°C/W
DLL, PLL						
MCLK input frequency	f_{MCLK}		1		16.66	MHz
MCLK modulated frequency		MCLK > 5 MHz			35	kHz
MCLK modulated amplitude			–3.5		0	%
DLL tap number				48		Taps
Maximum DLL and PLL lock-up time		MCLK = 1 MHz		10		ms
TRANSFER CHARACTERISTICS						
Channel			2		4	Channels
Resolution				16		Bits
Conversion rate		LVDS, two- and three-channel mode	1		16.66	MHz/Ch
		LVDS, four-channel mode	1		12.5	MHz/Ch
		CMOS 8-bit × 2, two-channel mode	1		16.66	MHz/Ch
		CMOS 4-bit × 4, two-channel mode	1		10	MHz/Ch
		CMOS 8-bit × 2, three-channel mode	1		13.3	MHz/Ch
		CMOS 4-bit × 4, three-channel mode	1		6.7	MHz/Ch
		CMOS 8-bit × 2, four-channel mode	1		10	MHz/Ch
		CMOS 4-bit × 4, four-channel mode	1		5	MHz/Ch
Maximum differential nonlinearity		Gain = 1 V/V, 12-bit		±0.5		LSB
Maximum integral nonlinearity		Gain = 1 V/V, 12-bit		±2		LSB
No missing codes				Specified		
Signal-to-noise ratio	SNR	Gain = 1 V/V	72(1)	76		dB
Analog channel crosstalk		Gain = 1 V/V, 12-bit, full-scale step		±6.5		LSB
Total absolute gain error			–10		10	%

(1) Specified by design.

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ELECTRICAL CHARACTERISTICS: VSP5611 (continued)

All specifications at T_A = +25°C, supply voltage = +3.3 V, conversion rate = 12.5 MHz, and four-channel mode, unless otherwise noted.

PARAMETER	TEST CONDITIONS	VSP5611 MIN	VSP5611 TYP	VSP5611 MAX	UNIT
ANALOG PROGRAMMABLE GAIN (APG)					
Gain range APG_x		0.5		3.5	V/V
Gain step			63		Steps
Gain relative error	Basis gain = 1 V/V	–10		10	%
Gain monotonicity	Only APG_x		Specified		
DIGITAL PROGRAMMABLE GAIN (DPG)					
Gain range DPG_x		1.0		2.0	V/V
Gain step			255		Steps
Gain monotonicity	Only DPG_x		Specified		
AIN REFERENCE LEVEL (REF_AIN)					
Internal DAC output V_{RINT}	Setting code = 2		0.5		V
	Setting code = 3		1.1		V
	Setting code = 0 (default)		1.5		V
	Setting code = 1		2.0		V
Internal DAC output tolerance V_{RINT}		–10		10	%
Internal DAC output temperature drift V_{RINT}	T_A = 0°C to +85°C(2)	–2		2	%
External reference range V_{REXT}		0.5		VDD – 0.9	V
INPUT CLAMP					
Clamp level V_{CLP}	Internal reference level clamp		V_{RINT}		V
	External reference level clamp		V_{REXT}		V
	Fixed level clamp		2.2		V
Clamp-on resistance R_{CLP}			500		Ω
OFFSET DAC					
Resolution			8		Bits
Output range			±250		mV
Setting tolerance		–10		10	%
Temperature drift	T_A = 0°C to +85°C(2)	–2		2	%

(2) Specified by design.

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ELECTRICAL CHARACTERISTICS: VSP5612

All specifications at T_A = +25°C, supply voltage = +3.3 V, conversion rate = 17.5 MHz, and four-channel mode, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP5612 MIN	VSP5612 TYP	VSP5612 MAX	UNIT
ANALOG INPUT						
Allowable input voltage			0		VDD	V
Full-scale range		Gain = 1 V/V		1		V_{PP}
Input capacitor				5		pF
DIGITAL INPUT						
Positive-going threshold	V_{T+}				DVDD_IO × 0.7	V
Negative-going threshold	$V_{T–}$		DVDD_IO × 0.3			V
Hysteresis ($V_{T+} – V_{T–}$)	ΔV_T		DVDD_IO × 0.13			V
Input current	I_{IN}				±1	µA
Input capacitor				5		pF
DIGITAL OUTPUT						
High-level output voltage	V_{OH}	I_{OH} = –2 mA	DVDD_IO – 0.45			V
		I_{OH} = –4 mA	DVDD_IO – 0.50			V
		I_{OH} = –8 mA	DVDD_IO – 0.50			V
Low-level output voltage	V_{OL}	I_{OL} = 2 mA			0.35	V
		I_{OL} = 4 mA			0.50	V
		I_{OL} = 8 mA			0.65	V
TG output timing skew		XP1, XP2, XP3, XP4	–1		1	ns
		Other signals	–2		2	ns
CMOS data output bit rate					80	MHz
LVDS DRIVER (TA, TB, TC, TCLK)						
Differential steady-state output voltage adjustment range	$\lvert V_{OD}\rvert$	R_L = 100 Ω	300	350	400	mV
Differential steady-state output adjustment step	$\lvert V_{OD}\rvert$			3		Steps
Differential steady-state output voltage tolerance	$\lvert V_{OD}\rvert$		–30		30	%
Change in the steady-state differential output voltage magnitude between opposite binary states	$\Delta\lvert V_{OD}\rvert$				35	mV
Steady-state common-mode output voltage	$V_{OC(SS)}$	R_L = 100 Ω	1.125		1.375	V
Peak-to-peak common-mode output voltage	$V_{OC(PP)}$			80	150	mV
Short-circuit output current	I_{OS}	V_O = 0 V (V_O = TA, TB, TC, TCLK)		–6	±24	mA
Hi-Z output current	I_{OZ}	V_O = 0 V to LVDD (V_O = TA, TB, TC, TCLK)			±10	µA
Transition time, differential output voltage	t_{LR}/t_{LF}			0.75	1.5	ns
TCLK clock rate			8		70	MHz
LVDS RECEIVER (RCLK)						
Positive-going differential input threshold voltage	V_{IT+}				100	mV
Negative-going differential input threshold voltage	$V_{IT–}$		–100			mV
RCLK clock rate			1		23.33	MHz

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ELECTRICAL CHARACTERISTICS: VSP5612 (continued)

All specifications at T_A = +25°C, supply voltage = +3.3 V, conversion rate = 17.5 MHz, and four-channel mode, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP5612 MIN	VSP5612 TYP	VSP5612 MAX	UNIT
POWER SUPPLY						
LDO and analog I/O supply voltage	VDD		3.0	3.3	3.6	V
Digital I/O supply voltage	DVDD_IO		3.0	3.3	3.6	V
LVDS/CMOS supply voltage	LVDD		3.0	3.3	3.6	V
LDO and analog I/O current	VDD			133		mA
Digital I/O current	DVDD_IO	Load = 10 pF		7.5		mA
CMOS current	LVDD			10		mA
LVDS current	LVDD	Three-pair data, one-pair clock		24		mA
Power consumption		LVDS, three-pair		542		mW
		CMOS output		507		mW
		Standby mode (MCLK = 0 MHz)		15		mW
TEMPERATURE RANGE						
Operation temperature	T_A		0		+85	°C
Thermal resistor (junction-to-air)	θ_{JA}	PCB (50 mm × 50 mm, four-layer), 0 lfm airflow		29		°C/W
Thermal resistor (junction-to-case)	θ_{JC}			24		°C/W
DLL, PLL						
MCLK input frequency	f_{MCLK}		1		23.33	MHz
MCLK modulated frequency		MCLK > 5 MHz			35	kHz
MCLK modulated amplitude			–3.5		0	%
DLL tap number				48		Taps
Maximum DLL and PLL lock-up time		MCLK = 1 MHz		10		ms
TRANSFER CHARACTERISTICS						
Channel			2		4	Channels
Resolution				16		Bits
Conversion rate		LVDS, two- and three-channel mode	1		23.33	MHz/Ch
		LVDS, four-channel mode	1		17.5	MHz/Ch
		CMOS 8-bit × 2, two-channel mode	1		20	MHz/Ch
		CMOS 4-bit × 4, two-channel mode	1		10	MHz/Ch
		CMOS 8-bit × 2, three-channel mode	1		13.3	MHz/Ch
		CMOS 4-bit × 4, three-channel mode	1		6.7	MHz/Ch
		CMOS 8-bit × 2, four-channel mode	1		10	MHz/Ch
		CMOS 4-bit × 4, four-channel mode	1		5	MHz/Ch
Maximum differential nonlinearity		Gain = 1 V/V, 12-bit		±0.5		LSB
Maximum integral nonlinearity		Gain = 1 V/V, 12-bit		±2		LSB
No missing codes				Specified		
Signal-to-noise ratio	SNR	Gain = 1 V/V	72(1)	75		dB
Analog channel crosstalk		Gain = 1 V/V, 12-bit, full-scale step		±15		LSB
Total absolute gain error			–10		10	%

(1) Specified by design.

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ELECTRICAL CHARACTERISTICS: VSP5612 (continued)

All specifications at T_A = +25°C, supply voltage = +3.3 V, conversion rate = 17.5 MHz, and four-channel mode, unless otherwise noted.

PARAMETER	TEST CONDITIONS	VSP5612 MIN	VSP5612 TYP	VSP5612 MAX	UNIT
ANALOG PROGRAMMABLE GAIN (APG)					
Gain range APG_x		0.5		3.5	V/V
Gain step			63		Steps
Gain relative error	Basis gain = 1 V/V	–10		10	%
Gain monotonicity	Only APG_x		Specified		
DIGITAL PROGRAMMABLE GAIN (DPG)					
Gain range DPG_x		1.0		2.0	V/V
Gain step			255		Steps
Gain monotonicity	Only DPG_x		Specified		
AIN REFERENCE LEVEL (REF_AIN)					
Internal DAC output V_{RINT}	Setting code = 2		0.5		V
	Setting code = 3		1.1		V
	Setting code = 0 (default)		1.5		V
	Setting code = 1		2.0		V
Internal DAC output tolerance V_{RINT}		–10		10	%
Internal DAC output temperature drift V_{RINT}	T_A = 0°C to +85°C(2)	–2		2	%
External reference range V_{REXT}		0.5		VDD – 0.9	V
INPUT CLAMP					
Clamp level V_{CLP}	Internal reference level clamp		V_{RINT}		V
	External reference level clamp		V_{REXT}		V
	Fixed level clamp		2.2		V
Clamp-on resistance R_{CLP}			500		Ω
OFFSET DAC					
Resolution			8		Bits
Output range			±250		mV
Setting tolerance		–10		10	%
Temperature drift	T_A = 0°C to +85°C(2)	–2		2	%

(2) Specified by design.

THERMAL INFORMATION

THERMAL METRIC(1)		VSP561xRSH RSH 56 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	25.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	13.2	
θ_{JB}	Junction-to-board thermal resistance	3.5	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	3.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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PARAMETERIC MEASUREMENT INFORMATION

Analog Input Specification (AIN1, AIN2, AIN3, AIN4)

The analog input specification has two signal inputs: negative and positive. These inputs are shown in Figure 1a and Figure 1b, respectively.

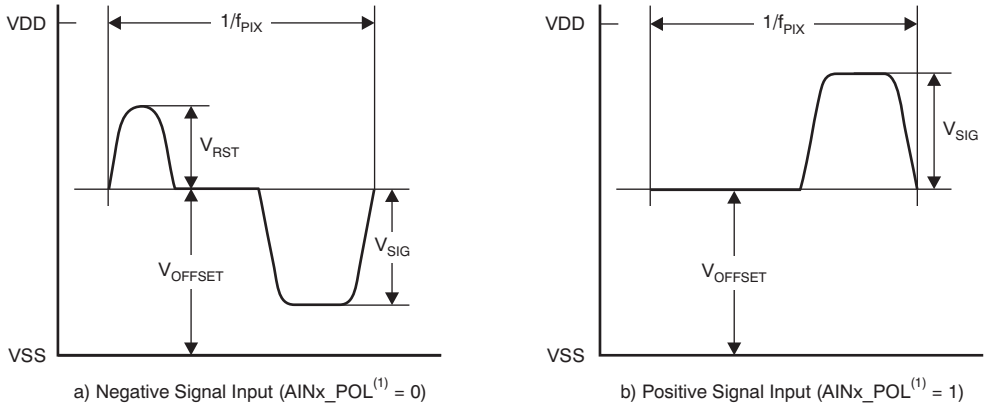


Figure 1. Analog Input Definition

Table 1. Timing Characteristics for Figure 1

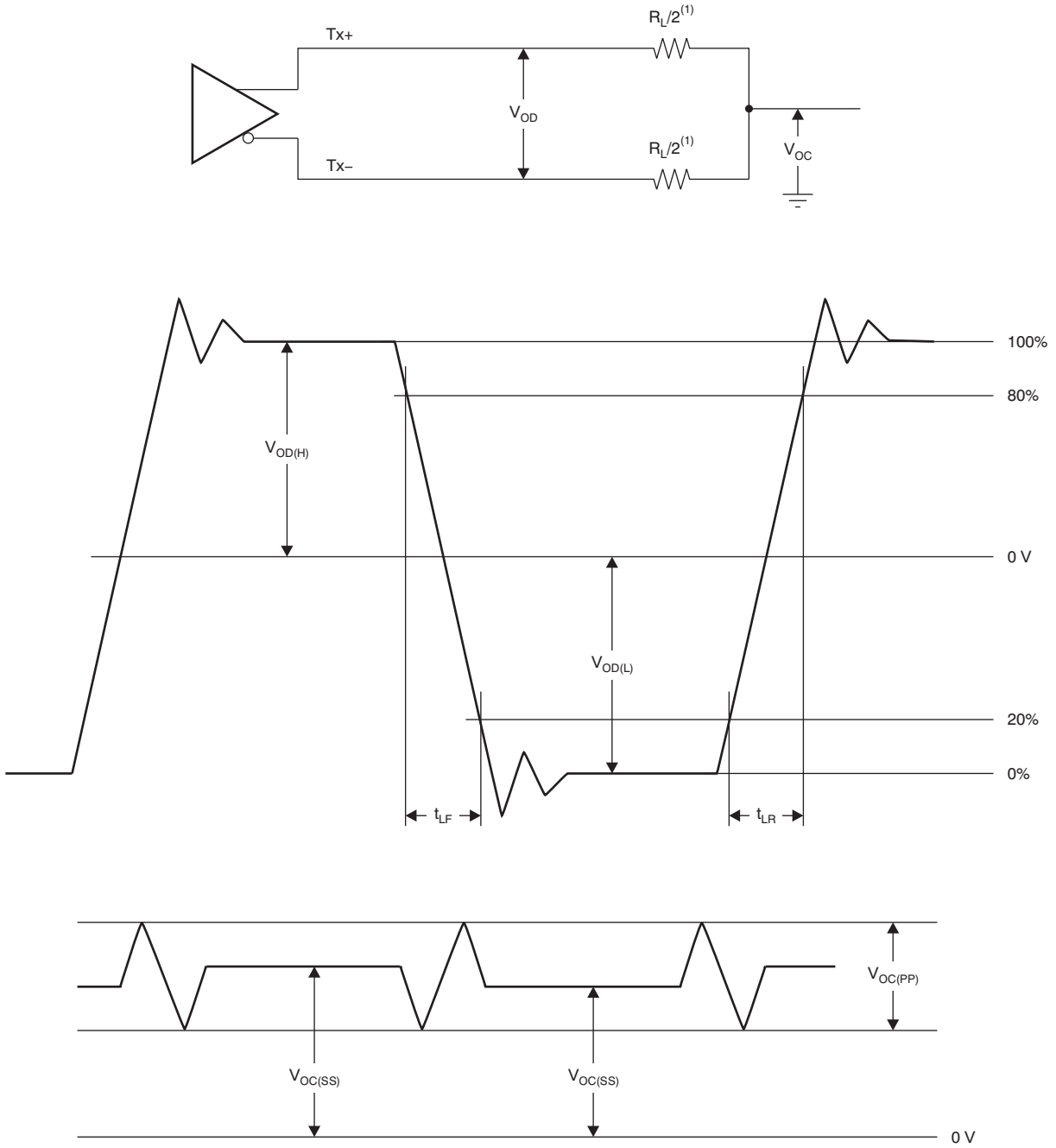
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input pixel rate	f_{PIX}	VSP5610	1		11.66	MHz/Ch
		VSP5611	1		16.66	MHz/Ch
		VSP5612	1		23.33	MHz/Ch
Signal range	V_{SIG}	Negative (AINx_POL(1) = 0)			V_{OFFSET}	V
		Positive (AINx_POL(1) = 1)			VDD – V_{OFFSET}	V
Maximum full-scale range	V_{SIG}	Gain = 0.5 V/V	1.8	2	2.2	V
Reset field through noise range	V_{RST}		$-V_{OFFSET}$		VDD – V_{OFFSET}	V
Offset level	V_{OFFSET}	Fixed level clamp mode (REF_SEL = 0)		2.2		V
		Internal reference level clamp mode (REF_SEL = 1)		V_{RINT}		V
		External reference level clamp mode (REF_SEL = 2)		V_{REXT}		V

(1) AINx_POL = Analog input polarity setting register (x = 1, 2, 3, and 4).

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LVDS Output Voltage Specification

The test load and voltage definition for the LVDS outputs are shown in Figure 2.

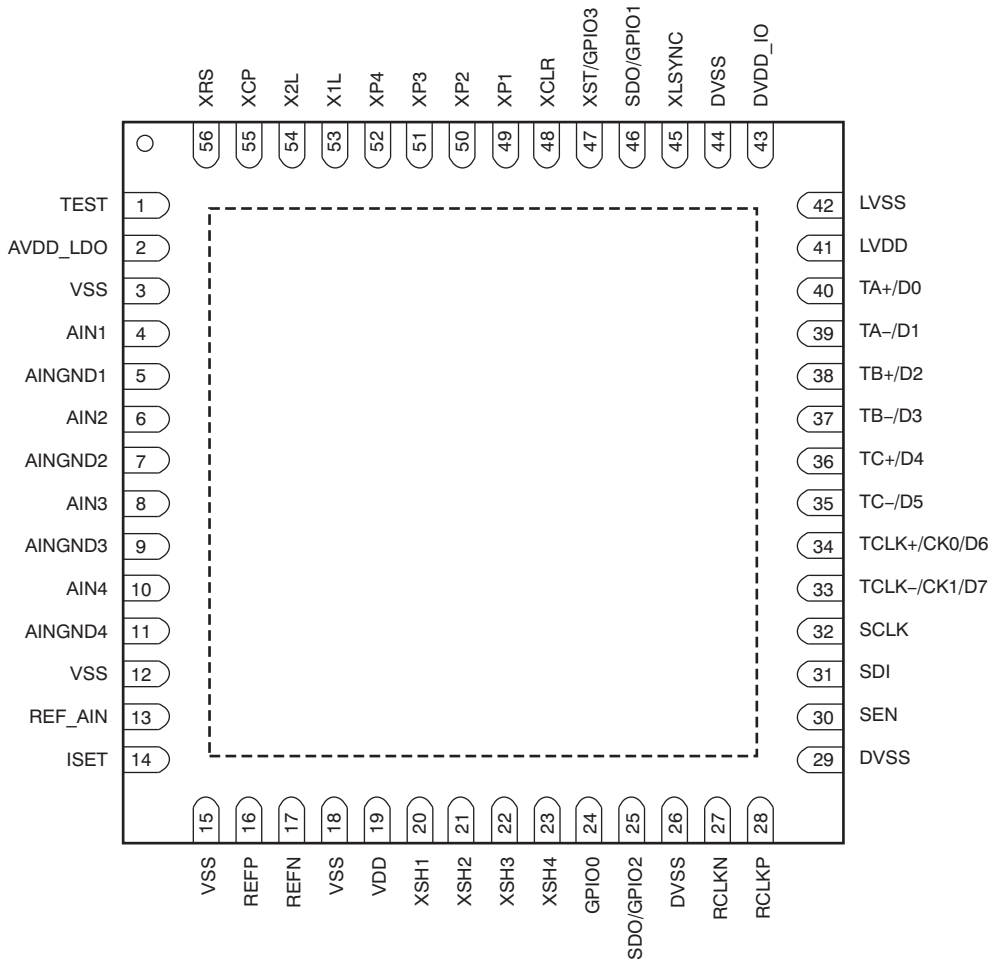


(1) $R_L/2$ = 49.9 Ω ± 1%

Figure 2. Test Load and Voltage Definition for LVDS Outputs

PIN CONFIGURATION

RSH PACKAGE
QFN-56
(TOP VIEW)



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PIN ASSIGNMENTS

PIN NUMBER	PIN NAME	TYPE(1)	DESCRIPTION
1	TEST	DI3.3	Internal test pin; connect to DGND
2	AVDD_LDO	AP1.8	Analog core power voltage output; not connected, open
3	VSS	AGND	LDO and analog I/O ground
4	AIN1	AI3.3	First channel analog signal input(2)
5	AINGND1	AI3.3	First channel analog signal ground(2)
6	AIN2	AI3.3	Second channel analog signal input(2)
7	AINGND2	AI3.3	Second channel analog signal ground(2)
8	AIN3	AI3.3	Third channel analog signal input(2)
9	AINGND3	AI3.3	Third channel analog signal ground(2)
10	AIN4	AI3.3	Fourth channel analog signal input(2)
11	AINGND4	AI3.3	Fourth channel analog signal ground(2)
12	VSS	AGND	LDO and analog I/O ground
13	REF_AIN	AI3.3/AO3.3	REF_DAC_IN 0 = Analog signal reference output (default) 1 = Analog signal reference input
14	ISET	LVO1.8	Internal reference voltage output;bypass to ground with a 10-kΩ ±1% resister
15	VSS	AGND	LDO and analog I/O ground
16	REFP	AO1.8	Positive reference; bypass to AGND with a 0.1-µF capacitor
17	REFN	AO1.8	Negative reference; bypass to AGND with a 0.1-µF capacitor
18	VSS	AGND	LDO and analog I/O ground
19	VDD	AP3.3	LDO and analog I/O power supply
20	XSH1	DO3.3	Sensor shift gate output 1
21	XSH2	DO3.3	Sensor shift gate output 2
22	XSH3	DO3.3	Sensor shift gate output 3
23	XSH4	DO3.3	Sensor shift gate output 4
24	GPIO0	DIO3.3	GPIO0_SEL 0 = GPI0, general-purpose input port 0 (default) (In case of input, internal pull-down resistor) 1 = GPO0, general-purpose output port 0
25	SDO/GPIO2	DIO3.3	GPIO2_SDO_SEL 0 = GPI2, general-purpose input port 2 (default) (In case of input, internal pull-down resistor) 1 = GPO2, general-purpose output port 2 2 = Reserved 3 = SDO, serial I/F data output
26	DVSS	DGND	Digital ground
27	RCLKN	LVI3.3	LVDS clock input
28	RCLKP	LVI3.3	CMOS master clock input/positive LVDS clock input
29	DVSS	DGND	Digital ground
30	SEN	DI3.3	Serial I/F enable; active low, internal pull-up resistor
31	SDI	DIO3.3	SDI_BUFF_CTRL 0 = Serial I/F data input 1 = Serial I/F data input/output (Internal pull-down resistor)
32	SCLK	DI3.3	Serial I/F clock (internal pull-down resistor)
33	TCLK–/CK1/ D7	LVO3.3	Negative LVDS clock output/Clock output 1/Data output bit 7
34	TCLK+/CK0/ D6	LVO3.3	Positive LVDS clock output/Clock output 0/Data output bit 6

(1) AP3.3 = 3.3-V analog power supply; AP1.8 = 1.8-V analog power supply; AGND = analog ground; GND = ground; AO3.3 = 3.3-V analog output; AO1.8 = 1.8-V analog output; AI3.3 = 3.3-V analog input; DP3.3 = 3.3-V digital power supply; DP1.8 = 1.8-V digital power supply; DGND = digital ground; DO3.3 = 3.3-V digital output; DI3.3 = 3.3-V digital input; DIO3.3 = 3.3-V digital I/O; LVP3.3 = 3.3-V LVDS power supply; LVGND = LVDS ground; LVO3.3 = 3.3-V LVDS output; LVI3.3 = 3.3-V LVDS input; and LVO = 3.3-V LVDS output.
(2) If these pins are unused, they can be opened or decoupled to GND with a decoupling capacitor.

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PIN ASSIGNMENTS (continued)

PIN NUMBER	PIN NAME	TYPE[1]	DESCRIPTION
35	TC–/D5	LVO3.3	Negative TC channel LVDS data output/Data output bit 5
36	TC+/D4	LVO3.3	Positive TC channel LVDS data output/Data output bit 4
37	TB–/D3	LVO3.3	Negative TB channel LVDS data output/Data output bit 3
38	TB+/D2	LVO3.3	Positive TB channel LVDS data output/Data output bit 2
39	TA–/D1	LVO3.3	Negative TA channel LVDS data output/Data output bit 1
40	TA+/D0	LVO3.3	Positive TA channel LVDS data output/Data output bit 0
41	LVDD	LVP3.3	LVDS/CMOS output power supply
42	LVSS	LVGND	LVDS/CMOS output ground
43	DVDD_IO	DP3.3	Digital I/O power supply
44	DVSS	DGND	Digital ground
45	XLSYNC	DIO3.3	XLSYNC_SEL 0 = Internal line synchronous signal output (default) (In case of input, internal pull-down resistor) 1 = External line synchronous signal input. Polarity is set by the XLSYNC_POL register (default is active high).
46	SDO/GPIO1	DIO3.3	GPIO1_SDO_SEL 0 = GPI1, general-purpose input port 1 (default) (In case of input, internal pull-down resistor) 1 = GPO1, general-purpose output port 1 2 = Reserved, internal test input 3 = SDO, serial I/F data output
47	XST/GPIO3	DIO3.3	GPIO3_XST_SEL 0 = GPI3, general-purpose input port 3 (default) (In case of input, internal pull-down resistor) 1 = GPO3, general-purpose output port 3 2 = Reserved, internal test input 3 = XST, storage pulse output
48	XCLR	DO3.3	Sensor clear gate output
49	XP1	DO3.3	Fast transfer clock output φ1
50	XP2	DO3.3	Fast transfer clock output φ2
51	XP3	DO3.3	Fast transfer clock output φ3
52	XP4	DO3.3	Fast transfer clock output φ4
53	X1L	DO3.3	Fast transfer clock output 1L
54	X2L	DO3.3	Fast transfer clock output 2L
55	XCP	DO3.3	Clamp gate clock output
56	XRS	DO3.3	Reset gate clock output

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FUNCTIONAL BLOCK DIAGRAM

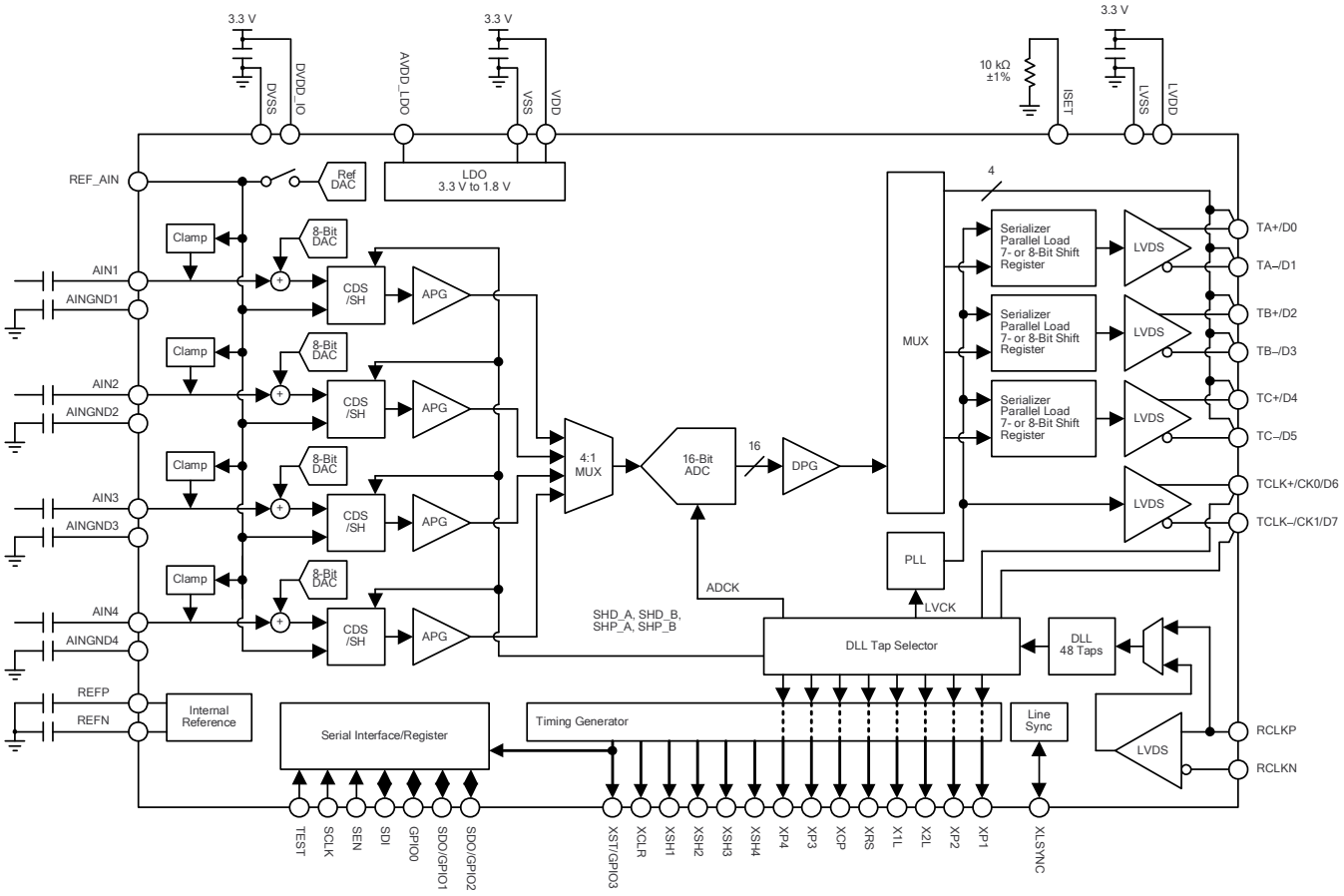


Figure 3. VSP5610/11/12 Block Diagram

SYSTEM OVERVIEW

INTRODUCTION

The VSP5610/11/12 are analog front-end (AFE) devices for CCD and CMOS line image sensor applications such as copiers, facsimile machines, etc. The VSP5610/11/12 each provide four independent data processing channels.

The data from each image sensor channel are sampled and held by either the SH or CDS circuit and are then converted into digital data by an ADC. The digital data for each channel are later converted into serial data that can be output in either LVDS mode or CMOS mode.

AFE BLOCK

ANALOG SIGNAL INPUT

These devices have four channels that can be used as analog input ports for an image sensor. In addition to the four-channel input, this AFE device also supports three-channel and two-channel inputs. Table 2 shows the register settings required to select the different channel modes.

Table 2. Analog Input Channel Mode Selection

MODE	AIN_CH_SEL	AIN1	AIN2	AIN3	AIN4
Two-channel	2	Active	Standby	Active	Standby
Three-channel	1	Active	Active	Active	Standby
Four-channel	0	Active	Active	Active	Active

Each analog input supports CDS and simple SH circuits to accommodate CCD and CMOS image sensors. The sampling mode can be selected independently for each channel by configuring the internal registers. As shown in Table 3, if AINx_SH_CDS is set to '0', then the corresponding channel operates in CDS mode.

Table 3. CDS/SH Mode Selection

AINx_SH_CDS(1)	SH/CDS
0	CDS
1	SH

(1) AINx_POL = Analog input polarity setting register (x = 1, 2, 3, and 4).

In addition, these devices also support independent selection of the input signal polarity for each channel. Input signal polarity can be set using the AINx_POL register, where x = 1, 2, 3, or 4. The input signal range and polarity are defined in the *Analog Input Specification* section.

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Correlated Double Sampler (CDS) Mode (AINx_SH_CDS = 0)

CDS mode is designed to accommodate inputs from the CCD sensor. The output signal of a CCD image sensor is sampled twice during one pixel period. First, the reference interval is sampled by the SHP pulse, then the data interval is sampled by the SHD pulse. Subtracting these two samples provides the video information of the pixel as well as removes any noise common to both intervals. Thus, CDS plays an important role in reducing the reset noise and other low-frequency noises that are present on the CCD output signal. Figure 4 shows a diagram of CDS mode.

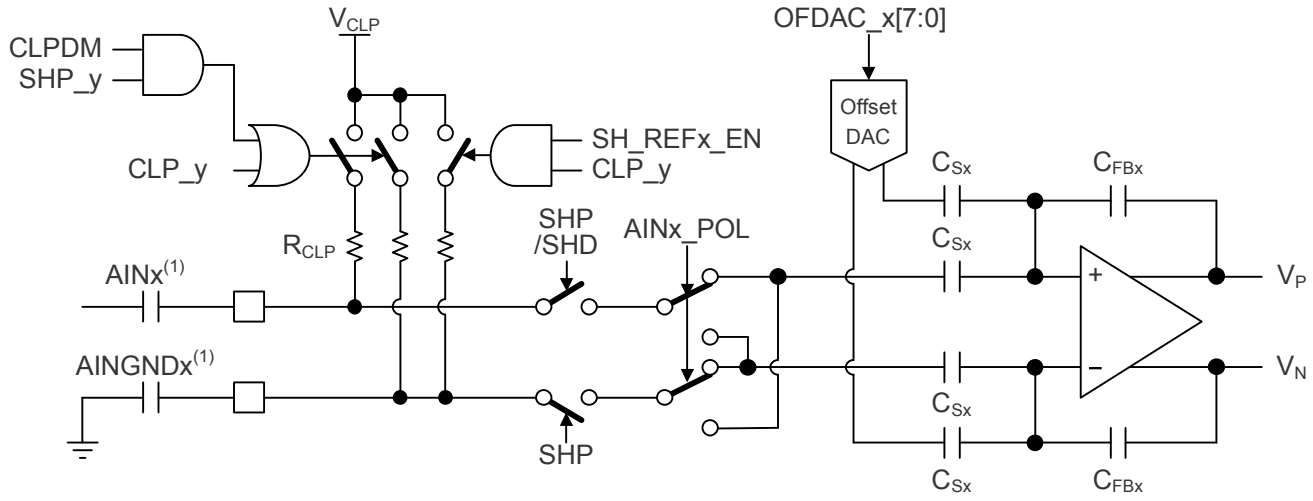
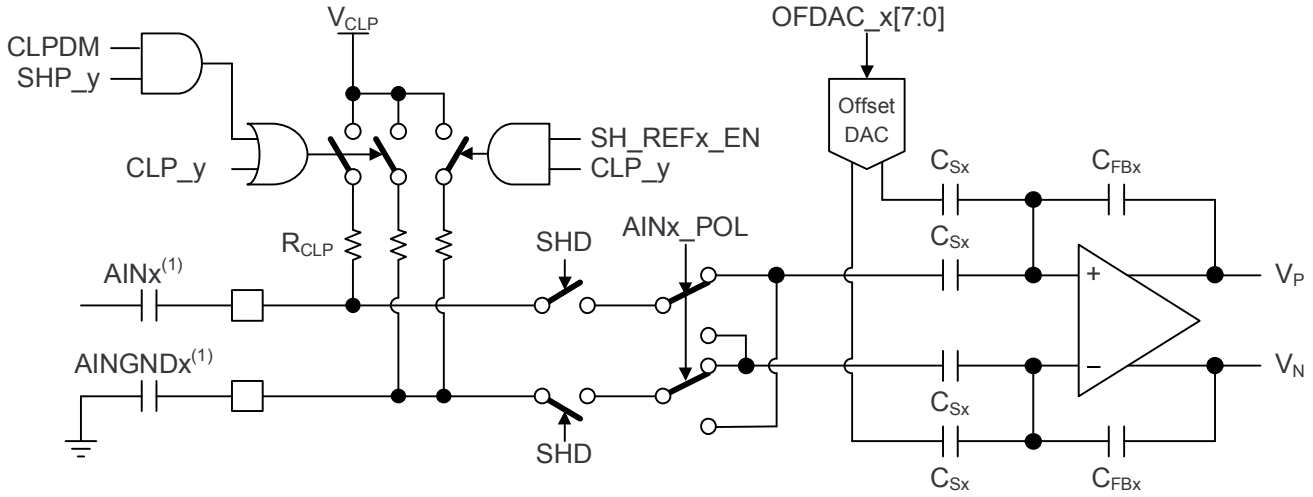


Figure 4. CDS Mode Input Circuit for CCD Signal

Sample Hold (SH) Mode (AINx_SH_CDS = 1)

SH mode supports CCD and CMOS sensors. For the CCD sensor, the sensor signal pedestal level is clamped to the V_{CLP} level using an internal clamp circuit. SH samples only once during a pixel period. The SHD pulse is used to sample the CCD signal data interval. After sampling, the SH circuit takes the difference of the data and V_{CLP} levels to extract the video information.

For the CMOS input, the input clamp function should be set according to the requirements. If the sensor output is within the allowable input range, an ac-coupling capacitor for analog input may not be needed. When the sensor signal is directly input to the AFE, the SH circuit requires a reference voltage to set the black level. To use V_{CLP} as a reference, SH_REFx_EN should be enabled and AINGNDx then opened or coupled to GND with a capacitor. To use an external reference, it can be input to AINGNDx with sensor signals connected to AINx. Figure 5 shows a diagram of the SH mode.



(1) Under some conditions, the sensor signal can be directly input to the AFE without requiring an external capacitor.

(2) In SH mode, the SHP clock should be programmed so that it does not overlap the SHD clock.

Figure 5. SH Mode Input Circuit for CCD or CMOS Signal

INPUT CLAMP AND SENSOR REFERENCE

The CCD output signal has a large dc offset that may exceed the input range of the AFE input circuit. Therefore, this output signal is ac-coupled to the AFE through a capacitor, and the internal dc level is set to the clamp voltage (V_{CLP}) by an internal clamp circuit. The VSP5610/11/12 provide three modes for clamp operation: pixel clamp, line clamp, and not clamped. These modes are shown in Table 4. The clamp mode can be set independently for each channel by configuring the AINx_CLP_SEL register.

Table 4. Clamp Mode Selection

CLAMP MODE	MODE SETTING	CLAMP ACTIVE CONDITION AND SETTING			
	AINx_CLP_SEL(1)	CDS/SH	CLP_y(2)	CLPDM AND SHP_y(2)	SH_REF_EN
Pixel clamp	0 (default)	CDS/SH	Active	Active	Off
Line clamp	1	CDS/SH	—	Active	Off
Not clamped	2	Only SH	—	—	On
	3	Only SH	—	—	Off

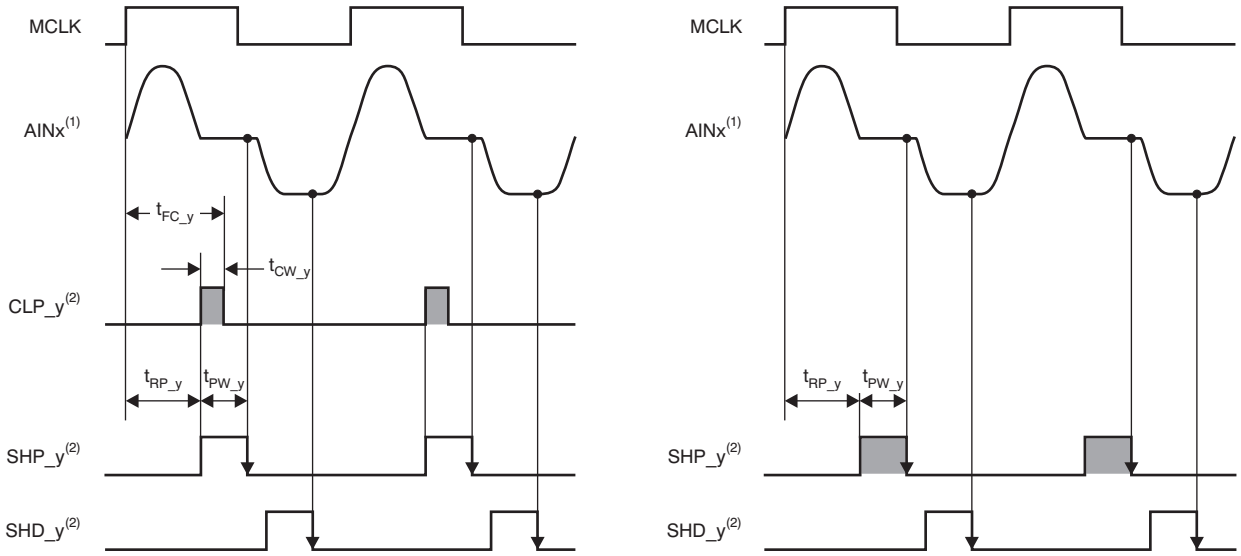
(1) AINx_CLP_SEL (x = 1, 2, 3, and 4).
(2) y = A and B.

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In pixel clamp mode, CLP_A/B is used for clamping. The input signal is clamped to V_{CLP} via the CLP_A/B pulse during each pixel period, as shown in Figure 6a. Because the ac-coupling capacitor is charged on a pixel-to-pixel basis, the clamp level droop can be controlled by the clamp pulse width.

In line clamp mode, SHP_A/B is used for clamping when CLPDM is active, as shown in Figure 6b. The input signal is clamped only in the CLPDM period within one line cycle of the sensor. The signal is clamped in this method because the charge leaks the least from the coupling capacitor during the CLPDM period. Accordingly, because there may be a large droop in the clamp level, this device does not support line clamp in the SH mode.

The *not-clamped* mode is mainly used in for a CMOS sensor input. If the sensor signal is directly connected to the AFE, this mode should be configured without an ac-coupling capacitor at the input port. This mode has two options to select a reference for the sensor black level: internal reference and external input. In the internal reference option, the internal reference (V_{CLP}) is used with AINx_CLP_SEL = 2. In the external input option, the external input is used from AINGNDx with AINx_CLP_SEL = 3.



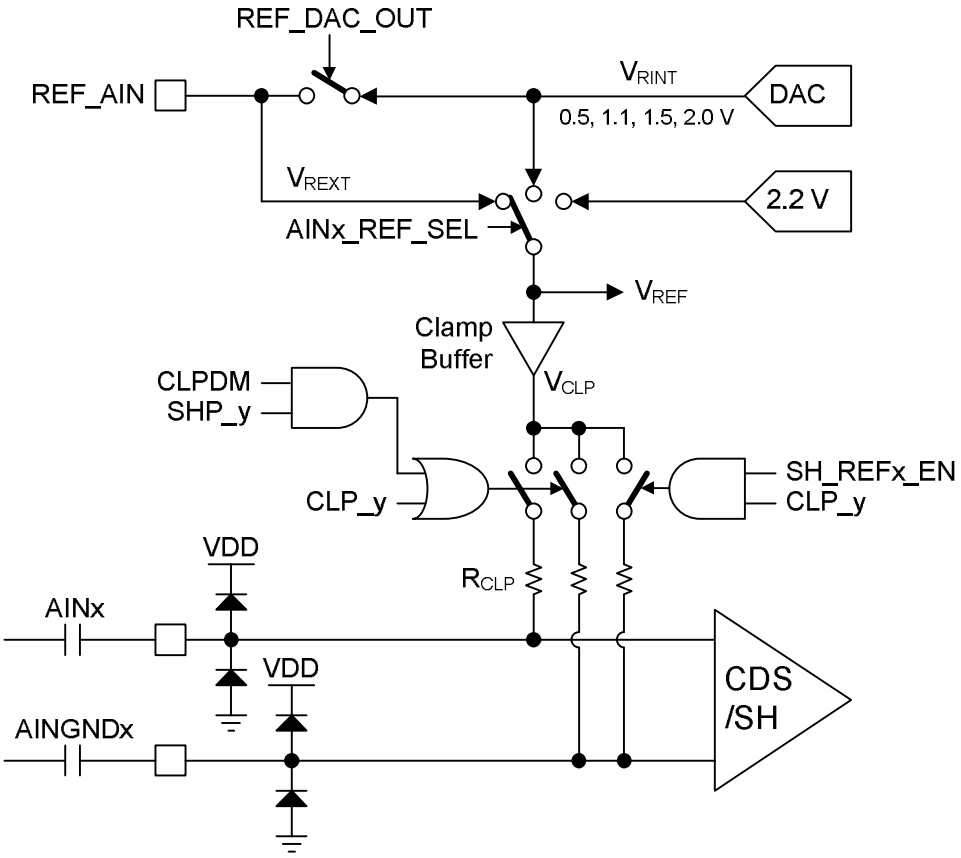
(1) x = AIN channel number, x = 1, 2, 3, and 4.

(2) y = Group code of sample pulse signals. When x = 1 or 2, y = A. When x = 3 or 4, y = B.

Figure 6. Input Clamp Function

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As shown in Figure 7, the internal V_{CLP} node provides the clamp reference voltage. As for the clamp level, it is possible to select three reference voltage modes by setting the AINx_REF_SEL register. The first mode provides a fixed 2.2 V, the second mode provides selectable outputs (0.5 V, 1.1 V, 1.5 V, and 2.0 V) of an internal DAC, and the third mode allows an external input from the REF_AIN pin to be used as the clamp reference. This REF_AIN pin is bidirectional and also acts as an output of the internal DAC. Table 5 shows the relationship between the register and clamp level. Table 6 shows the DAC configuration.



(1) If the sensor signal is directly input to the AFE, the enternal capacitor should not be connected.

Figure 7. V_{CLP} Block Diagram

Table 5. Clamp Level Selection

MODE SETTING AINx_REF_SEL[1:0] (1)	CLAMP LEVEL	
0	2.2 V	
1	V_{RINT}	Reference DAC (0.5 V, 1.1 V, 1.5 V, and 2.0 V)
2	V_{REXT}	REF_AIN external input

(1) AINx_CLP_SEL (x = 1, 2, 3, and 4).

Table 6. V_{RINT} Voltage Selection

SETTING CODE VRINT_SEL	REF DAC V_{RINT} (V)
2	0.5
3	1.1
0	1.5 (default)
1	2.0

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If line clamp mode is used, the CLPDM period should be configured by the internal registers. The CLPDM period is determined with reference to the line cycle signal for the sensor (LS). Thus, the start and end of CLPDM are each defined as the number of pixels from the LS falling edge. Because CLPDM is used as the clamp period, it should be assigned for the interval of any dummy or optical black pixels. Figure 8 shows the relationship between LS and CLPDM.

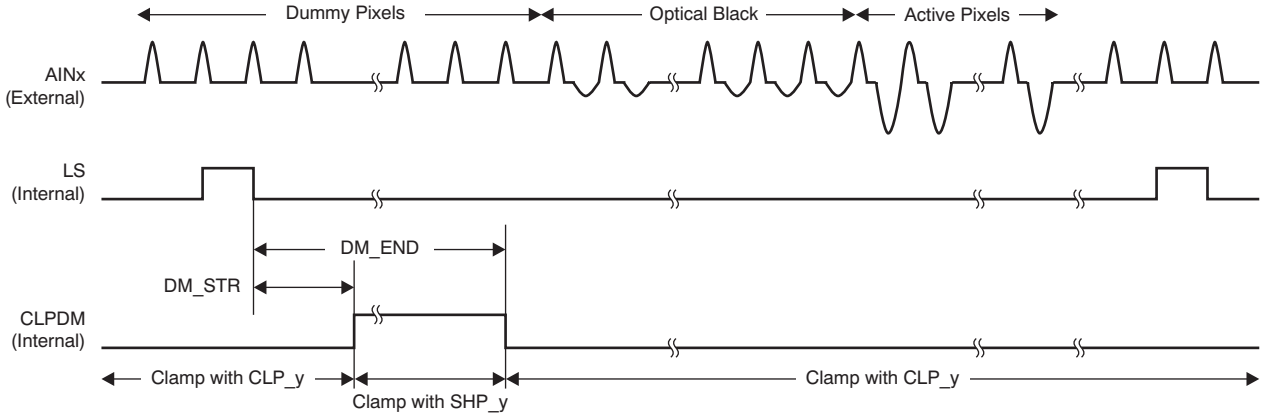


Figure 8. Line Clamp Period Setting

Pixel Clamp Period Setting

In pixel clamp mode, without CLPDM, the sensor signal is clamped with CLP_A and CLP_B pulses. CLP_A corresponds to AIN1 and AIN2; CLP_B corresponds to AIN3 and AIN4. The start of these pulses is synchronized with the SHP_y rising edge (where y = A or B). There are two options to configure the end position: first, to automatically set the pulse width to 50% that of SHP_y; and second, to manually configure the end position using an internal register. Figure 9 and Figure 10 illustrate the details of the clamp pulse function in automatic and manual modes, respectively.

Automatic Mode (CLP_TF_AT_DIS = 0)

Figure 9 shows the automatic mode when CLP_TF_AT_DIS is '0'.

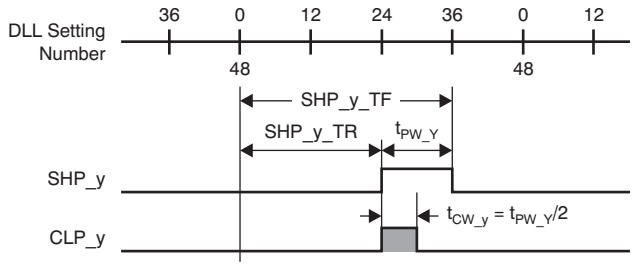


Figure 9. Automatic Mode

Manual Mode (CLP_TF_AT_DIS = 1)

Figure 10 shows the manual mode when CLP_TF_AT_DIS is '1'.

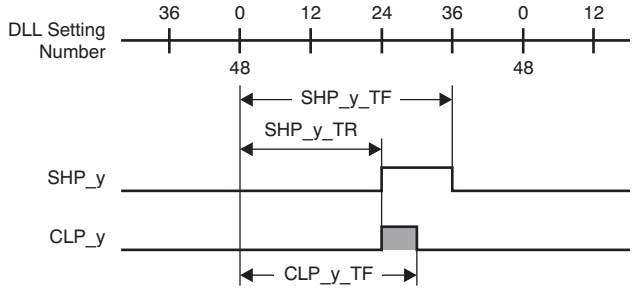
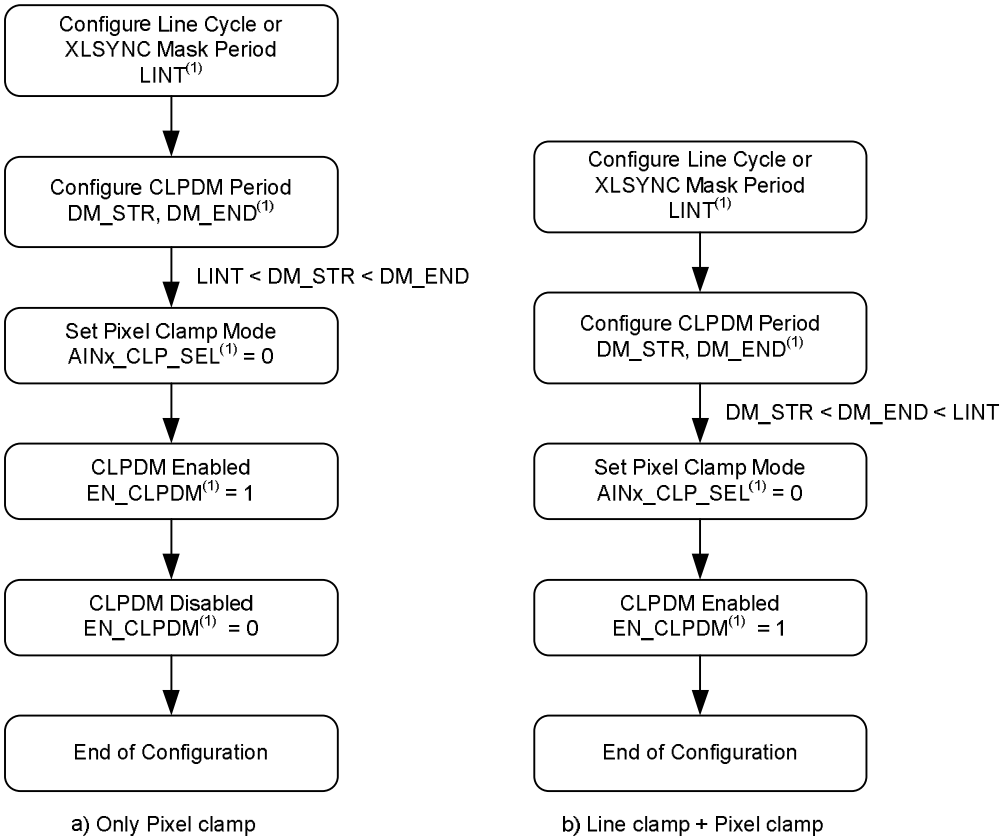


Figure 10. Manual Mode

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In pixel clamp mode when CLPDM is active, the sensor signal is clamped with SHP_y. Therefore, the pixel clamp operation is closely related with the status of CLPDM. The condition of CLPDM should be properly defined with the internal registers. Because CLPDM is always high during a default condition after reset or power up, the status of CLPDM should be defined according to this sequence. Furthermore, the CLPDM status should be defined in the second step of the flowchart shown in Figure 11 for either configuration. All other user-dependent settings, except XLSYNC_SEL and EN_OUT of the software reset sequence, are described in Figure 11.



(1) Internal registers: AINx_CLP_SEL = addresses 16 and 17; LINT = address 7; DM_STR = address 8; DM_END = address 9; and EN_CLPDM = address 399, bit 1.

Figure 11. Configuration Sequence for Pixel Clamp

ANALOG PROGRAMMABLE GAIN (APG)

The SH output can be amplified using programmable analog gain. This gain can be set from 0.5 V/V to 3.5 V/V with a step size of 3/64 V/V.

The gain setting can be controlled by an internal register (APG_x). Equation 1 shows the relationship between the setting code and gain. The gain of each of the four channels can be set independently using different registers. Note that the black pixel level may possibly change as a result of the change in the gain; therefore, the appropriate timing of the gain change should be used to avoid degradation in image quality. Figure 12 shows analog gain as a function of gain control code in terms of V/V. Figure 13 shows the maximum allowed input signal as a function of gain control code.

$$\text{APG (V/V)} = \frac{3}{63} \times \text{Code} + 0.5 \qquad \text{(Code = 0 LSB to 63 LSB)} \tag{1}$$

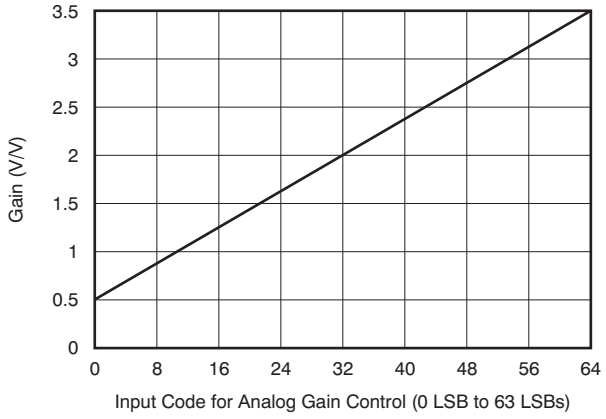


Figure 12. Analog Gain vs Setting Code

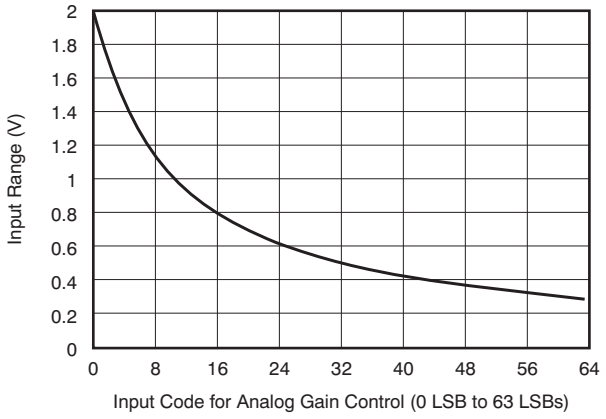


Figure 13. Input Range vs Analog Gain Setting Code

DIGITAL PROGRAMMABLE GAIN (DPG)

The VSP5610/11/12 provide a maximum digital gain of 2 V/V. The total gain is fixed by the combination of CDS/SH analog gain (APG) and digital gain (DPG). DPG is controlled by an 8-bit internal register (DPG_x) that can set the gain from 1 V/V to 2 V/V, as defined by Equation 2. This register is included in each of the four channels, so the gain of each channel can be set independently.

Figure 14 shows the relationship between the digital gain and register code. Note that the default value is 1 V/V.

$$\text{DPG (V/V)} = \frac{1}{256} \times \text{Code} + 1 \qquad \text{(Code = 0 LSB to 255 LSB)} \tag{2}$$

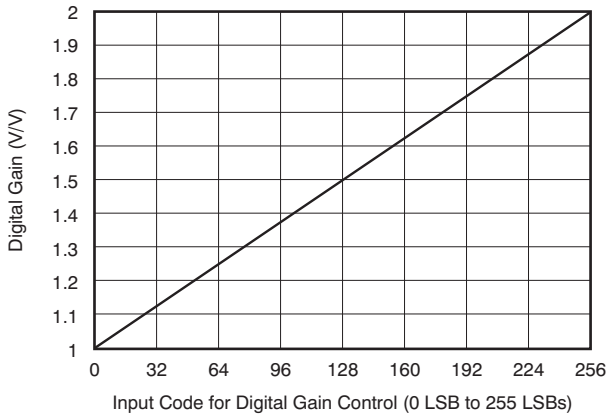


Figure 14. Digital Gain Setting Code

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ADC

The ADC output format is selectable as twos complement or offset binary by configuring a register. Table 7 shows the relationship between register setting and condition.

Table 7. ADC Data Format Configuration

ADC_DAT_FRM	MODE
0 (default)	Twos complement
1	Offset binary

OFFSET DAC

The VSP5610/11/12 have an independent DAC in each channel for offset level correction of the input signal. The correction range is ±250 mV and resolution is 8 bits. The DAC output voltage can be set by register settings. Table 8 and Figure 15 show the relationship between the output and setting codes. The setting code is defined in twos complement format. The DAC output offset voltage in millivolts as a function of the register setting is given in Equation 3.

Table 8. Offset DAC Setting Code

SETTING CODE OFDAC_x[7:0](1)	OUTPUT (mV)
7Fh	248.05
7Eh	246.09
…	…
01h	1.95
00h	0
FFh	–1.95
…	…
81h	–248.05
80h	–250.00

(1) × = 1, 2, 3, and 4.

$$\text{DAC Output (mV)} = \frac{250}{128} \times \text{OFDAC_x[7:0]} \quad (3)$$

where:

x = 1, 2, 3, and 4

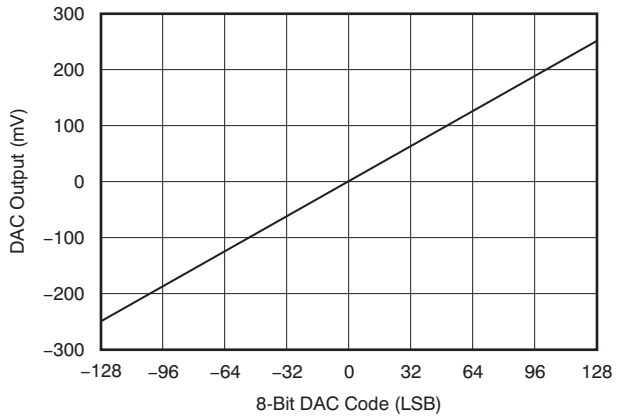


Figure 15. Offset DAC Setting Code vs Output Voltage

TIMING GENERATOR (TG)

The image sensor timing generator (TG) is incorporated into these devices. The TG provides six signals that function as slow transfer clocks and eight signals that function as fast transfer clocks. In addition, the fast clock signals can also be used as slow clock signals. The TG signals are synchronized with LS (which is the image sensor line cycle) and are completely controlled by the internal registers. Because the TG output is locked under the default setting, EN_OUT (address 2, bit 10) should be set to '1' to enable the outputs.

LINE SYNCHRONOUS FUNCTION

The VSP5610/11/12 have two modes for synchronizing the sensor line cycle: internal line (Figure 16) and external line syncronous mode (Figure 17). In internal line synchronous mode, the line cycle signal (LS) is generated after a certain number of MCLK cycles that are counted by an internal counter (PIX_CNT). The number of MCLK cycles is determined by the LINT[19:0] register; the counter clears after LS is generated. The active LS period is equal to one MCLK cycle period.

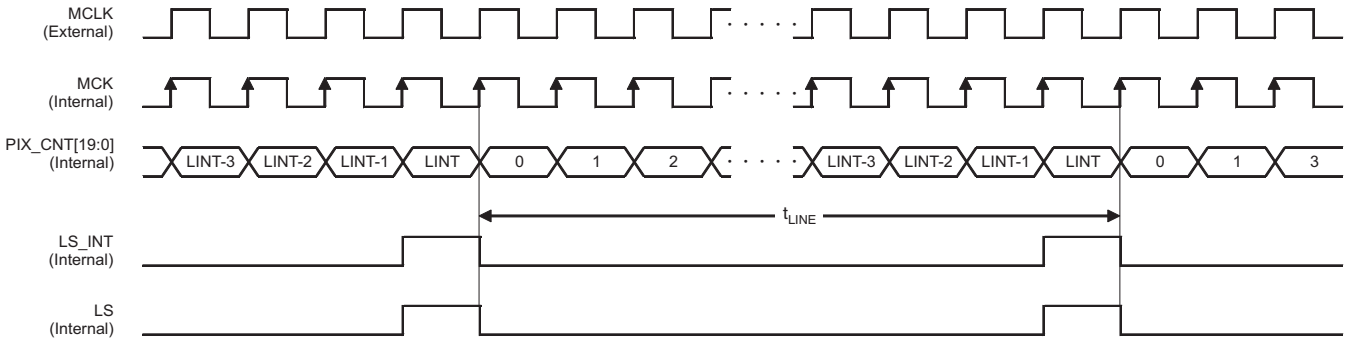


Figure 16. Internal Line Synchronous Mode (XLSYNC_SEL = 1)

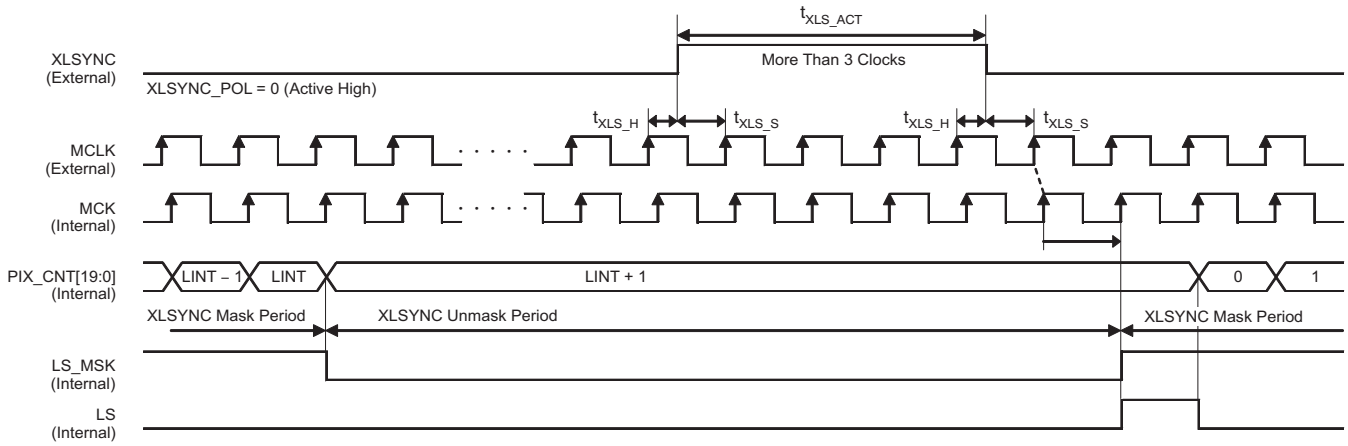


Figure 17. External Line Synchronous Mode (XLSYNC_SEL = 0, default)

Table 9. Timing Requirements for Figure 16 and Figure 17

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{LINE}	Line cycle period setting	XLSYNC = 1	3	LINT + 1	$2^{20} - 1$	Clocks
t_{XLS_ACT}	XLSYNC active period	XLSYNC = 0	3			Clocks
t_{XLS_S}	XLSYNC setup to MCLK	XLSYNC = 0	10			ns
t_{XLS_H}	XLSYNC hold to MCLK	XLSYNC = 0	10			ns

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The other mode is the external line synchronous mode which requires an external signal (XLSYNC). In this mode, if the logic circuit detects an active XLSYNC period for more than three MCLK cycles, the internal line synchronous signal (LS) is generated. This mode has a function that mask XLSYNC in order to avoid noise interference. The duration of the XLSYNC mask can be set by the LINT[19:0] register, which is also used in the internal line synchronous mode.

The two line synchronous modes and the polarity can be selected by the XLSYNC_SEL and XLSYNC_POL registers, respectively. The default settings are external mode and active high polarity. XLSYNC can be used to output some internal signals. Table 10 shows the register settings required to select the desired output signals.

PIX_CNT can be automatically reset by LS_CNT_RST (which is an internal register). Before performing this function, a software reset must be executed in order set RST_ALL to '1'. If LS_CNT_RST is set to '1' after a software reset, the pixel counter is then held at '0'. To make the counter active, LS_CNT_RST should return to '0'.

Table 10. XLSYNC Output Signal (XLSYNC_SEL = 1)

REGISTER SETTING XLSYNC_OUT	OUTPUT SIGNAL
0	LS
1	CLPDM
2	Reserved
3	Reserved

SLOW TRANSFER CLOCK SETTING (XST, XSHn, XCLR)

XST, XSHn (where n = 1 to 4), and XCLR are slow transfer clocks that can be configured by setting the initial polarity and toggle points. As shown in Table 11, the predetermined number of toggle points is different for each signal. Because the two toggles generate one pulse, the number of pulses is half the number of toggles.

Table 11. Toggle Number and Generated Pulse

SIGNAL	TOGGLE	PULSE
XST	8	4
XSHn	16	8
XCLR	48	24

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Each toggle position is defined by a register that is exclusive for each signal. The toggle position is synchronized with LS and the gap between the toggle position and the LS falling edge. The LS falling edge is defined in terms of t_{MCLK}, the cycle period of MCLK. This gap is set by register settings and is defined by Equation 4:

$$t = (Xn_T(k) + 1) \times t_{MCLK}$$

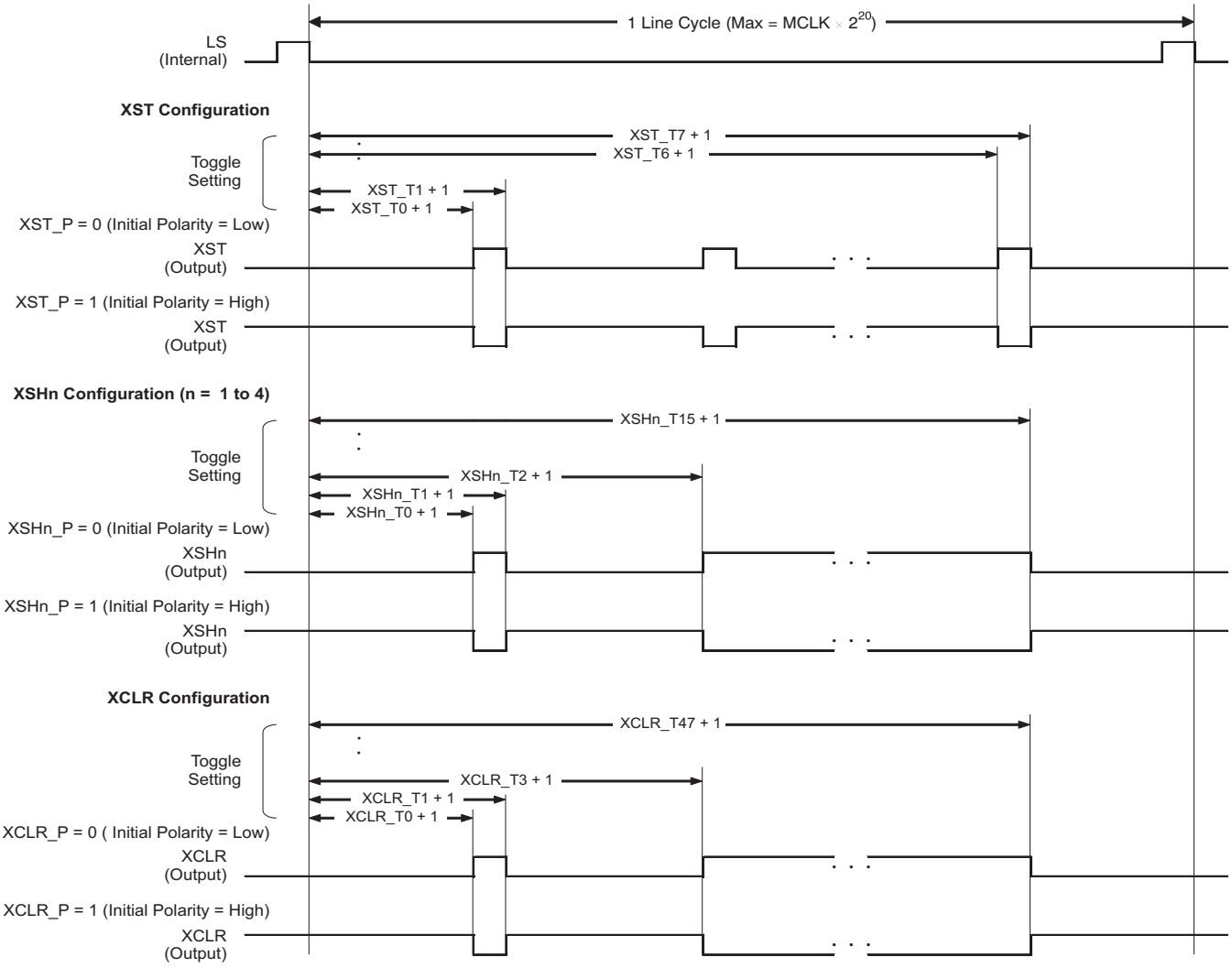
where:

n = ST, SHn, CLR

k = 0 to 7 (XST); k = 0 to 15 (XSHn); k = 0 to 47 (XCLR)

Xn_T(k) is less than LINT and is the register value of the toggle setting (4)

The toggle for each signal can be disabled with register settings. To make the toggle active, Xn_TGL_EN should be set to '1'. However, because XST shares a pin with GPIO3, pin function should be configured with the GPIO3_XST_SEL register. Figure 18 shows the configuration regarding the slow transfer clock.



(1) If Xn_Tn is set to '0', the toggle position is ignored (except for Xn_T0).

(2) The period between the toggle position and LS falling edge = $(Xn_T(k) + 1) \times t_{MCLK}$.

(3) The following requirement must be satisfied: Xn_T(k) < Xn_T(k + 1).

(4) The signal is set to the desired polarity settings at the falling edge of LS.

Figure 18. Slow Transfer Gate Signal Setting for XST, XSHn, and XCLR

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FAST TRANSFER CLOCK PULSE SETTING

XP1/2, X1L, X2L, XRS, XCP, and XP3/4 are fast transfer clock signals with rising and falling edges that are configurable via register settings. Figure 19 shows the block diagram of the fast clock configuration. In Figure 19, the *DLL Tap Selector* is used to select both the rising and the falling edges of each signal from among 48 tap positions.

The XP2 clock signal is an inverse of XP1 and shares rising and falling edge settings. Similarly, XP4 is an inverse of XP3 and likewise shares rising and falling edge settings. The other signals have individual configuration registers for setting the position of both edges.

In addition, it is possible to change the clock rate of each signal with register settings. The clock rate is based on the frequency of MCLK. XP1 and XP2 can select x1, x2, or x4 modes with common settings. XP3 and XP4 can also select x1, x2, or x4 modes with common settings. The other signals can choose between the x1 and x2 rate settings.

Note that two independent sets of registers are available to set the clock rate, the clock rising edge, and the clock falling edge for operation in x1-mode and x2-mode.

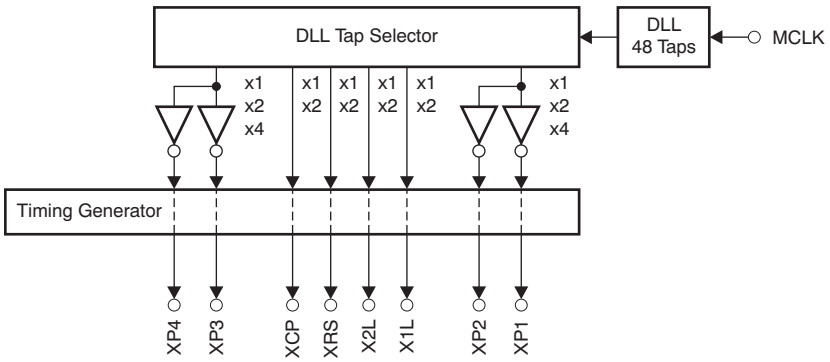


Figure 19. Fast Transfer Clock Pulse Generator

Fast Transfer Clock Pulse Timing

This section describes the timing of the fast transfer clock pulse for XRS (Figure 20), XCP (Figure 21), XP1 and XP2 (Figure 22), XP3 and XP4 (Figure 23), and X1L and X2L (Figure 24).

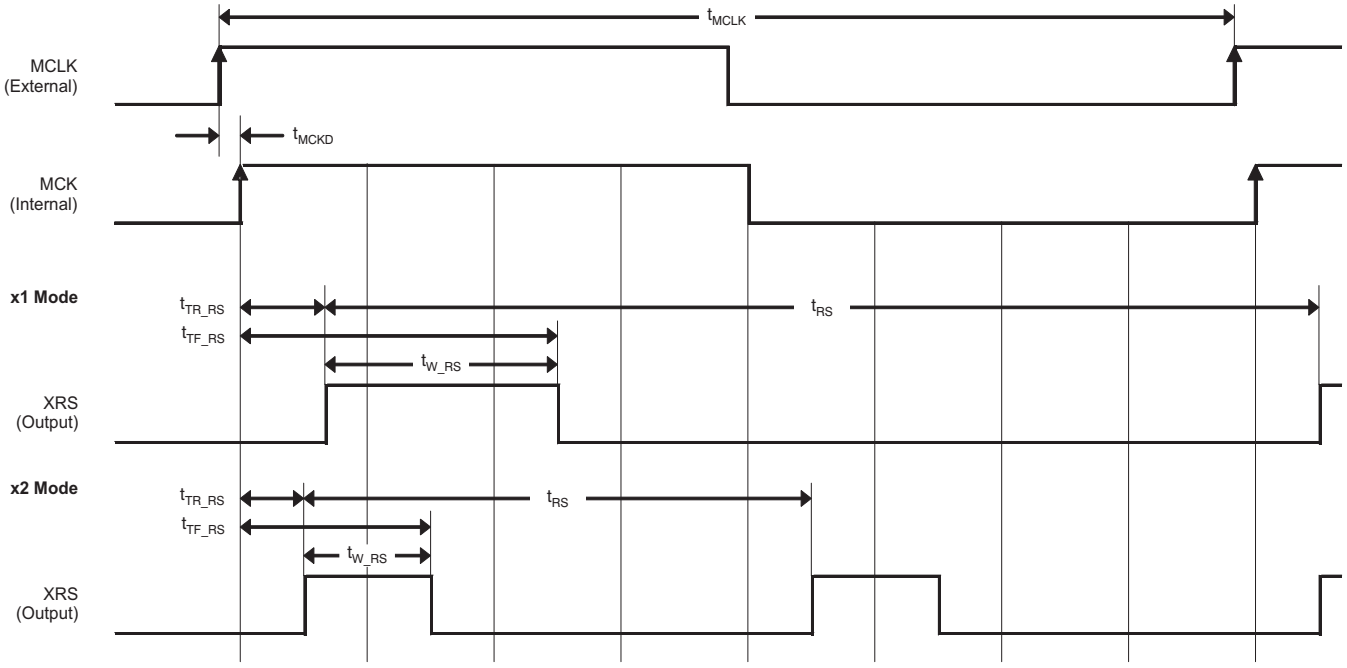


Figure 20. XRS Fast Transfer Clock Pulse Setting

Table 12. Timing Requirements for Figure 20

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MCLK}	MCLK frequency	VSP5610	1		11.66	MHz
		VSP5611	1		16.66	MHz
		VSP5612	1		23.33	MHz
t_{MCLK}	MCLK period			$1/f_{MCLK}$		ns
t_{MCKD}	MCLK to MCK delay			2		ns
t_{RS}	XRS period	x1 mode		t_{MCLK}		ns
		x2 mode		$t_{MCLK} \times 1/2$		ns
t_{TR_RS}	XRS rising edge delay from MCK	x1 mode	0		$t_{MCLK} \times 47/48$	ns
		x2 mode	0		$t_{MCLK} \times 23/24$	ns
t_{TF_RS}	XRS falling edge delay from MCK	x1 mode	0		$t_{MCLK} \times 47/48$	ns
		x2 mode	0		$t_{MCLK} \times 23/24$	ns
t_{W_RS}	XRS pulse width	x1 mode	2		$t_{MCLK} - 2$	ns
		x2 mode	2		$t_{MCLK} \times 1/2 - 2$	ns

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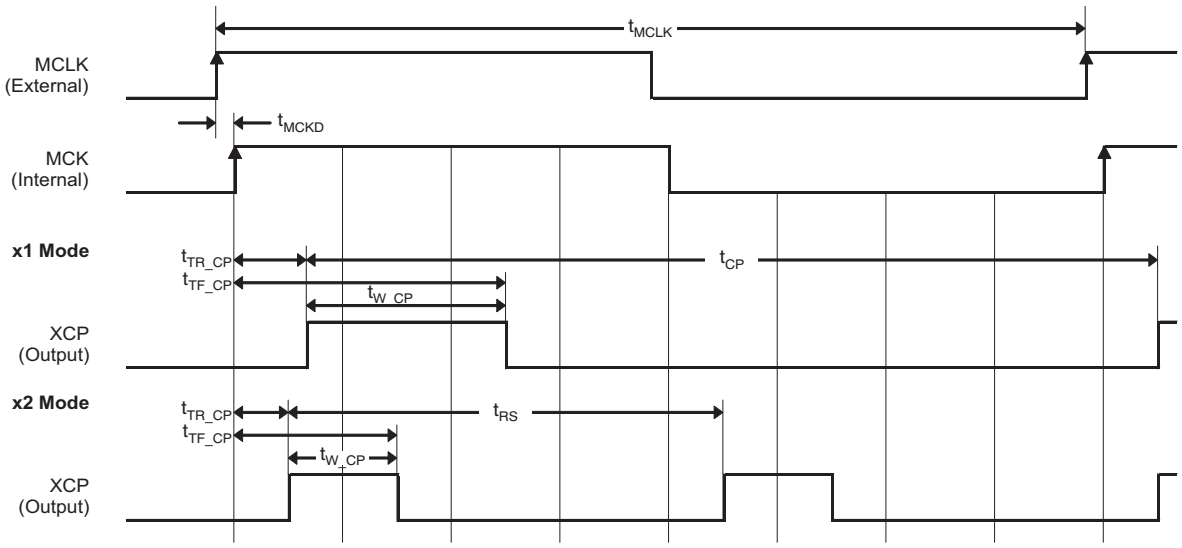


Figure 21. XCP Fast Transfer Clock Pulse Setting

Table 13. Timing Requirements for Figure 21

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MCLK}	MCLK frequency	VSP5610	1		11.66	MHz
		VSP5611	1		16.66	MHz
		VSP5612	1		23.33	MHz
t_{MCLK}	MCLK period			$1/f_{MCLK}$		ns
t_{MCKD}	MCLK to MCK delay			2		ns
t_{CP}	XCP period	x1 mode		t_{MCLK}		ns
		x2 mode		t_{MCLK} × 1/2		ns
t_{TR_CP}	XCP rising edge delay from MCK	x1 mode	0		t_{MCLK} × 47/48	ns
		x2 mode	0		t_{MCLK} × 23/24	ns
t_{TF_CP}	XCP falling edge delay from MCK	x1 mode	0		t_{MCLK} × 47/48	ns
		x2 mode	0		t_{MCLK} × 23/24	ns
t_{W_CP}	XCP pulse width	x1 mode	2		t_{MCLK} – 2	ns
		x2 mode	2		t_{MCLK} × 1/2 – 2	ns

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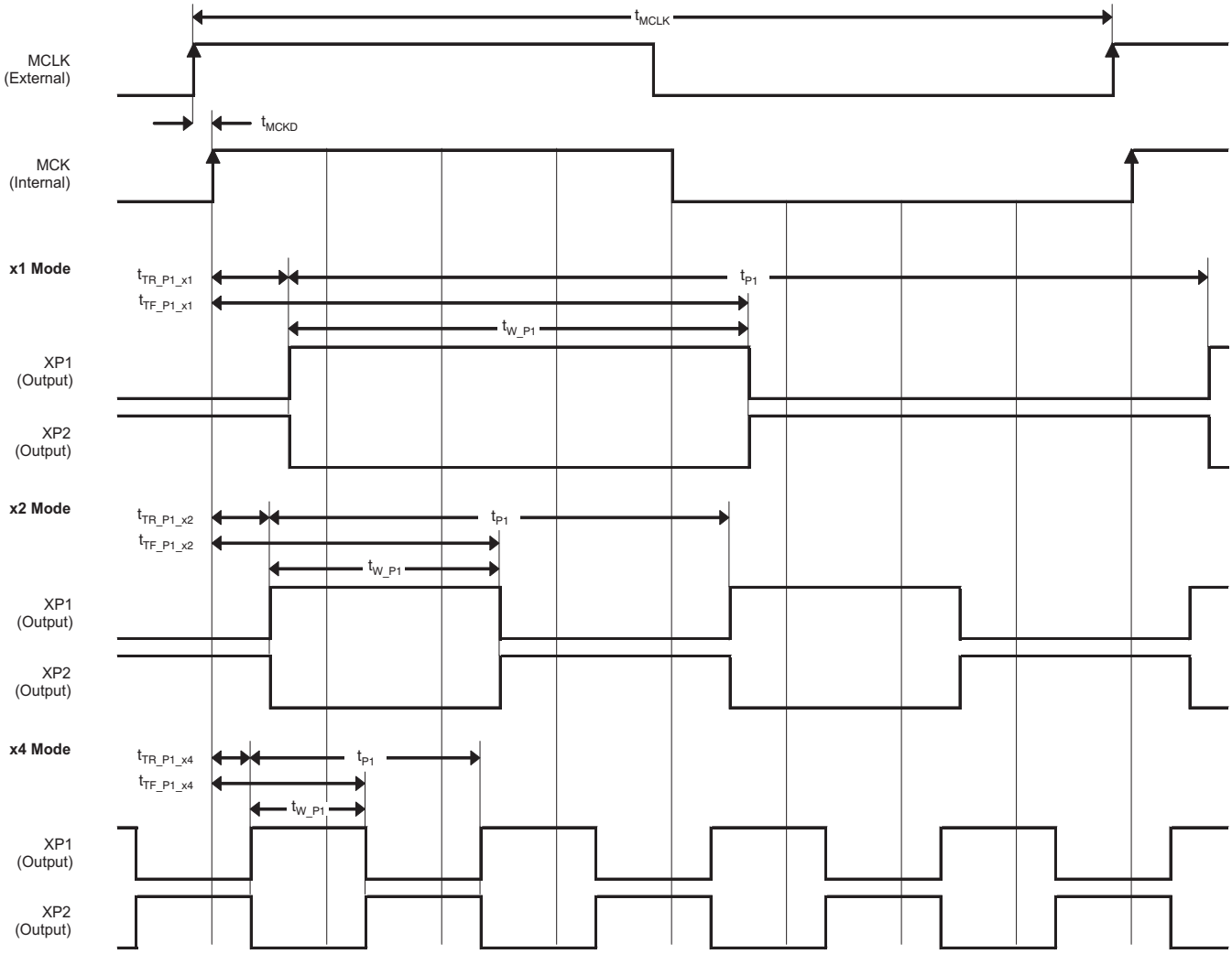


Figure 22. XP1 and XP2 Fast Transfer Clock Pulse Setting

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Table 14. Timing Requirements for Figure 22

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MCLK}	MCLK frequency	VSP5610	1		11.66	MHz
		VSP5611	1		16.66	MHz
		VSP5612	1		23.33	MHz
t_{MCLK}	MCLK period			$1/f_{MCLK}$		ns
t_{MCKD}	MCLK to MCK delay			2		ns
t_{Pn}	XP1, XP2 period	x1 mode		t_{MCLK}		ns
		x2 mode		$t_{MCLK} \times 1/2$		ns
		x4 mode		$t_{MCLK} \times 1/4$		ns
$t_{TR_P_x1}$	XP1, XP2 rising edge delay from MCK	x1 mode	0		$t_{MCLK} \times 47/48$	ns
$t_{TR_P_x2}$		x2 mode	0		$t_{MCLK} \times 23/24$	ns
$t_{TR_P_x3}$		x4 mode	0		$t_{MCLK} \times 11/12$	ns
$t_{TF_P_x1}$	XP1, XP2 falling edge delay from MCK	x1 mode	0		$t_{MCLK} \times 47/48$	ns
$t_{TF_P_x2}$		x2 mode	0		$t_{MCLK} \times 23/24$	ns
$t_{TF_P_x3}$		x4 mode	0		$t_{MCLK} \times 11/12$	ns
t_{W_P1}	XP1, XP2 pulse width	x1 mode	2		$t_{MCLK} - 2$	ns
		x2 mode	2		$t_{MCLK} \times 1/2 - 2$	ns
		x4 mode	2		$t_{MCLK} \times 1/4 - 2$	ns

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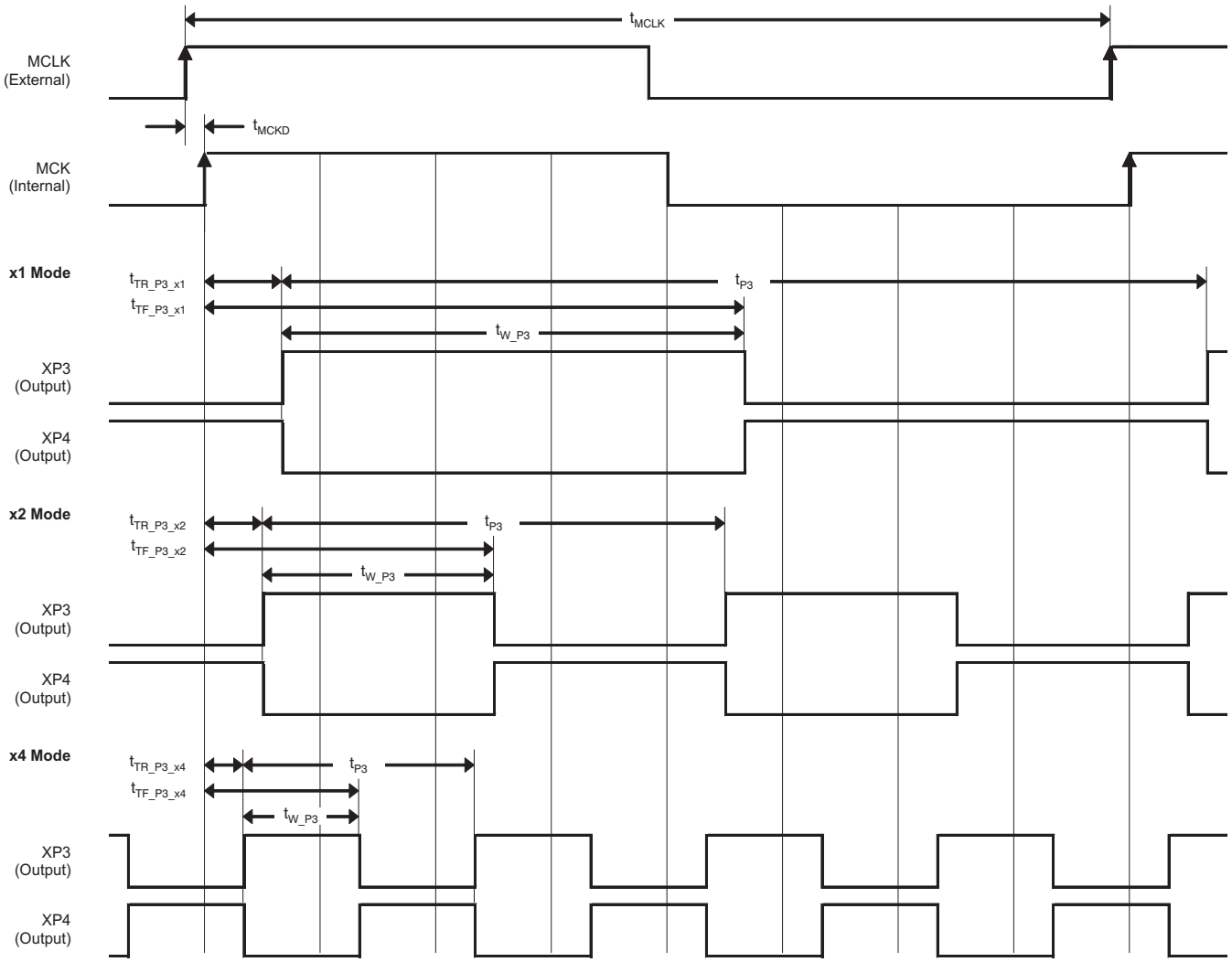


Figure 23. XP3 and XP4 Fast Transfer Clock Pulse Setting

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Table 15. Timing Requirements for Figure 23

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MCLK}	MCLK frequency	VSP5610	1		11.66	MHz
		VSP5611	1		16.66	MHz
		VSP5612	1		23.33	MHz
t_{MCLK}	MCLK period			$1/f_{MCLK}$		ns
t_{MCKD}	MCLK to MCK delay			2		ns
t_{P3}	XP3, XP4 period	x1 mode		t_{MCLK}		ns
		x2 mode		$t_{MCLK} \times 1/2$		ns
		x4 mode		$t_{MCLK} \times 1/4$		ns
$t_{TR_P3_x1}$	XP3, XP4 rising edge delay from MCK	x1 mode	0		$t_{MCLK} \times 47/48$	ns
$t_{TR_P3_x2}$		x2 mode	0		$t_{MCLK} \times 23/24$	ns
$t_{TR_P3_x3}$		x4 mode	0		$t_{MCLK} \times 11/12$	ns
$t_{TF_P3_x1}$	XP3, XP4 falling edge delay from MCK	x1 mode	0		$t_{MCLK} \times 47/48$	ns
$t_{TF_P3_x2}$		x2 mode	0		$t_{MCLK} \times 23/24$	ns
$t_{TF_P3_x3}$		x4 mode	0		$t_{MCLK} \times 11/12$	ns
t_{W_P3}	XP3, XP4 pulse width	x1 mode	2		$t_{MCLK} - 2$	ns
		x2 mode	2		$t_{MCLK} \times 1/2 - 2$	ns
		x4 mode	2		$t_{MCLK} \times 1/4 - 2$	ns

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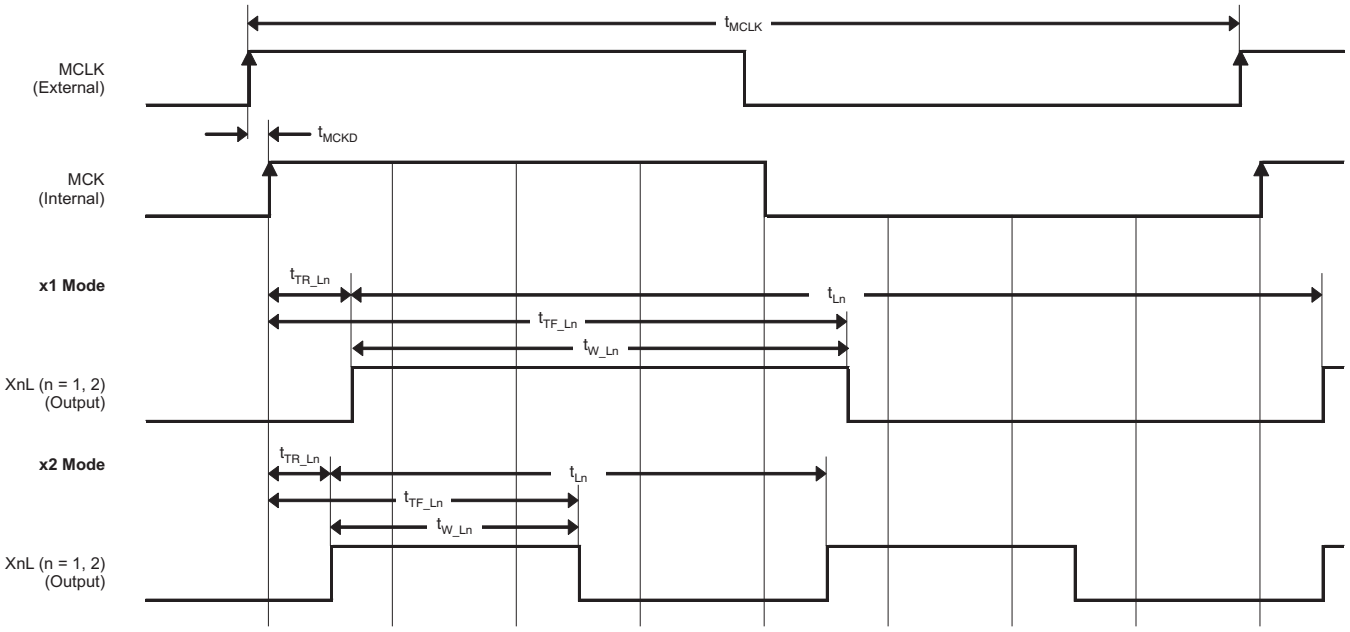


Figure 24. X1L and X2L Fast Transfer Clock Pulse Setting

Table 16. Timing Requirements for Figure 24

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MCLK}	MCLK frequency	VSP5610	1		11.66	MHz
		VSP5611	1		16.66	MHz
		VSP5612	1		23.33	MHz
t_{MCLK}	MCLK period			$1/f_{MCLK}$		ns
t_{MCKD}	MCLK to MCK delay			2		ns
t_{Ln}	XLn period (n = 1,2)	x1 mode		t_{MCLK}		ns
		x2 mode		$t_{MCLK} \times 1/2$		ns
t_{TR_Ln}	XLn rising edge delay from MCK (n = 1,2)	x1 mode	0		$t_{MCLK} \times 47/48$	ns
		x2 mode	0		$t_{MCLK} \times 23/24$	ns
t_{TF_Ln}	XLn falling edge delay from MCK (n = 1,2)	x1 mode	0		$t_{MCLK} \times 47/48$	ns
		x2 mode	0		$t_{MCLK} \times 23/24$	ns
t_{W_Ln}	XLn pulse width (n = 1,2)	x1 mode	2		$t_{MCLK} - 2$	ns
		x2 mode	2		$t_{MCLK} \times 1/2 - 2$	ns

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SERIAL INTERFACE

All device functions and settings are controlled through the serial interface. The serial interface consists of three signals (SCLK, SEN, and SDI) for register writing, and a fourth signal (SDO) for readback. SDO shares the terminal with the GPIO signal; thus, a register setting is required to activate the SDO function. Other signals are assigned to individual terminals.

Serial data are composed of 30 bits total, as shown in Figure 25. 10 bits are assigned for the register address and 20 bits for register data. The input serial data at SDI are sequentially stored in a shift register at the SCLK rising edge. Data shift operation is performed at the SCLK rising edges with SEN low. All 30 input data bits are loaded to a parallel latch in an internal register at the rising edge of SEN.

This device has two modes: read and write. The mode selection can be made via the SPL_RW internal register, located at bit 0 of address 0. SPL_RW = 0 implies a write mode and SPL_RW = 1 implies read mode.

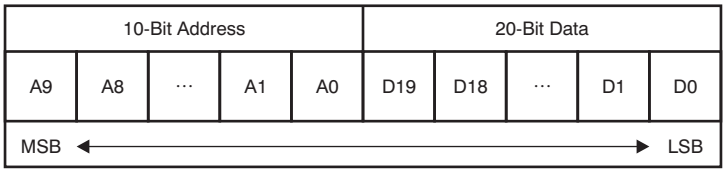


Figure 25. Serial I/F Data Format

WRITE MODE (SPI_RW = 0, Default)

Normally, one serial interface command is sent by one address and data combination. The address should be sent MSB first. Data are stored into the respective register, as indicated by the address. If the serial data at the end of the data stream are less than 30 bits, the last incomplete serial data are discarded. Figure 26 shows the SPI signal flow while in write mode.

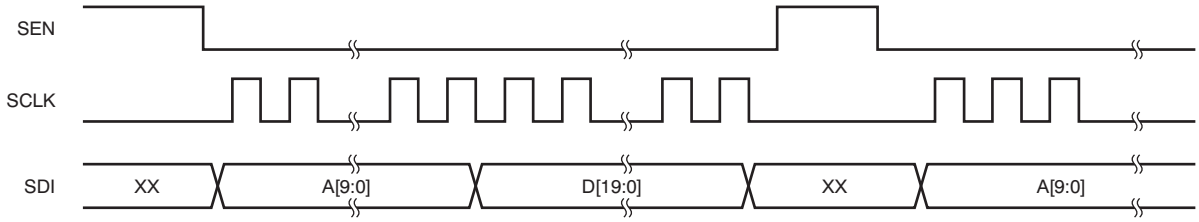


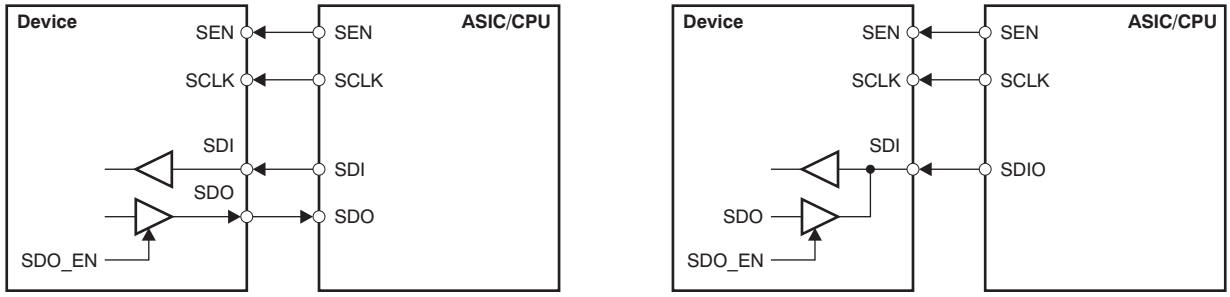
Figure 26. SPI Signal Flow of Write Mode

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READ MODE (SPI_RW = 1)

In read mode, two types of connections are possible between the AFE and external systems such as an ASIC or CPU. One connection is the four-wire connection in which the SDI and SDO pins are separately connected to the system as shown in Figure 27a.

The other connection is a three-wire connection in which only the SDI pin is connected to the bidirectional I/O port of the external system, as shown in Figure 27b. In this case, SDI_BUFF_CTRL should be set to '1' to create an SPI bidirectional port. The bit flow of the four-wire connection is shown in Figure 28. The bit flow of the three-wire connection is shown in Figure 29. As shown in Figure 29, SDI changes from an input to an output at the SCLK falling edge after the end of the A[9:0] input. Because the SDI port is always in pull down mode, the external pull down resistance is unnecessary.



a) Four-Wire Connection
SDI Input Port: SDI_BUFF_CTRL = 0

b) Three-Wire Connection
SDI Bidirectional Port: SDI_BUFF_CTRL = 1

Figure 27. SPI Connection Between AFE and System

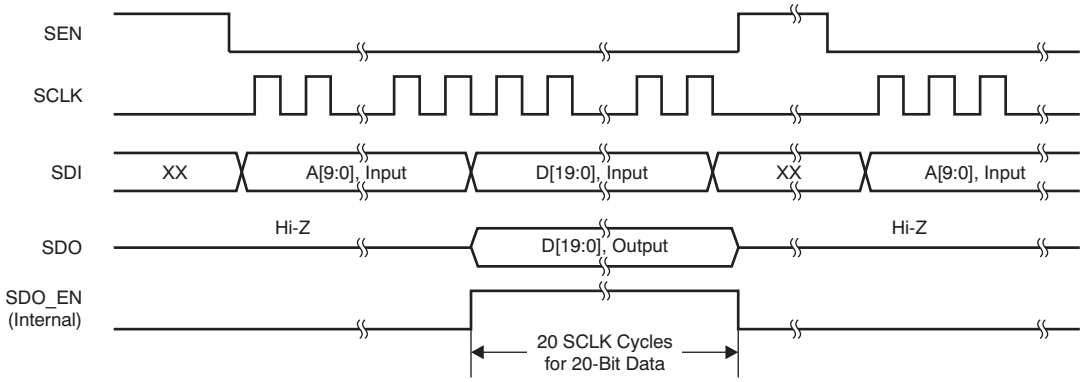


Figure 28. SPI Signal Flow of Read Mode for Four-Wire Connection

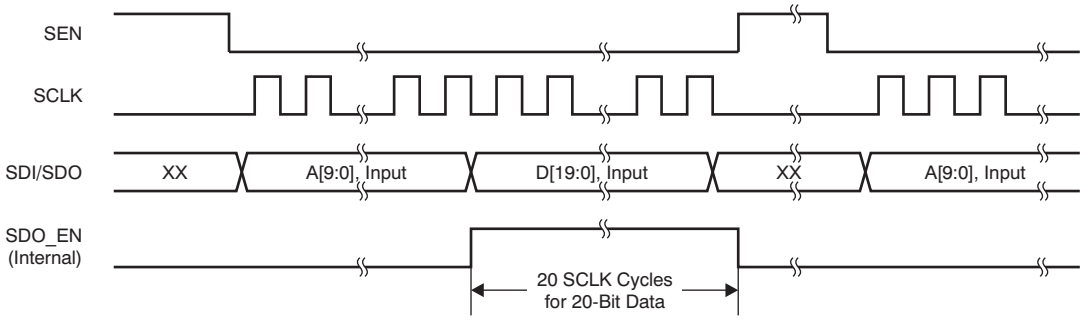


Figure 29. SPI Signal Flow of Read Mode for Three-Wire Connection

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VSP5610RSHR	ACTIVE	VQFN	RSH	56	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	0 to 85	VSP 5610	Samples
VSP5611RSHR	ACTIVE	VQFN	RSH	56	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	0 to 85	VSP 5611	Samples
VSP5612RSHR	ACTIVE	VQFN	RSH	56	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	0 to 85	VSP 5612	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

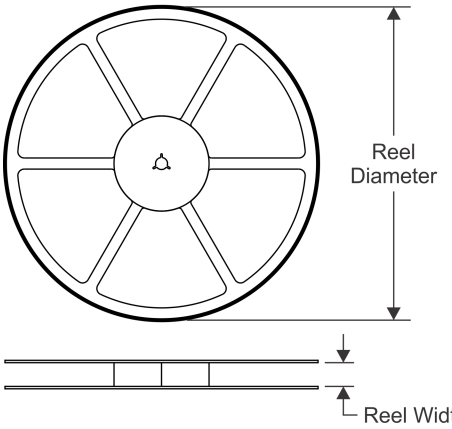
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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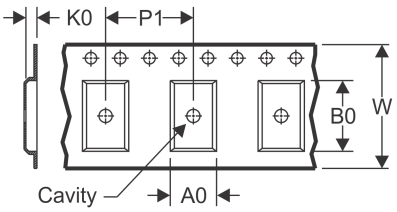
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

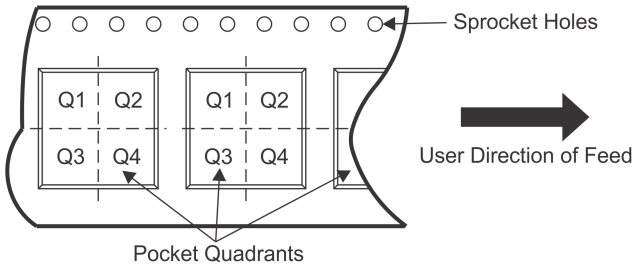


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

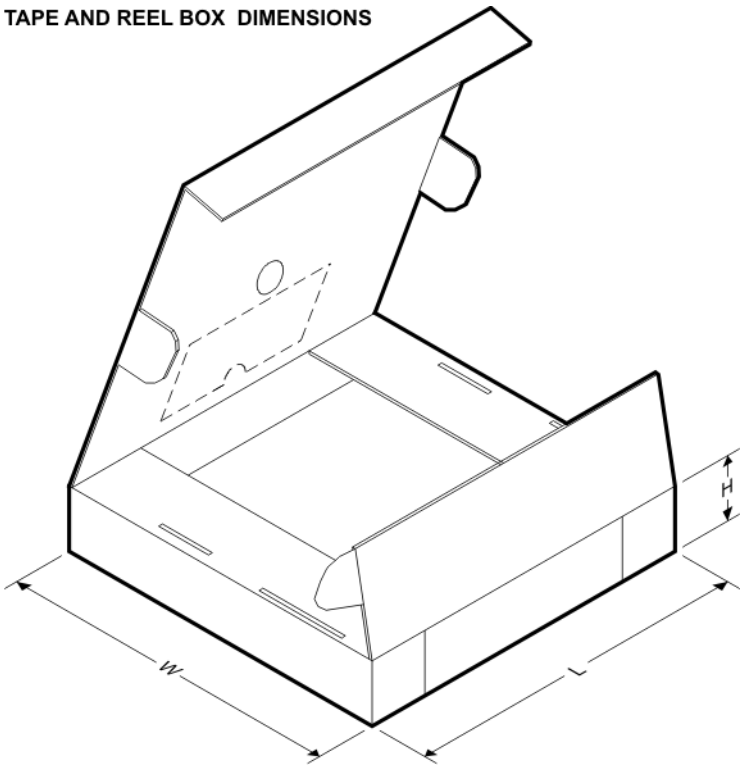
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VSP5610RSHR	VQFN	RSH	56	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
VSP5611RSHR	VQFN	RSH	56	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
VSP5612RSHR	VQFN	RSH	56	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

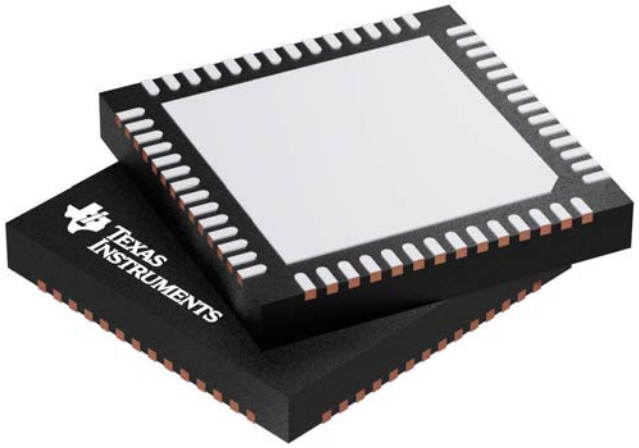
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VSP5610RSHR	VQFN	RSH	56	2500	367.0	367.0	38.0
VSP5611RSHR	VQFN	RSH	56	2500	367.0	367.0	38.0
VSP5612RSHR	VQFN	RSH	56	2500	367.0	367.0	38.0

GENERIC PACKAGE VIEW

RSH 56

VQFN - 1 mm max height

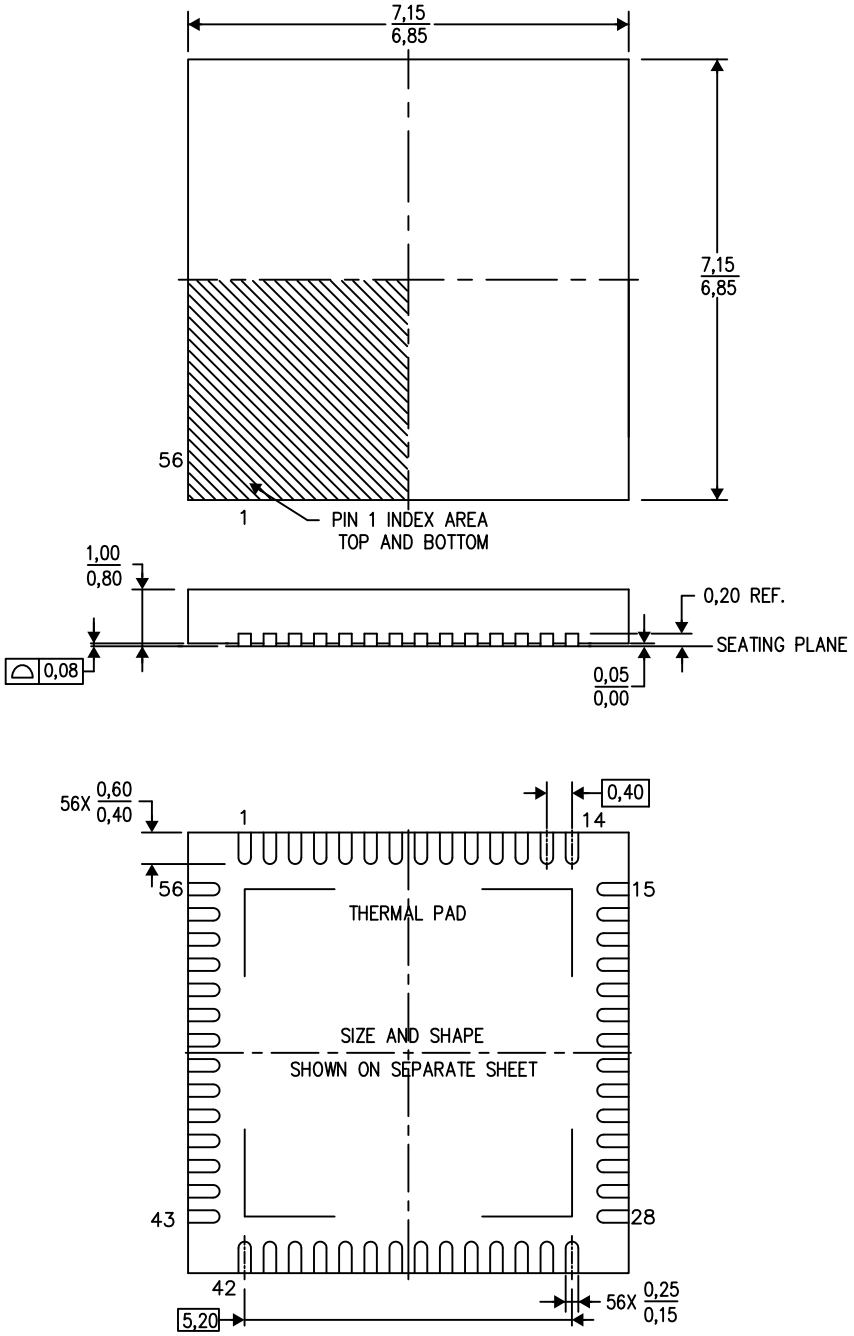
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207513/D

RSH (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

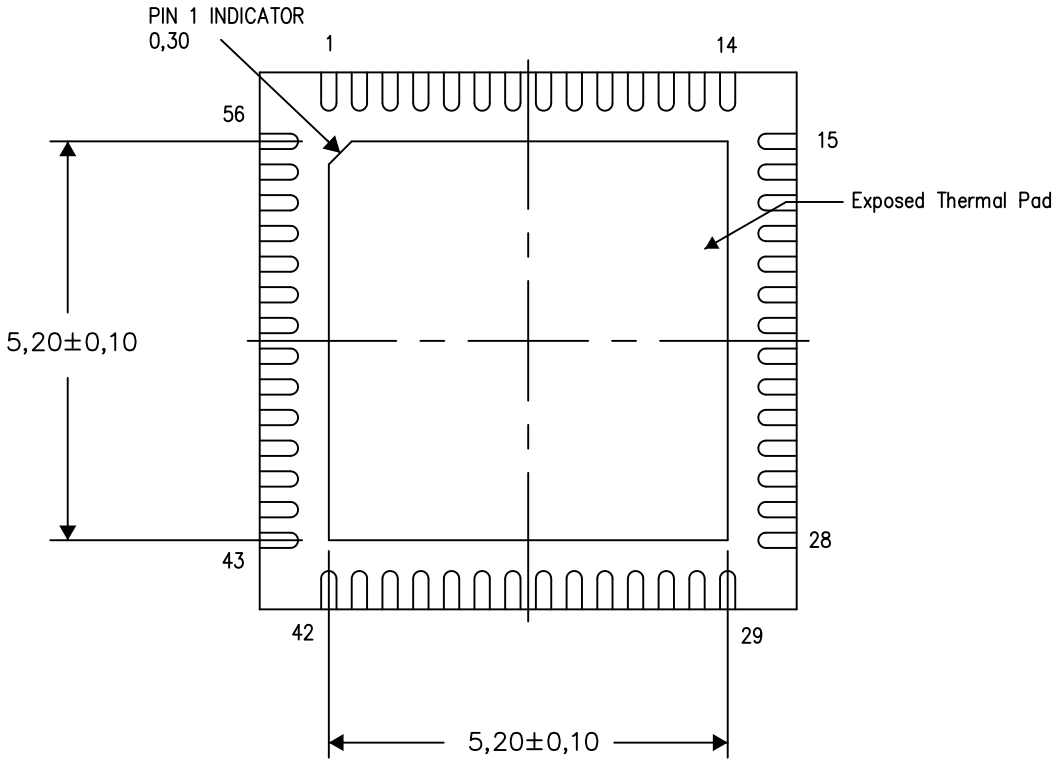
RSH (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



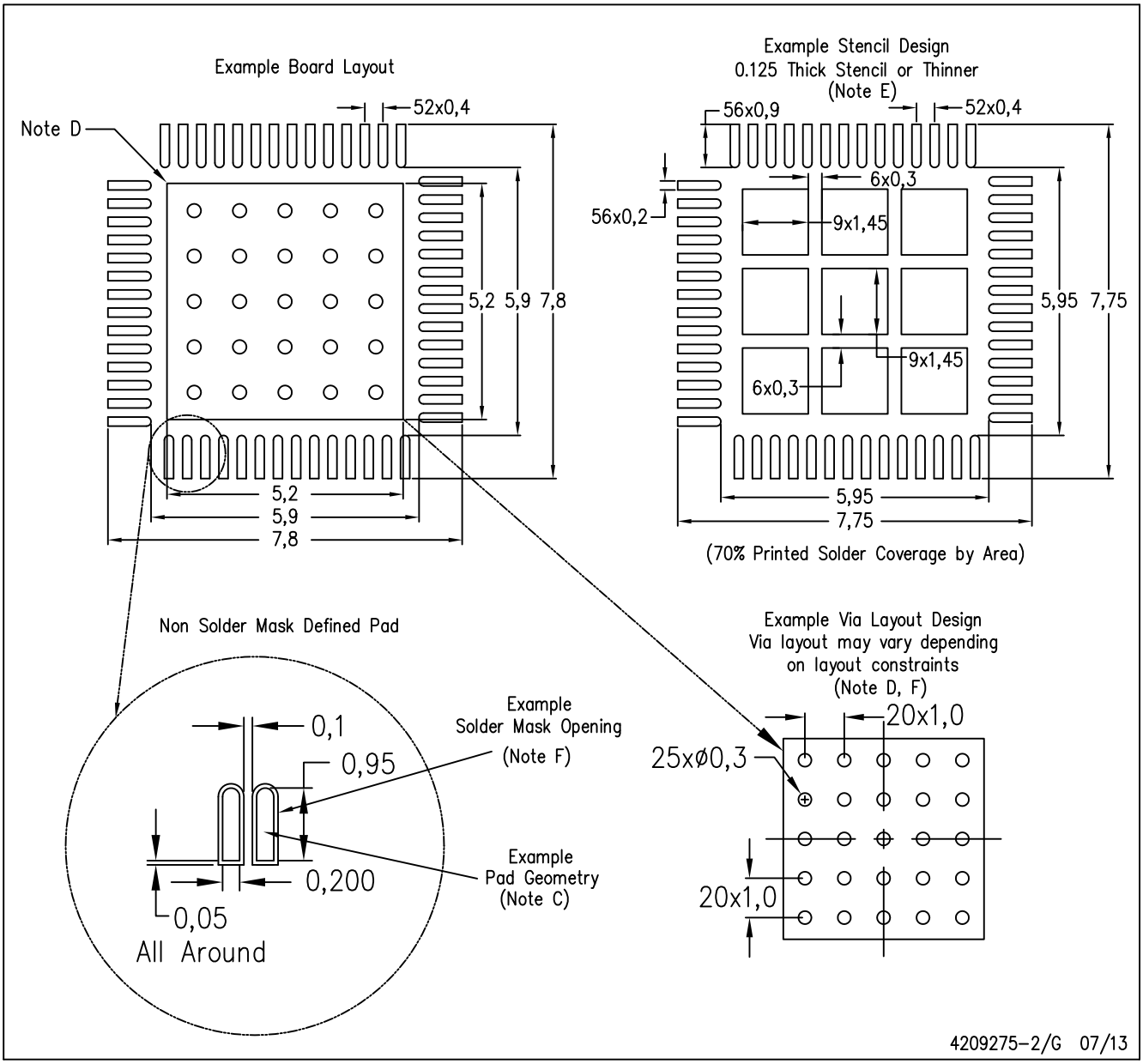
Bottom View

Exposed Thermal Pad Dimensions

4207553–2/I 07/13

NOTE: All linear dimensions are in millimeters

RSH (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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