

IttyBitty Low-Side MOSFET Driver

Features

- +4.5V to +18V Operation
- Low Steady-State Supply Current
 - 50 μ A Typical, Control Input Low
 - 370 μ A Typical, Control Input High
- 1.2A Nominal Peak Output
 - 3.5 Ω Typical Output Resistance at 18V Supply
 - 7.8 Ω Typical Output Resistance at 5V Supply
- 25 mV Maximum Output Offset from Supply or Ground
- Operates in Low-Side Switch Circuits
- TTL-Compatible Input Withstands -20V
- ESD Protection
- Inverting and Non-Inverting Versions

Applications

- Battery Conservation
- Solenoid and Motion Control
- Lamp Control
- Switch-Mode Power Supplies

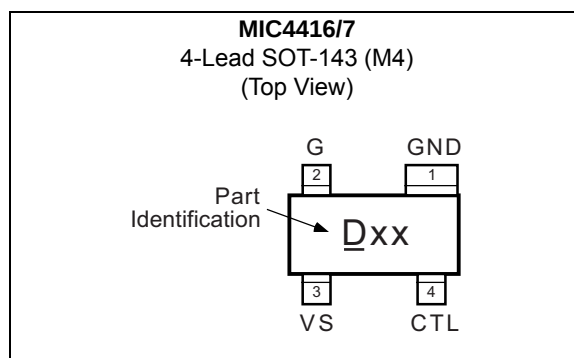
General Description

The MIC4416 and MIC4417 IttyBitty low-side MOSFET drivers are designed to switch an N-channel enhancement-type MOSFET from a TTL-compatible control signal in low-side switch applications. The MIC4416 is non-inverting and the MIC4417 is inverting. These drivers feature short delays and high peak current to produce precise edges and rapid rise and fall times. Their tiny 4-lead SOT-143 package uses minimal space.

The MIC4416/7 are powered from a +4.5V to +18 supply voltage. The on-state drive output voltage is approximately equal to the supply voltage (no internal regulators or clamps). High supply voltages, such as 10V, are appropriate for use with standard N-channel MOSFETs. Low supply voltages, such as 5V, are appropriate for use with logic-level N-channel MOSFETs.

In a low-side configuration, the drive can control a MOSFET that switches any voltage up to the rating of the MOSFET. The MIC4416/7 are available in the SOT-143 package and are rated for the -40°C to +85°C ambient temperature range.

Package Type



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_S)	+20V
Control Voltage (V_{CTL})	–20V to +20V
Gate Voltage (V_G)	+20V
Junction Temperature (T_J).....	+150°C
Lead Temperature (Soldering, 5 sec.).....	+260°C

Operating Ratings ††

Supply Voltage (V_S)	+4.5V to +18V
Control Voltage (V_{CTL})	0V to V_S
Ambient Temperature Range (T_A).....	–40°C to +85°C
Package Thermal Resistance	
SOT-143 (θ_{JA}) (Note 1)	220°C/W

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† **Notice:** The device is not guaranteed to function outside its operating ratings.

Note 1: Soldered to 0.25 in² copper ground plane.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Typical values at $T_A = +25^\circ\text{C}$. Minimum and maximum values indicate performance at $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$. Parts production tested at $+25^\circ\text{C}$. Devices are ESD protected, however handling precautions are recommended. [Note 1](#)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Current	I_S	—	50	200	μA	$4.5\text{V} \leq V_S \leq 18\text{V}$, $V_{CTL} = 0\text{V}$
		—	370	1500		$4.5\text{V} \leq V_S \leq 18\text{V}$, $V_{CTL} = 5\text{V}$
Control Input Voltage	V_{CTL}	—	—	0.8	V	$4.5\text{V} \leq V_S \leq 18\text{V}$, V_{CTL} for logic 0 input
		2.4	—	—		$4.5\text{V} \leq V_S \leq 18\text{V}$, V_{CTL} for logic 1 input
Control Input Current	I_{CTL}	-10	—	10	μA	$0\text{V} \leq V_{CTL} \leq V_S$
Delay Time, V_{CTL} Rising	t_D	—	42	—	ns	$V_S = 5\text{V}$, $C_L = 1000\text{ pF}$, Note 2
		—	33	60		$V_S = 18\text{V}$, $C_L = 1000\text{ pF}$, Note 2
Delay Time, V_{CTL} Falling	t_D	—	42	—	ns	$V_S = 5\text{V}$, $C_L = 1000\text{ pF}$, Note 2
		—	23	40		$V_S = 18\text{V}$, $C_L = 1000\text{ pF}$, Note 2
Output Rise Time	t_r	—	24	—	ns	$V_S = 5\text{V}$, $C_L = 1000\text{ pF}$, Note 2
		—	14	40		$V_S = 18\text{V}$, $C_L = 1000\text{ pF}$, Note 2
Output Fall Time	t_f	—	28	—	ns	$V_S = 5\text{V}$, $C_L = 1000\text{ pF}$, Note 2
		—	16	40		$V_S = 18\text{V}$, $C_L = 1000\text{ pF}$, Note 2
Gate Output Offset Voltage		—	-25	—	mV	$4.5\text{V} \leq V_S \leq 18\text{V}$, $V_G = \text{high}$
		—	25	—		$4.5\text{V} \leq V_S \leq 18\text{V}$, $V_G = \text{low}$
Output Resistance	R_O	—	7.6	—	Ω	$V_S = 5\text{V}$, $I_{OUT} = 10\text{ mA}$, P-channel (source) MOSFET
		—	7.8	—		$V_S = 5\text{V}$, $I_{OUT} = 10\text{ mA}$, N-channel (sink) MOSFET
		—	3.5	10	Ω	$V_S = 18\text{V}$, $I_{OUT} = 10\text{ mA}$, P-channel (source) MOSFET
		—	3.5	10		$V_S = 18\text{V}$, $I_{OUT} = 10\text{ mA}$, N-channel (sink) MOSFET
Gate Output Reverse Current		250	—	—	mA	No latch up.

Note 1: Specification for packaged product only.

2: Refer to “MIC4416 Timing Definitions” and “MIC4417 Timing Definitions” diagrams.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	-40	—	+125	°C	—
Ambient Storage Temperature	T_S	-65	—	+150	°C	—
Package Thermal Resistances						
Thermal Resistance, 3x3 DFN 12-Ld	θ_{JA}	—	60	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A , T_J , θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

Definitions

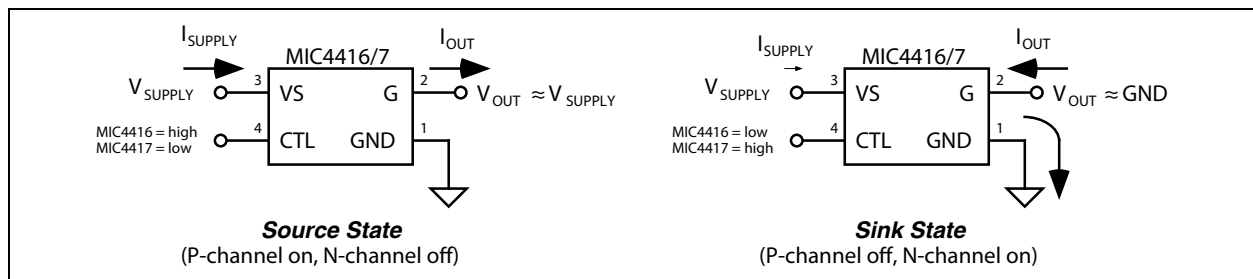


FIGURE 1-1: MIC4416/7 Operating States.

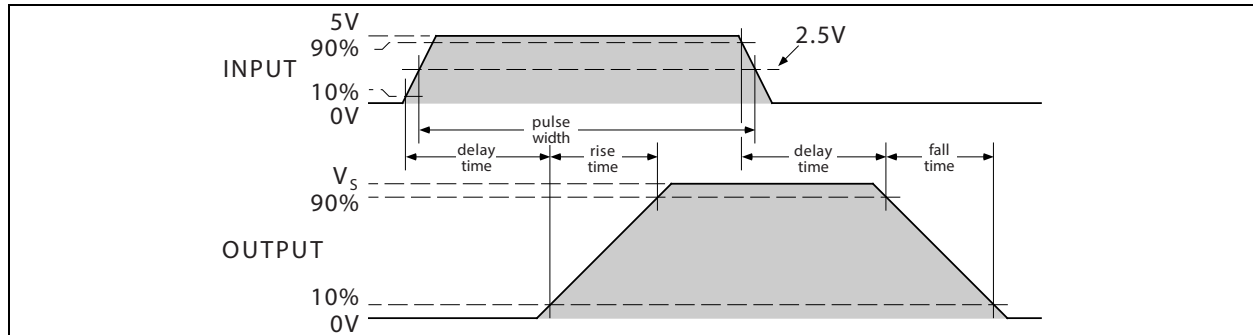


FIGURE 1-2: MIC4416 (Non-Inverting) Timing Definitions.

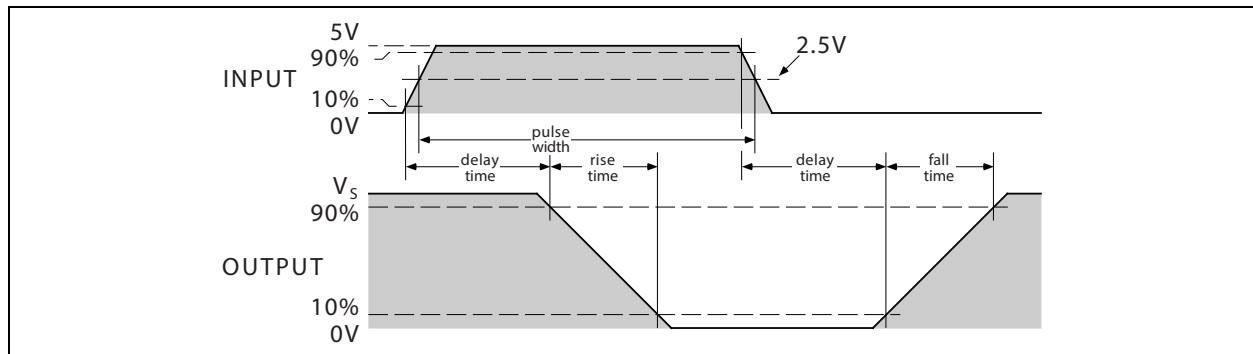


FIGURE 1-3: MIC4417 (Inverting) Timing Definitions.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Typical characteristics at $T_A = +25^\circ\text{C}$, $V_S = 5\text{V}$, $C_L = 1000\text{ pF}$ unless noted.

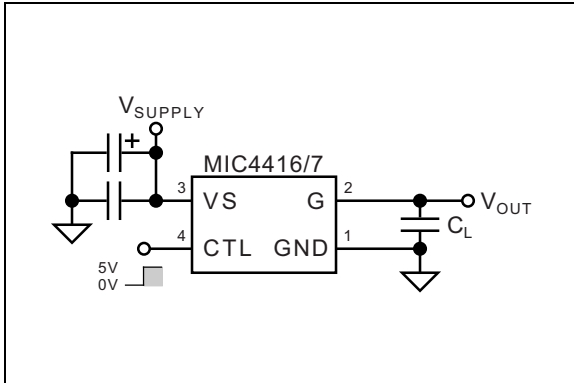


FIGURE 2-1: Test Circuit.

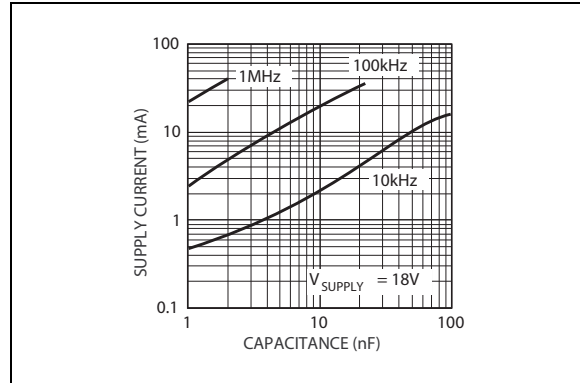


FIGURE 2-4: Supply Current vs. Load Capacitance.

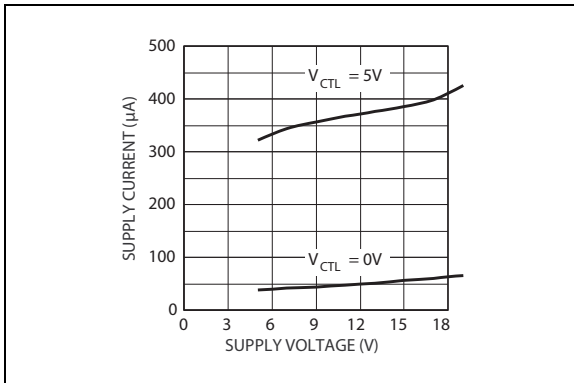


FIGURE 2-2: Quiescent Current vs. Supply Voltage.

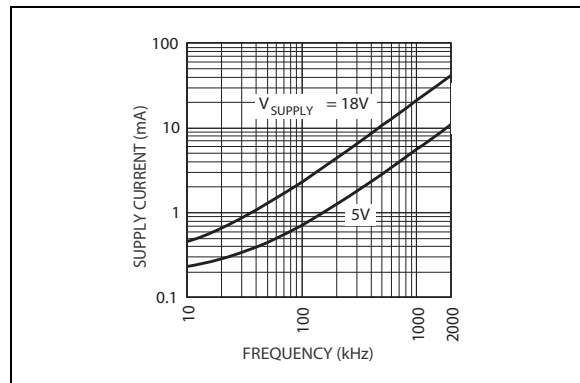


FIGURE 2-5: Supply Current vs. Frequency.

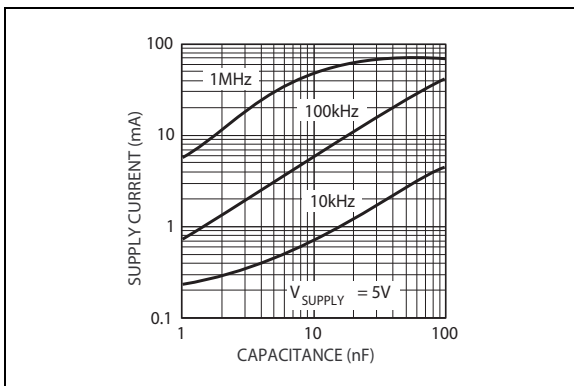


FIGURE 2-3: Supply Current vs. Load Capacitance.

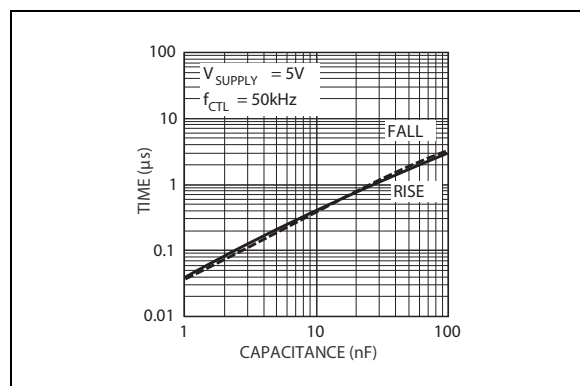


FIGURE 2-6: Output Rise and Fall Time vs. Load Capacitance.

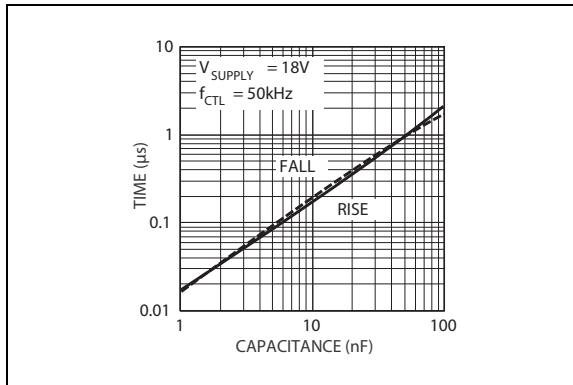


FIGURE 2-7: Output Rise and Fall Time vs. Load Capacitance.

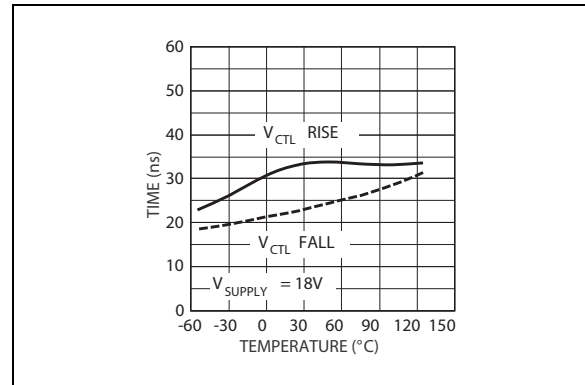


FIGURE 2-10: Delay Time vs. Temperature.

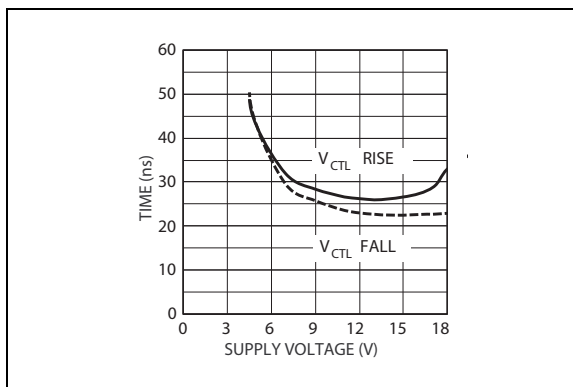


FIGURE 2-8: Delay Time vs. Supply Voltage.

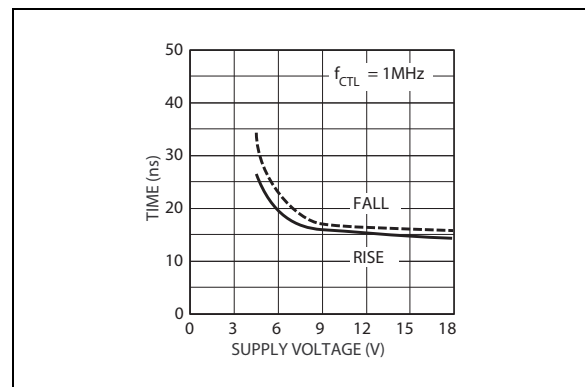


FIGURE 2-11: Rise and Fall Time vs. Supply Voltage.

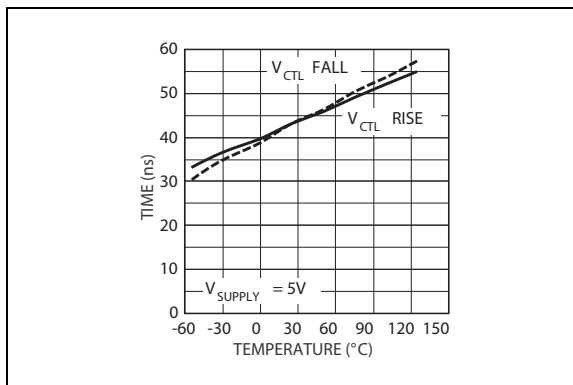


FIGURE 2-9: Delay Time vs. Temperature.

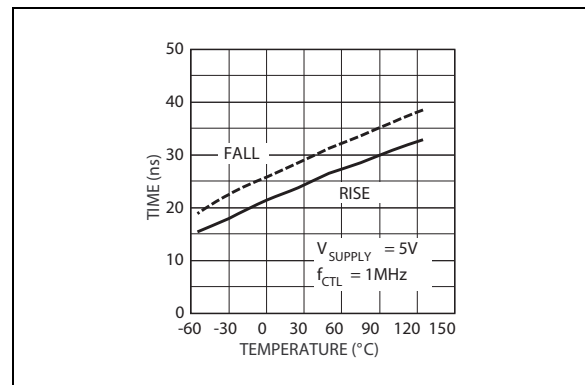


FIGURE 2-12: Rise and Fall Time vs. Temperature.

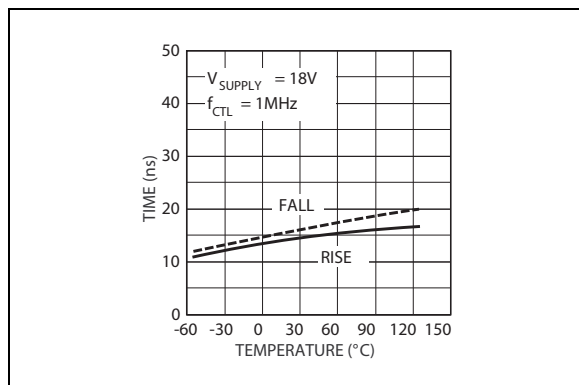


FIGURE 2-13: Rise and Fall Time vs. Temperature.

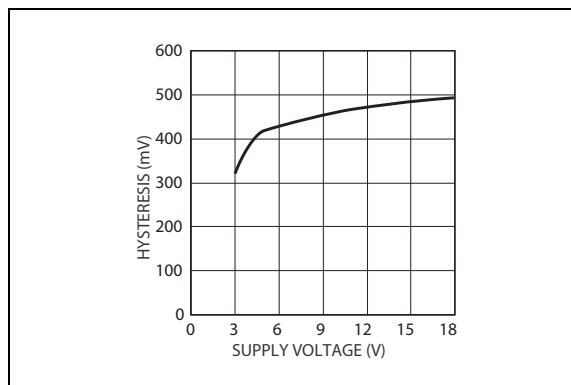


FIGURE 2-16: Control Input Hysteresis vs. Supply Voltage.

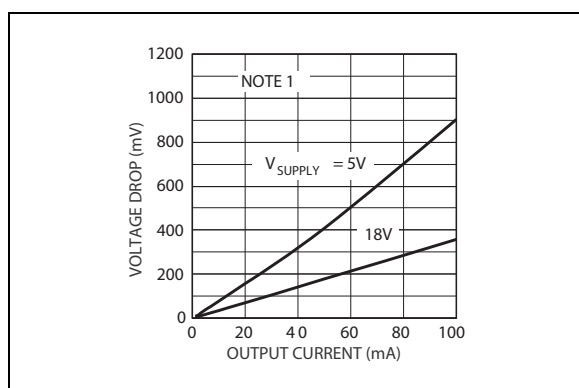


FIGURE 2-14: Output Voltage Drop vs. Output Source Current ([Note 1](#)).

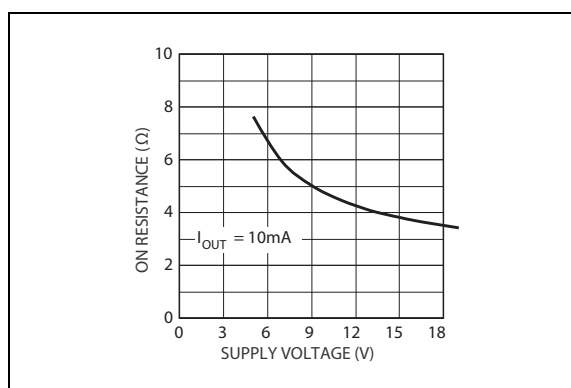


FIGURE 2-17: Output Source Resistance.

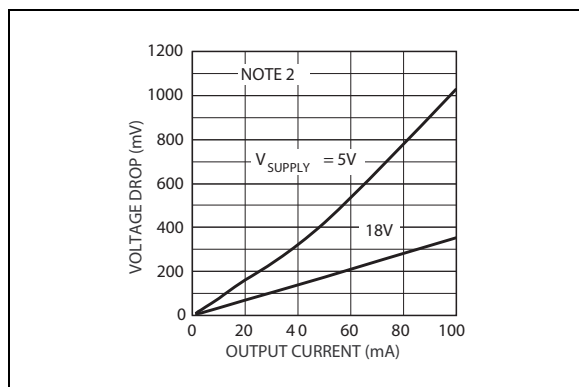


FIGURE 2-15: Output Voltage Drop vs. Output Sink Current ([Note 2](#)).

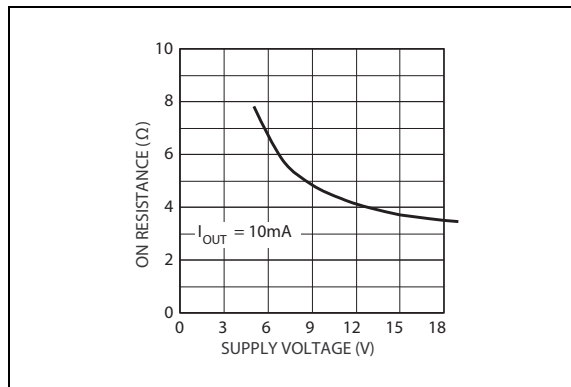


FIGURE 2-18: Output Sink Resistance.

Note 1: Source-to-drain voltage drop across the internal P-Channel MOSFET is $V_S - V_G$.

2: Source-to-drain voltage drop across the internal N-Channel MOSFET is $V_G - V_{GND}$ (Voltage applied to G).

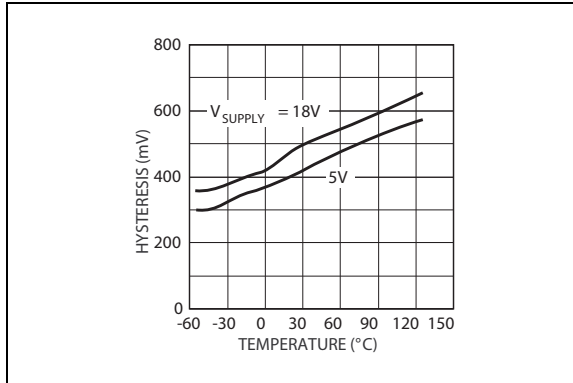


FIGURE 2-19: Control Input Hysteresis vs. Temperature.

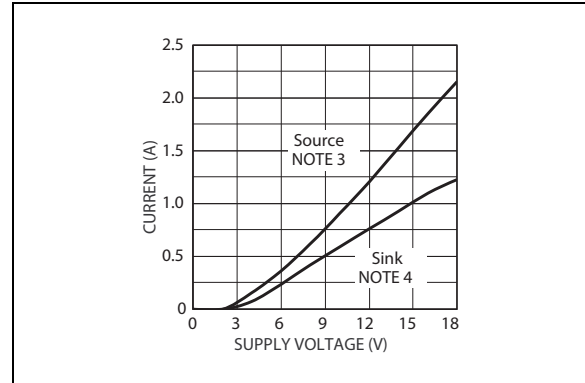


FIGURE 2-22: Peak Output Current vs. Supply Voltage (Note 3, Note 4).

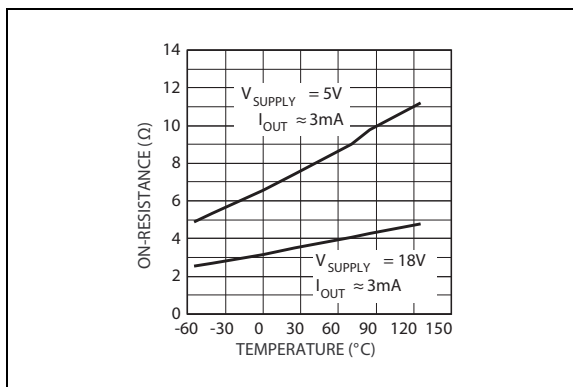


FIGURE 2-20: Output Source Resistance vs. Temperature.

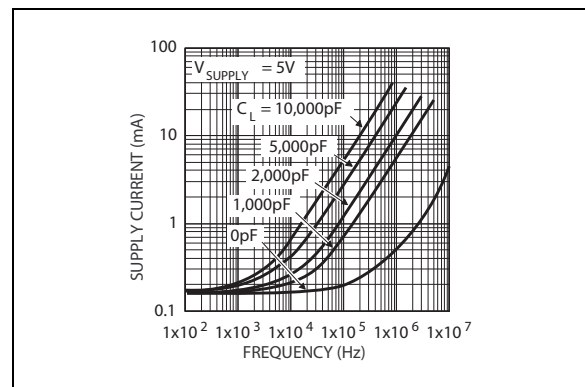


FIGURE 2-23: Supply Current vs. Frequency.

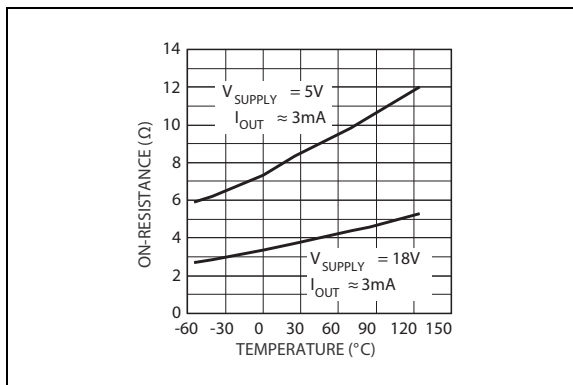


FIGURE 2-21: Output Sink Resistance vs. Temperature.

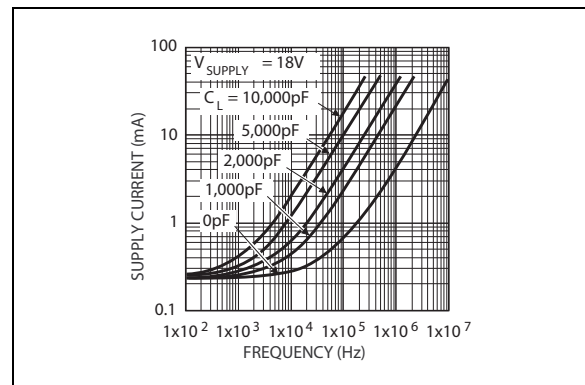


FIGURE 2-24: Supply Current vs. Frequency.

- 3:** 1 μ s pulse test, 50% duty cycle. OUT connected to GND. OUT sources current. (MIC4416, $V_{CTL} = 5V$; MIC4417, $V_{CTL} = 0V$).
- 4:** 1 μ s pulse test, 50% duty cycle. VS connected to OUT. OUT sinks current. (MIC4416, $V_{CTL} = 0V$; MIC4417, $V_{CTL} = 5V$).

MIC4416/7

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	GND	Ground. Power return.
2	G	Gate (output): Gate connection to external MOSFET.
3	VS	Supply (input): +4.5V to +18V supply.
4	CTL	Control (input): TTL-compatible on/off control input. MIC4416 only: Logic high forces the gate output to the supply voltage. Logic low forces the gate output to ground. MIC4417 only: Logic high forces the gate output to ground. Logic low forces the gate output to the supply voltage.

4.0 FUNCTIONAL DESCRIPTION

Refer to the [Functional Block Diagram](#).

The MIC4416 is a non-inverting driver. A logic high on the CTL (control) input produces gate drive output. The MIC4417 is an inverting driver. A logic low on the CTL (control) input produces gate drive output. The G (gate) output is used to turn on an external N-channel MOSFET.

4.1 Supply

VS (supply) is rated for +4.5V to +18V. External capacitors are recommended to decouple noise.

4.2 Control

CTL (control) is a TTL-compatible input. CTL must be forced high or low by an external signal. A floating input will cause unpredictable operation.

A high input turns on Q1, which sinks the output of the 0.3 mA and the 0.6 mA current source, forcing the input of the first inverter low.

4.3 Hysteresis

The control threshold voltage, when CTL is rising, is slightly higher than the control threshold voltage when CTL is falling.

When CTL is low, Q2 is on, which applies the additional 0.6 mA current source to Q1. Forcing CTL high turns on Q1 which must sink 0.9 mA from the two current sources. The higher current through Q1 causes a larger drain-to-source voltage drop across Q1. A slightly higher control voltage is required to pull the input of the first inverter down to its threshold.

Q2 turns off after the first inverter output goes high. This reduces the current through Q1 to 0.3 mA. The lower current reduces the drain-to-source voltage drop across Q1. A slightly lower control voltage will pull the input of the first inverter up to its threshold.

4.4 Drivers

The second (optional) inverter permits the driver to be manufactured in inverting and non-inverting versions.

The last inverter functions as a driver for the output MOSFETs Q3 and Q4.

4.5 Gate Output

G (gate) is designed to drive a capacitive load. V_G (gate output voltage) is either approximately the supply voltage or approximately ground, depending on the logic state applied to CTL.

If CTL is high, and VS (supply) drops to zero, the gate output will be floating (unpredictable).

4.6 ESD Protection

D1 protects VS from negative ESD voltages. D2 and D3 clamp positive and negative ESD voltages applied to CTL. R1 isolates the gate of Q1 from sudden changes on the CTL input. D4 and D5 prevent Q1's gate voltage from exceeding the supply voltage or going below ground.

5.0 APPLICATION INFORMATION

The MIC4416/7 is designed to provide high peak current for charging and discharging capacitive loads. The 1.2A peak value is a nominal value determined under specific conditions. This nominal value is used to compare its relative size to other low-side MOSFET drivers. The MIC4416/7 is not designed to directly switch 1.2A continuous loads.

5.1 Supply Bypass

Capacitors from VS to GND are recommended to control switching and supply transients. Load current and supply lead length are some of the factors that affect capacitor size requirements.

A 4.7 μF or 10 μF tantalum capacitor is suitable for many applications. Low-ESR (equivalent series resistance) metalized film capacitors may also be suitable. An additional 0.1 μF ceramic capacitor is suggested in parallel with the larger capacitor to control high-frequency transients.

The low ESR of tantalum capacitors makes them especially effective, but also makes them susceptible to uncontrolled inrush current from low impedance voltage sources (such as NiCd batteries or automatic test equipment). Avoid instantaneously applying voltage capable of very high peak current directly to or near tantalum capacitors without additional current limiting. Normal power supply turn-on (slow rise time) or printed circuit trace resistance is usually adequate for normal product usage.

5.2 Circuit Layout

Avoid long power supply and ground traces. They exhibit inductance that can cause voltage transients (inductive kick). Even with resistive loads, inductive transients can sometimes exceed the ratings of the MOSFET and the driver.

When a load is switched off, supply lead inductance forces current to continue flowing—resulting in a positive voltage spike. Inductance in the ground (return) lead to the supply has similar effects, except the voltage spike is negative.

Switching transitions momentarily draw current from VS to GND. This combines with supply lead inductance to create voltage transients at turn on and turn off.

Transients can also result in slower apparent rise or fall times when the driver's ground shifts with respect to the control input.

Minimize the length of supply and ground traces or use ground and power planes when possible. Bypass capacitors should be placed as close as practical to the driver.

5.3 MOSFET Selection

5.3.1 STANDARD MOSFET

A standard N-channel power MOSFET is fully enhanced with a gate-to-source voltage of approximately 10V and has an absolute maximum gate-to-source voltage of $\pm 20\text{V}$.

The MIC4416/7's on-state output is approximately equal to the supply voltage. The lowest usable voltage depends upon the behavior of the MOSFET.

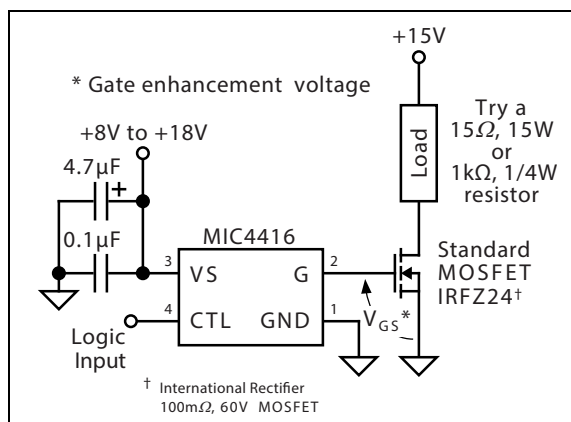


FIGURE 5-1: Using a Standard MOSFET.

5.3.2 LOGIC-LEVEL MOSFET

Logic-level N-channel power MOSFETs are fully enhanced with a gate-to-source voltage of approximately 5V and have an absolute maximum gate-to-source voltage of $\pm 10\text{V}$. They are less common and generally more expensive.

The MIC4416/7 can drive a logic-level MOSFET if the supply voltage, including transients, does not exceed the maximum MOSFET gate-to-source rating (10V).

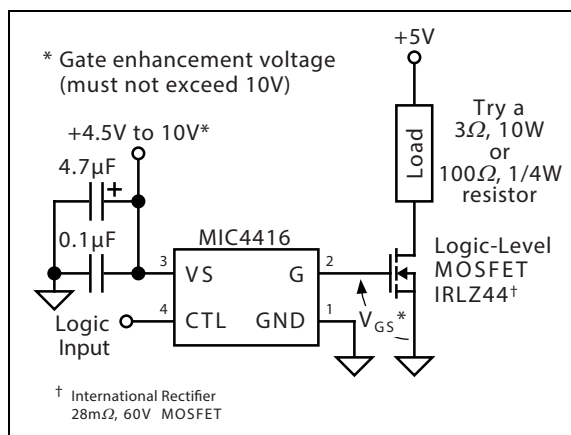


FIGURE 5-2: Using a Logic-Level MOSFET.

At low voltages, the MIC4416/7's internal P- and N-channel MOSFET's on-resistance will increase and slow the output rise time. Refer to the [Typical Performance Curves](#) graphs.

5.4 Inductive Loads

Switching off an inductive load in a low-side application forces the MOSFET drain higher than the supply voltage (as the inductor resists changes to current). To prevent exceeding the MOSFET's drain-to-gate and drain-to-source ratings, a Schottky diode should be connected across the inductive load.

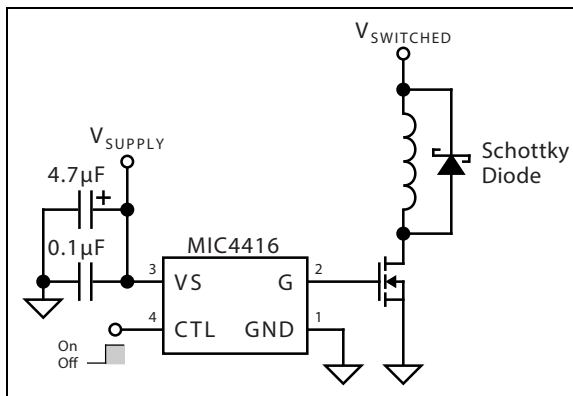


FIGURE 5-3: Switching an Inductive Load.

5.5 Power Dissipation

The maximum power dissipation must not be exceeded to prevent die meltdown or deterioration.

Power dissipation in on/off switch applications is negligible.

Fast repetitive switching applications, such as SMPS (switch mode power supplies), cause a significant increase in power dissipation with frequency. Power is dissipated each time current passes through the internal output MOSFETs when charging or discharging the external MOSFET. Power is also dissipated during each transition when some current momentarily passes from VS to GND through both internal MOSFETs.

Power dissipation is the product of supply voltage and supply current:

EQUATION 5-1:

$$P_D = V_S \times I_S$$

Where:

P_D = Power dissipation (in watts)

V_S = Supply voltage (in volts)

I_S = Supply current (in amps)

Supply current is a function of supply voltage, switching frequency, and load capacitance. Determine this value from [Figure 2-23](#) and [Figure 2-24](#) or measure it in the actual application.

Do not allow P_D to exceed $P_{D(MAX)}$.

T_J (junction temperature) is the sum of T_A (ambient temperature) and the temperature rise across the thermal resistance of the package. In another form:

EQUATION 5-2:

$$P_{D(MAX)} \leq \frac{150 - T_A}{220}$$

Where:

$P_{D(MAX)}$ = Maximum power dissipation (in watts)

150 = Maximum junction temperature (in °C)

T_A = Ambient temperature (in °C)

220 = Package thermal resistance (in °C/W)

Maximum power dissipation at 20°C with the driver soldered to a 0.25 in² ground plane is approximately 600 mW.

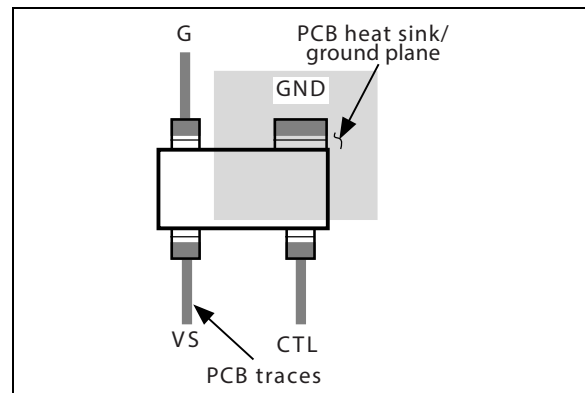


FIGURE 5-4: Heat Sink Plane.

The SOT-143 package θ_{JA} (junction-to-ambient thermal resistance) can be improved by using a heat sink larger than the specified 0.25 in² ground plane. Significant heat transfer occurs through the large (GND) lead. This lead is an extension of the paddle to which the die is attached.

5.6 High Frequency Operation

Although the MIC4416/7 driver will operate at frequencies greater than 1 MHz, the MOSFET's capacitance and the load will affect the output waveform (at the MOSFET's drain).

For example, an MIC4416/IRL3103 test circuit using a 47Ω 5W load resistor will produce an output waveform that closely matches the input signal shape up to about 500 kHz. The same test circuit with a 1 kΩ load resistor operates only up to about 25 kHz before the MOSFET source waveform shows significant change.

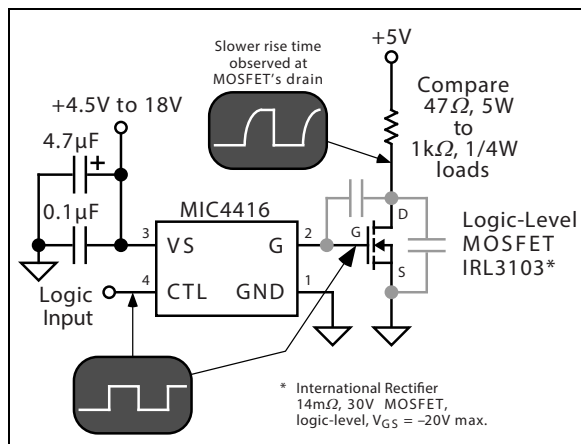


FIGURE 5-5: MOSFET Capacitance Effect at High Switching Frequency.

When the MOSFET is driven off, the slower rise occurs because the MOSFET's output capacitance recharges through the load resistance (RC circuit). A lower load resistance allows the output to rise faster. For the fastest driver operation, choose the smallest power MOSFET that will safely handle the desired voltage, current, and safety margin. The smallest MOSFETs generally have the lowest capacitance.

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

4-Lead SOT-143*

Example

<u>XXX</u> NNN

<u>D10</u> 287

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

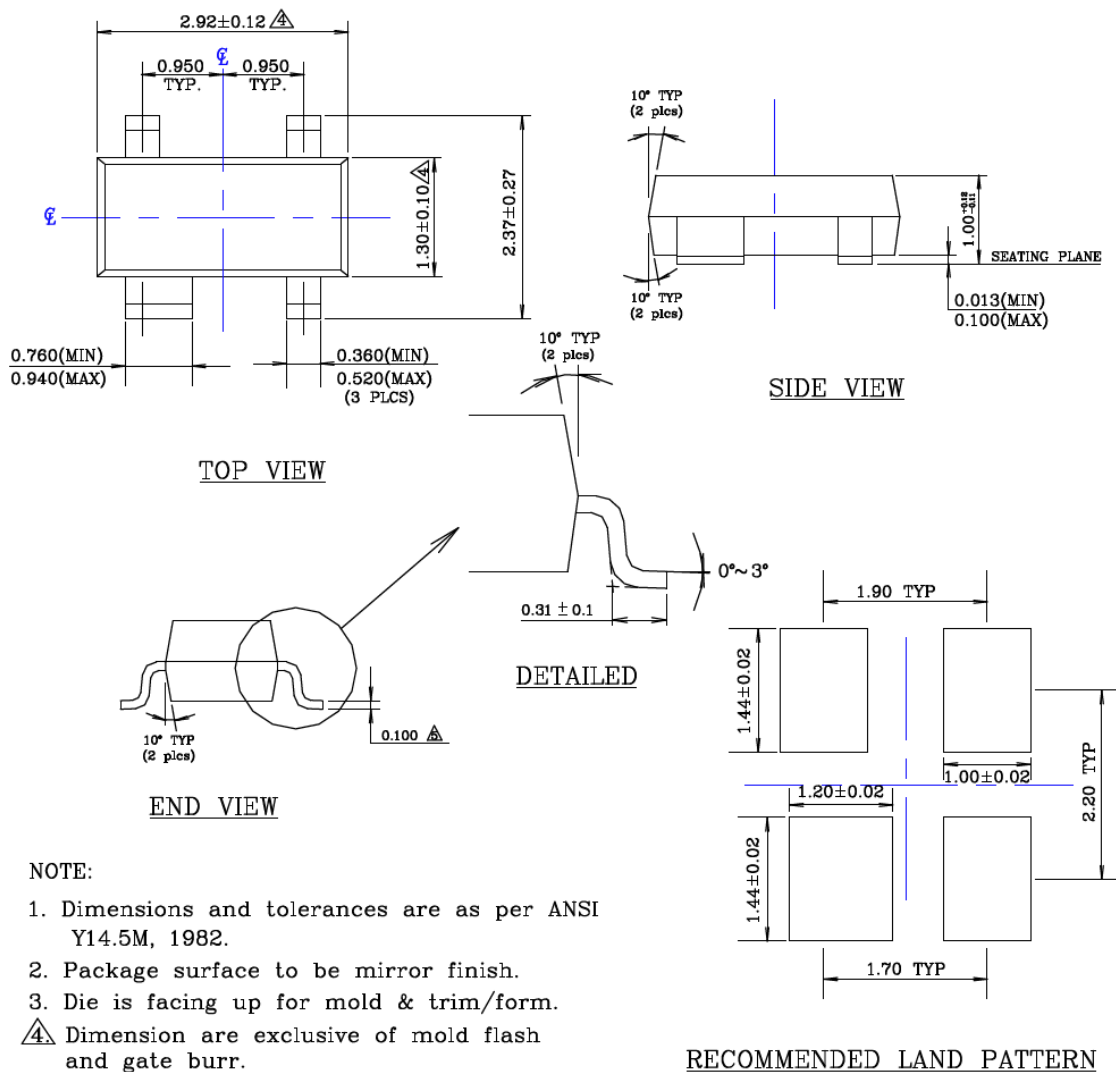
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. Underbar () and/or Overbar () symbol may not be to scale.	
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4-Lead SOT-143 Package Outline & Recommended Land Pattern

TITLE

4 LEAD SOT143 PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOT143-4LD-PL-1	UNIT	MM
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NOTE:

1. Dimensions and tolerances are as per ANSI Y14.5M, 1982.
2. Package surface to be mirror finish.
3. Die is facing up for mold & trim/form.
4. Δ Dimension are exclusive of mold flash and gate burr.
5. Δ Dimension are exclusive of solder plating.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

APPENDIX A: REVISION HISTORY

Revision A (October 2018)

- Converted Micrel document MIC4416/7 to Microchip data sheet template DS20006077A.
- Minor grammatical text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	<u>X</u>	<u>XX</u>	<u>-XX</u>
Part No.	Junction Temp. Range	Package	Media Type
Device:	MIC4416:	IttyBitty Low-Side Non-Inverting MOSFET Driver	
	MIC4417:	IttyBitty Low-Side Inverting MOSFET Driver	
Junction Temperature Range:	Y =	-40°C to +85°C, RoHS-Compliant	
Package:	M4 =	4-Lead SOT-143	
Media Type:	TR =	3,000/Reel	

Examples:

a) MIC4416YM4-TR: MIC4416, -40°C to +85°C Temperature Range, 4-Lead SOT-143, 3,000/Reel

b) MIC4417YM4-TR: MIC4417, -40°C to +85°C Temperature Range, 4-Lead SOT-143, 3,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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ISBN: 978-1-5224-3586-0

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