AND9012/D

A5191HRTNGEVB User Manual

Prepared by: Koenraad Van den Eeckhout
ON Semiconductor

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APPLICATION NOTE

Introduction

The A5191HRTNGEVB evaluation board includes all external components needed for operating the A5191HRT IC and demonstrates the small PCB surface area such an implementation requires. The EVB allows easy design of HART implementations using A5191HRT.

Overview

The A5191HRT is a single−chip, CMOS modem for use in highway addressable remote transducer (HART) field instruments and masters. The modem and a few external passive components provide all of the functions needed to satisfy HART physical layer requirements including modulation, demodulation, receive filtering, carrier detect, and transmit−signal shaping.

The A5191HRT uses phase continuous frequency shift keying (FSK) at 1200 bits per second. To conserve power the receive circuits are disabled during transmit operations and vice versa. This provides the half−duplex operation used in HART communications.

Features

- Single−chip, Half−duplex 1200 Bits per Second FSK Modem
- Bell 202 Shift Frequencies of 1200 Hz and 2200 Hz
- 3.0 V – 5.5 V Power Supply
- Transmit−signal Wave Shaping
- Receive Band−pass Filter
- Low Power: Optimal for Intrinsically Safe Applications
- Compatible with 3.3 V or 5 V microcontroller
- Internal Oscillator Requires 460.8 kHz Crystal or Ceramic Resonator
- Meets HART Physical Layer Requirements
- Industrial Temperature Range of −40°C to +85°C
- Available in 28−pin PLCC, 32−pin QFN and 32−pin LQFP Packages

Applications

- HART multiplexers
- HART Modem Interfaces
- 4 – 20 mA Loop Powered Transmitters

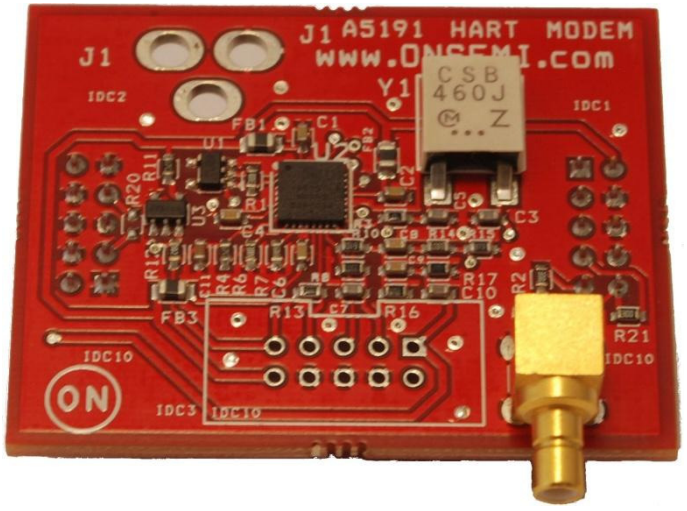


Figure 1. The A5191HRTNGEVB Evaluation Board

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ELECTRICAL CHARACTERISTICS

Table 1. ELECTRICAL CHARACTERISTICS OF THE A5191HRTNGEVB BOARD

Symbol	Parameter / Condition	Value			Unit
		Min	Typ	Max	
V_{DD}	Supply voltage	2.78	3	6.00	V
CURRENT CONSUMPTION					
I_{DD}	V_{DD} = 2.78V, idle		417		μA
I_{DD}	V_{DD} = 3.00 V, idle		420		μA
I_{DD}	V_{DD} = 6.00V, idle		780		μA
I_{DD}	External clock, V_{DD} = 3.00 V, idle		350		μA
TRANSMITTED FREQUENCY					
f_M	Mark “1”		1197		Hz
f_S	Space “0”		2194		Hz
LEVELS					
V_{TxA}	Amplitude Transmit Output		500		mV_{pp}
V_{CD}	Carrier Detect Level		110		mV_{pp}
REFERENCE VOLTAGES					
V_{AREF}	AREF		1.212		V
V_{CDREF}	CDREF		1.128		V

A5191HRT DESCRIPTION

The A5191HRT modem is a single−chip CMOS modem for use in HART field instruments and masters. It includes on−chip oscillator and a modulator and demodulator module communicating with a UART without internal buffer. The A5191HRT requires some external filter components and a 460.8 kHz clock source. This clock source can either be the interface oscillator by using a crystal or ceramic resonator, or an external clock signal.

When the device is transmitting data, the receive module is shut down and vice versa to conserve power. With simple power−saving maneuvers, the IC can be made to operate with a current consumption of as little as 250 μA. For more information related to this subject a Design Note “A5191HRT Design for Low−Power Environments” will be released shortly.

TEST AND MEASUREMENT TOOLS

Listed below are the tools used to acquire the values presented in this application note.

Oscilloscope	Tektronix DPO4034 350 MHz
Signal Generator	Agilent 33120A
Network Analyzer	AP Instruments 300

A5191HRTNGEVB DESCRIPTION

Schematic Diagram – BOM List

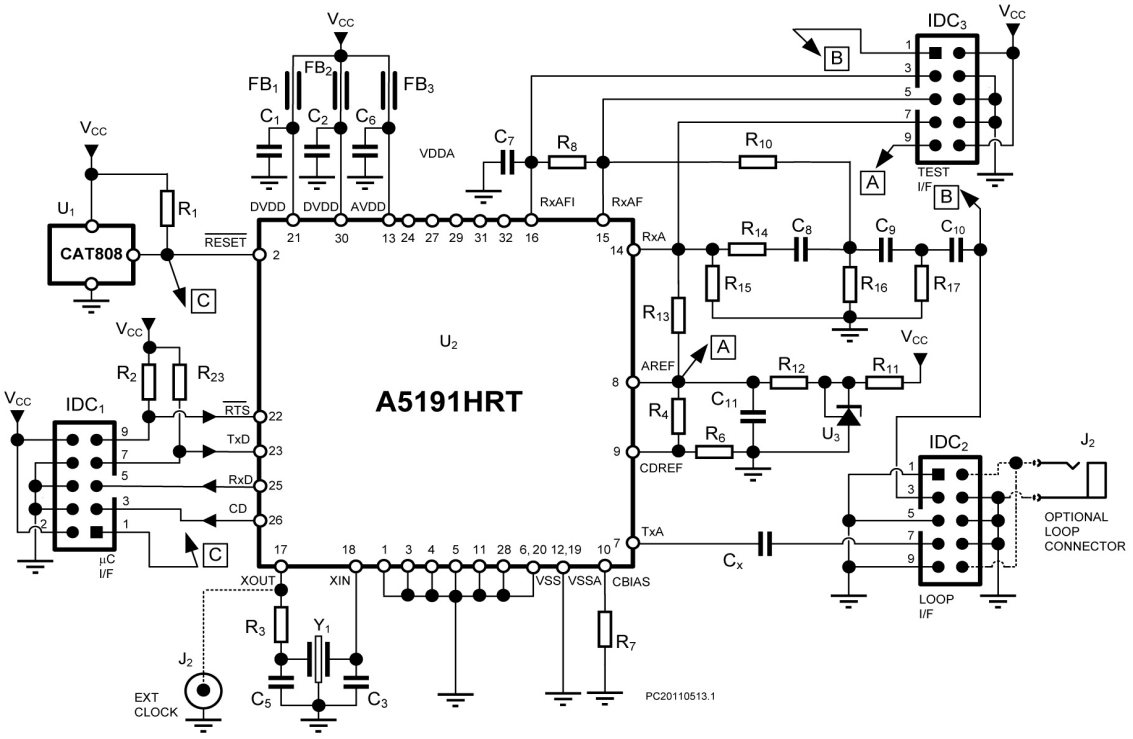


Figure 2. Schematic of A5191HRTNEVB

Table 2. A5191HRTNEVB BILL OF MATERIALS

Quantity	Reference	Value; Size	Manufacturer & Comments
4	C1, C2, C4, C6	100 nF, 0603	
3	C3, C5, C7	220 pF, 0603	
2	C8, C9	1 nF, 0603	
2	C10, C11	470 pF, 0603	
3	FB1, FB2, FB3	600Z, 0805	
3	IDC1, IDC2, IDC3	0.1” header, 10 pin	
1	J1	Barrel connector	Not populated
1	J2	SMB connector	Not populated
4	R1, R2, R6, R21	200k, 0603	
1	R3	0R, 0603	
2	R4, R11	14k7, 0603	
2	R7, R14	499k, 0603	
3	R8, R16, R17	215k, 0603	
1	R12	1k, 0603	
1	R10	422k, 0603	
1	R13	3M, 0603	
1	R15	787k, 0603	
1	R18	24k, 0603	
1	R20	DNP, 0603	Not populated
1	U1	CAT808NTDI−27GT3	ON Semiconductor
1	U2	A5191HRT	ON Semiconductor
1	U3	TLV431ASNT1G	ON Semiconductor
1	Y1	460.8 kHz	Murata CSB460J

General Overview

The A5191HRTNGEVB evaluation board demonstrates the external components required for the operation of the IC. We will cover the different sections below as well as possible alternatives. A drawing of the board where the different sections are indicated is shown below.

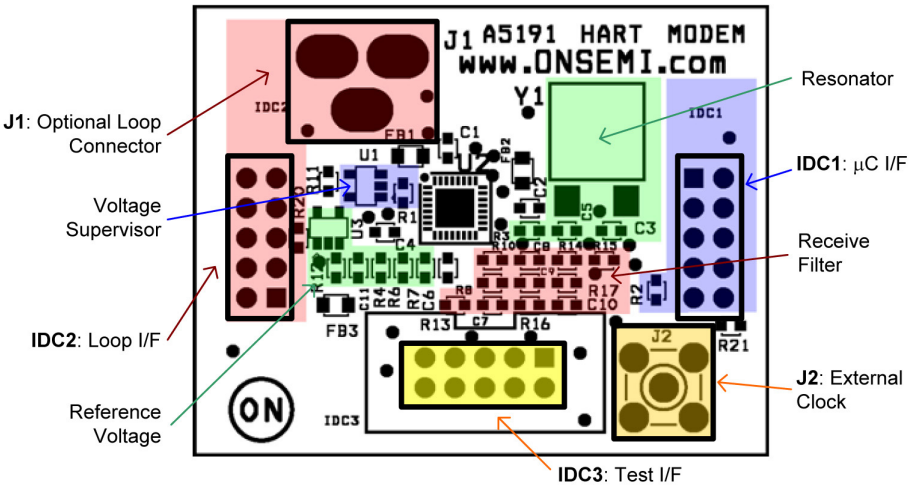


Figure 3. Board Drawing With Indication of Different Sections

Power Supply and References

Power Supply

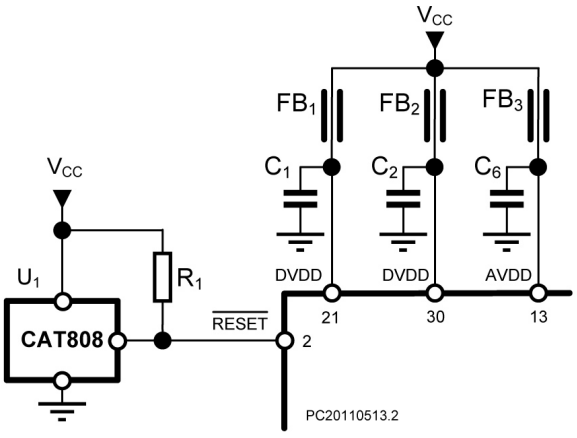


Figure 4. Supply Voltage and Power on Reset

The A5191HRTNGEVB is designed for a nominal voltage of 3 V. However, A5191HRT can be operated up to 6 V. For optimal functioning of the board, the values of several resistors should be changed for operation at voltages higher than 3 V. See the sections on reference voltages and bias for more information on this.

Current consumption of the module is very limited, making it ideal to be battery or loop−powered. Measurements of the power consumption of the module are listed in Table 3.

Table 3. MODULE CURRENT CONSUMPTION

Symbol	Condition	Current Consumption
I_{DD}	V_{DD} = 2.78 V, Transmit	428 μA
I_{DD}	V_{DD} = 2.78 V, Receive	417 μA
I_{DD}	V_{DD} = 3 V, Transmit	443 μA
I_{DD}	V_{DD} = 3 V, Receive	419 μA
I_{DD}	V_{DD} = 6 V, Transmit	837 μA
I_{DD}	V_{DD} = 6 V, Receive	781 μA
I_{DD}	V_{DD} = 3 V, Transmit, Ext. Osc.	362 μA
I_{DD}	V_{DD} = 3 V, Receive, Ext. Osc.	350 μA

The module will use less power when clock signal is applied externally, as this allows the modem to shut down the oscillator circuit. As is to be expected, a higher supply voltage increases current consumption.

It is advised to use a voltage supervisor such as CAT808 to prevent the modem to begin operation when the supply voltage is not yet reliable. This will guarantee correct operation of the digital circuitry.

The voltage supervisor will keep the RESETB pin low until its threshold value is reached (2.7 V on the A5191HRTNGEVB). This ensures that some time has passed after the supply voltage reaches the turn−on voltage level of 2.5 V.

The RESETB and VDD pin signals during startup are shown in Figure 5. The measured start−up delay is 2.6 ms.

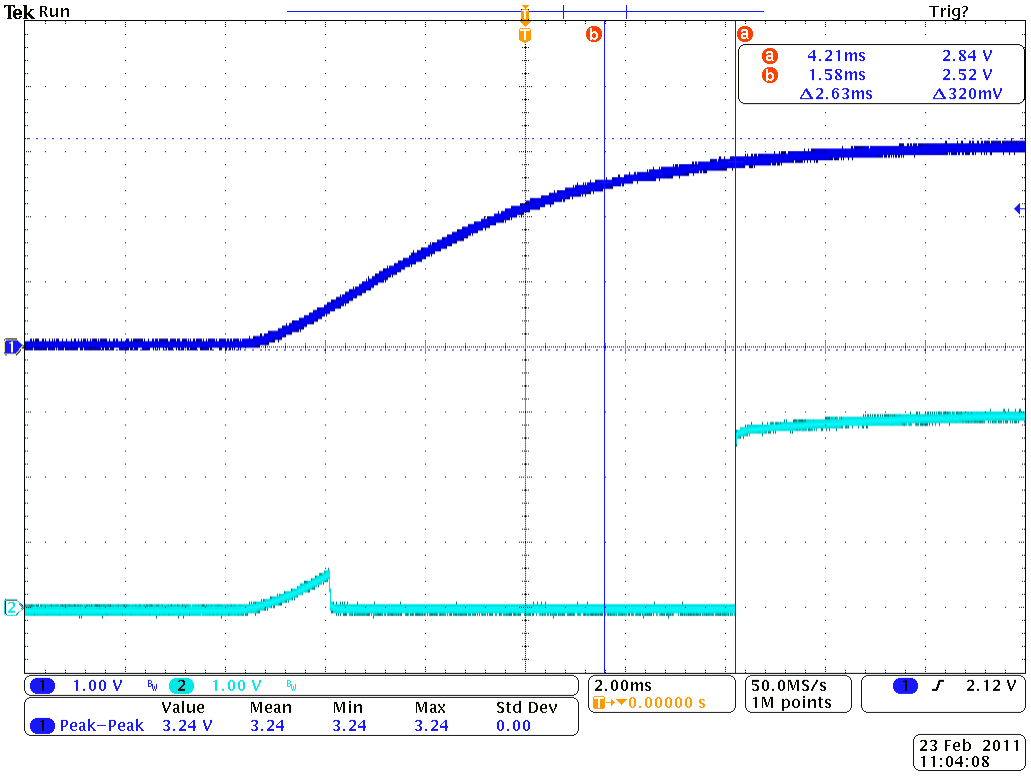


Figure 5. Power and RESETB Waveform During Startup, Showing 2.63 ms Startup Delay

C1, C2 and C6 are 100 nF ceramic decoupling capacitors located directly adjacent to each power pin. For analog power pins, an additional large−value ceramic capacitor may be needed in addition to the 100 nF decoupling capacitor when the application is intended for high−noise environments.

For loop powered devices, additional decoupling with a large value capacitor is advised to prevent digital noise from being transmitted on the current loop.

The ferrite beads FB1, FB2 and FB3 in series with power supply lines help to reduce EMI.

Reference voltages and comparator bias

A5191HRT needs an external analog reference voltage for the receiver or demodulator (RX) comparator and carrier detect (CD).

The AREF reference voltage sets the trip point of the demodulation operational amplifier of the 5191HRT. The AREF reference voltage is also used in setting the DC operating point of the received signal after it has passed through the band−pass receive filter. The ideal value for the AREF reference voltage depends on the voltage supply, and is chosen roughly half−way the operating range of the operational amplifiers. This ensures the range of the operational amplifier is maximized. For operation at 3 V, a 1.24 V reference voltage is recommended. For operation at 5 V, a 2.5 V reference voltage is recommended.

For A5191HRTNGEVB, the TLV431 shunt regulator is used with an internal reference of 1.24 V. This reference is compared against the output voltage, and the shunt transistor base is adjusted until it sinks enough current to drop the output to 1.24 V.

A simple low pass filter formed by R12 and C11 is added to increase reference stability. A slight voltage drop is observed over this filter caused by loading of the reference voltage. However, the voltage drop and the influence on the operation of the IC is minimal. Measurements show a voltage drop of 22 mV over R12, indicating a current of 22 μA. Of this current ca. 5 μA is consumed by the CDREF resistor division. The rest (ca. 17 μA) is used internally by the IC through the AREF pin. Current consumption through the CDREF pin is negligible.

The CDREF reference voltage sets the threshold for the carrier detect comparator. As the received signal is biased at AREF, the difference between CDREF and AREF will determine the minimum amplitude needed for the carrier detect comparator to flip. A (AREF−CDREF) of 80 mV corresponds to signal of approximately 100 mV peak−to−peak at the input of the receive filter. The CDREF reference voltage on the A5191HRTNGEVB is generated by a resistor division of the AREF reference. This will create an extra load on the low pass filter of AREF. However, the drop on the resistor of the low pass can be considered negligible.

An external resistor is required to set the bias current. The voltage over the bias resistor is regulated to AREF, so that the resistor determines a bias current. This bias current controls the operating parameters of the internal operational amplifiers and comparators and should be set to approximately 2.5 μA. A bias resistor of 499 kΩ is used on the A5191HRTNGEVB. For low cost solutions, a 470 kΩ is acceptable with minimal effect on operation.

Table 4. REFERENCE VOLTAGES

Description	Value
AREF reference voltage	1.212 V
CDREF reference voltage	1.128 V
Current through R_{12}	22 μA

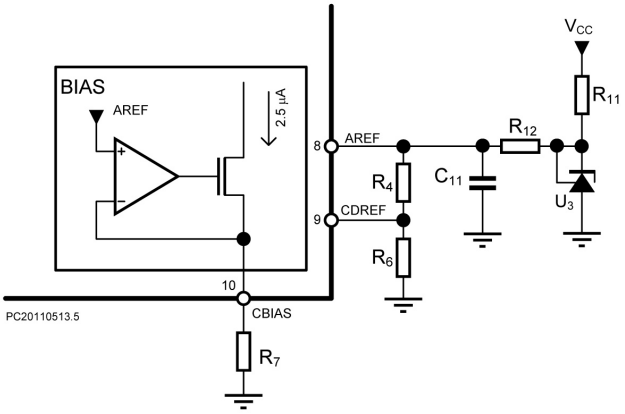


Figure 6. Reference Voltages Schematic

Clock Generation

A5191HRT is operated on a 460.8 kHz clock signal. The A5191HRTNGEVB has two options for providing this clock signal. The first method is by using a ceramic resonator or a crystal. The standard populated option is a Murata CSB460J ceramic resonator, loaded with two 220 pF capacitors.

Alternatively, a clock signal can be provided externally when R3 is removed and C3 is replaced by a resistor of 0 Ω. This signal can be provided by a microcontroller or any other external oscillator circuit. The module uses less power when clock signal is applied externally, as this allows the modem to shut down the oscillator circuit. A typical current consumption

witnessed by utilizing an external oscillator is 70 – 100 μA less. However, care must be taken that this external signal has the required accuracy (1%).

Duty cycle of the clock signal is specified between 40% and 60%. No errors were observed during testing in operation between 20% and 80% duty cycle. However, operation on such very small or very large duty cycle is not recommended, due to the possibility of timing errors that may occur under specific circumstances (including, but not limited to, temperature variations).

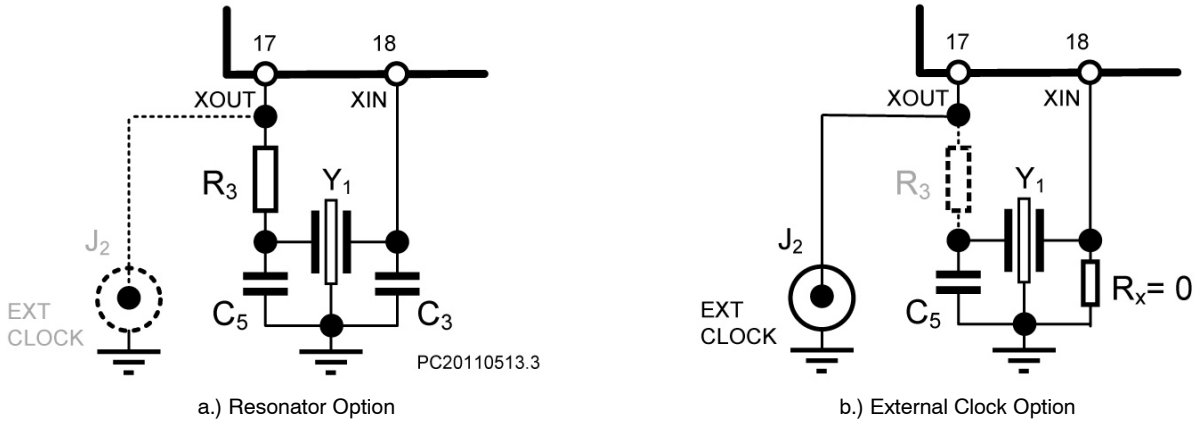


Figure 7. Clock Generation Circuit

Microcontroller Interface IDC1

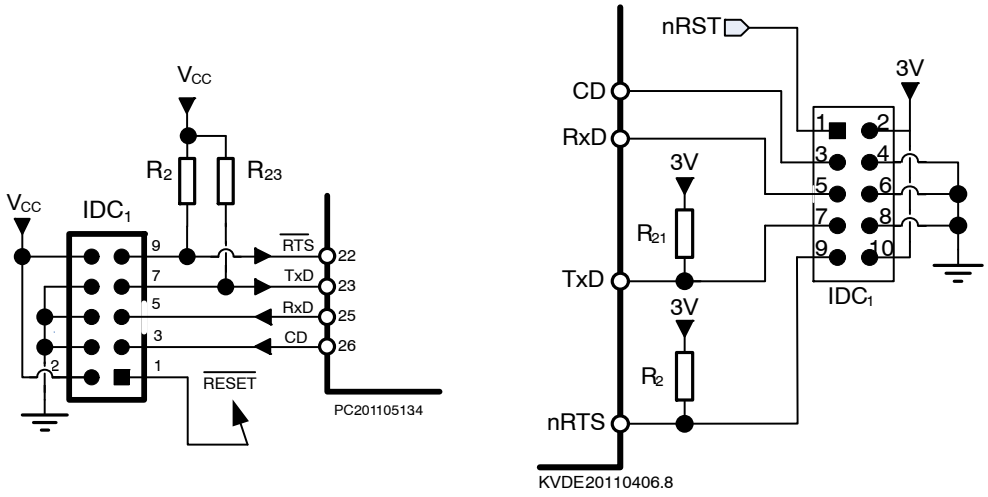


Figure 8. Microcontroller Interface

Table 5. MICROCONTROLLER INTERFACE

Pin Number	Signal	Type	Description
1	$\overline{\text{RST}}$	Open drain	Reset signal from the voltage supervisor, open drain with pull−up
3	CD	Output	Carrier Detect
5	RxD	Input	Receive from microcontroller
7	TxD	Output	Transmit towards microcontroller
9	RTSB	Input	Request to send
2, 10	VDD	Power	3 V nominal
4, 6, 8	GND	Power	

The interface towards a microcontroller is provided in IDC1. This interface can also be used to supply power to the module. The nominal supply voltage for the module is 3 V. For more information see the section on power supply and references.

The RESETB line to the modem is an open drain signal. A pull−up resistor of 200 kΩ is provided on the board, and should not be duplicated on the microcontroller side. The reset signal is generated on the board, and could be used as reset signal for other IC such as the microcontroller.

The CD signal rises when a HART signal of ca. 100 mV_{pp} is detected on the current loop. See the section on reference voltages for more information on these threshold level settings. When no signal, or a signal of limited amplitude is present, the CD line is pulled down to 0 V.

The RxD, TxD, and RTSB signals implement a standard UART interface at 1200 baud with start bit 8 data bits, parity bit and stop bit (11−bit frame). The RTSB signal disconnects the transmitter circuit when pulled high, and should be held low before any data is transmitted. Data frames are not buffered by the modem. Instead, data is transmitted bit by bit. Care should be taken to avoid clock skew in the receiving UART. If the same time base is used for both the modem and the UART, a 1% accurate time base may not be sufficient. The problem is a combination of receive data jitter and clock skew between transmitting and receiving HART devices. If the transmit time base is at 99% of nominal and the receive time base in another device is at 101% of nominal, the receive data (at the receiving UART) will be skewed by roughly 21% of one bit time at the end of each 11−bit byte. This is shown in Figure 9. The skew time is measured from the initial falling edge of the start bit to the center of the 11th bit cell. This 21% skew by itself is a relatively good result. However, there is another error source for bit boundary jitter. The Phase Lock Loop demodulator in the A5191HRT produces jitter in the receive data that can be as large as 12% of a bit time. Therefore, a bit boundary can be shifted by as much as 24% of a bit time relative to its ideal location based on the start−bit transition. (The start−bit transition and a later transition can be shifted in opposite directions for a total of 24%.)

The clock skew and jitter added together is 45%, which is the amount that a bit boundary could be shifted from its expected position. UARTs that sample at mid−bit will not be affected. However, there are UARTs that take multiple samples during each bit to try to improve on error performance. These UARTs may not be satisfactory, depending on how close the samples are to each other, and how samples are interpreted. A UART that takes a majority vote of three samples is acceptable.

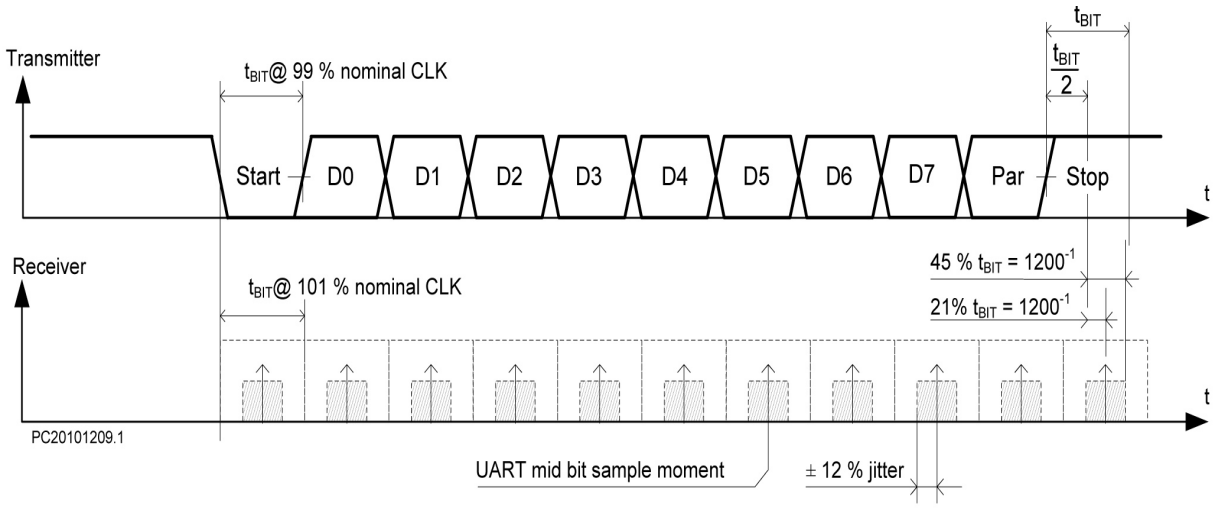


Figure 9. Clock Skew

Even if your own time base is perfect, you still must plan on a possible 35% shift in a bit boundary, since you don't have control over time bases in other HART devices.

Transmitter

The TxA modem pin is decoupled through a 100 nF capacitor to pin 7 of IDC2. For certain applications, it might be required to remove this capacitor and replace it by a 0 Ω resistor. The output on this pin is a 500 mV_{pp} signal trapezoid waveform shown in Figures 10 and 11. This pin can only drive impedances higher than 30 kΩ, and as a consequence may need to be amplified to drive low impedances. For a given implementation of a master or slave, it may be required to remove C4 and replace it with a 0 Ω resistor to allow the decoupling to occur elsewhere in the master implementation.

The nominal frequency of the output is 1196.9 Hz for "mark" and 2194.3 Hz for "space". These frequencies are dependent on the accuracy of the A5191 clock.

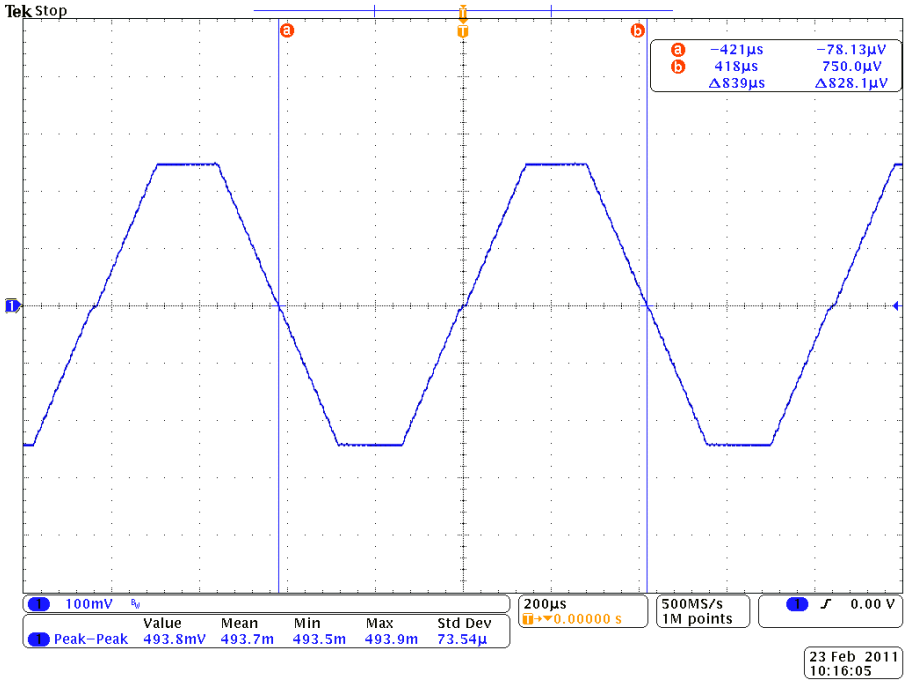


Figure 10. Output Waveform (Mark)

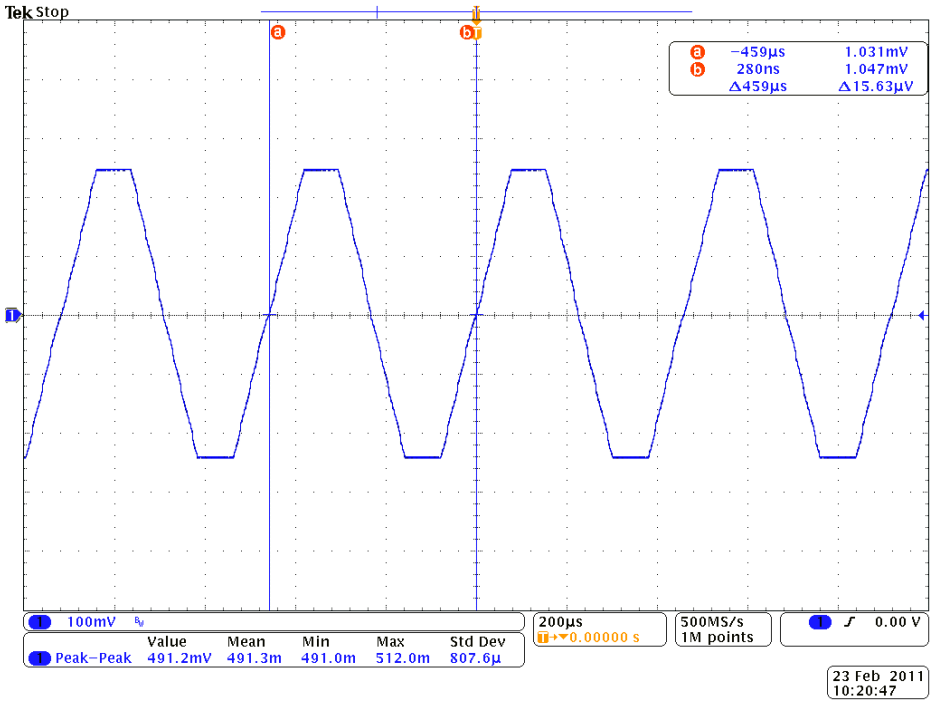


Figure 11. Output Waveform (Space)

Receiver

The receive band pass filter is implemented on the A5191HRTNGEVB. The values are listed in Table 6 and the filter schematic is displayed in Figure 12. For cost purposes, this filter can be implemented using E12 value resistors with minimal changes to the filter characteristic. This implementation will have a slightly reduced gain in the pass band.

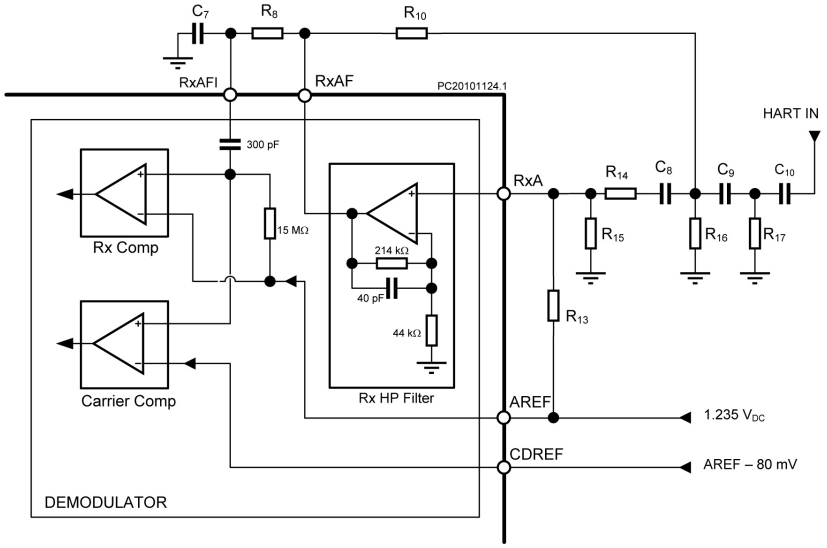


Figure 12. Receive Filter

Table 6. RECEIVE FILTER COMPONENT VALUES

Reference	Value E96	Value E12 (Low−cost)
R_{16}	215 kΩ 1%	220 kΩ 1%
R_{17}	215 kΩ 1%	220 kΩ 1%
R_{14}	499 kΩ 1%	470 kΩ 1%
R_{15}	787 kΩ 1%	680 kΩ 1%
R_{10}	422 kΩ 1%	470 kΩ 1%
R_8	215 kΩ 1%	220 kΩ 1%
R_{13}	3 MΩ 1%	3.3 MΩ 1%
C_{10}	470 pF 5%	470 pF 5%
C_8	1 nF 5%	1 nF 5%
C_9	1 nF 5%	1 nF 5%
C_7	220 pF 5%	220 pF 5%

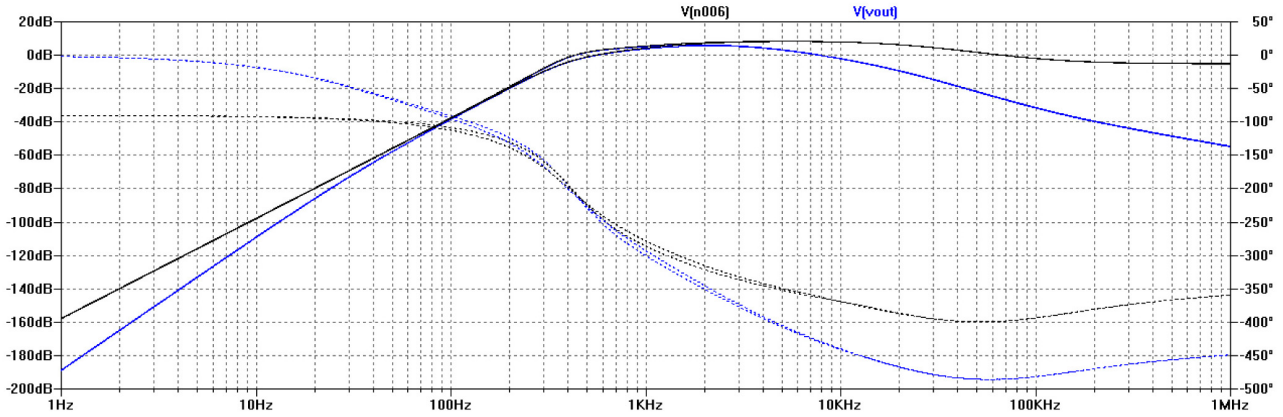


Figure 13. Filter Characteristic (First Stage = black, Total = Blue)

In Figure 13 the simulated characteristic of the entire filter is shown, in both variations, for the first stage (black) and total filter (blue). The normal and low−cost variations are superimposed, showing that the variations are minimal. However, when the tolerance on the values is also loosened, a bigger variation in the characteristic is observed. Figures 14a and 14b show a monte carlo analysis for resistors of 1% and 10%. It is advised to use resistors of at least 1% accuracy.

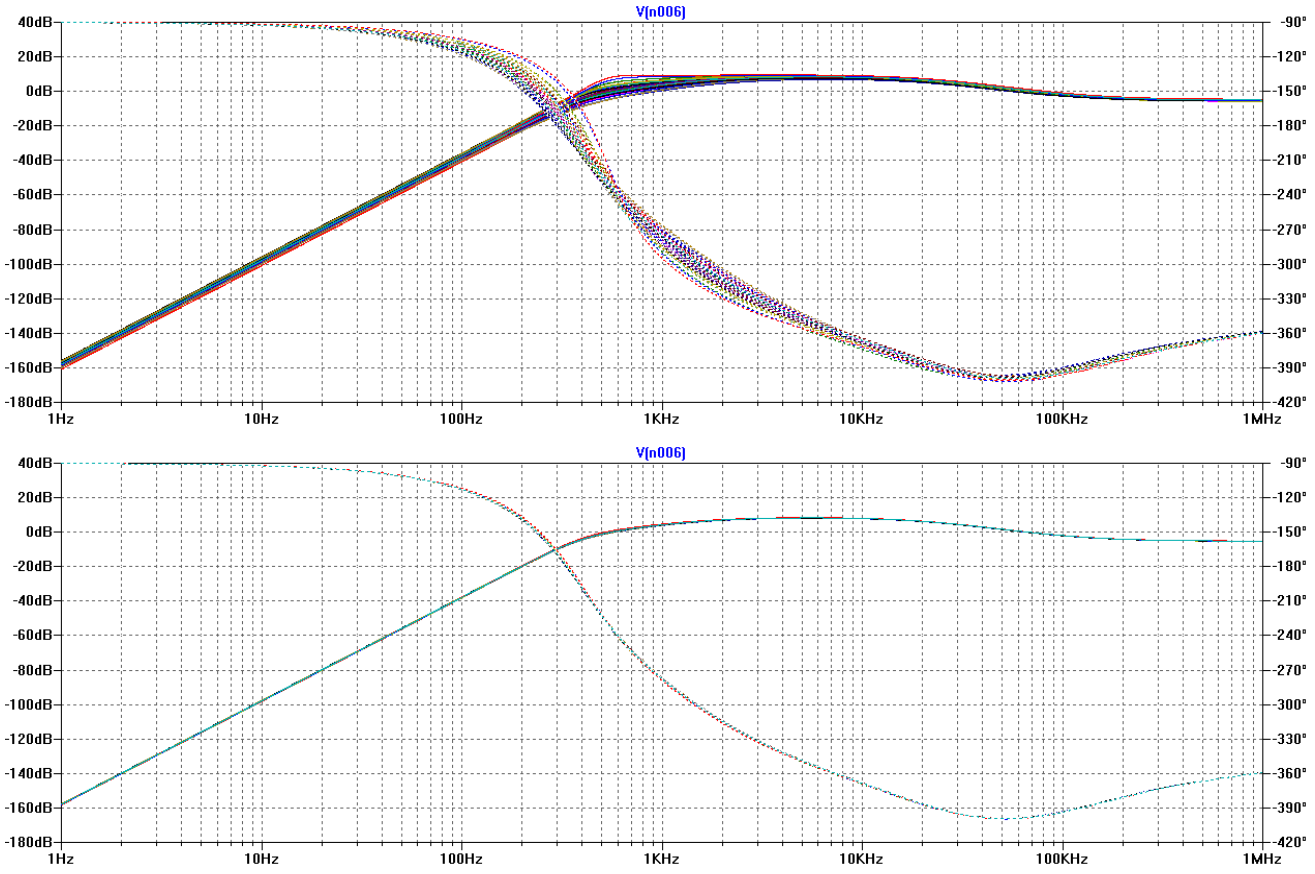


Figure 14. Monte Carlo Analysis of the First Filter Stage for 10% (above) and 1% (below) Accuracy

In Figure 15 the measured filter characteristic of both variations are shown next to a simulated result. These characteristics are only of the first stage of the filter as the output of the second stage is not accessible. We notice an additional pole showing up at high frequencies. This only improves the filter by rejecting high frequency noise, and is too high in frequency to have an influence on the phase of HART signals. Figure 16 shows the group delay of the total filter. It is important that the difference in group delay between the mark and space is minimal, so that the output of the filter still has coherence between both signals. The plot of Figure 16 shows that the difference is indeed minimal.

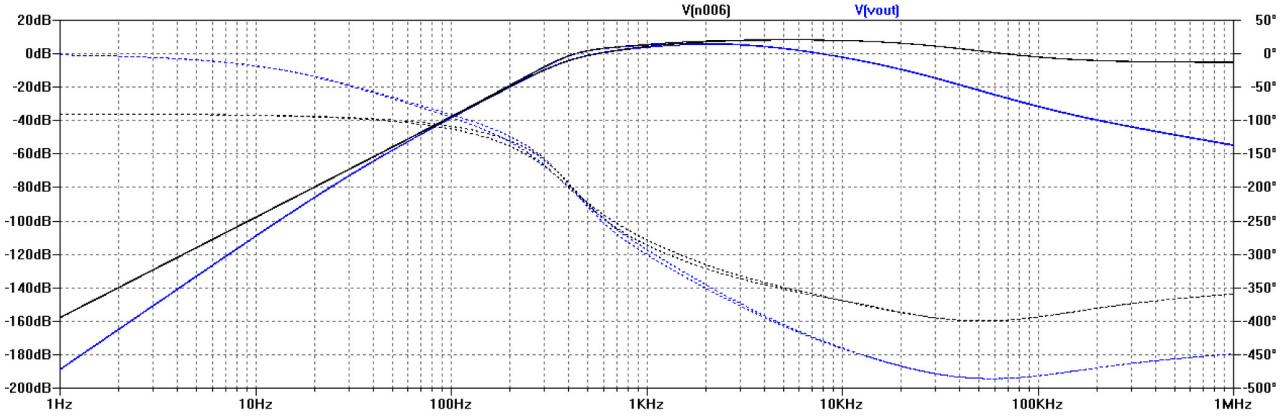


Figure 15. Measured and Simulated Filter Characteristic of the First Filter Stage

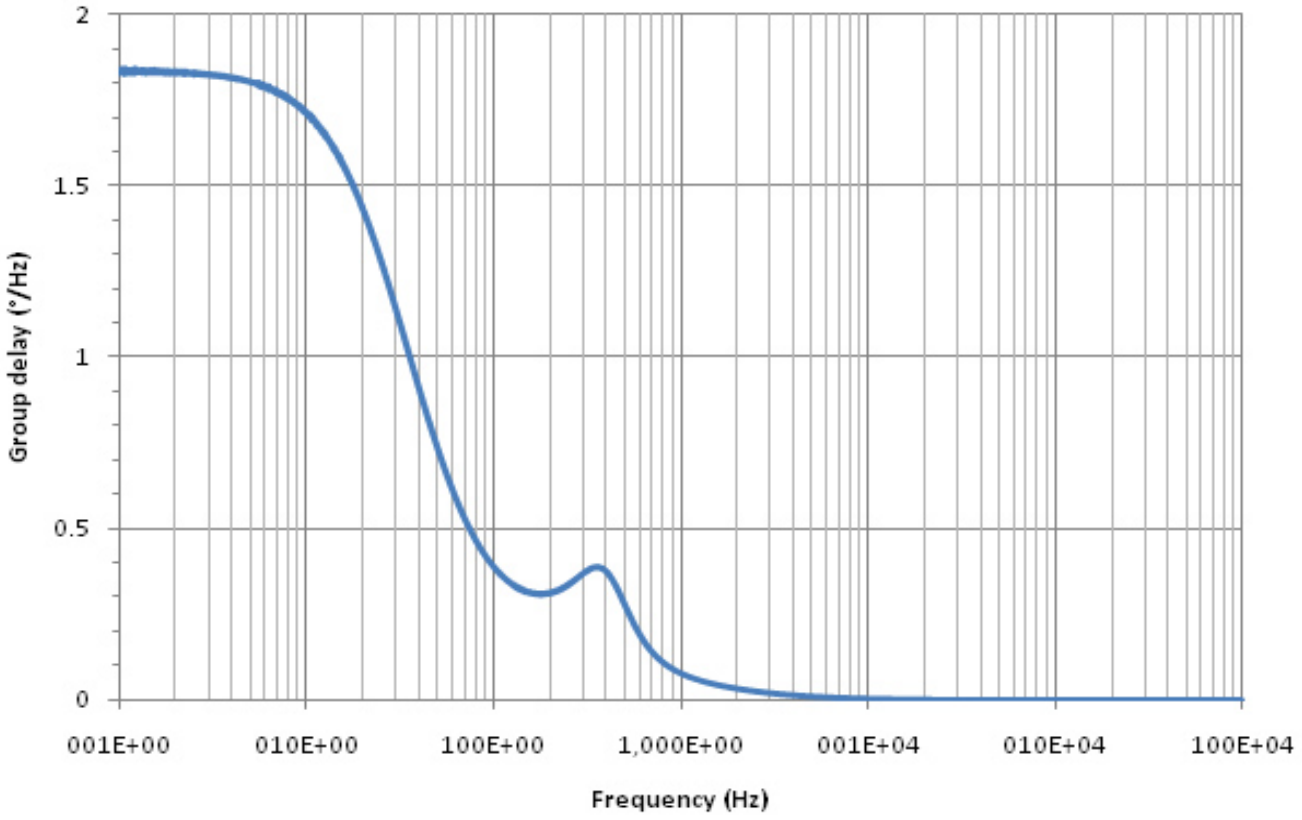


Figure 16. Group Delay of the Total Filter

First Stage

The first stage of the filter is implemented as a modified third−order high pass active filter.

Consider the circuit shown in Figure 17. This resembles the implemented filter except for the coupling capacitor on the operational amplifier, and the removal of R_{14}. The filter is a variation on the Sallen−Key topology with three poles. The AREF voltage serves here as a biasing voltage, but can for ac frequencies be regarded as ground. For a complete analysis of this filter type, see the Appendix on Page 17.

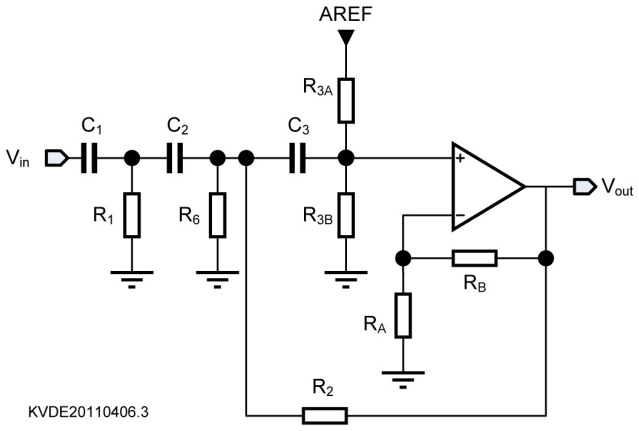


Figure 17. Simplified First Filter Stage Schematic

The transfer function of this type of filter is:

$$H(s) = \frac{K * s^3}{s^3 + a_2 * s^2 + a_1 * s + a_0}$$

Taking into account the compensation capacitance present on the operational amplifier between input and output introduces another high frequency pole and zero pair. The zero of which can easily be determined to be:

$$z = \frac{1}{2\pi * C * (R1//R2)} = 109\ kHz$$

Determining the exact location of the extra pole requires extra calculation. Indeed, the location of the other poles will also be shifted by this extra circuit element.

Introducing R_{14} does not introduce another pole or zero but changes the denominator of the transfer function, and thus the location of the poles.

The final transfer function of the first filter stage is thus a fourth order filter of the form:

$$H(s) = \frac{G * s^3 * (1 + b_2 * s)}{s^4 + b_3 s^3 + b_2 * s^2 + b_1 * s + b_0}$$

The poles of this transfer function are located at:

p_1, p_2 = 195 Hz

p_3 = 1.220 kHz

p_4 = 22 kHz

The input impedance of this filter stage is higher than 89 kΩ at frequencies below 50 kHz.

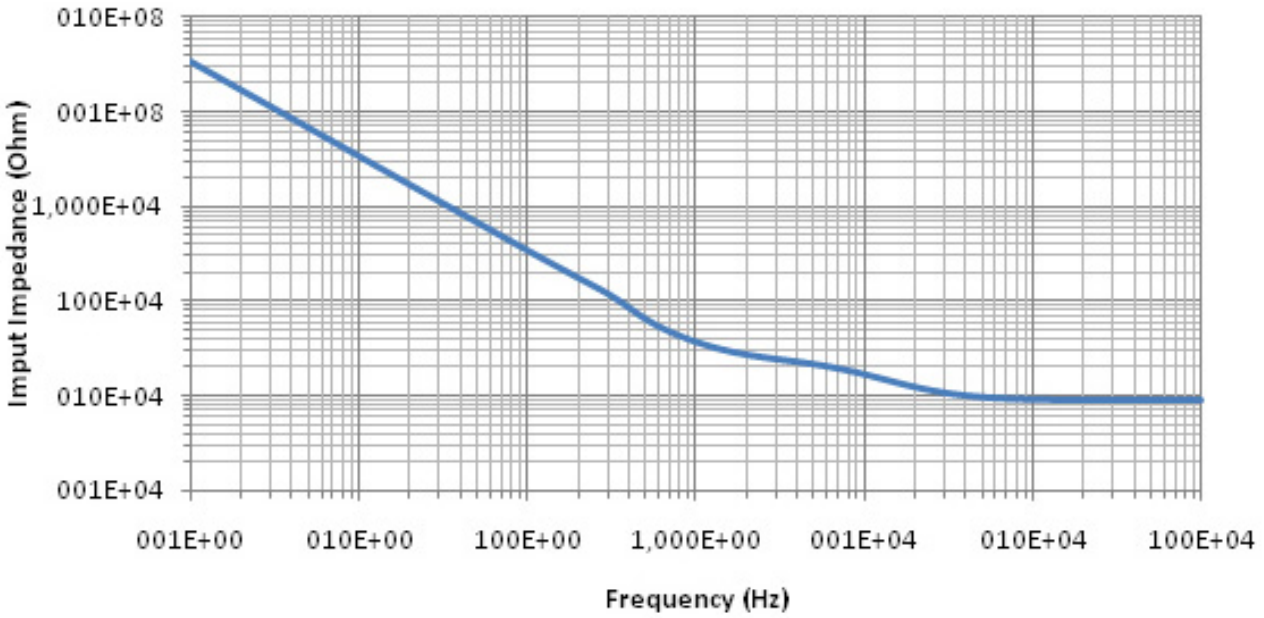


Figure 18. Input Impedance of the First Filter Stage

Second Stage

The second stage of the receive filter is a simple band pass filter consisting of cascaded passive low− and high−pass filter.

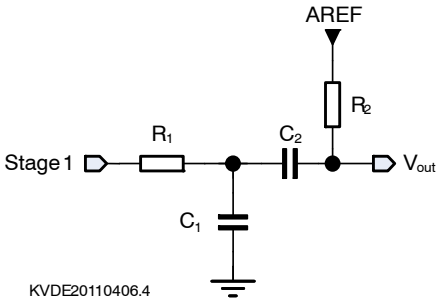


Figure 19. Second Filter Stage Schematic

Again the AREF voltage can be considered ground for AC frequencies, and serves only to bias the output of the filter around AREF. It can be shown that this stage has the following transfer function:

$$H(s) = \frac{s * R2 * C2}{1 + s(R1C1 - R1C2 + R2C2) + s^2 R1R2C1C2}$$

This stage has two poles that can easily be calculated:

p_1 = 36 Hz

p_2 = 3316 Hz

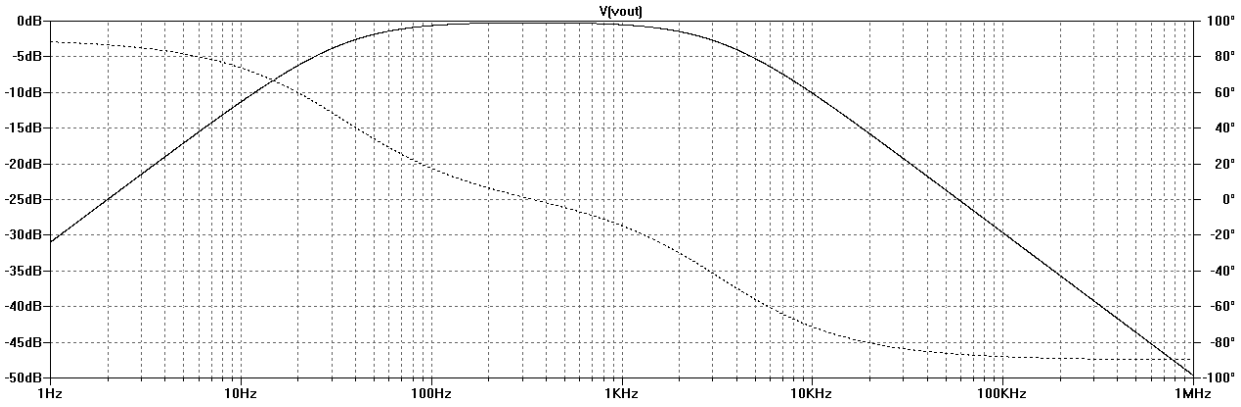


Figure 20. Characteristic of the Second Stage of the Filter

APPLICATION IDEAS

The A5191HRT takes care of the HART modulation. This HART signal must then be superimposed on a 4−20mA current loop. Below are some possible implementations of both a master and slave transmitter.

Slave implementation

A simple slave implementation is shown in Figure 21. The analog loop current is set by a DAC from the microcontroller, while HART signals are added in from the A5191HRT. The DAC can be PWM or sigma−delta topology. To explain the operation of this circuit, let us first look at an example where the DAC is not of a switching topology. In this case, R_2 and R_3 can be 0 Ω, and C_2, C_3 and C_5 can be left out. As one end of R_6 is tied to local ground, it can easily be seen that the voltage at the negative loop terminal is negative with respect to the local ground. Resistors R_4 and R_5 are then chosen so that in steady state their common terminal is a virtual ground point in the absence of HART signals, since the negative terminal of the amplifier is also connected to ground. A similar principle applies when HART signals are applied. So both amplifier inputs are regulated to ground. A compensation capacitor C_4 may be required depending on the operational amplifier used. To avoid offset generated by bias current in the operational amp, R_3 should be dimensioned to approach the impedance seen by the positive terminal.

The amplifier will then determine the current flowing through the loop by changing the base of a transistor in emitter feedback configuration. The value for R_7 is determined by the output range $V_{o,max}$ of the amplifier used:

$$R_{7,max} = \frac{V_{o,max} - V_{BE}}{20\ mA}$$

It is often recommended to take a value as large as possible, so that noise effects are minimal.

Typically the value of R_6 is chosen equal to R_7. The voltage over R_6 and R_7 combined should however be less than 12 V when the current setting is 20 mA.

Next, the values of R_4 and R_5 are chosen depending on the most significant bit of the DAC.

$$2\,V_{MSB}\,R_5 = 20mA\ R_6\,R_4$$

When the DAC is not a switching topology, we can now choose R_1 and C_1. We have:

$$500mV\ R_5 = 1mA\ R_6\,Z$$

Where:

$$Z = |sC_1 + R_1|$$

In practice, C_1 is chosen sufficiently small so that $Z \approx R_1$.

For a PWM or sigma−delta output DAC, the circuit gets a bit more complicated, as we need to filter away high frequency DAC components, but leave HART signals intact. If the bandwidth of the DAC is larger than 2.2 kHz, adding C_3 introduces a low−pass filter to the loop that will remove most of the switching noise.

$$C_3 = \frac{1}{2\pi\ f_{3\,dB}\,R_p}$$

Where R_p is the parallel circuit of R_4, R_5 and R_1.

If the bandwidth of the DAC is close to the HART frequencies, an alternate high−frequency feedback path must be introduced so that HART signals are not removed by the low pass filter of the DAC. The exact calculation of component values in this case is more complicated. However, it is based on a similar principle, but now with two summing junctions, for low−frequency and high−frequency signals separated.

Resistor R_3 may be needed to compensate for amplifier bias current. It is chosen so that its resistance is similar to resistance seen on the positive terminal. Depending on the amplifier used, it may also be required to provide a compensation capacitance C_4.

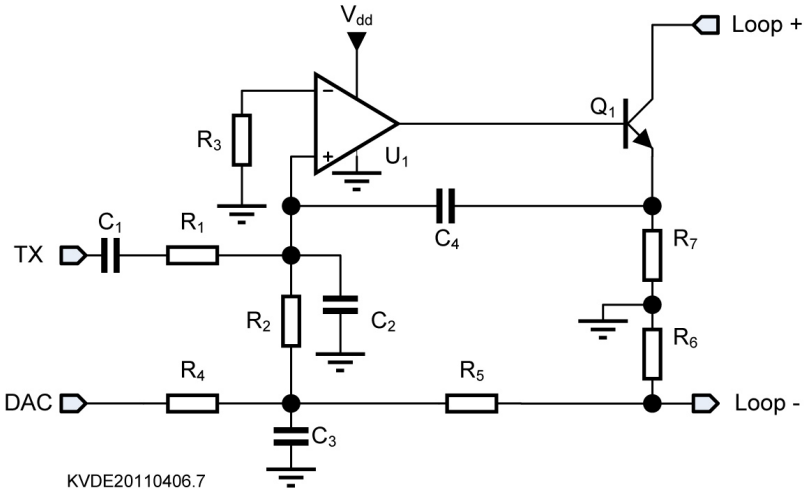


Figure 21. Sample Slave Implementation

Master Implementation

An example of a possible master implementation is shown in Figure 22. To use this schematic, the coupling capacitor C4 on the A5191HRTNGEVB will need to be replaced by a 0 Ω resistor, or new biasing must be provided.

The current loop master has a sense resistor over which the current flowing through the loop can be measured. The value of this resistor varies depending on the sensitivity required and range of the ADC. A HART Master can have a sense resistor ranging from 230 Ω to 600 Ω. Increasing the sense resistor will result in higher amplitude HART signal received, but will also reduce the voltage available on the slave side. Furthermore, if you wish to sense the analog transmitted signal, the MSB of your DAC may limit the resistor size. If this limitation is too stringent, the sense resistor can be split in two resistors, as shown in the figure, effectively creating a resistor divider.

To transmit a HART signal, the TxA signal will need to be amplified, as the A5191HRT transmit circuit can only drive high impedance circuits (>30 kΩ). An additional operational amplifier is required. Depending on the sense resistor used, some gain or attenuation may be required to get a 1 mA peak−to−peak HART output signal. This can be accomplished by the resistors R_3 and R_4. For a typical sense resistor of 500 Ω, a unity gain suffices and a unity gain operational amplifier configuration can be used instead.

The amplifier however has a low impedance output, which cannot be paralleled with the sense resistor, as this would cause problems when the slave is transmitting. This problem is solved by adding a series switch (such as MC74VHC1G66DTT1G), controlled by the RTS signal. For a normally open switch, the nRTS signal as applied to the A5191 must be inverted first. To reduce power usage, the operational amplifier can be disabled when the transmitter is turned off. This is both done by inserting PNP transistor Q_1on the V_{DD} connection of the amplifier.

To couple the signal into the current loop, a single capacitor was used. For other coupling techniques see application note AND8346/D.

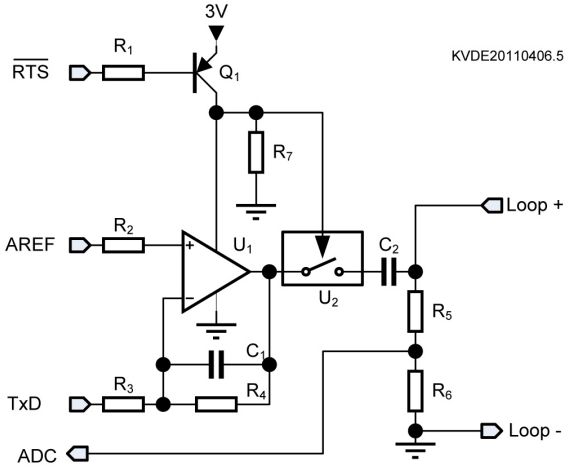


Figure 22. Sample Master Implementation

APPENDIX

Calculation of a three Pole Sallen−Key High Pass Filter

The first stage of the receive filter uses a three pole active high pass filter with a topology similar to the one shown in Figure 17. We will derive the transfer function of this filter below. We will denote the gain configured with R_A and R_B as K.

$$K = \frac{R_A + R_B}{R_A}$$

Resistors R_{3A} and R_{3B} serve only to bias the amplifier input in DC, and can for the rest of the calculations be considered parallel and replaced by one resistor:

$$R_3 = \frac{R_{3A} + R_{3B}}{R_{3A}R_{3A}}$$

Using Kirkhof's current law, we get in the three nodes of the filter:

$$(V_3 - V_2)sC_3 + \frac{V_3}{R_3} = 0 \quad \text{(eq. 1)}$$

$$(V_2 - V_1)sC_2 + (V_2 - V_3)sC_3 + \frac{V_2}{R_6} + \frac{(V_3 - V_{out})}{R_2} = 0 \quad \text{(eq. 2)}$$

$$(V_1 - V_{in})sC_1 + (V_1 - V_2)sC_2 + \frac{V_1}{R_1} = 0 \quad \text{(eq. 3)}$$

Solving Equations 1 and 3 for V1 resp. V2 we find:

$$V_2 = \frac{1 + sR_3C_3}{sR_3C_3}V_3 \quad \text{(eq. 4)}$$

$$V_1 = \frac{sR_1C_1V_{in} + sR_1C_2V_2}{1 + sR_1(C_1 + C_2)} \quad \text{(eq. 5)}$$

For Equation 2 we find:

$$V_2\left(sC_2 + sC_3 + \frac{1}{R_6} + \frac{1}{R_2}\right) = V_1sC_2 + V_3\left(sC_3 + \frac{K}{R_2}\right) \quad \text{(eq. 6)}$$

Or, with the substitution:

$$\frac{\alpha}{R} = \frac{1}{R} + \frac{1}{R}$$

Equation 6 simplifies to:

$$V_2\left(sC_2 + sC_3 + \frac{\alpha}{R_2}\right) = V_1 sC_2 + V_3\left(sC_3 + \frac{K}{R_2}\right) \quad \text{(eq. 7)}$$

Substituting V1 and V2 in Equation 7 using Equations 4 and 5, and simplifying we find the transfer function:

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{K * s^3}{s^3 + a_2 * s^2 + a_1 * s + a_0}$$

Where:

$$a_2 = \frac{1}{R_1C_1} + \frac{1}{R_3C_3} + \frac{1}{R_3C_2} + \frac{1}{R_3C_1} + (\alpha - K)\left(\frac{1}{R_2C_2} + \frac{1}{R_2C_1}\right)$$

$$a_1 = \frac{1}{R_1R_3C_1C_3} + \frac{1}{R_1R_3C_1C_2} + \frac{\alpha - K}{R_1R_2C_1C_2} + \frac{\alpha}{R_2R_3C_2C_3} + \frac{\alpha}{R_2R_3C_1C_3}$$

$$a_0 = \frac{\alpha}{R_1R_2R_3C_1C_2C_3}$$

Adding the compensation capacitor on the operational amplifier results in the following transformation on the transfer function:

$$K \rightarrow K\frac{1 + s\,R_pC_4}{1 + s\,R_4C_4}$$

Where:

$$R_p = R_1 // R_4$$

Since K is present in the numerator of the transfer function, the zero of this factor will be present in the transformed transfer function. The denominator of the transformed transfer function is a forth order function with the following coefficients. The transfer function now has the following form:

$$H(s) = \frac{K * s^3 * (1 + b_z * s)}{s^4 + b_3s^3 + b_2 * s^2 + b_1 * s + b_0}$$

Where:

$$b_z = R_pC_4$$

$$b_3 = \frac{1}{R_4C_4} + \frac{1}{R_1C_1} + \frac{1}{R_3C_3} + \frac{1}{R_3C_2} + \frac{1}{R_3C_1} + \left(\alpha - K\frac{R_p}{R_4}\right)\left(\frac{1}{R_2C_2} + \frac{1}{R_2C_1}\right)$$

$$b_2 = \frac{1}{R_1C_1R_4C_4} + \frac{1}{R_3C_3R_4C_4} + \frac{1}{R_3C_2R_4C_4} + \frac{1}{R_3C_1R_4C_4} + \frac{\alpha - K}{R_4C_4}\left(\frac{1}{R_2C_2} + \frac{1}{R_2C_1}\right) + \frac{1}{R_1R_3C_1C_3}$$
$$+ \frac{1}{R_1R_3C_1C_2} + \frac{\alpha}{R_2R_3C_2C_3} + \frac{\alpha}{R_2R_3C_1C_3} + \left(\alpha - K\frac{R_p}{R_4}\right)\frac{1}{R_1R_2C_1C_2}$$

$$b_1 = \frac{\alpha}{R_1R_2R_3C_1C_2C_3} + \frac{1}{R_1R_3R_4C_1C_3C_4} + \frac{1}{R_1R_3R_4C_1C_2C_4} + \frac{\alpha - K}{R_1R_2R_4C_1C_2C_4}$$
$$+ \frac{\alpha}{R_2R_3R_4C_2C_3C_4} + \frac{\alpha}{R_2R_3R_4C_1C_3C_4}$$

$$b_0 = \frac{\alpha}{R_1 R_2 R_3 R_4 C_1 C_2 C_3 C_4}$$

Adding a series resistor to the capacitor results in the following transformation:

$$C_3 \rightarrow \frac{C_3}{1 + s\, R_7 C_3}$$

Since C3 is not present in the numerator or in the highest−order coefficient, no extra poles or zeros will be introduced by this transformation. The form of the transfer function hence remains the same.
The transformed coefficients are:

$$b_3 = \frac{1}{R_4 C_4} + \frac{1}{R_1 C_1} + \frac{1}{R_3 + R_7}\left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}\right) + \left(\alpha - K\frac{R_p}{R_4}\frac{R_3}{R_3 + R_7}\right)\frac{1}{R_2}\left(\frac{1}{C_2} + \frac{1}{C_1}\right)$$

$$\begin{aligned} b_2 = {} & \frac{1}{R_1 R_4 C_1 C_4} + \frac{1}{(R_3 + R_7) R_4 C_4}\left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}\right) + \frac{1}{R_1 (R_3 + R_7) C_1}\left(\frac{1}{C_2} + \frac{1}{C_3}\right) \\ & + \left(\alpha - K\frac{R_3}{R_3 + R_7}\right)\frac{1}{R_2 R_4 C_4}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) + \frac{\alpha}{R_2 (R_3 + R_7) C_3}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) \\ & + \left(\alpha - K\frac{R_p}{R_4}\frac{R_3}{R_3 + R_7}\right)\frac{1}{R_2 R_1 C_1 C_2} \end{aligned}$$

$$\begin{aligned} b_1 = {} & \frac{1}{R_1 (R_3 + R_7) R_4 C_1 C_4}\left(\frac{1}{C_2} + \frac{1}{C_3}\right) + \left(\alpha - K\frac{R_3}{R_3 + R_7}\right)\frac{1}{R_1 R_2 R_4 C_1 C_2 C_4} \\ & + \frac{\alpha}{R_2 (R_3 + R_7) R_4 C_3 C_4}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) + \frac{\alpha}{R_1 R_2 (R_3 + R_7) C_1 C_2 C_3} \end{aligned}$$

$$b_0 = \frac{\alpha}{R_1 R_2 (R_3 + R_7) R_4 C_1 C_2 C_3 C_4}$$

EVALUATION BOARD

Layout

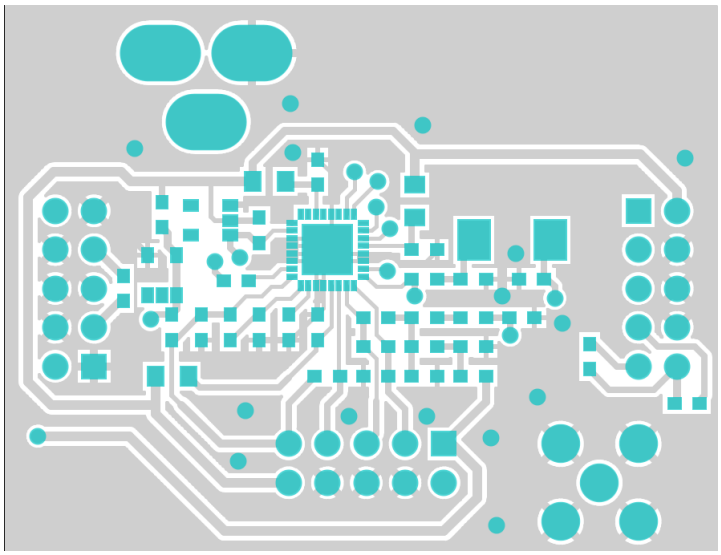


Figure 23. Top Layer Layout

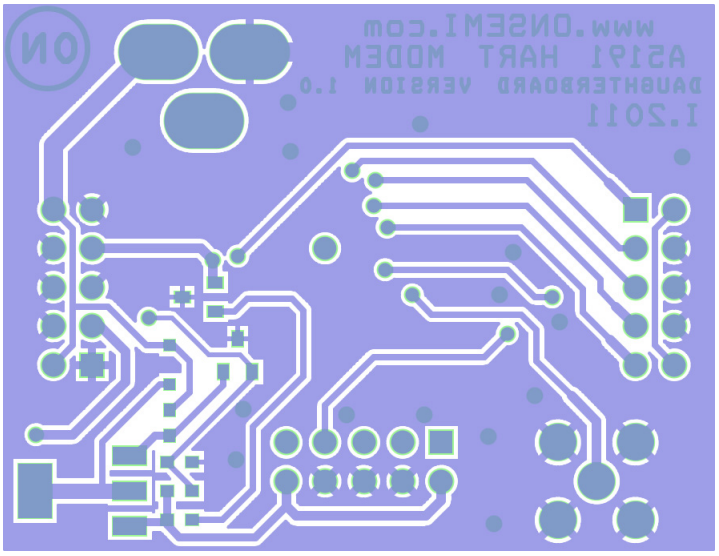


Figure 24. Bottom Layer Layout

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