MP28248

High-Efficiency, Fast-Transient, 3A, 4.2V-20V Input Synchronous Step-down Converter in a QFN12 (2x3mm) Package

The Future of Analog IC Technology

DESCRIPTION

The MP28248 is a fully-integrated, high-efficiency, synchronous, step-down, switch mode converter. It offers a very compact solution that can achieve a 3A continuous output current over a wide input supply range with excellent load and line regulation. The MP28248 operates at high efficiency over a wide output-current load range.

Constant-On-Time control mode provides fast transient response and eases loop stabilization.

Full protective features include short-circuit protection, over-current protection, over-voltage protection, under-voltage protection, and thermal shutdown.

The MP28248 requires a minimal number of readily-available standard external components.

This device is available in a space-saving 2mmx3mm 12-pin QFN package.

FEATURES

- Wide 4.2V to 20V Operating Input Range
- 3A Output Current
- Low R_{DS}(ON) Internal Power MOSFETs
- Proprietary Switching-Loss Reduction Technique
- Soft Startup/Shutdown
- Programmable Switching Frequency
- SCP, OCP, UVP, OVP, and Thermal Shutdown
- Output Adjustable from 0.815V to 13V
- Available in a QFN12 (2mmx3mm) Package

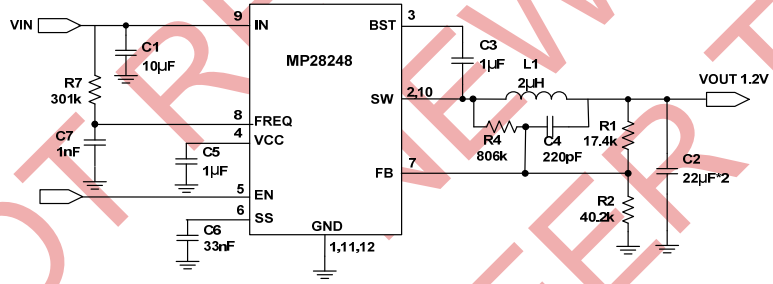
APPLICATIONS

- Networking Systems
- Distributed Power Systems

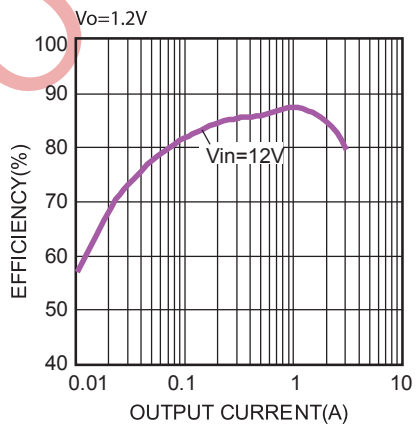
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TYPICAL APPLICATION



Efficiency vs. Load Current



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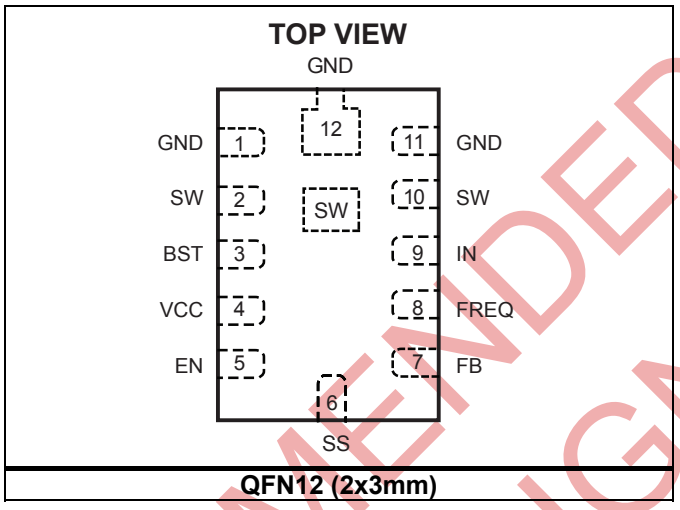
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ORDERING INFORMATION

Part Number	Package	Top Marking
MP28248GD*	QFN12 (2x3mm)	ACR

*For Tape & Reel, add suffix –Z (e.g. MP28248GD–Z).

PACKAGE REFERENCE



QFN12 (2x3mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 22V
V_{SW} ..... -0.3V to (V_{IN} + 0.3V)
V_{BS} ..... V_{SW} + 6V
$I_{VIN\ (RMS)}$ 3.5A
All Other Pins ..... -0.3V to +6V
Continuous Power Dissipation (T_A = 25°C) (2)
QFN12 (2X3mm)..... 1.8W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 4.2V to 20V
Output Voltage V_{OUT}..... 0.815V to 13V
Maximum Junction Temp. (T_J).... -40°C to 125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN12 (2mmx3mm) ..... 70 ..... 15 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		0		μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.9V		440	490	μA
HS switch-on resistance(5)	HS_{RDS-ON}			120		mΩ
LS switch-on resistance(5)	LS_{RDS-ON}			50		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V		0	1	μA
Current limit	I_{LIMIT}	After Soft-Start time-out	4	5		A
One-shot on-time	t_{ON}	R_7 = 600kΩ, V_{OUT} = 1.2V		480		ns
		R_7 = 200kΩ, V_{OUT} = 1.2V		160		ns
		R_7 = 120kΩ, V_{OUT} = 1.2V		100		ns
Minimum off time	t_{OFF}			125		ns
Fold-back off Time(5)	t_{FB}-OCP	IL=ILIM=1 FB=0.6V		5		μs
	t_{FB}-SCP	IL=ILIM=1 FB=0.2V		10		μs
OCP hold-off time(5)	t_{OC}	IL=ILIM=1 FB=0.6V		50		μs
Feedback voltage	V_{FB}	T_A=25°C	807	815	823	mV
Feedback current	I_{FB}	V_{FB}=815mV		30	50	nA
EN rising threshold	EN_{Vth-Hi}		1.05	1.3	1.6	V
EN threshold hysteresis	$EN_{Vth-Hys}$			500		mV
EN input current	I_{EN}	V_{EN} = 2V		1.5		μA
		V_{EN} = 0V		0		μA
Soft-start charging current	ISS	VSS = 0V		14		μA
Soft stop charging current	ISS	VSS=0.815V		4.5		μA
V_{IN} under-voltage lockout threshold rising	$INUV_{Vth}$				3.1	V
V_{IN} under-voltage lockout threshold hysteresis	$INUV_{HYS}$			300		mV
Thermal shutdown	T_{SD}			150		°C
Thermal shutdown hysteresis	T_{SD-HYS}			25		°C

Note:

5) Guaranteed by design and characterization

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PIN FUNCTIONS

QFN12 (2x3mm) Pin #	Name	Description
1, 11, 12	GND	System Ground. Reference ground for the regulated output voltage. Requires special consideration during PCB layout.
2, 10, exposed pad	SW	Switch Output. Connect using wide PCB traces.
3	BST	Bootstrap. Requires a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver.
4	VCC	Internal Bias Supply. Decouple with a 1µF ceramic capacitor as close to the pin as possible.
5	EN	EN = 1 to enable the MP28248. For automatic start-up, connect EN pin to VIN with a pull-up resistor.
6	SS	Soft-Start. Connect an external SS capacitor to program the soft-start time for the switch mode regulator. When the EN pin goes high, an internal current source (14µA) charges up the SS capacitor and the SS voltage smoothly ramps up from 0 to V_{FB}. When the EN pin goes low, an internal current source (4.5µA) discharges the SS capacitor and the SS voltage smoothly drops.
7	FB	Feedback. Sets the output voltage when connected to the tap of an external resistor divider that is connected between output and GND.
8	FREQ	Frequency. Set during CCM operation. Connect a resistor R_7 to IN to set the switching frequency. Decouple with a 1nF capacitor.
9	IN	Supply Voltage. The MP28248 operates from a +4.2V to +20V input rail. Requires C1 to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.

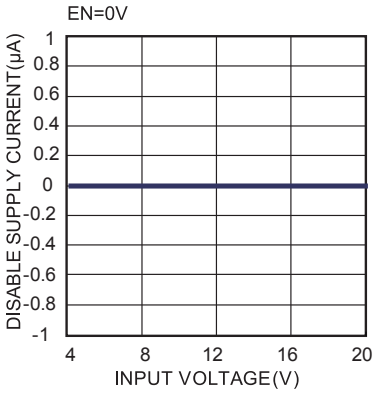
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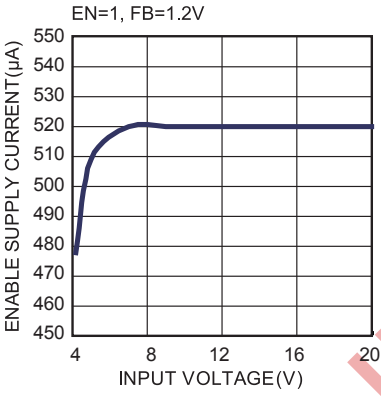
TYPICAL CHARACTERISTICS

V_{IN}=12V, V_{out}=1.2V, L=2μH, T_A=+25°C,unless otherwise noted.

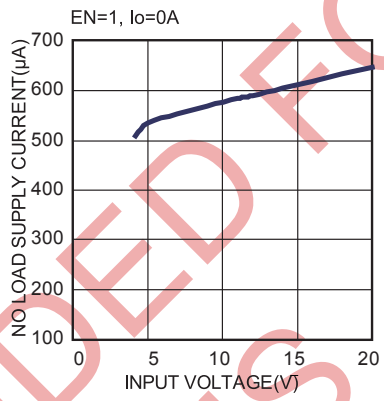
Disable Supply Current vs. Input Voltage



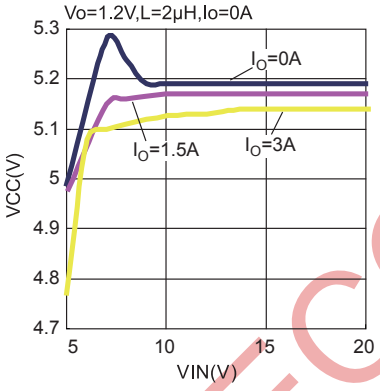
Enable Supply Current vs. Input Voltage



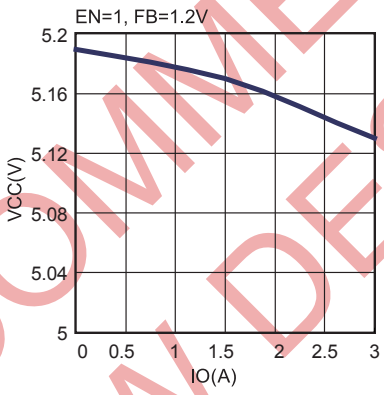
No Load Supply Current vs. Input Voltage



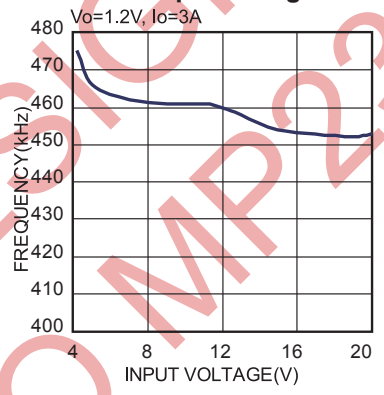
VCC vs. Input Voltage



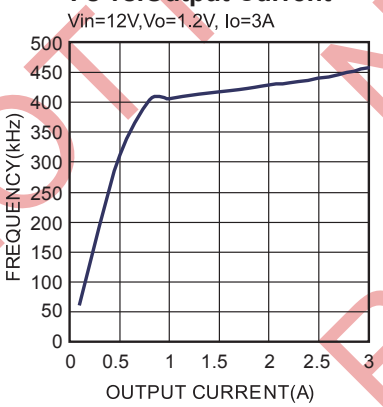
VCC vs. Io



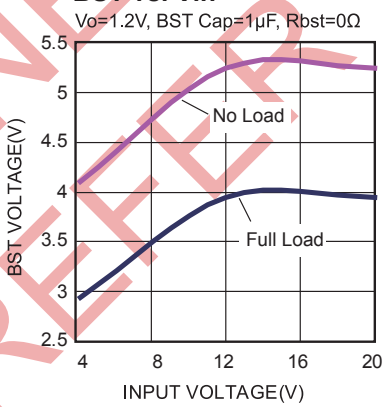
Fs vs. Input Voltage



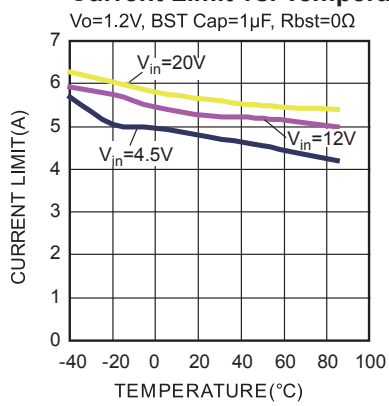
Fs vs.Output Current



BST vs. Vin



Current Limit vs. Temperature



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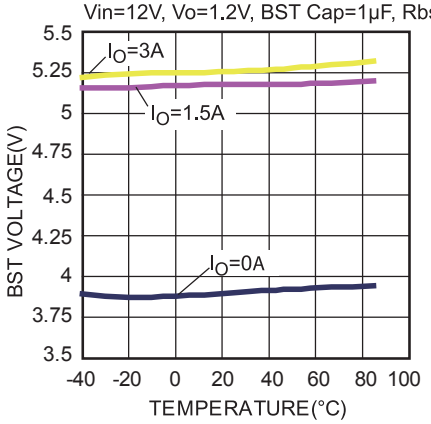
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TYPICAL CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{out}=1.2V, L=2µH, T_A=+25°C,unless otherwise noted.

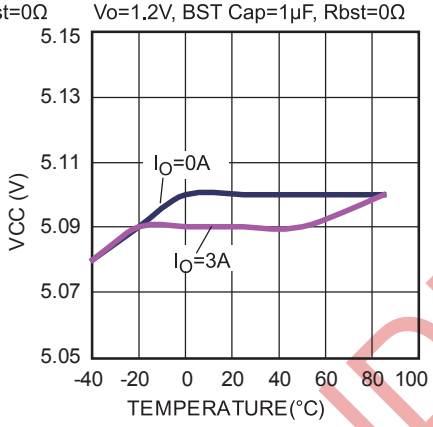
BST Voltage vs. Temperature

Vin=12V, Vo=1.2V, BST Cap=1µF, Rbst=0Ω



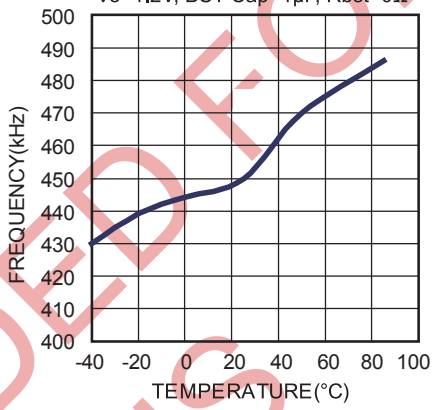
VCC vs. Temperature

Vo=1.2V, BST Cap=1µF, Rbst=0Ω



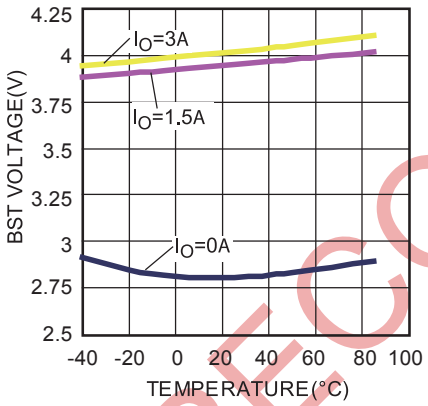
Fs vs. Temperature

Vo=1.2V, BST Cap=1µF, Rbst=0Ω



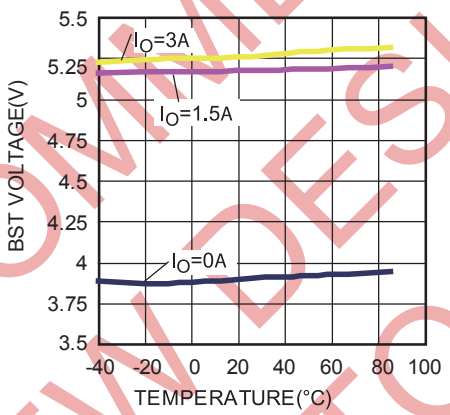
BST Voltage vs. Temperature

Vin=4.2V, Vo=1.2V, BST Cap=1µF, Rbst=0Ω



BST Voltage vs. Temperature

Vin=20V, Vo=1.2V, BST Cap=1µF, Rbst=0Ω



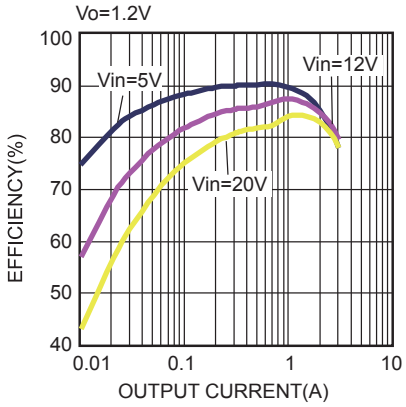
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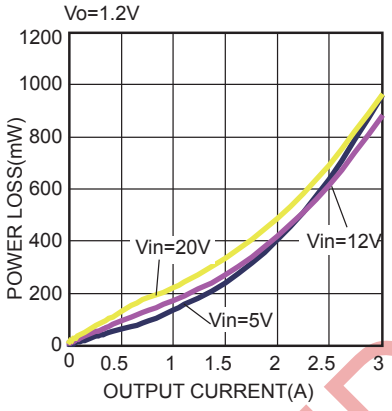
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, L = 2µH, T_A = 25°C, unless otherwise noted.

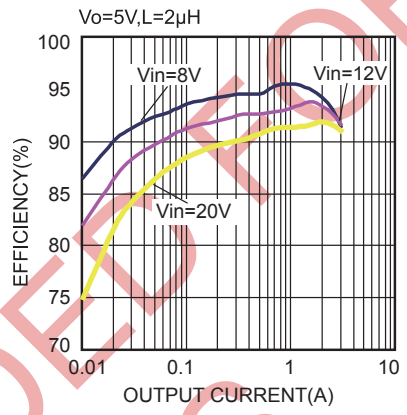
Efficiency vs. Load Current



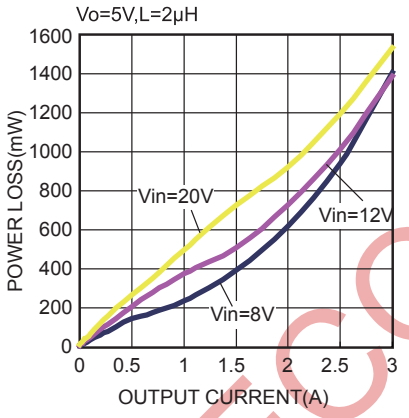
Power Loss vs. Load Current



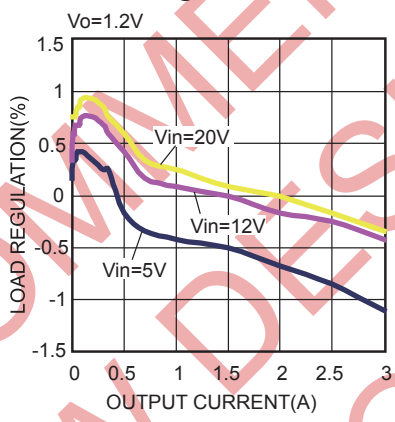
Efficiency vs. Load Current



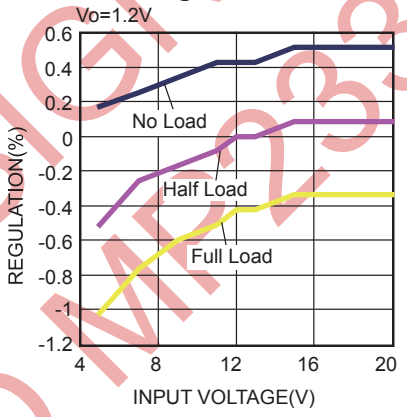
Power Loss vs. Load Current



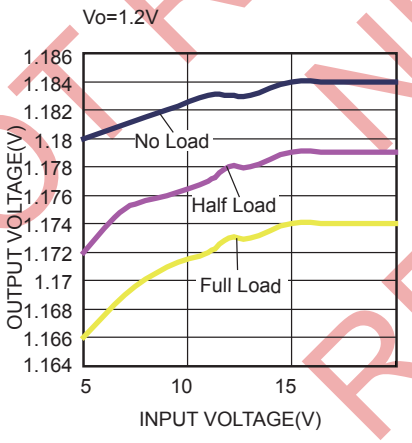
Load Regulation



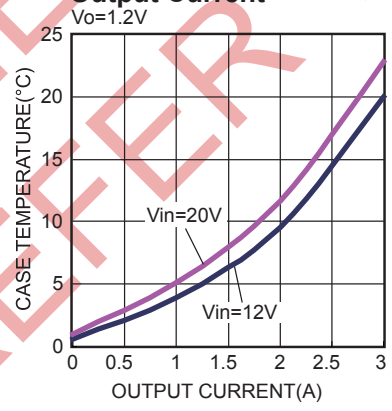
Line Regulation



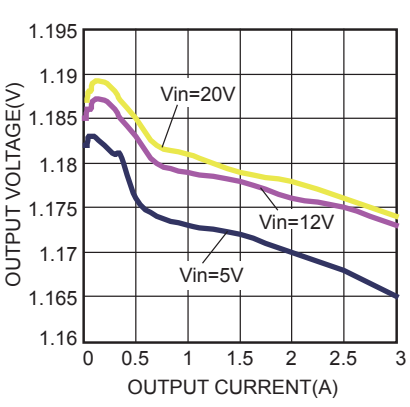
Vo vs. Vin



Case Temperature Rise vs. Output Current



Vo vs. Io



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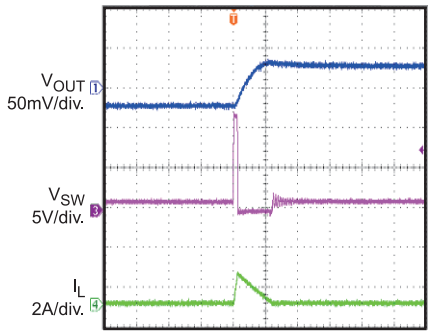
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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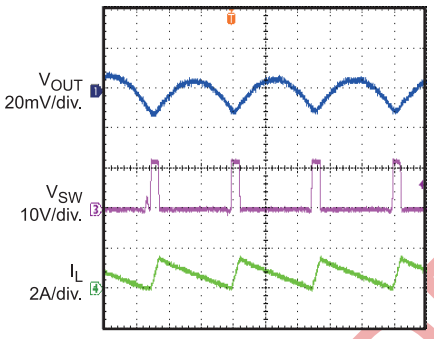
Output Voltage Ripple

Io=0A



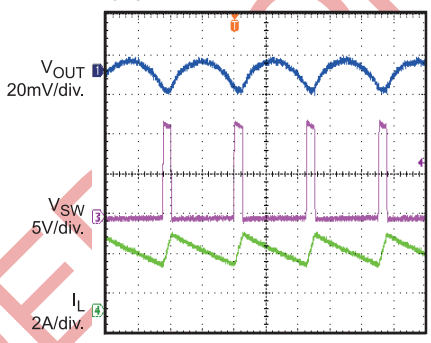
Output Voltage Ripple

Io=0.7A



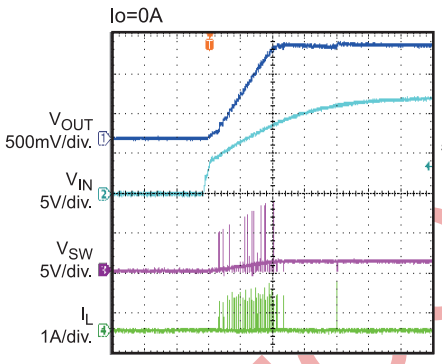
Output Voltage Ripple

Io=3A



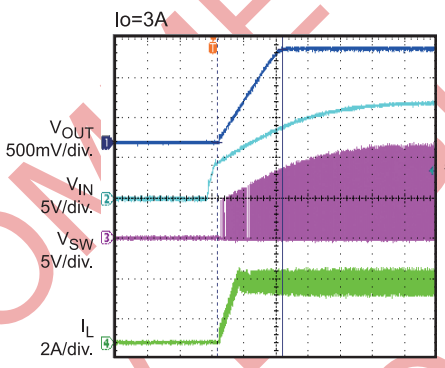
Start Up Through Vin

Io=0A



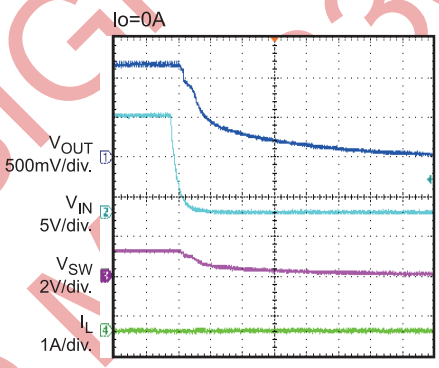
Start Up Through Vin

Io=3A



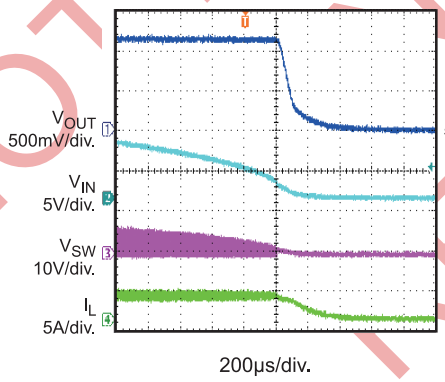
Shut Down Through Vin

Io=0A



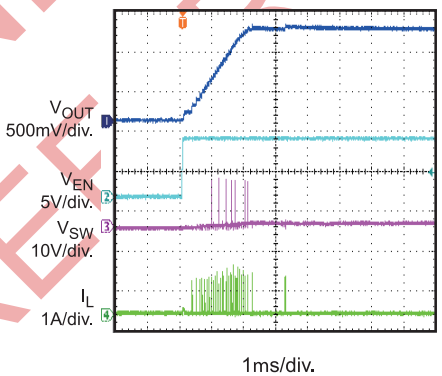
Shut Down Through Vin

Io=3A



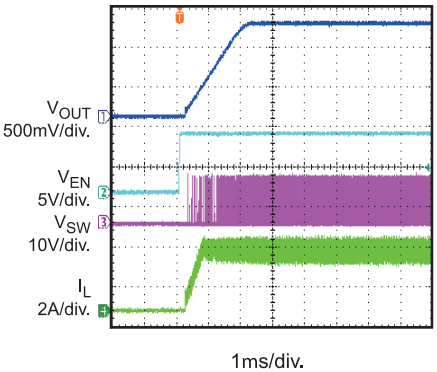
Start Up Through EN

Io=0A



Start Up Through EN

Io=3A



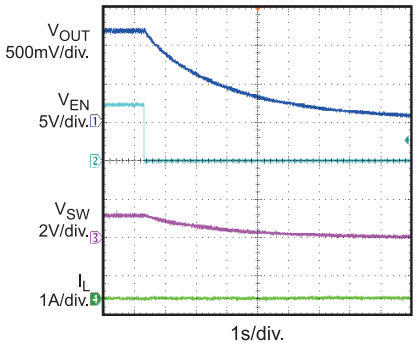
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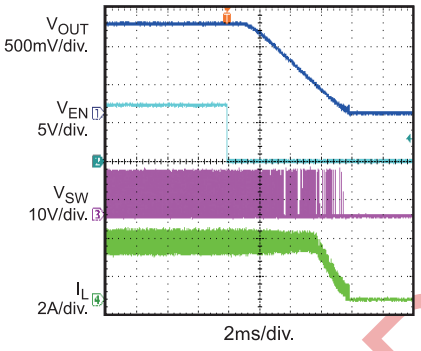
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, L = 2µH, T_A = 25°C, unless otherwise noted.

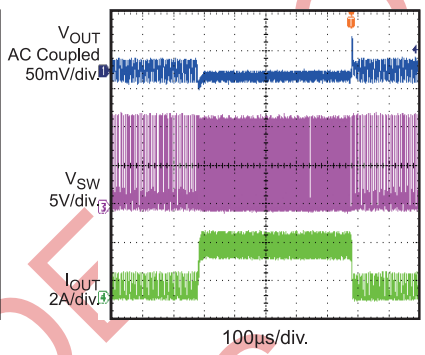
Shut Down through EN
I_{OUT} =0A



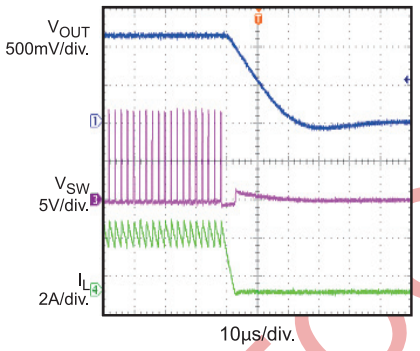
Shut Down through EN
I_{OUT} =3A



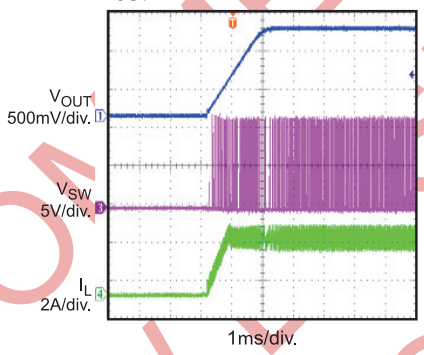
Transient Response
I_{OUT}=0.3~2.7A @ 2.5A/µs, C_{OUT}=22x2µF



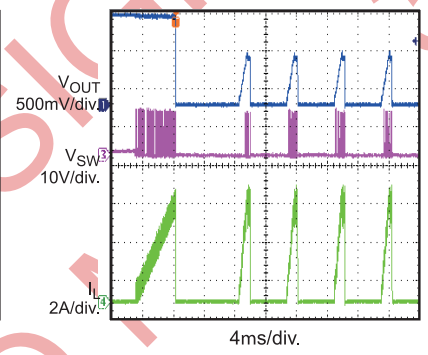
Thermal Shutdown
I_{OUT} =3A



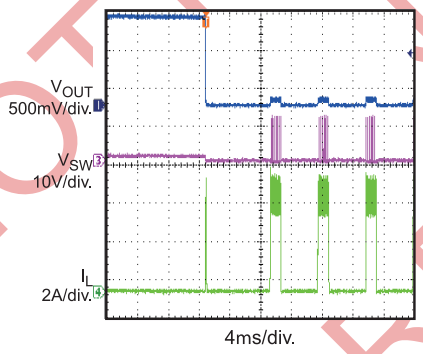
Thermal Recovery
I_{OUT} =3A



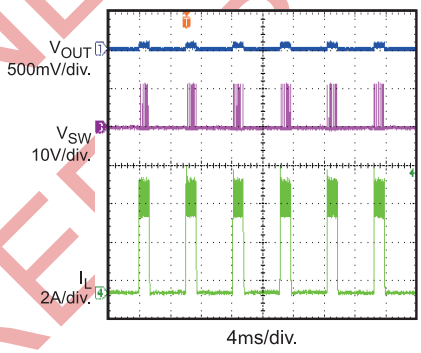
OCP



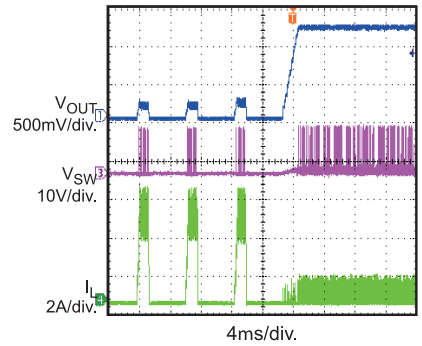
SCP Entry



SCP Steady State



SCP Recovery



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BLOCK DIAGRAM

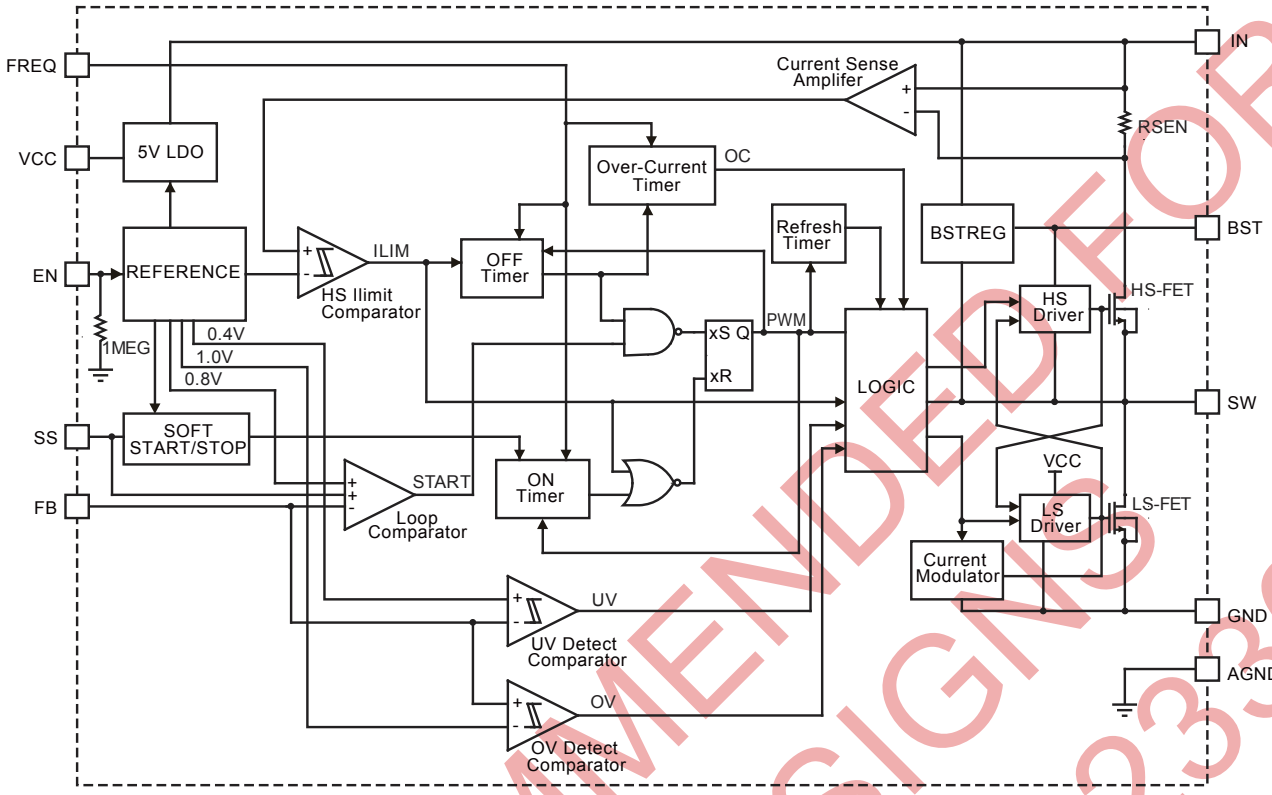


Figure 1: Functional Block Diagram

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OPERATION

PWM Operation

The MP28248 is a fully-integrated, synchronous, rectified, step-down switch converter. The device uses constant-on-time (COT) control to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns ON whenever the feedback voltage (V_{FB}) is lower than the reference voltage (V_{REF})—a low V_{FB} indicates insufficient output voltage. The input voltage and the frequency-set resistor determine the ON period as follows:

$$t_{ON} = \frac{9.3 \times R_7(k\Omega)}{V_{IN}(V) - 0.4} + 40(ns) \quad (1)$$

After the ON period elapses, the HS-FET enters the OFF state. By cycling HS-FET between the ON and OFF states, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its OFF state to minimize the conduction loss.

Shoot-through occurs when both the HS-FET and the LS-FET are turned on at the same time, causing a dead short between input and GND. Shoot-through dramatically reduces efficiency, and the MP28248 avoids this by internally generating a dead-time (DT) between when HS-FET turns off and LS-FET turns on, and when LS-FET turns off and HS-FET turns on.

Heavy-Load Operation

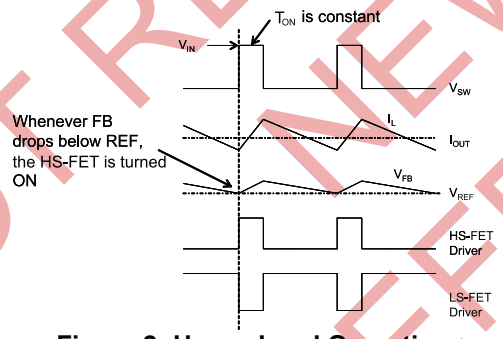


Figure 2: Heavy-Load Operation

During heavy-load operation—when the output current is high—the MP28248 enters continuous-conduction mode (CCM) where the HS-FET and LS-FET repeat the on/off operation described for PWM operation, the inductor current never goes to zero, and the switching frequency (f_{SW}) is fairly constant. Figure 2 shows the timing diagram during this operation.

Light-Load Operation

During light-load operation—when the output current is low—the MP28248 reduces the switching frequency to maintain high efficiency, and the inductor current drops near zero. When the inductor current reaches zero, the LS-FET driver goes into tri-state (high Z). The current modulator controls the LS-FET and limits the inductor current to around -1mA as shown in Figure 3. Hence, the output capacitors discharge slowly to GND through LS-FET, R1, and R2. This operation greatly improves device efficiency when the output current is low.

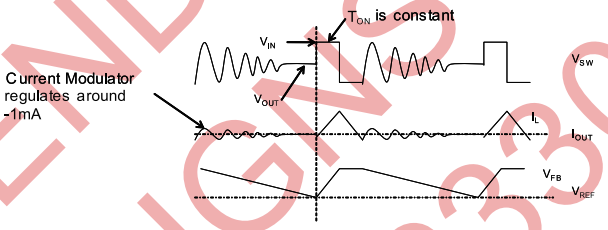


Figure 3: Light-Load Operation

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as during heavy-load conditions. The frequency at which the HS-FET turns on is a function of the output current—as the output current increases, the time period that the current modulator regulates becomes shorter, and the HS-FET turns on more frequently. The switching frequency increases in turn. The output current reaches the critical level when the current modulator time is zero, and can be determined using the following equation:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (2)$$

The device reverts to PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

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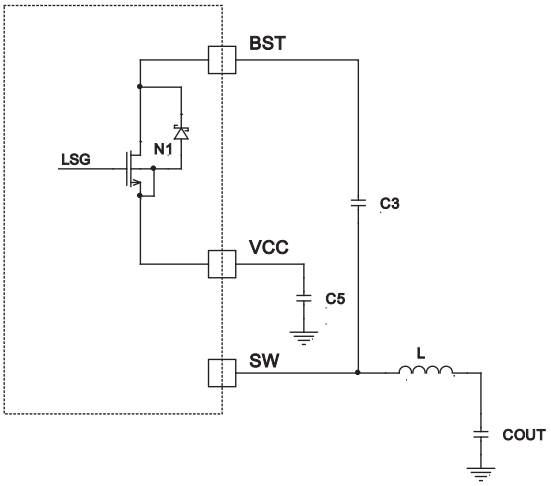


Figure 4: Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. The bootstrap capacitor is charged from VCC through N1 (Figure 4). N1 turns on when the LS-FET turns on and turns off when the LS-FET turns off.

Switching Frequency

MP28248 uses constant-on-time control because there is no dedicated oscillator in the IC. The input voltage is feed-forwarded to the on-time one-shot timer through the resistor R_7. The duty ratio is kept as V_{OUT}/V_{IN}, and the switching frequency is fairly constant over the input voltage range. The switching frequency can be determined with the following equation:

$$f_{SW}(kHz)=\frac{10^6}{\frac{9.3\times R_7(k\Omega)}{V_{IN}(V)-0.4}\times\frac{V_{IN}(V)}{V_{OUT}(V)}+t_{DELAY}(ns)} \quad (3)$$

Where t_{DELAY} is the comparator delay, and equals approximately 40ns.

MP28248 is optimized to operate at high switching frequency with high efficiency. High switching frequency makes it possible to use small-sized LC filter components to save system PCB space.

Jitter and FB Ramp Slope

Jitter occurs in both PWM and skip modes when the noise in the V_{FB} ripple propagates a delay to the HS-FET driver, as shown in Figure 5 and Figure 6. Jitter can affect system stability, with noise immunity proportional to the steepness of V_{FB}'s downward slope. However, V_{FB} ripple does not directly affect noise immunity.

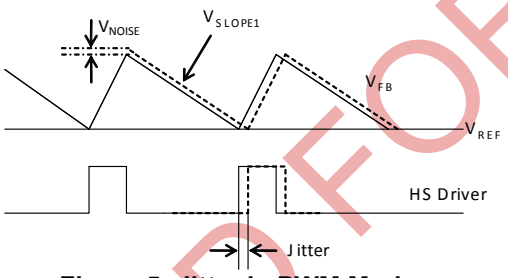


Figure 5: Jitter in PWM Mode

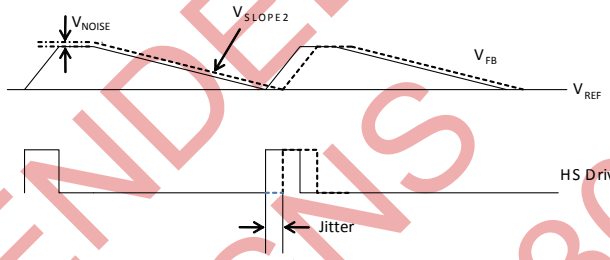


Figure 6: Jitter in Skip Mode

Ramp with Large ESR Capacitor

For POSCAP or other types of capacitors with large ESR as the output capacitors, the ESR ripple dominates the output ripple, and the slope on the FB is related to the ESR. Figure 7 shows an equivalent circuit in PWM mode with the HS-FET off and without an external ramp circuit. Go to the application information section for design recommendations for large ESR capacitors.

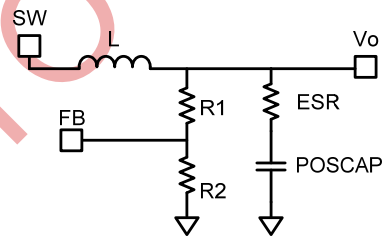


Figure 7: Simplified Circuit in PWM Mode without External Ramp Compensation

To realize a stable output without an external ramp, select an ESR value using the following equation:

$$R_{ESR}\geq\frac{\frac{t_{SW}}{0.7\times\pi}+\frac{t_{ON}}{2}}{C_{OUT}} \quad (4)$$

Where t_{SW} is the switching period.

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Ramp with small ESR Capacitor

When using ceramic output capacitors, the ESR is insufficient to stabilize the system and requires external ramp compensation. The application section discusses this in further depth.

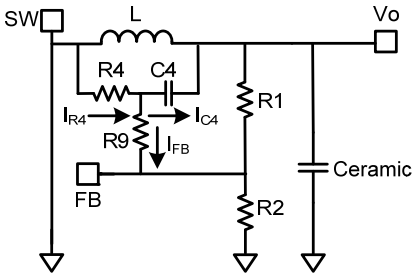


Figure 8: Simplified Circuit in PWM Mode with External Ramp Compensation

Figure 8 shows a simplified external ramp compensation circuit (R4 and C4) for PWM mode, with the HS-FET off. Chose R1, R2, and C4 of the external ramp to meet the following condition:

$$\frac{1}{2\pi \times f_{SW} \times C_4} < \frac{1}{5} \times \left(\frac{R_1 \times R_2}{R_1 + R_2} + R_9 \right) \quad (5)$$

Where:

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (6)$$

And V_{RAMP} on V_{FB} can then be estimated as:

$$V_{RAMP} = \frac{V_{IN} - V_{OUT}}{R_4 \times C_4} \times t_{ON} \times \frac{R_1 // R_2}{R_1 // R_2 + R_9} \quad (7)$$

The downward slope of the V_{FB} ripple then follows:

$$V_{SLOPE1} = \frac{-V_{RAMP}}{t_{off}} = \frac{-V_{OUT}}{R_4 \times C_4} \quad (8)$$

As shown in equation 8, either reduce R4 or C4 if there is instability in PWM mode. If C4 can not be reduced further due to limitation from equation 5, then reduce R4. For stable PWM operation, design V_{slope1} based on equation 9.

$$-V_{slope1} \geq \frac{\frac{t_{SW}}{0.7 \times \pi} + \frac{t_{ON}}{2} - R_{ESR} C_{OUT}}{2 \times L \times C_{OUT}} V_{OUT} + \frac{Io(mA)}{t_{SW} - t_{on}} \quad (9)$$

Where I_O is the load current.

In skip mode, the downward slope of the V_{FB} ripple is the same whether the external ramp is used or not. Figure 9 shows the simplified circuit of the skip mode when both the HS-FET and LS-FET are off.

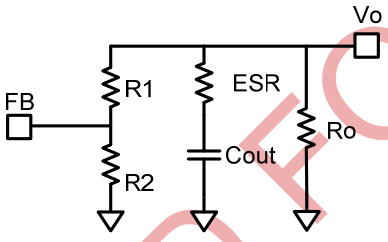


Figure 9: Simplified Circuit in Skip Mode

The downward slope of the V_{FB} ripple in skip mode can be determined as follow:

$$V_{SLOPE2} = \frac{-V_{REF}}{((R_1 + R_2) // Ro) \times C_{OUT}} \quad (10)$$

Where R_O is the equivalent load resistor.

As shown in Figure 6, V_{SLOPE2} in skip mode is lower than that is in the PWM mode, so generally the jitter in skip mode is larger. For a system with less jitter in light-load condition, select smaller V_{FB} resistors, though smaller resistors decrease the light-load efficiency.

When using a large-ESR capacitor on the output, add a 10µF or smaller ceramic capacitor in parallel to minimize ESL effects.

Soft-Start/Stop

The MP28248 employs a soft start/stop (SS) mechanism to ensure smooth output during power up and power shut-down. When the EN pin goes high, an internal current source (14µA) charges up the external SS cap. The SS cap voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once the SS voltage reaches V_{REF}, it continues to ramp up while the PWM comparator only compares the V_{REF} and the V_{FB}. At this point, the soft start finishes and it enters into steady state operation.

When the EN pin goes low, an internal 4.5µA current source discharges the external SS cap voltage. Once the SS voltage falls below the V_{REF}, the PWM comparator will only compare the V_{FB} to the SS voltage. The output voltage will decrease smoothly with the SS voltage until the voltage level zeros out at high load. The SS cap value can be determined as follows:

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$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (11)$$

If the output capacitors are large, avoid setting a short SS time to avoid hitting the current limit during SS. Table 1 lists SS times with different external capacitor value.

Table 1: Soft-Start Time vs. Capacitor Value

t_{SS}(ms)	C_{SS}(nF)
0.58	10
1.92	33
2.74	47
3.96	68
5.82	100

Over-Current Protection and Short-Circuit Protection

The MP28248 has cycle-by-cycle over-current limit control that monitors the inductor current during the HS-FET ON state. Once the inductor current exceeds the current limit, the HS-FET turns off. At the same time, the OCP timer—set at 50μs—starts. OCP will trigger if the current reaches or exceeds the current limit every cycle during those 50μs, and the MP28248 enters hiccup mode to periodically restart the part.

If V_{FB} < 0.5xV_{REF} and the current hits its limit, the MP28248 triggers the short-circuit protection (SCP) immediately and the MP28248 enters hiccup mode to periodically restart the part.

If V_{FB} < 0.5xV_{REF} and the inductor current peak value exceeds the set current limit threshold, MP28248 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output shorts to ground, greatly reducing the average short-circuit current and any thermal build-up to protect the regulator. The MP28248 exits the hiccup mode once the over current condition is removed.

Over-Voltage Protection (OVP)

MP28248 monitors the output voltage through the tap of a resistor divider connected to FB. When V_{FB} exceeds 1.25xV_{REF}, MP28248 triggers OVP. LS-FET is then left on, while the HS-FET is off. Exiting OVP requires power cycling the MP28248.

UVLO protection

MP28248 has UVLO protection. When V_{IN} exceeds the UVLO rising threshold voltage, the chip powers up. It shuts off when V_{IN} is less than the UVLO falling threshold voltage. This is non-latch protection.

Thermal Shutdown

The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (typically 150°C), the converter shuts off. This is non-latch protection. There is about 25°C hysteresis. Once the junction temperature drops to around 125°C, it initiates a soft start.

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APPLICATION INFORMATION

Setting the Output Voltage—Large ESR Capacitors

For applications that use electrolytic or POS capacitors as output capacitors, the output voltage is set by feedback resistors R1 and R2 as shown in Figure 10.

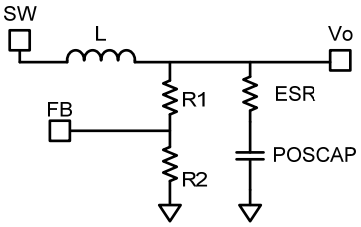


Figure 10: Simplified Circuit of POS Capacitor

To design the feedback circuit, first select a value for R2: a small R2 will lead to considerable quiescent current loss while a large R2 makes the FB pin noise-sensitive. For best results, choose a value between 5kΩ and 50kΩ for R2, and choose a comparatively larger R2 when V_O is low—e.g. 1.05V—and a smaller R2 when V_O is high. Then determine R1 using the following equation that takes the output ripple into consideration:

$$R_1 = \frac{V_{OUT} - \frac{1}{2}\Delta V_{OUT} - V_{REF}}{V_{REF}} \cdot R_2 \quad (12)$$

Where ΔV_{OUT} is the output ripple determined by equation 21.

Setting the Output Voltage—Small ESR Capacitors

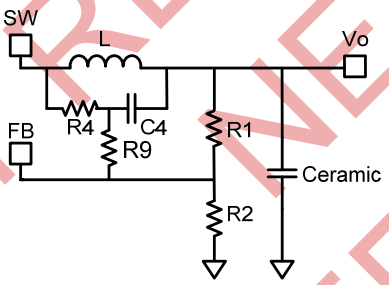


Figure 11: Simplified Circuit with Ceramic Capacitor

When using a low-ESR ceramic capacitors on the output, add an external voltage ramp to the FB pin. As Figure 11 shows, the resistive divider and the ramp voltage, V_{RAMP}, influences the output voltage. As discussed in the previous section, the V_{RAMP} can be calculated as per equation 7. Select an appropriate R2: typically in the range of 5kΩ to 50kΩ for most applications; use a relatively large R2 when V_O is low—e.g.,1.05V—and a small R2 when V_O is high. Determine R1 as follows:

$$R_1 = \frac{R_2}{\frac{V_{FB(AVG)}}{(V_{OUT} - V_{FB(AVG)})} \cdot R_2 - \frac{R_2}{R_4 + R_9}} \quad (13)$$

Where $V_{FB(AVG)}$ is the average value on the FB pin. Its value in skip mode is lower than in PWM mode, meaning load regulation is strictly conditional to the $V_{FB(AVG)}$. Line regulation is also related to $V_{FB(AVG)}$. For improved load or line regulation, use a lower V_{RAMP} as per equation 9.

For PWM mode, use the following equation to determine $V_{FB(AVG)}$:

$$V_{FB(AVG)} = V_{REF} + \frac{1}{2}V_{RAMP} \times \frac{R_1 // R_2}{R_1 // R_2 + R_9} \quad (14)$$

Typically R9 is 0Ω, but the appropriate non-zero value, as per equation 15, improves noise immunity. Select a value that is around 0.2×R1//R2 to minimize its effect on V_{RAMP}.

$$R_9 = \frac{1}{2\pi \times C_4 \times 2f_{SW}} \quad (15)$$

To simplify the calculation of R1 for equation 14, add a DC-blocking capacitor, C_{DC}, to filter the DC influence from R4 and R9. Figure 12 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. Approximating R1 is now much easier with C_{DC} using equation 16 for PWM mode.

$$R_1 = \frac{(V_{OUT} - V_{REF} - \frac{1}{2}V_{RAMP})}{V_{REF} + \frac{1}{2}V_{RAMP}} R_2 \quad (16)$$

Select a C_{DC} value at least 10× the value of C4 for better DC blocking, though do not select a C_{DC} that exceeds 0.47μF to avoid long start-up times. Larger C_{DC} values improve FB noise immunity when combined with smaller R1 and R2 values to limit system start-up effects. Note that even with C_{DC}, the load and line regulation are still V_{RAMP}-related.

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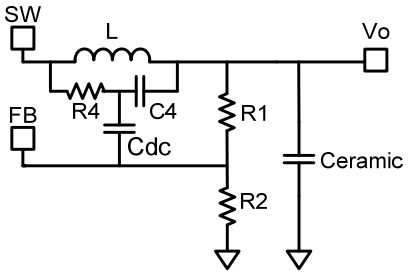


Figure 12: Simplified Ceramic Capacitor Circuit with DC Blocking Capacitor

Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the V_{IN} pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (17)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (18)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (19)$$

Under worst-case conditions where $V_{IN} = 2V_{OUT}$:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (20)$$

Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic or POSCAP capacitors for best results. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (21)$$

For ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (22)$$

The output voltage ripple caused by ESR is very small and requires an external ramp to stabilize the system. The external ramp can be generated through resistor R4 and capacitor C4 following equations 5, 8 and 9.

For POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system and therefore does not need an external ramp. Use a minimum ESR value of around 12mΩ to ensure stable converter operation. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (23)$$

The application design must also consider the maximum output capacitor value. If the output capacitor value is too high, the output voltage can't reach the designated value during the soft-start time, and then the device will fail to regulate. The maximum output capacitor value C_{O_MAX} can be approximately by:

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times t_{ss} / V_{OUT} \quad (24)$$

Where I_{LIM_AVG} is the average start-up current during soft-start period and t_{ss} is the soft-start time.

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Inductor

The inductor supplies constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger-value inductor will have a larger physical footprint, higher series resistance, and/or lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 40% of the maximum output current, and that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L=\frac{V_{OUT}}{f_{SW}\times\Delta I_L}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (25)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated by:

$$I_{LP}=I_{OUT}+\frac{V_{OUT}}{2f_{SW}\times L}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (26)$$

Design Example

Some design examples with typical outputs are provided in the following tables:

Table 2: 1.2V V_{OUT} (L = 2µH)

V_{IN} (V)	V_{OUT} (V)	R7 (Ω)	R4 (Ω)	C4 (F)	R1 (Ω)	R2 (Ω)	F_{SW} (Hz)
12	1.2	301k	806k	220p	17.4k	40.2k	440k

Table 3: 1.8V V_{OUT} (L = 2µH)

V_{IN} (V)	V_{OUT} (V)	R7 (Ω)	R4 (Ω)	C4 (F)	R1 (Ω)	R2 (Ω)	F_{SW} (Hz)
12	1.8	402k	649k	220p	30k	24.3k	500k

Table 4: 2.5V V_{OUT} (L = 2µH)

V_{IN} (V)	V_{OUT} (V)	R7 (Ω)	R4 (Ω)	C4 (F)	R1 (Ω)	R2 (Ω)	F_{SW} (Hz)
12	2.5	499k	499k	330p	21.5k	10k	544k

Table 5: 3.3V V_{OUT} (L = 4.7µH)

V_{IN} (V)	V_{OUT} (V)	R7 (Ω)	R4 (Ω)	C4 (F)	R1 (Ω)	R2 (Ω)	F_{SW} (Hz)
12	3.3	680k	806k	330p	31.6k	10k	520k

Table 6: 5V V_{OUT} (L = 8µH)

V_{IN} (V)	V_{OUT} (V)	R7 (Ω)	R4 (Ω)	C4 (F)	R1 (Ω)	R2 (Ω)	F_{SW} (Hz)
12	5	1M	1.2M	220p	53.6k	10k	544k

The detailed application schematic is shown in Figure 13. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more possible applications of this device, please refer to related Evaluation Board Data Sheets.

Typical Application Schematic

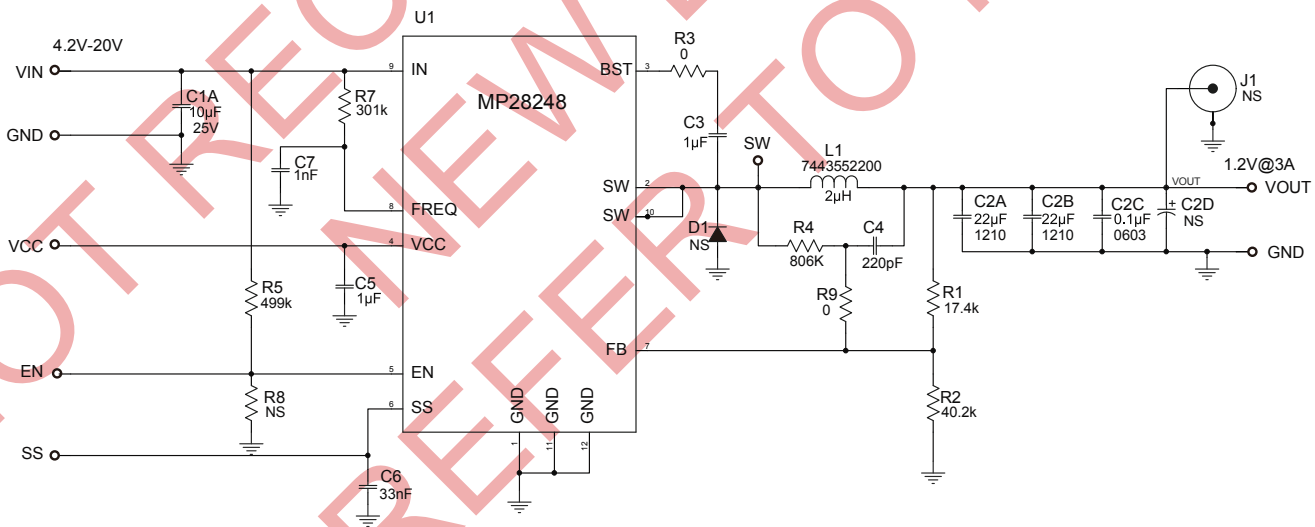


Figure 13: Detailed Application Schematic

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Layout Recommendation

1) The high current paths (GND, IN, and SW) should be placed very close to the device with short, wide, and direct traces.
2) Put the input capacitors as close to the IN and GND pins as possible.
3) Put the decoupling capacitor as close to the V_{CC} and GND pins as possible.
4) Keep the switching node SW short and away from the feedback network.

The external feedback resistors should be placed next to the FB pin. Make sure that there is no via on the FB trace.

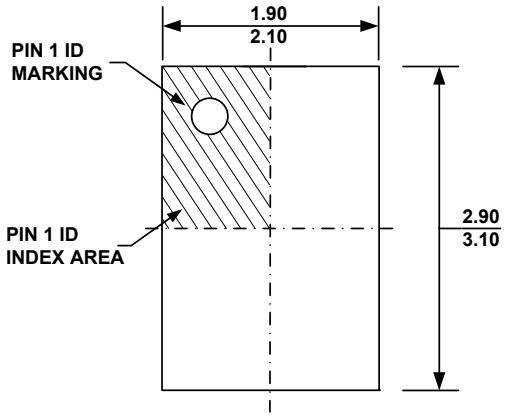
5) Keep the BST voltage path (BST, R3, C3, and SW) as short as possible.
6) Use a four-layer board to achieve better thermal performance.

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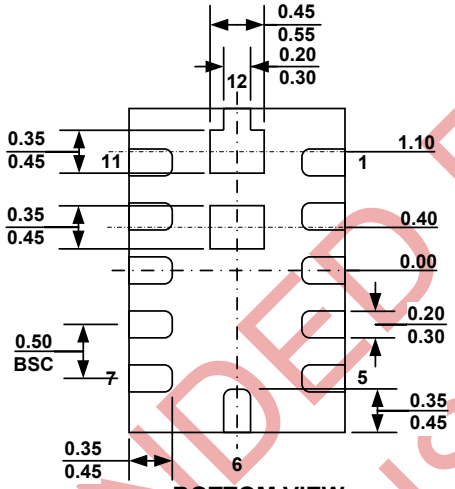
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PACKAGE INFORMATION

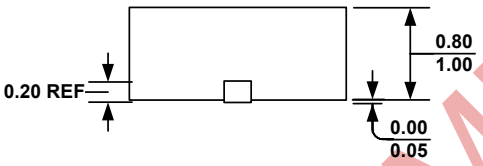
QFN12 (2x3mm)



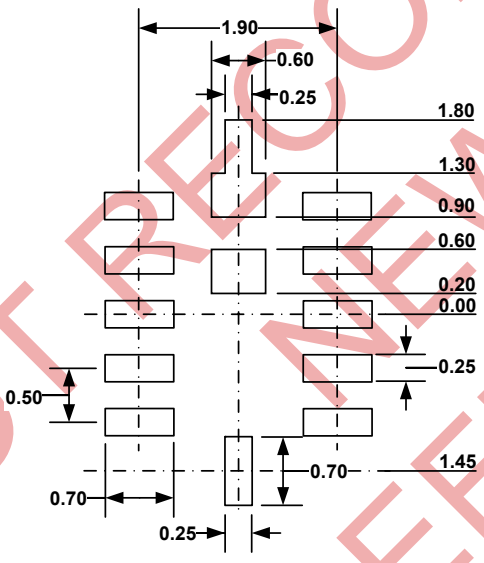
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE DRAWING IS JEDEC MO-220
5) DRAWING IS NOT TO SCALE.

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