MX575ABC50M0000

Ultra-Low Jitter 50MHz LVCMOS XO

ClockWorks® FUSION

General Description

The MX575ABC50M0000 is an ultra-low phase jitter XO with LVCMOS output optimized for high line rate applications.

Features

- 50MHz LVCMOS
- Typical phase noise:
  - 96fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 7mm x 5mm LGA package

Absolute Maximum Ratings[1]

Supply Voltage (VIN).....+4.6V
Lead Temperature (soldering, 10s).....260°C
Case Temperature.....115°C
Storage Temperature (T_S).....-65°C to +125°C
ESD Machine Model.....200V
ESD Rating (HBM).....2kV

Operating Ratings[2]

Supply Voltage (VIN).....+2.375V to +3.63V
Ambient Temperature (TA).....-40°C to +85°C
Junction Thermal Resistance
LGA (T_{JA}) Still Air.....53°C/W

Electrical Characteristics

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, output terminated with 50 Ohms to VDD/2.[3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				95	mA
F0	Center Frequency			50		MHz
	Frequency Stability	Note 4			±50	ppm
Øj	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		135 96		fsRMS
Tstart	Start-Up Time				20	ms
TR/TF	Rise/Fall time		100		500	ps
	Duty Cycle		45		55	%
VIH	Input High Voltage	3.3V Operation	2		VDD + 0.3	V
VIL	Input Low Voltage	3.3V Operation	-0.3		0.8	V
VOH	Output High Voltage	LVCMOS output levels	VDD - 0.8			V
VOL	Output Low Voltage	LVCMOS output levels			0.6	V

Notes:
1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. Guaranteed after thermal equilibrium.
4. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

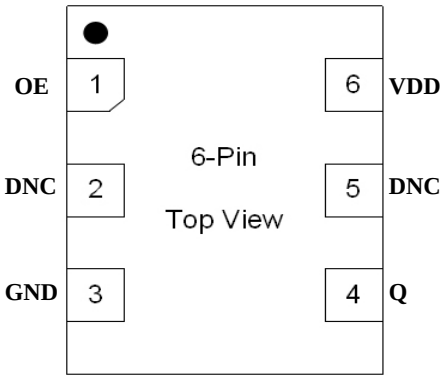
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Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX575ABC50M0000	MX575AB	C50M0000	Tube	6-Pin 7mm x 5mm LGA
MX575ABC50M0000-TR	MX575AB	C50M0000	Tape and Reel	6-Pin 7mm x 5mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVCMOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, DNC	O, SE	LVCMOS	Clock Output Frequency = 50MHz
6	VDD	PWR		Power Supply

Environmental Specifications

Thermal Shock	MIL-STD-883, Method 1011, Condition A
Moisture Resistance	MIL-STD-883, Method 1004
Mechanical Shock	MIL-STD-883, Method 2002, Condition E
Mechanical Vibration	MIL-STD-883, Method 2007, Condition C
Resistance to Soldering Heat	J-STD-020C, Table 5-2 Pb-free devices (except 2 cycles max)
Hazardous Substance	Pb-Free / RoHS / Green Compliant
Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Terminal Strength	MIL-STD-883, Method 2004, Test Condition D
Gross Leak	MIL-STD-883, Method 1014, Condition C
Fine Leak	MIL-STD-883, Method 1014, Condition A2, R1=2x10-8 atm cc/s
Solvent Resistance	MIL-STD-202, Method 215

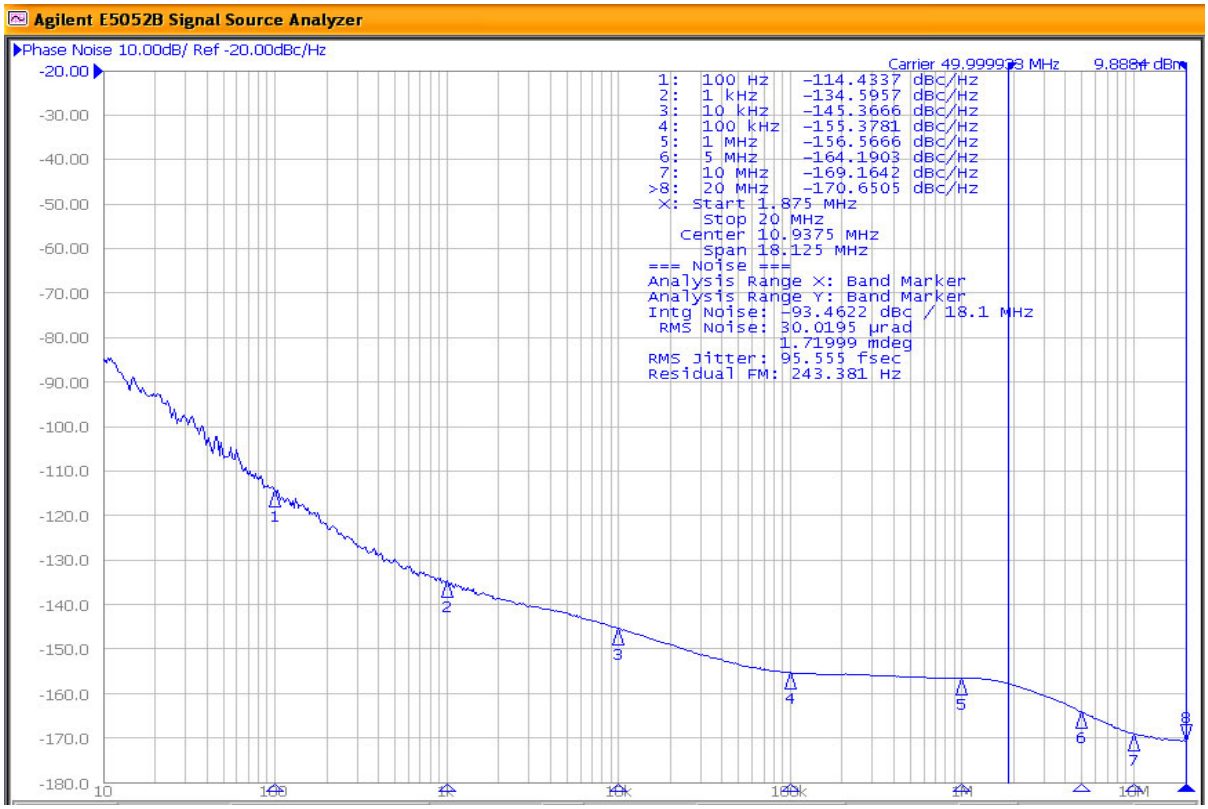


Figure 1. LVCMOS Output 50MHz 1.875kHz-20MHz 96fs

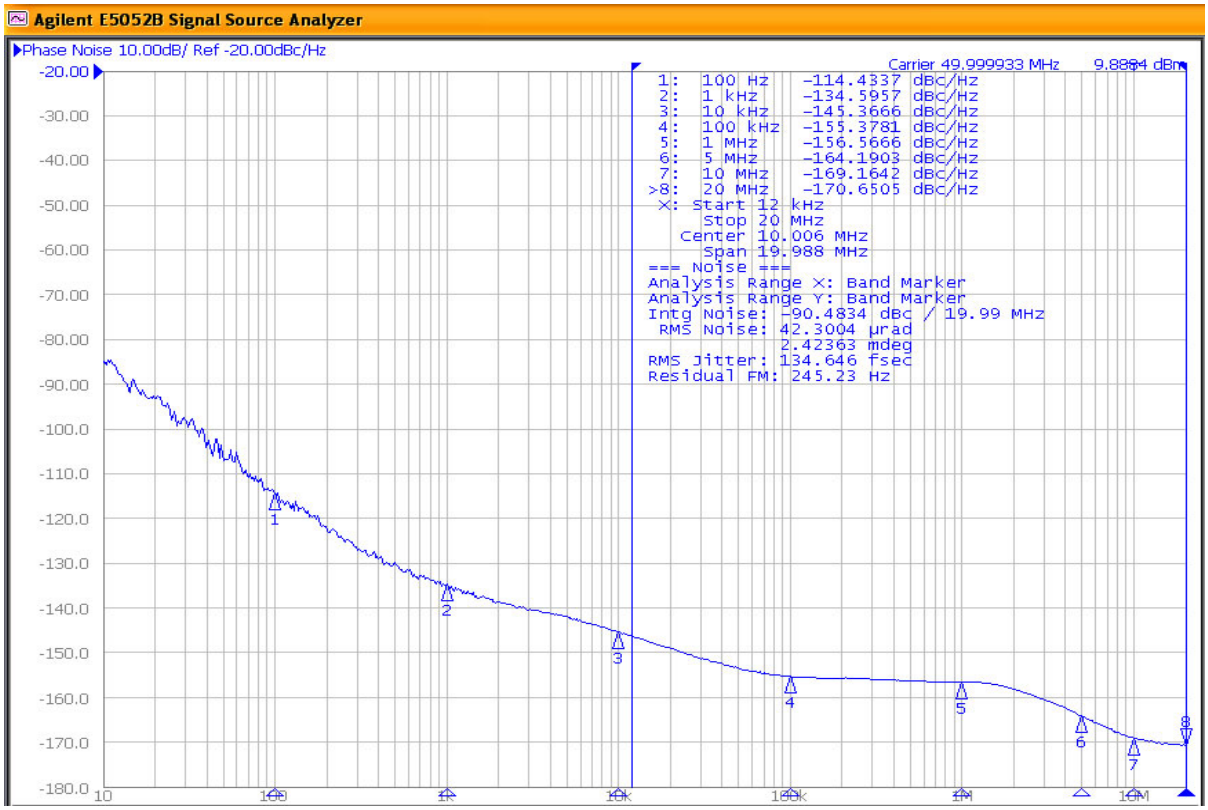
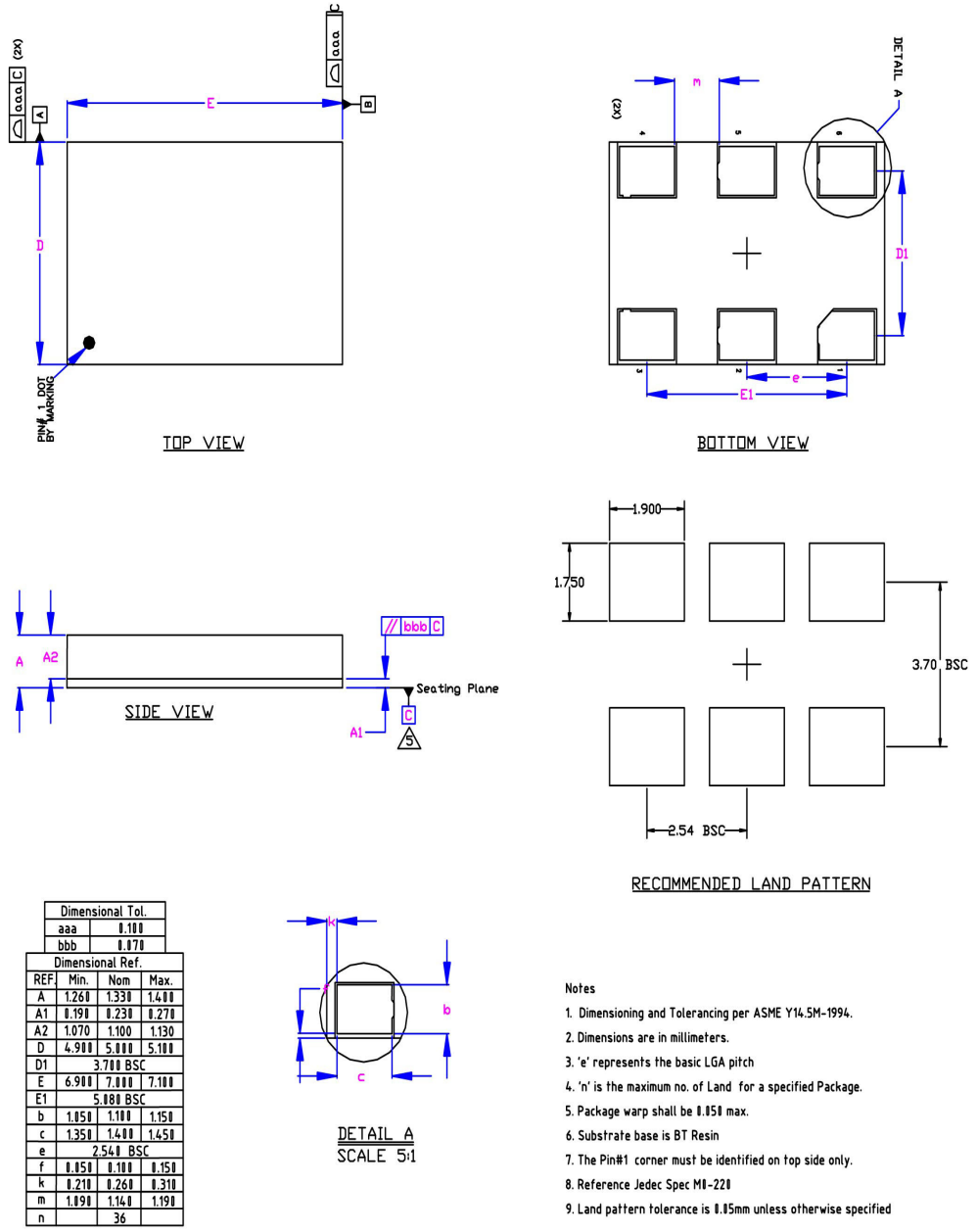


Figure 2. LVCMOS Output 50MHz 12kHz-20MHz 135fs

Package Information and Recommended Land Pattern for 6-Pin LGA[3]



Dimensional Tol.	
aaa	0.100
bbb	0.070

Dimensional Ref.			
REF.	Min.	Nom	Max.
A	1.260	1.330	1.400
A1	0.190	0.230	0.270
A2	1.070	1.100	1.130
D	4.900	5.000	5.100
D1	3.700 BSC		
E	6.900	7.000	7.100
E1	5.080 BSC		
b	1.050	1.100	1.150
c	1.350	1.400	1.450
e	2.540 BSC		
f	0.050	0.100	0.150
k	0.210	0.260	0.310
m	1.090	1.140	1.190
n		36	

Notes

1. Dimensioning and Tolerancing per ASME Y14.5M-1994.
2. Dimensions are in millimeters.
3. 'e' represents the basic LGA pitch
4. 'n' is the maximum no. of Land for a specified Package.
5. Package warp shall be 0.050 max.
6. Substrate base is BT Resin
7. The Pin#1 corner must be identified on top side only.
8. Reference Jedec Spec MO-220
9. Land pattern tolerance is 0.05mm unless otherwise specified

6-Pin LGA (7x5mm)

Note:

3. Package information is correct as of the publication date. For updates and most current information, go to www.microchip.com.

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