CDCLVP2102 Four-LVPECL Output, High-Performance Clock Buffer

1 Features

- Dual 1:2 Differential Buffer
- Two Clock Inputs
- Universal Inputs Can Accept LVPECL, LVDS, LVCMOS/LVTTL
- Four LVPECL Outputs
- Maximum Clock Frequency: 2 GHz
- Maximum Core Current Consumption: 48 mA
- Very Low Additive Jitter: <100 fs, RMS in 10-kHz to 20-MHz Offset Range
- 2.375-V to 3.6-V Device Power Supply
- Maximum Propagation Delay: 450 ps
- Maximum Within Bank Output Skew: 10 ps
- LVPECL Reference Voltage, V_{AC_REF}, Available for Capacitive-Coupled Inputs
- Industrial Temperature Range: –40°C to +85°C
- Supports 105°C PCB Temperature (Measured with a Thermal Pad)
- Available in 3-mm × 3-mm, 16-Pin VQFN (RGT) Package
- ESD Protection Exceeds 2000 V (HBM)

2 Applications

- Wireless Communications
- Telecommunications/Networking
- Medical Imaging
- Test and Measurement Equipment

3 Description

The CDCLVP2102 is a highly versatile, low additive jitter buffer that can generate four copies of LVPECL clock outputs from two LVPECL, LVDS, or LVCMOS inputs for a variety of communication applications. It has a maximum clock frequency up to 2 GHz. Each buffer block consists of one input that feeds two LVPECL outputs. The overall additive jitter performance is less than 0.1 ps, RMS from 10 kHz to 20 MHz, and overall output skew is as low as 10 ps, making the device a perfect choice for use in demanding applications.

The CDCLVP2102 clock buffer distributes two clock inputs (IN0, IN1) to four pairs of differential LVPECL clock outputs (OUT0, OUT3) with minimum skew for clock distribution. Each buffer block consists of one input that feeds two LVPECL clock outputs. The inputs can be LVPECL, LVDS, or LVCMOS/LVTTL.

The CDCLVP2102 is specifically designed for driving 50-Ω transmission lines. When driving the inputs in single-ended mode, the LVPECL bias voltage (V_{AC_REF}) should be applied to the unused negative input pin. However, for high-speed performance up to 2 GHz, differential mode is strongly recommended.

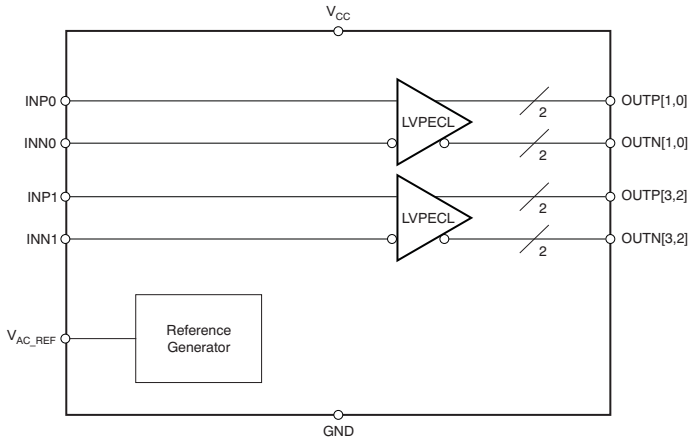
The CDCLVP2102 is characterized for operation from –40°C to +85°C and is available in a 3-mm × 3-mm, VQFN-16 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCLVP2102	VQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2011) to Revision C **Page**

- Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Added support for 105°C thermal pad temperature ... 1
- Deleted *Device Comparison* table; information in POA ... 1
- Changed order of *Pin Functions* table to alphabetical by pin name ... 4
- Added PCB temperature to *Recommended Operating Conditions* ... 5
- Added V_{OH} specification for T_{PCB}≤ 105ºC in *Electrical Characteristics: LVPECL Output, at V_{CC} = 2.375 V to 2.625 V* ... 6
- Added V_{OL} specification for T_{PCB}≤ 105ºC in *Electrical Characteristics: LVPECL Output, at V_{CC} = 2.375 V to 2.625 V* ... 6
- Added I_{EE} specification for T_{PCB}≤ 105ºC in *Electrical Characteristics: LVPECL Output, at V_{CC} = 2.375 V to 2.625 V* ... 6
- Added I_{CC} specification for T_{PCB}≤ 105ºC in *Electrical Characteristics: LVPECL Output, at V_{CC} = 2.375 V to 2.625 V* ... 6
- Added V_{OH} specification for T_{PCB}≤ 105ºC in *Electrical Characteristics: LVPECL Output, at V_{CC} = 3 V to 3.6 V* ... 6
- Added V_{OL} specification for T_{PCB}≤ 105ºC in *Electrical Characteristics: LVPECL Output, at V_{CC} = 3 V to 3.6 V* ... 7
- Added I_{EE} specification for T_{PCB}≤ 105ºC in *Electrical Characteristics: LVPECL Output, at V_{CC} = 3 V to 3.6 V* ... 7
- Added I_{CC} specification for T_{PCB}≤ 105ºC in *Electrical Characteristics: LVPECL Output, at V_{CC} = 3 V to 3.6 V* ... 7
- Added t_{RJIT} for f $_{OUT}$ = 100 MHz, Input AC coupled, V_{ICM} = V_{AC_REF}, 12 kHz to 20 MHz ... 8
- Added t_{RJIT} for f_{OUT} = 122.88 MHz, Input AC coupled, V_{ICM} = V_{AC_REF}, 12 kHz to 20 MHz ... 8
- Added t_{RJIT} for f_{OUT} = 156.25 MHz, Input AC coupled, V_{ICM} = V_{AC_REF}, 12 kHz to 20 MHz ... 8
- Added t_{RJIT} for f_{OUT} = 312.5 MHz, Input AC coupled, V_{ICM} = V_{AC_REF}, 12 kHz to 20 MHz ... 8
- Added *100 MHz Wenzel oscillator, Input slew rate = 0.9 V/ns (single-ended)* footnote ... 8

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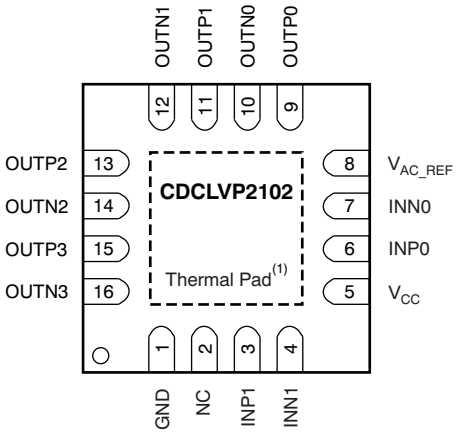
Changes from Revision A (October 2009) to Revision B **Page**

- Revised description of pin 8 in 4
- Corrected V_{IL} parameter description in *Electrical Characteristics* table for LVCMOS input 6
- Added footnote (2) to *Electrical Characteristics: LVPECL Output, at V_{CC} = 2.375 V to 2.625 V* 6
- Changed recommended resistor values in Figure 12(a) 14
- Changed recommended resistor values in Figure 16 16
- Changed recommended resistor values in Figure 17 16

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5 Pin Configuration and Functions

RGT Package
16-Pin VQFN
Top View



Thermal pad must be soldered to ground.

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	1	Ground	Device ground
INP0, INN0	6, 7	Input	Differential input pair or single-ended input no. 0
INP1, INN1	3, 4	Input	Differential input pair or single-ended input no. 1
OUTP0 OUTN0	9, 10	Output	Differential LVPECL output pair no. 0
OUTP1, OUTN1	11, 12	Output	Differential LVPECL output pair no. 1
OUTP2, OUTN2	13, 14	Output	Differential LVPECL output pair no. 2
OUTP3, OUTN3	15, 16	Output	Differential LVPECL output pair no. 3
V_{AC_REF}	8	Output	Bias voltage output for capacitive-coupled input pair no. 0. Do not use V_{AC_REF} at V_{CC} < 3 V. If used, TI recommends using a 0.1-µF capacitor to GND on this pin. The output current is limited to 2 mA.
V_{CC}	5	Power	2.5-V or 3.3-V supply for the device
NC	2	—	Do not connect

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	–0.5	4.6	V
V_{IN}	Input voltage(3)	–0.5	V_{CC} + 0.5	V
V_{OUT}	Output voltage(3)	–0.5	V_{CC} + 0.5	V
I_{IN}	Input current		20	mA
I_{OUT}	Output current		50	mA
T_A	Specified free-air temperature (no airflow)	–40	85	°C
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All supply voltages must be supplied simultaneously.
(3) The input and output negative voltage ratings may be exceeded if the input clamp-current and output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.375	2.5/3.3	3.60	V
T_A	Ambient temperature	–40		85	°C
T_{PCB}	PCB temperature (measured at thermal pad)		105		°C

6.4 Thermal Information

THERMAL METRIC(1)(2)(3)		CDCLVP2102 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (0 LFM)	51.8(4)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79	°C/W
$R_{\theta JP}$(5)	Junction-to-pad thermal resistance	6.12(4)	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.12	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The package thermal resistance is calculated in accordance with JESD 51 and JEDEC 2S2P (high-K board).
(3) Connected to GND with four thermal vias (0.3-mm diameter).
(4) 2 × 2 vias on pad
(5) $R_{\theta JP}$ (junction-to-pad) is used for the VQFN package, because the primary heat flow is from the junction to the GND pad of the VQFN package.

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6.5 Electrical Characteristics: LVCMOS Input, at V_{CC} = 2.375 V to 3.6 V

at T_A = –40°C to +85°C and T_{PCB} ≤ 105°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{IN}	Input frequency				200	MHz
V_{th}	Input threshold voltage	External threshold voltage applied to complementary input	1.1		1.8	V
V_{IH}	Input high voltage		V_{th} + 0.1		V_{CC}	V
V_{IL}	Input low voltage		0		V_{th} – 0.1	V
I_{IH}	Input high current	V_{CC} = 3.6 V, V_{IH} = 3.6 V			40	µA
I_{IL}	Input low current	V_{CC} = 3.6 V, V_{IL} = 0 V			–40	µA
ΔV/ΔT	Input edge rate	20% to 80%	1.5			V/ns
I_{CAP}	Input capacitance			5		pF

(1) Figure 5 and Figure 6 show DC test setup.

6.6 Electrical Characteristics: Differential Input, at V_{CC} = 2.375 V to 3.6 V

at T_A = –40°C to +85°C and T_{PCB} ≤ 105°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{IN}	Input frequency	Clock input			2000	MHz
$V_{IN, DIFF, PP}$	Differential input peak-peak voltage	f_{IN} ≤ 1.5 GHz	0.1		1.5	V
		1.5 GHz ≤ f_{IN} ≤ 2 GHz	0.2		1.5	V
V_{ICM}	Input common-mode level		1		V_{CC} – 0.3	V
I_{IH}	Input high current	V_{CC} = 3.6 V, V_{IH} = 3.6 V			40	µA
I_{IL}	Input low current	V_{CC} = 3.6 V, V_{IL} = 0 V			–40	µA
ΔV/ΔT	Input edge rate	20% to 80%	1.5			V/ns
I_{CAP}	Input capacitance			5		pF

(1) Figure 7 and Figure 8 show DC test setup. Figure 9 shows AC test setup.

6.7 Electrical Characteristics: LVPECL Output, at V_{CC} = 2.375 V to 2.625 V

at T_A = –40°C to +85°C and T_{PCB} ≤ 105°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output high voltage	T_A = –40°C to 85°C	V_{CC} – 1.26		V_{CC} – 0.9	V
		T_{PCB} ≤ 105°C	V_{CC} – 1.26	=	V_{CC} – 0.83	
V_{OL}	Output low voltage	T_A = –40°C to 85°C	V_{CC} – 1.7		V_{CC} – 1.3	V
		T_{PCB} ≤ 105°C	V_{CC} – 1.7		V_{CC} – 1.25	
$V_{OUT, DIFF, PP}$	Differential output peak-peak voltage	f_{IN} ≤ 2 GHz	0.5		1.35	V
V_{AC_REF}	Input bias voltage (2)	I_{AC_REF} = 2 mA	V_{CC} – 1.6		V_{CC} – 1.1	V
I_{EE}	Supply internal current	Outputs unterminated, T_A ≤ 85°C			48	mA
		Outputs unterminated, T_{PCB} ≤ 105°C			49	
I_{CC}	Output and internal supply current	All outputs terminated, 50 Ω to V_{CC} – 2 T_A ≤ 85°C			173	mA
		All outputs terminated, 50 Ω to V_{CC} – 2 T_{PCB} ≤ 105°C			189	

(1) Figure 10 and Figure 11 show DC and AC test setup.
(2) Internally generated bias voltage (V_{AC_REF}) is for 3.3-V operation only. TI recommends applying externally generated bias voltage for V_{CC} < 3 V.

6.8 Electrical Characteristics: LVPECL Output, at V_{CC} = 3 V to 3.6 V

at T_A = –40°C to +85°C and T_{PCB} ≤ 105°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output high voltage	T_A ≤ 85°C	V_{CC} – 1.26		V_{CC} – 0.9	V
		T_{PCB} ≤ 105°C	V_{CC} – 1.26		V_{CC} – 0.85	

(1) Figure 10 and Figure 11 show DC and AC test setup.

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Electrical Characteristics: LVPECL Output, at V_{CC} = 3 V to 3.6 V (continued)

at T_A = –40°C to +85°C and T_{PCB} ≤ 105°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output low voltage	T_A ≤ 85°C	V_{CC} – 1.7		V_{CC} – 1.3	V
		T_{PCB} ≤ 105°C	V_{CC} – 1.7		V_{CC} – 1.3	
$V_{OUT, DIFF, PP}$	Differential output peak-peak voltage	f_{IN} ≤ 2 GHz	0.65		1.35	V
V_{AC_REF}	Input bias voltage	I_{AC_REF} = 2 mA	V_{CC} – 1.6		V_{CC} – 1.1	V
I_{EE}	Supply internal current	Outputs unterminated, T_A ≤ 85°C			48	mA
		Outputs unterminated, T_{PCB} ≤ 105°C			49	
I_{CC}	Output and internal supply current	All outputs terminated, 50 Ω to V_{CC} – 2 T_A ≤ 85°C			173	mA
		All outputs terminated, 50 Ω to V_{CC} – 2 T_{PCB} ≤ 105°C			189	

6.9 Timing Requirements, at V_{CC} = 2.375 V to 2.625 V

Refer to Figure 1 and Figure 2.

			MIN	NOM	MAX	UNIT
t_{PD}	Propagation delay	$V_{IN, DIFF, PP}$ = 0.1 V			450	ps
		$V_{IN, DIFF, PP}$ = 0.3 V			450	
$t_{SK,PP}$	Part-to-part skew				100	ps
t_{SK,O_WB}	Within bank output skew				10	ps
t_{SK,O_BB}	Bank-to-bank output skew	Both inputs have equal skew			15	ps
$t_{SK,P}$	Pulse skew (with 50% duty cycle input)	Crossing-point-to-crossing-point distortion, f_{OUT} = 100 MHz	–50		50	ps
t_{RJIT}	Random additive jitter (with 50% duty cycle input)	f_{OUT} = 100 MHz, $V_{IN,SE}$ = V_{CC}, V_{th} = 1.25 V, 10 kHz to 20 MHz		0.089		ps, RMS
		f_{OUT} = 100 MHz, $V_{IN,SE}$ = 0.9 V, V_{th} = 1.1 V, 10 kHz to 20 MHz		0.093		ps, RMS
		f_{OUT} = 2 GHz, $V_{IN,DIFF,PP}$ = 0.2 V, V_{ICM} = 1 V, 10 kHz to 20 MHz		0.037		ps, RMS
		f_{OUT} = 100 MHz, $V_{IN,DIFF,PP}$ = 0.15 V, V_{ICM} = 1 V, 10 kHz to 20 MHz		0.094		ps, RMS
		f_{OUT} = 100 MHz, $V_{IN,DIFF,PP}$ = 1 V, V_{ICM} = 1 V, 10 kHz to 20 MHz		0.091		ps, RMS
		$f_{OUT,8}$ = 500 MHz, $V_{IN,DIFF,PP,0}$ = 0.15 V, $V_{ICM,\ 0}$ = 1 V, $f_{OUT,\ 7}$ = 62.5 MHz, $V_{IN,SE,1}$ = V_{CC}, $V_{th,\ 1}$ = V_{CC}/2		–52.5		dBc
P_{SPUR}	Coupling on differential OUT8 from OUT7 in the frequency spectrum of $f_{OUT,\ 8}$ ±($f_{OUT,\ 8}$/2) with synchronous inputs	$f_{OUT,8}$ = 500 MHz, $V_{IN,DIFF,PP,0}$ = 0.15 V, $V_{ICM,\ 0}$ = 1 V, $f_{OUT,\ 7}$ = 62.5 MHz, $V_{IN,DIFF,PP,1}$ = 1 V, $V_{ICM,\ 1}$ = 1 V		–66.8		dBc
		$f_{OUT,8}$ = 500 MHz, $V_{IN,DIFF,PP,0}$ = 0.15 V, $V_{ICM,\ 0}$ = 1 V, $f_{OUT,\ 7}$ = 15.625 MHz, $V_{IN,SE,1}$ = V_{CC}, $V_{th,\ 1}$ = V_{CC}/2		–52		
		$f_{OUT,8}$ = 500 MHz, $V_{IN,DIFF,PP,0}$ = 0.15 V, $V_{ICM,\ 0}$ = 1 V, $f_{OUT,\ 7}$ = 15.625 MHz, $V_{IN,DIFF,PP,1}$ = 1 V, $V_{ICM,\ 1}$ = 1 V		–66.4		
t_R/t_F	Output rise/fall time	20% to 80%			200	ps

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6.10 Timing Requirements, at V_{CC} = 3 V to 3.6 V

Refer to Figure 1 and Figure 2.

			MIN	NOM	MAX	UNIT
t_{PD}	Propagation delay	$V_{IN,\ DIFF,\ PP}$ = 0.1 V			450	ps
		$V_{IN,\ DIFF,\ PP}$ = 0.3 V			450	
$t_{SK,PP}$	Part-to-part skew				100	ps
t_{SK,O_WB}	Within bank output skew				10	ps
t_{SK,O_BB}	Bank-to-bank output skew	Both inputs have equal skew			15	ps
$t_{SK,P}$	Pulse skew (with 50% duty cycle input)	Crossing-point-to-crossing-point distortion, f_{OUT} = 100 MHz	–50		50	ps
t_{RJIT}	Random additive jitter (with 50% duty cycle input)	f_{OUT} = 100 MHz,(1) $V_{IN,SE}$ = V_{CC}, V_{th} = 1.65 V, 10 kHz to 20 MHz		0.081		ps, RMS
		f_{OUT} = 100 MHz,(1) $V_{IN,SE}$ = 0.9 V, V_{th} = 1.1 V, 10 kHz to 20 MHz		0.097		ps, RMS
		f_{OUT} = 2 GHz, $V_{IN,DIFF,PP}$ = 0.2 V, V_{ICM} = 1 V, 10 kHz to 20 MHz		0.05		ps, RMS
		f_{OUT} = 100 MHz,(1) $V_{IN,DIFF,PP}$ = 0.15 V, V_{ICM} = 1 V, 10 kHz to 20 MHz		0.098		ps, RMS
		f_{OUT} = 100 MHz,(1) $V_{IN,DIFF,PP}$ = 1 V, V_{ICM} = 1 V, 10 kHz to 20 MHz		0.095		ps, RMS
		$f_{OUT,8}$ = 500 MHz, $V_{IN,DIFF,PP,0}$ = 0.15 V, $V_{ICM,\ 0}$ = 1 V, $f_{OUT,\ 7}$ = 62.5 MHz, $V_{IN,SE,1}$ = V_{CC}, $V_{th,\ 1}$ = V_{CC}/2		–55.3		dBc
		f_{OUT} = 100 MHz(2), Input AC-coupled, V_{ICM} = V_{AC_REF}, 12 kHz to 20 MHz		0.068		ps, RMS
		f_{OUT} = 122.88 MHz(3), Input AC-coupled, V_{ICM} = V_{AC_REF}, 12 kHz to 20 MHz		0.056		ps, RMS
		f_{OUT} = 156.25 MHz(4), Input AC-coupled, V_{ICM} = V_{AC_REF}, 12 kHz to 20 MHz		0.047		ps, RMS
		f_{OUT} = 312.5 MHz(5), Input AC-coupled, V_{ICM} = V_{AC_REF}, 12 kHz to 20 MHz		0.026		ps, RMS
P_{SPUR}	Coupling on differential OUT8 from OUT7 in the frequency spectrum of $f_{OUT,\ 8}$ ±($f_{OUT,\ 8}$/2) with synchronous inputs	$f_{OUT,8}$ = 500 MHz, $V_{IN,DIFF,PP,0}$ = 0.15 V, $V_{ICM,\ 0}$ = 1 V, $f_{OUT,\ 7}$ = 62.5 MHz, $V_{IN,SIFF,PP,1}$ = 1 V, $V_{ICM,\ 1}$ = 1 V		–65.1		dBc
		$f_{OUT,8}$ = 500 MHz, $V_{IN,DIFF,PP,0}$ = 0.15 V, $V_{ICM,\ 0}$ = 1 V, $f_{OUT,\ 7}$ = 15.625 MHz, $V_{IN,SE,1}$ = V_{CC}, $V_{th,\ 1}$ = V_{CC}/2		–54.7		
		$f_{OUT,8}$ = 500 MHz, $V_{IN,DIFF,PP,0}$ = 0.15 V, $V_{ICM,\ 0}$ = 1 V, $f_{OUT,\ 7}$ = 15.625 MHz, $V_{IN,DIFF,PP,1}$ = 1 V, $V_{ICM,\ 1}$ = 1 V		–66.7		
t_R/t_F	Output rise/fall time	20% to 80%			200	ps

(1) 100-MHz Wenzel oscillator, Input slew rate = 0.9 V/ns (single-ended)
(2) 100-MHz Wenzel oscillator, Input slew rate = 3.4 V/ns (differential)
(3) 122.88-MHz Rohde & Schwarz SMA100A, Input slew rate = 3.7 V/ns (differential)
(4) 156.25-MHz Crystek CPRO33 oscillator, Input slew rate = 2.9 V/ns (differential)
(5) 312.5-MHz Rohde & Schwarz SMA100A, Input slew rate = 4 V/ns (differential)

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Figure 1 shows the output voltage and rise/fall time. Output and part-to-part skew are shown in Figure 2.

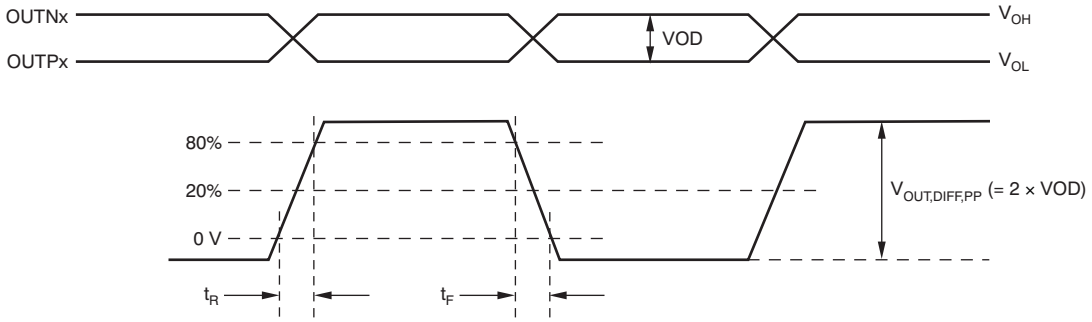
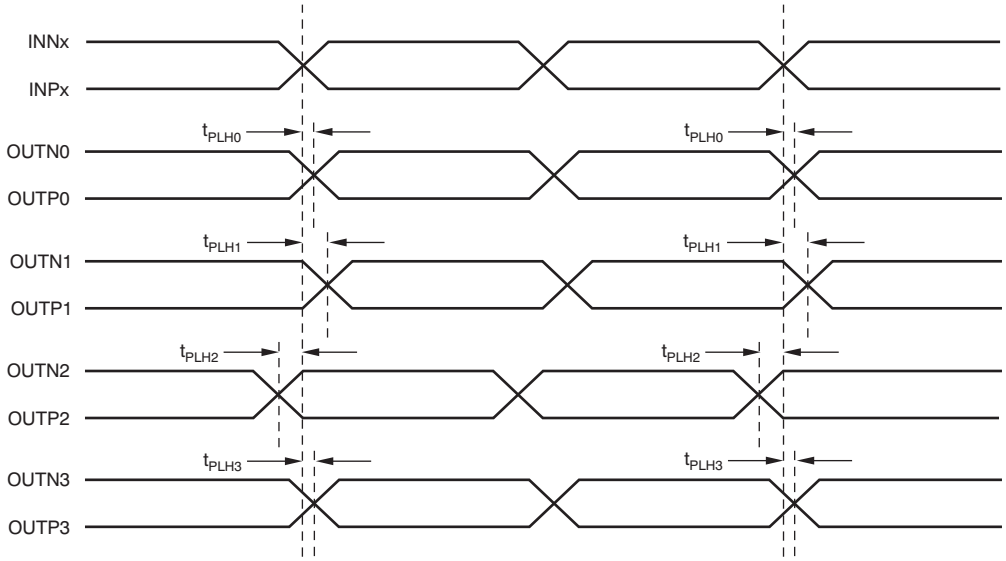


Figure 1. Output Voltage and Rise/Fall Time



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest t_{PLHn} (n = 0, 1, 2, 3), or as the difference between the fastest and the slowest t_{PHLn} (n = 0, 1, 2, 3).

(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest t_{PLHn} (n = 0, 1, 2, 3) across multiple devices, or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1, 2, 3) across multiple devices.

Figure 2. Output and Part-to-Part Skew

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6.11 Typical Characteristics

at T_A = –40°C to +85°C (unless otherwise noted)

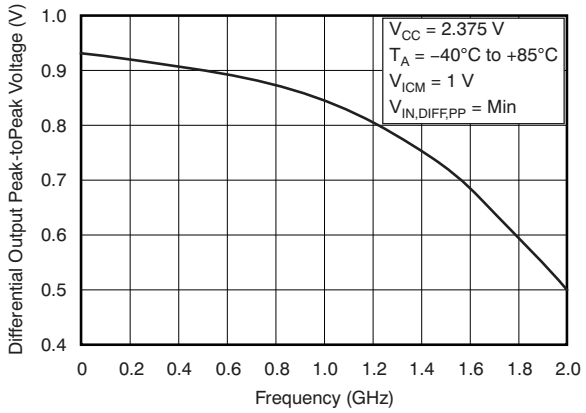


Figure 3. Differential Output Peak-to-Peak Voltage vs Frequency

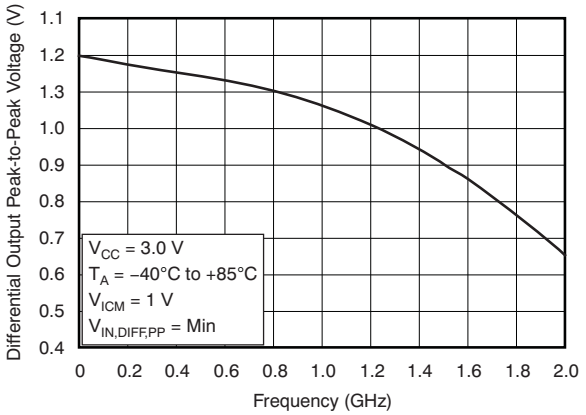


Figure 4. Differential Output Peak-to-Peak Voltage vs Frequency

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7 Parameter Measurement Information

7.1 Test Configurations

Figure 5 through Figure 11 show how the device should be set up for a variety of test configurations.

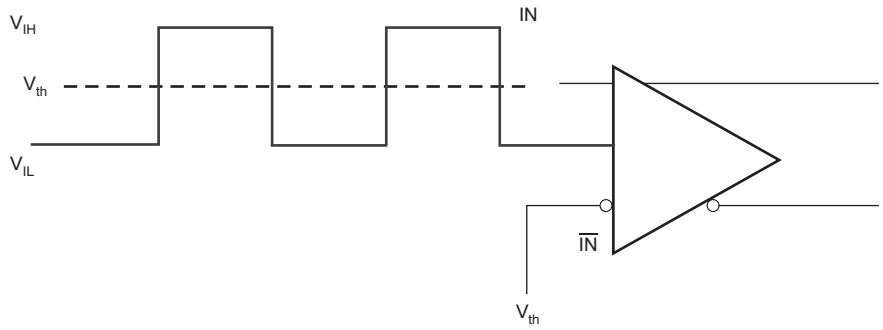


Figure 5. DC-Coupled LVCMOS Input During Device Test

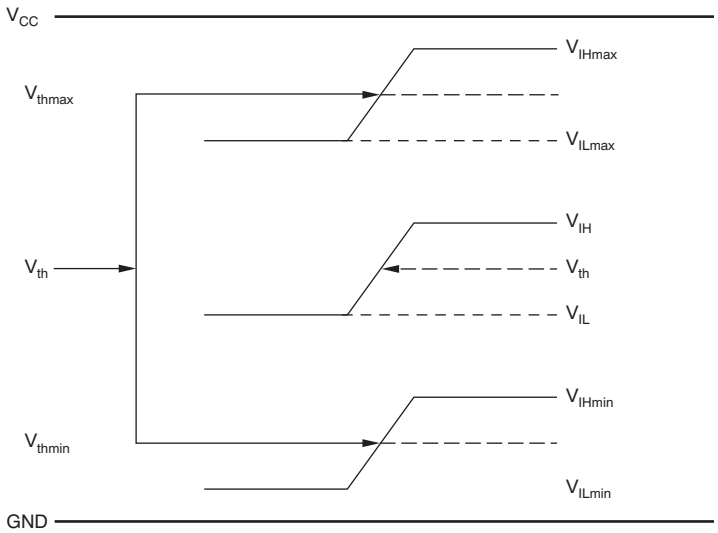


Figure 6. V_{th} Variation over LVCMOS Levels

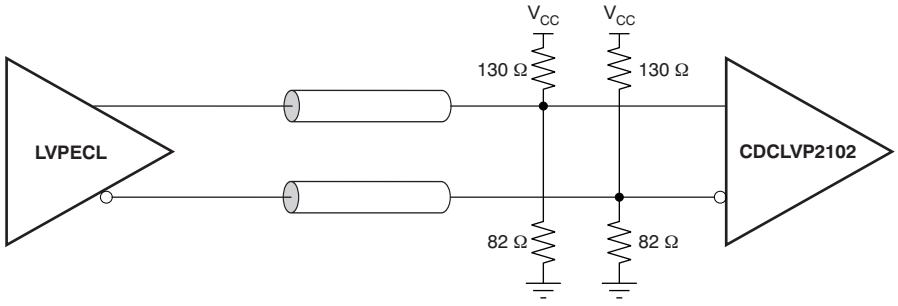


Figure 7. DC-Coupled LVPECL Input During Device Test

Test Configurations (continued)

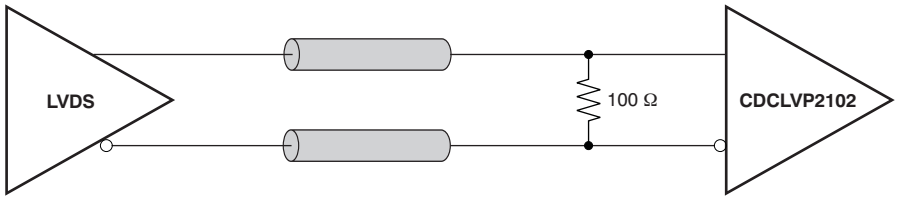


Figure 8. DC-Coupled LVDS Input During Device Test

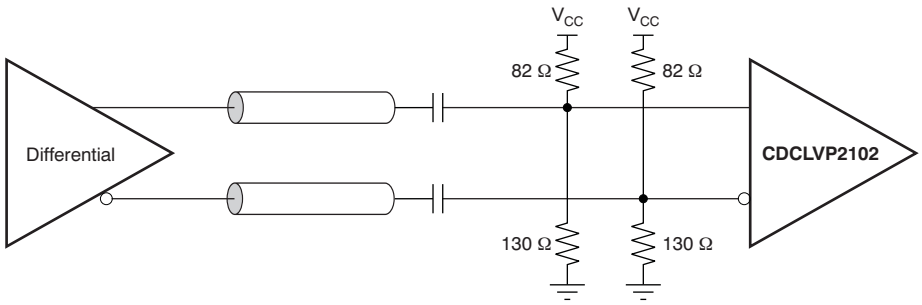


Figure 9. AC-Coupled Differential Input to Device

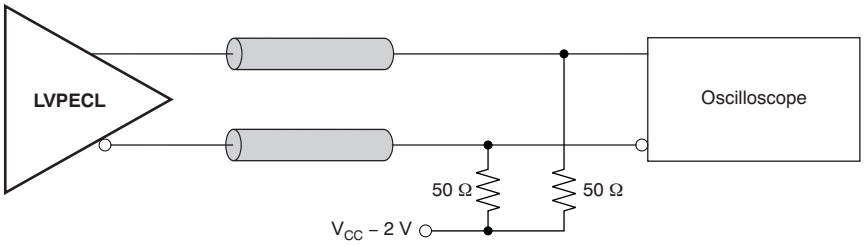


Figure 10. LVPECL Output DC Configuration During Device Test

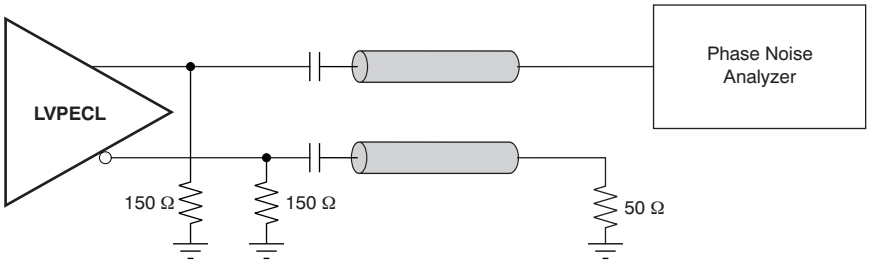


Figure 11. LVPECL Output AC Configuration During Device Test

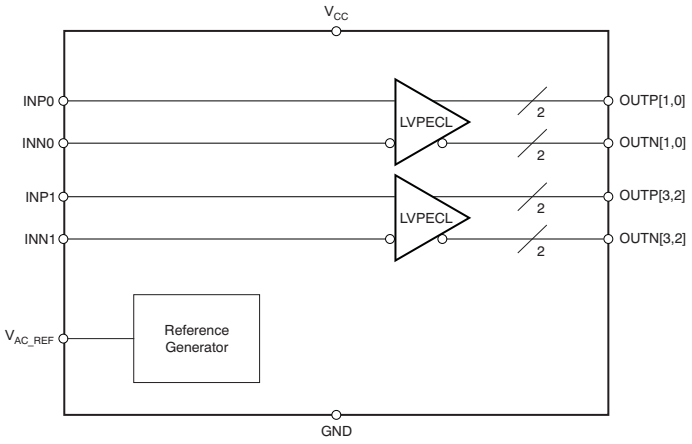
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8 Detailed Description

8.1 Overview

The CDCLVP2102 is an open emitter for LVPECL outputs. Therefore, proper biasing and termination are required to ensure correct operation of the device and to minimize signal integrity. The proper termination for LVPECL outputs is a 50 Ω to (V_{CC} – 2) V, but this direct-coupled (DC) voltage is not readily available on PCB. Therefore, a Thevenin equivalent circuit is worked out for the LVPECL termination in both DC- and AC-coupled configurations. These configurations are shown in Figure 12 (a and b) for V_{CC} = 2.5 V and Figure 13 (a and b) for V_{CC} = 3.3 V, respectively. TI recommends placing all resistive components close to either the driver end or the receiver end. If the supply voltage for the driver and receiver is different, AC coupling is required.

8.2 Functional Block Diagram



8.3 Feature Description

The CDCLVP2102 is a low-additive jitter universal to LVPECL fan-out buffer with two independent inputs. The small package, low output skew, and low-additive jitter make for a flexible device in demanding applications.

8.4 Device Functional Modes

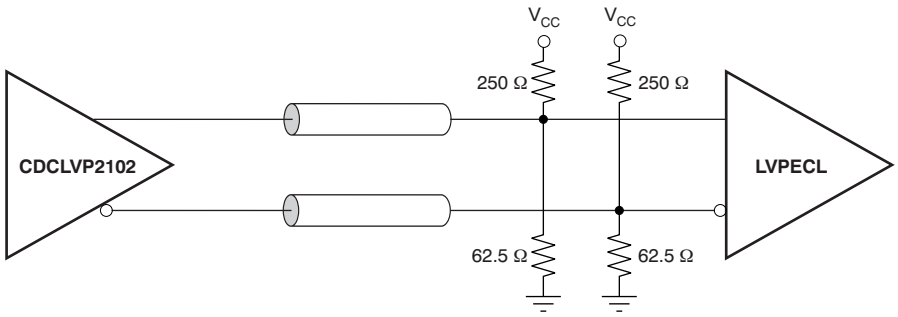
The two independent inputs of the CDCLVP2102 distribute the input clock to two outputs each. Unused inputs and outputs can be left floating to reduce overall component cost. Both AC- and DC coupling schemes can be used with the CDCLVP1204 to provide greater system flexibility.

8.4.1 LVPECL Output Termination

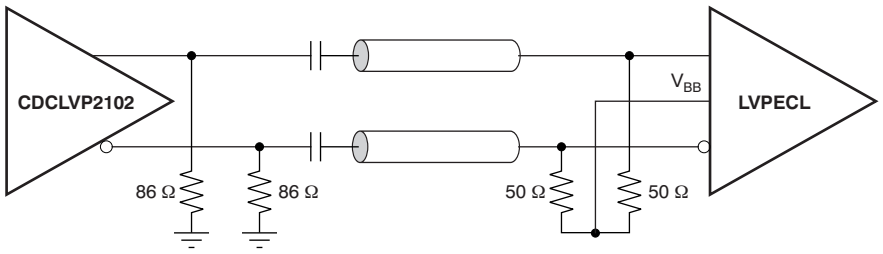
The CDCLVP2102 is an open emitter for LVPECL outputs. Therefore, proper biasing and termination are required to ensure correct operation of the device and to minimize signal integrity. The proper termination for LVPECL outputs is a 50 Ω to (V_{CC} –2) V, but this DC voltage is not readily available on PCB. Therefore, a Thevenin equivalent circuit is worked out for the LVPECL termination in both DC- and AC-coupled configurations. These configurations are shown in Figure 12 a and b for V_{CC} = 2.5 V and Figure 13 a and b for V_{CC} = 3.3 V, respectively. TI recommends placing all resistive components close to either the driver end or the receiver end. If the supply voltage for the driver and receiver is different, AC coupling is required.

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Device Functional Modes (continued)



(a) Output DC Termination

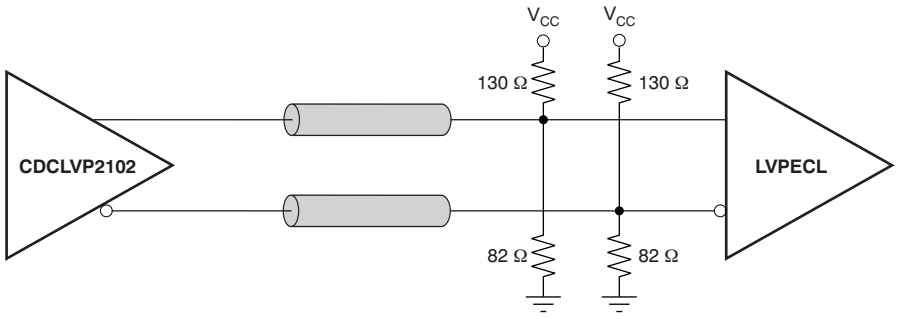


(b) Output AC Termination

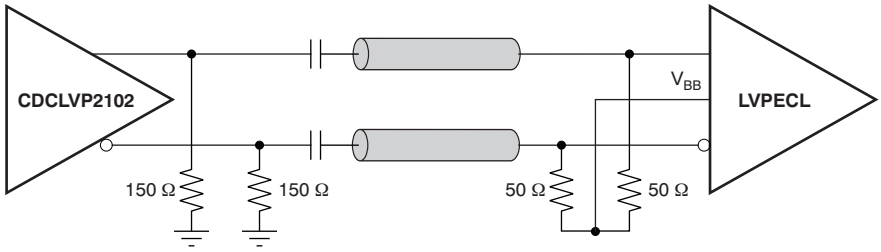
Figure 12. LVPECL Output DC and AC Termination for V_{CC} = 2.5 V

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Device Functional Modes (continued)



(a) Output DC Termination



(b) Output AC Termination

Figure 13. LVPECL Output DC and AC Termination for V_{CC} = 3.3 V

8.4.2 Input Termination

The CDCLVP2102 inputs can be interfaced with LVPECL, LVDS, or LVCMOS drivers. Figure 14 shows how to DC-couple an LVCMOS input to the CDCLVP2102. The series resistance (R_S) must be placed close to the LVCMOS driver; its value is calculated as the difference between the transmission line impedance and the driver output impedance.

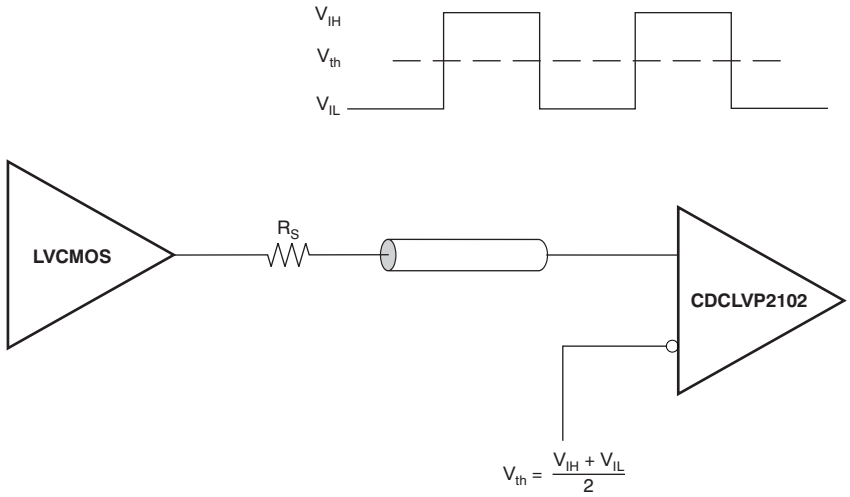


Figure 14. DC-Coupled LVCMOS Input to CDCLVP2102

Device Functional Modes (continued)

Figure 15 shows how to DC-couple LVDS inputs to the CDCLVP2102. Figure 16 and Figure 17 describe the method of DC coupling LVPECL inputs to the CDCLVP2102 for V_{CC} = 2.5 V and V_{CC} = 3.3 V, respectively.

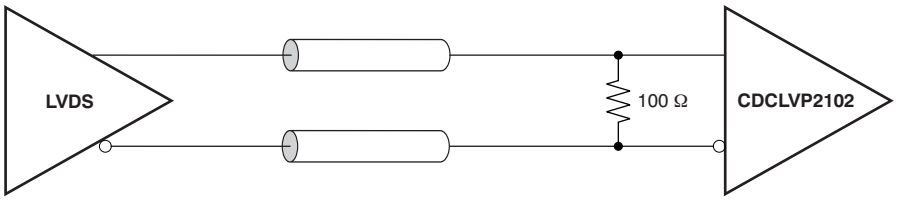


Figure 15. DC-Coupled LVDS Inputs to CDCLVP2102

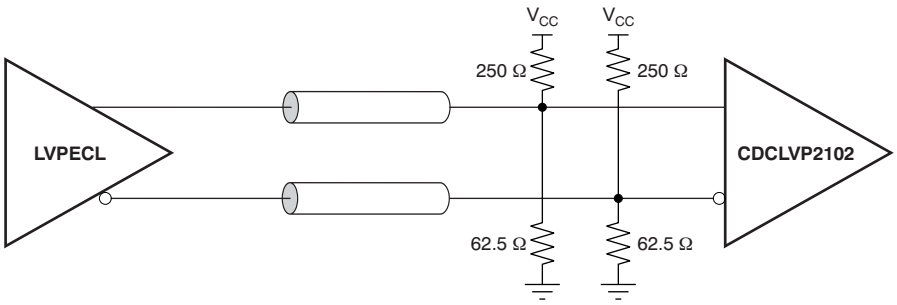


Figure 16. DC-Coupled LVPECL Inputs to CDCLVP2102 (V_{CC} = 2.5 V)

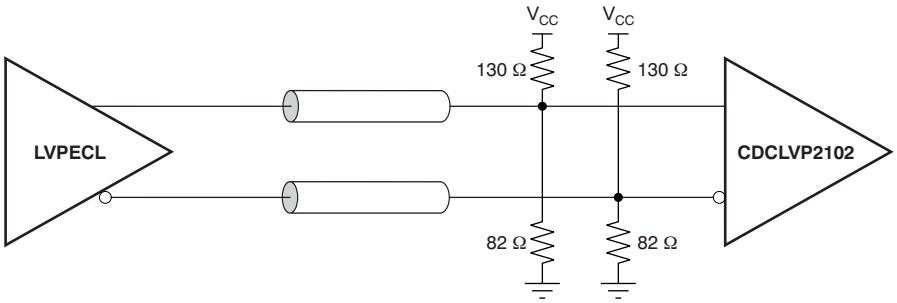


Figure 17. DC-Coupled LVPECL Inputs to CDCLVP2102 (V_{CC} = 3.3 V)

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Device Functional Modes (continued)

Figure 18 and Figure 19 show the technique of AC coupling differential inputs to the CDCLVP2102 for V_{CC} = 2.5 V and V_{CC} = 3.3 V, respectively. TI recommends placing all resistive components close to either the driver end or the receiver end. If the supply voltages of the driver and receiver are different, AC coupling is required.

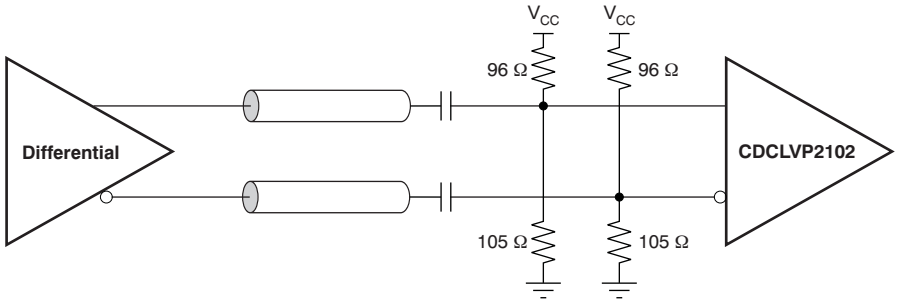


Figure 18. AC-Coupled LVPECL Inputs to CDCLVP2102 (V_{CC} = 2.5 V)

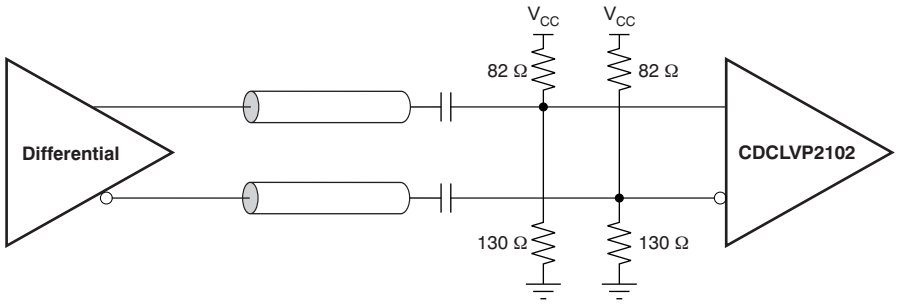


Figure 19. AC-Coupled LVPECL Inputs to CDCLVP2102 (V_{CC} = 3.3 V)

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The CDCLVP2102 is a low additive jitter LVPECL fan-out buffer that can generate two copies each of two independent LVPECL, LVDS, or LVCMOS inputs. The CDCLVP2102 can accept reference clock frequencies up to 2 GHz while providing low output skew.

9.2 Typical Application

Figure 20 shows a fan-out buffer for line-card application.

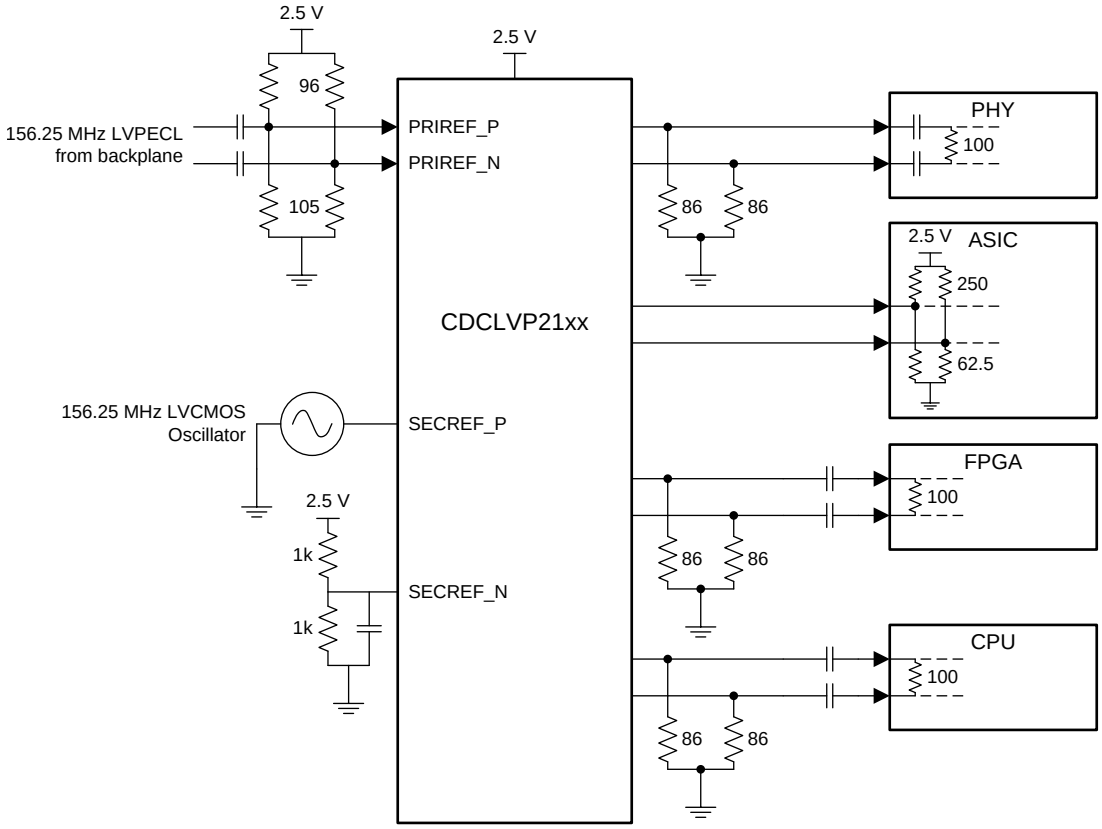


Figure 20. CDCLVP2102 Typical Application

9.2.1 Design Requirements

The CDCLVP2102 shown in Figure 20 is configured to be able to select two inputs: a 156.25-MHz LVPECL clock from the backplane, or a secondary 156.25-MHz LVCMOS 2.5-V oscillator. Either signal can be then fanned out to desired devices, as shown.

The configuration example is driving 4 LVPECL receivers in a line-card application with the following properties:

- The PHY device has internal AC coupling and appropriate termination and biasing. The CDCLVP2102 must be provided with 86-Ω emitter resistors near the driver for proper operation.
- The ASIC is capable of DC coupling with a 2.5-V LVPECL driver such as the CDCLVP2102. This ASIC features internal termination so no additional components are needed.

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Typical Application (continued)

- The FPGA requires external AC coupling but has internal termination. Again, 86-Ω emitter resistors are placed near the CDCLVP2102, and 0.1 µF are placed to provide AC coupling. Similarly, the CPU is internally terminated and requires external AC coupling capacitors.

9.2.2 Detailed Design Procedure

Refer to *Input Termination* for proper input terminations, dependent on single ended or differential inputs.

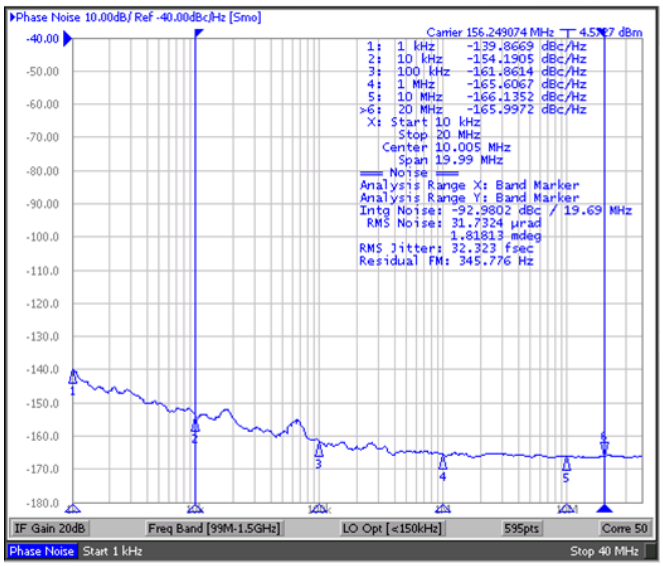
Refer to *LVPECL Output Termination* for output termination schemes depending on the receiver application.

Unused outputs can be left floating.

In Figure 20, the PHY, ASIC, and FPGA/CPU require different schemes. Power supply filtering and bypassing is critical for low-noise applications.

See *Power Supply Recommendations* for recommended filtering techniques. A reference layout is provided on the CDCLVP2102 Evaluation Module, *Low Additive Phase Noise Clock Buffer Evaluation Board User's Guide* (SCAU033).

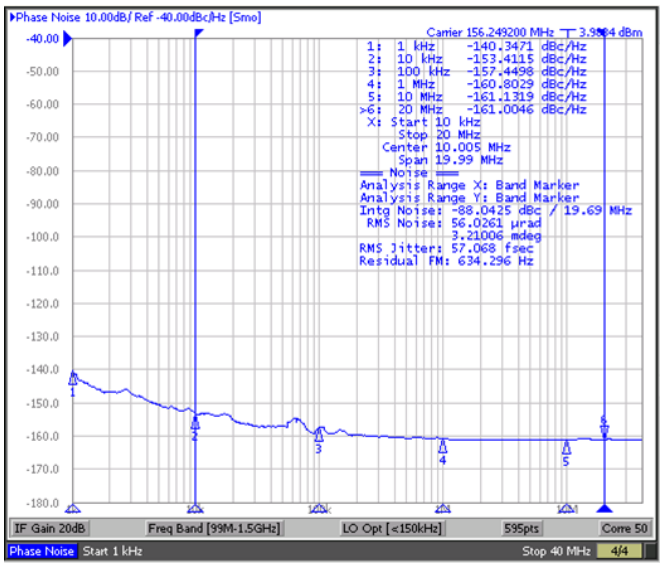
9.2.3 Application Curves



Reference signal is low-noise Crystek XO CPRO33.156.25

32 fs, RMS 10 kHz to 20 MHz

Figure 21. CDCLVP21xx Reference Phase Noise



57 fs, RMS 10 kHz to 20 MHz

Figure 22. CDCLVP21xx Output Phase Noise

The low additive noise of the CDCLVP2102 can be shown in this line-card application. The low noise 156.25 MHz XO with 32-fs, RMS jitter drives the CDCLVP2102, resulting in 57 fs, RMS when integrated from 10 kHz to 20 MHz. The resultant additive jitter is a low 47 fs, RMS for this configuration.

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10 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is very critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply pins and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1-μF) bypass capacitors as there are supply pins in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with very low DC resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

Figure 23 shows this recommended power-supply decoupling method.

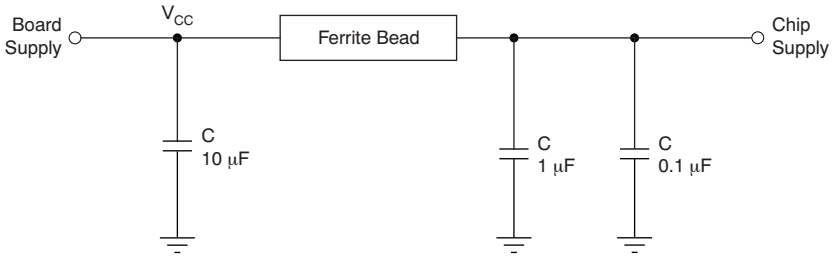


Figure 23. Power-Supply Decoupling

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11 Layout

11.1 Layout Guidelines

Power consumption of the CDCLVP2102 can be high enough to require attention to thermal management. For reliability and performance reasons, the die temperature must be limited to a maximum of 125°C. That is, as an estimate, ambient temperature (T_A) plus device power consumption times $R_{\theta JA}$ must not exceed 125°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. Figure 24 shows a recommended land and via pattern.

11.2 Layout Example

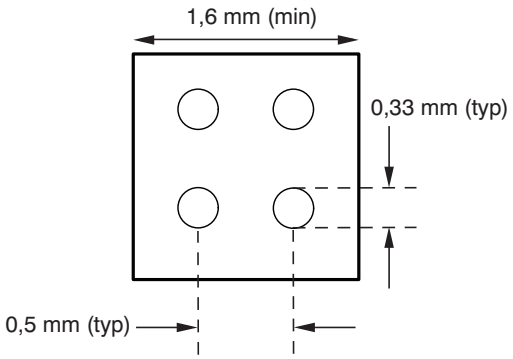


Figure 24. Recommended PCB Layout

11.3 Thermal Considerations

The CDCLVP2102 supports high temperatures on the printed circuit board (PCB) measured at the thermal pad. The system designer must ensure that the maximum junction temperature is not exceeded. Ψ_{JB} can allow the system designer to measure the board temperature with a fine gauge thermocouple and back calculate the junction temperature using Equation 1. Note that Ψ_{jb} is close to $R_{\theta JB}$ because 75 to 95% of the heat of a device is dissipated by the PCB. Further information can be found at SPRA953 and SLUA566.

$$T_{junction} = T_{PCB} + (\Psi_{JB} \times Power) \quad (1)$$

Example:

Calculation of the junction-lead temperature with a 4-layer JEDEC test board using four thermal vias:

T_{PCB} = 105°C

Ψ_{JB} = 19°C/W

$Power_{inclTerm} = I_{max} \times V_{max}$ = 189 mA × 3.6 V = 680 mW (maximum power consumption including termination resistors)

$Power_{exclTerm}$ = 529 mW (maximum power consumption excluding termination resistors, see SLYT127 for further details)

$\Delta T_{junction} = \Psi_{JB} \times Power_{exclTerm}$ = 19°C/W × 529 mW = 10.06°C

$T_{junction} = \Delta T_{junction} + T_{Chassis}$ = 10.06°C + 105°C = 115°C (the maximum junction temperature of 125°C is not violated)

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- CDCLVP2102 Evaluation Module, *Low Additive Phase Noise Clock Buffer Evaluation Board User's Guide* (SCAU033)
- *Using Thermal Calculation Tools for Analog Components* (SLUA566)
- *Power Consumption of LVPECL and LVDS* (SLYT127)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCLVP2102RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2102	Samples
CDCLVP2102RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2102	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

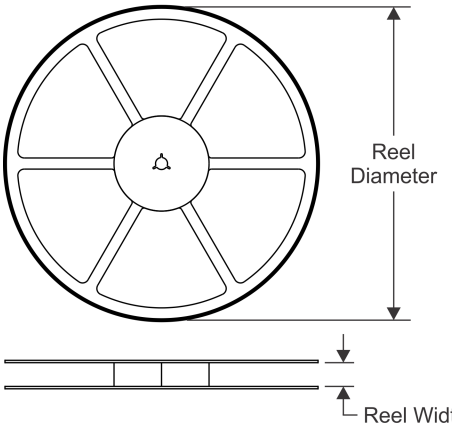
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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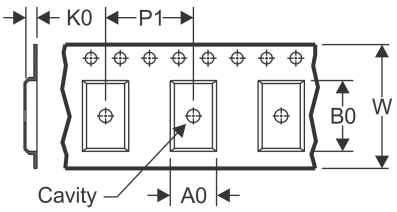
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

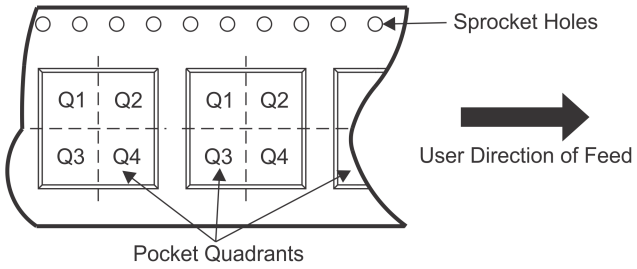


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

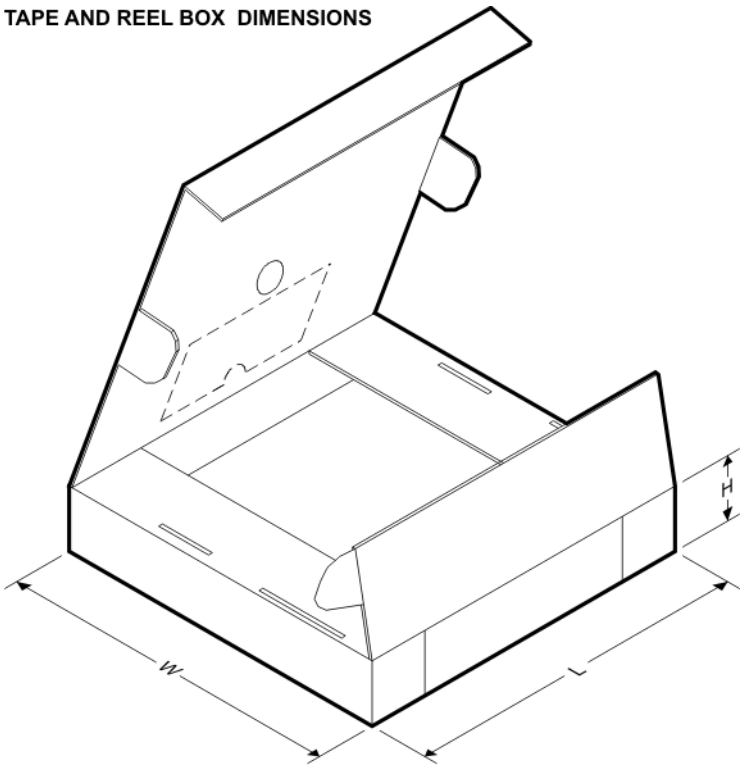
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVP2102RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
CDCLVP2102RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

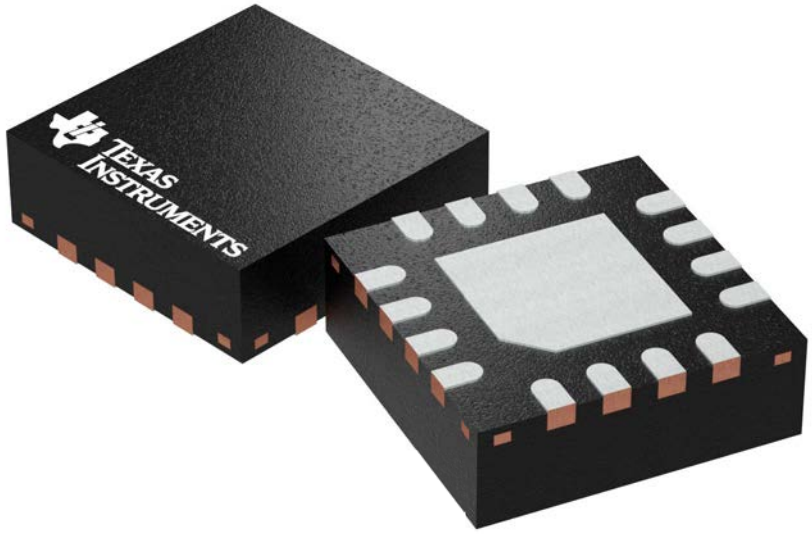


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVP2102RGTR	VQFN	RGT	16	3000	350.0	350.0	43.0
CDCLVP2102RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



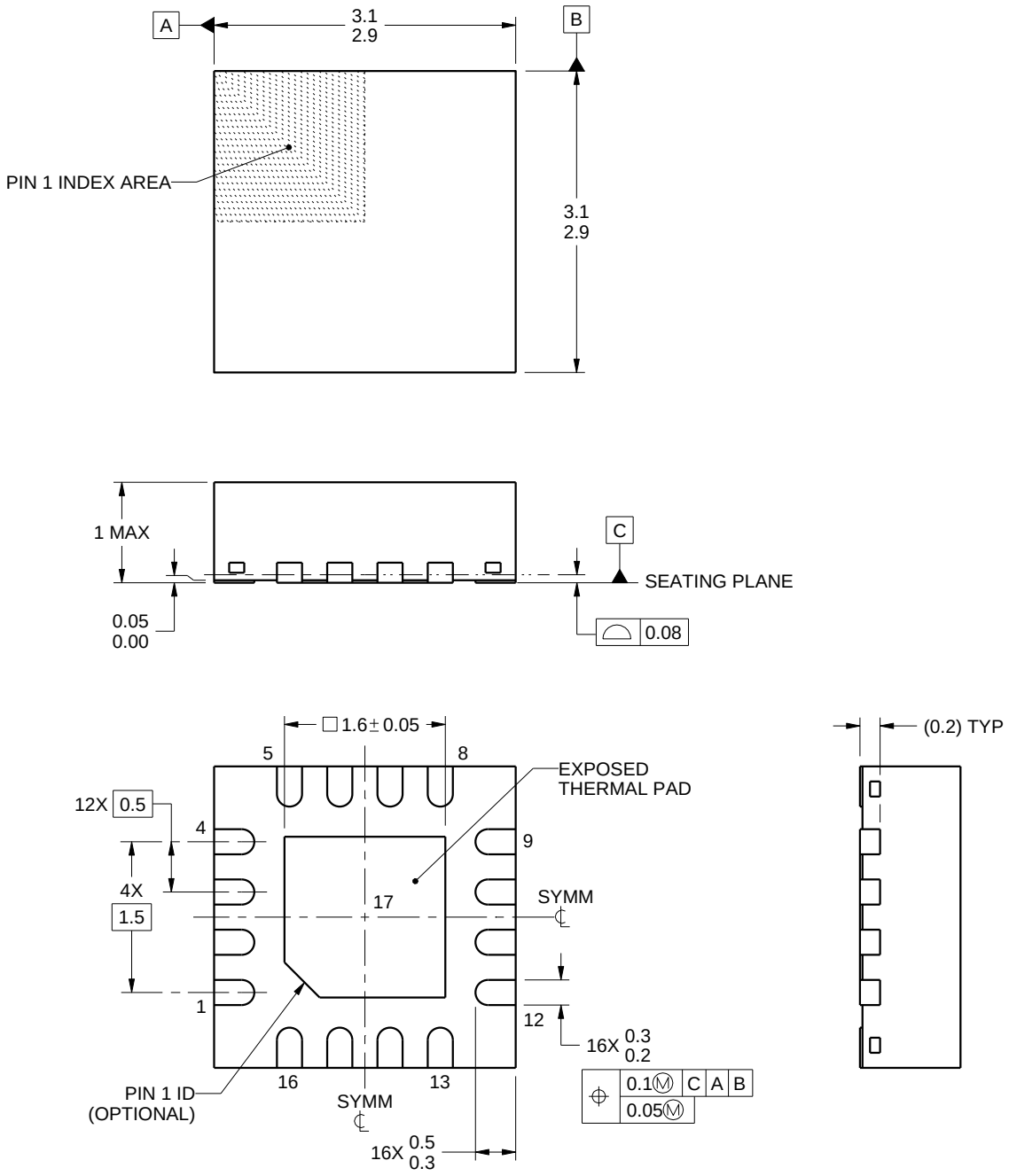
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016B

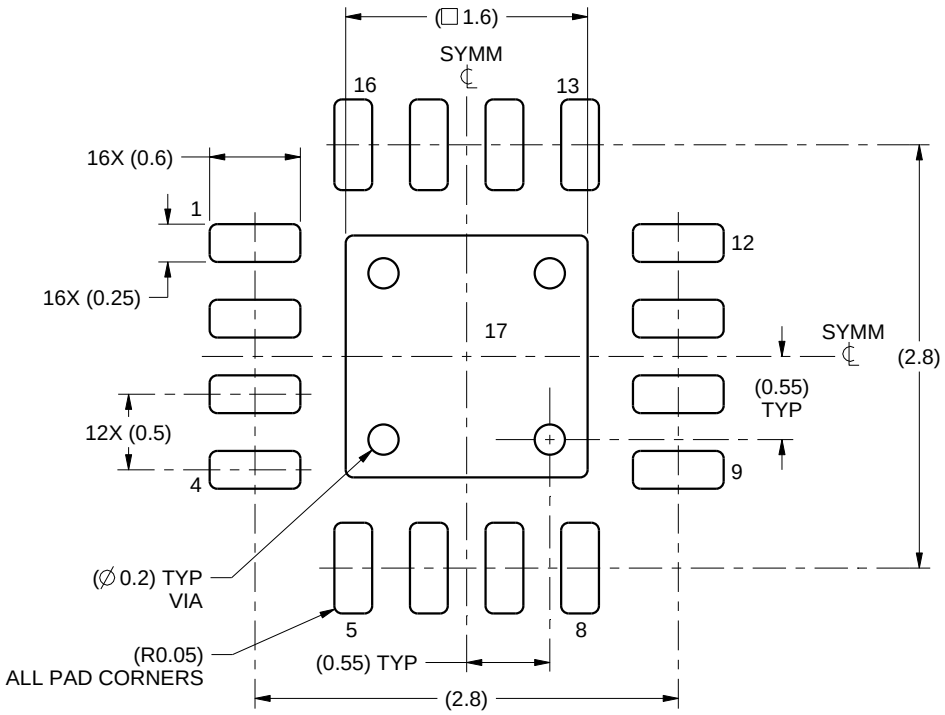
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

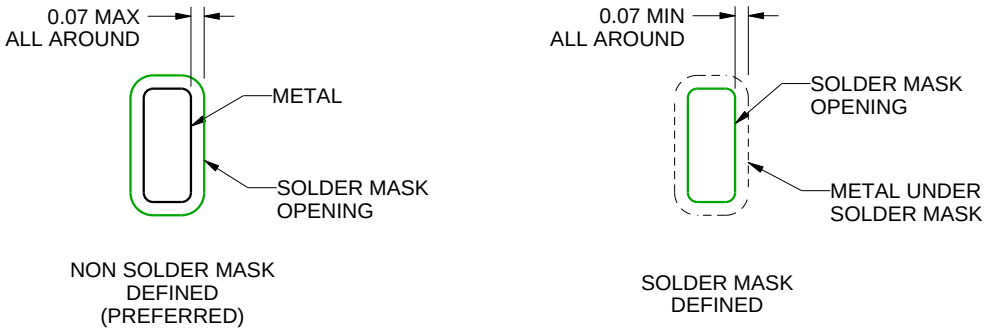


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

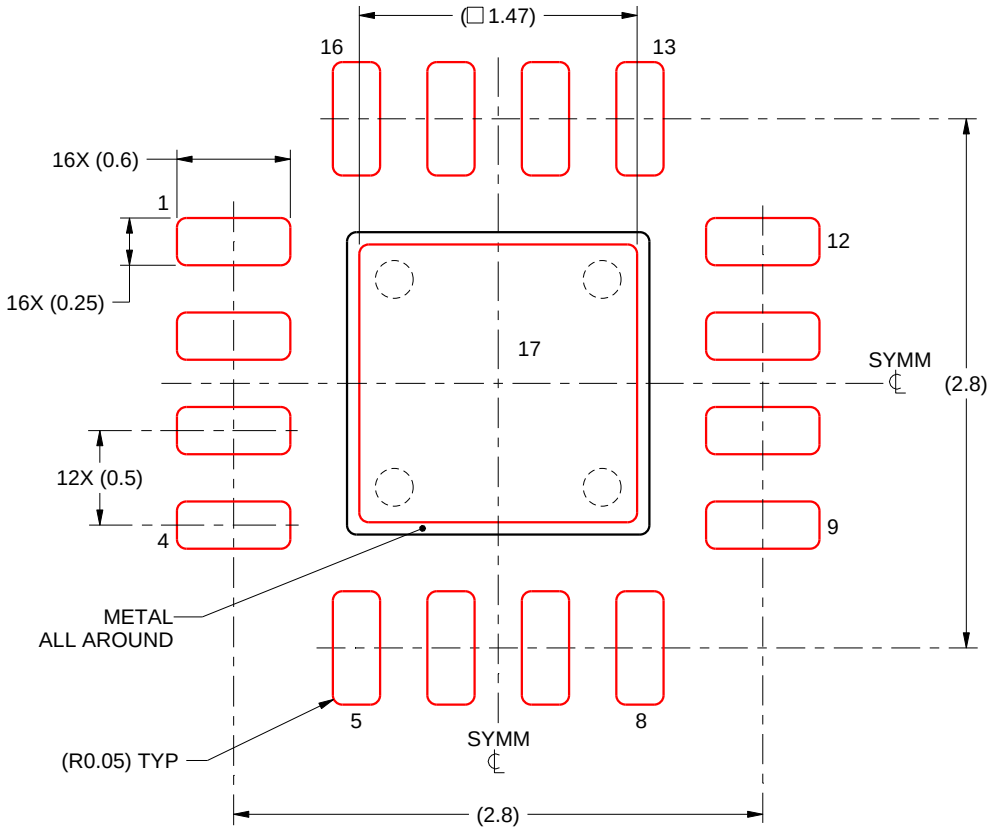


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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