SN65LBC173A-EP Quadruple RS-485 Differential Line Receiver

1 Features

- Designed for TIA/EIA-485, TIA/EIA-422 and ISO 8482 Applications
- Signaling Rates (1) up to 50 Mbps.
- Fail-Safe in Bus Short-Circuit, Open-Circuit, and Idle-Bus Conditions
- ESD Protection on Bus Inputs Exceeds 6 kV
- Common-Mode Bus Input Range –7 V to 12 V
- Propagation Delay Times < 18 ns
- Low-Standby Power Consumption < 32 µA
- Pin-Compatible Upgrade for AM26LS32, DS96F173, LTC488, and SN75173

2 Applications

- Supports Defense, Aerospace, and Medical Applications
  - Controlled Baseline
  - One Assembly and Test Site
  - One Fabrication Site
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

3 Description

The SN65LBC173A is a quadruple differential line receiver with tri-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 (Euro RS-485) applications.

This device is optimized for balanced multipoint bus communication at data rates up to and exceeding 50 million bits per second. The transmission media may be twisted-pair cables, printed-circuit board traces, or backplanes. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The receiver operates over a wide range of positive and negative common-mode input voltages, and features ESD protection to 6 kV, making it suitable for high-speed multipoint data transmission applications in harsh environments. These devices are designed using LinBiCMOS®, facilitating low-power consumption and robustness.

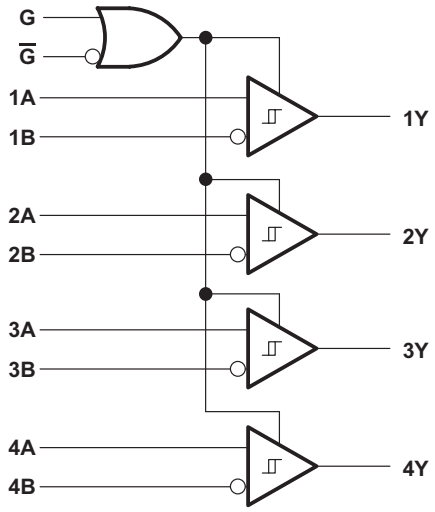
The G and $\overline{G}$ inputs provide enable control logic for either positive- or negative-logic enabling all four drivers. When disabled or powered off, the receiver inputs present a high-impedance to the bus for reduced system loading.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LBC173A-EP	SOIC (16)	9.90 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram



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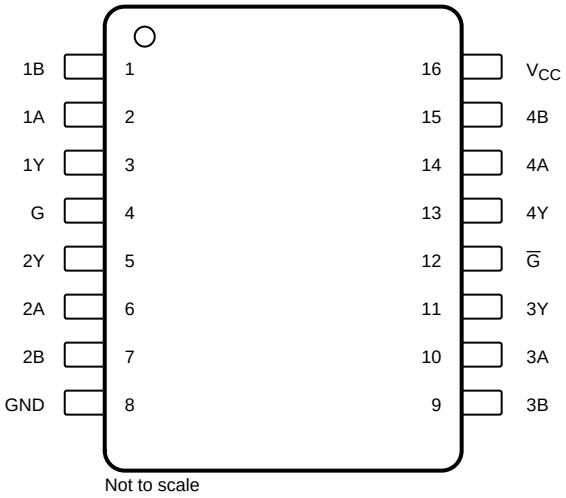
4 Revision History

DATE	REVISION	NOTES
November 2016	*	Initial release.

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5 Pin Configuration and Functions

D Package
16-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	2	I	RS-485 differential input (noninverting).
1B	1	I	RS-485 differential input (inverting).
1Y	3	O	Logic level output.
2A	6	I	RS-485 differential input (noninverting).
2B	7	I	RS-485 differential input (inverting).
2Y	5	O	Logic level output.
3A	10	I	RS-485 differential input (noninverting).
3B	9	I	RS-485 differential input (inverting).
3Y	11	O	Logic level output.
4A	14	I	RS-485 differential input (noninverting).
4B	15	I	RS-485 differential input (inverting).
4Y	13	O	Logic level output.
$\overline{G}$	12	I	Active-low select.
G	4	I	Active-high select.
GND	8	—	Ground.
V_{CC}	16	—	Power supply.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{CC}(2)	–0.3	6	V
Voltage at any bus input (DC)	–10	15	V
Voltage at any bus input (transient pulse through 100 Ω, see Figure 10)	–30	30	V
Input voltage at G and $\overline{G}$, V_I	–0.5	V_{CC} + 0.5	V
Receiver output current, I_O	–10	10	mA
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to GND.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	A and B to GND	±6000	V
			All pins	±5000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
	Voltage at any bus terminal	A, B	–7		12	V
V_{IH}	High-level input voltage	G, $\overline{G}$	2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
	Output current	Y	–8		8	mA
T_J	Junction temperature		–55		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		SN65LBC173A-EP D (SOIC) 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	78	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	39.5	°C/W
θ_{JB}	Junction-to-board thermal resistance	35.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over recommended operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold		–7 V ≤ V_{CM} ≤ 12 V (V_{CM} = (V_A + V_B) / 2)			–80	–10	mV
V_{IT-}	Negative-going differential input voltage threshold				–200	–120		mV
V_{HYS}	Hysteresis voltage (V_{IT+} – V_{IT-})					40		mV
VIK	Input clamp voltage		I_I = –18 mA		–1.5	–0.8		V
V_{OH}	High-level output voltage		V_{ID} = 200 mV, I_{OH} = –8 mA	See Figure 6	2.7	4.8		V
V_{OL}	Low-level output voltage		V_{ID} = –200 mV, I_{OL} = 8 mA			0.2	0.4	V
I_{OZ}	High-impedance-state output current		V_O = 0 V to V_{CC}		–1		1	µA
I_I	Line input current		Other input at 0 V, V_{CC} = 0 V or 5 V	V_I = 12 V			0.9	mA
				V_I = –7 V	–0.7			
I_{IH}	High-level input current	Enable inputs G, $\overline{G}$					110	µA
I_{IL}	Low-level input current				–100			µA
R_I	Input resistance	A, B inputs			12			kΩ
I_{CC}	Supply current		V_{ID} = 5 V	G at 0 V, $\overline{G}$ at V_{CC}			32	µA
			No load	G at V_{CC}, $\overline{G}$ at 0 V		11	16	mA

(1) All typical values are at V_{CC} = 5 V and 25°C.

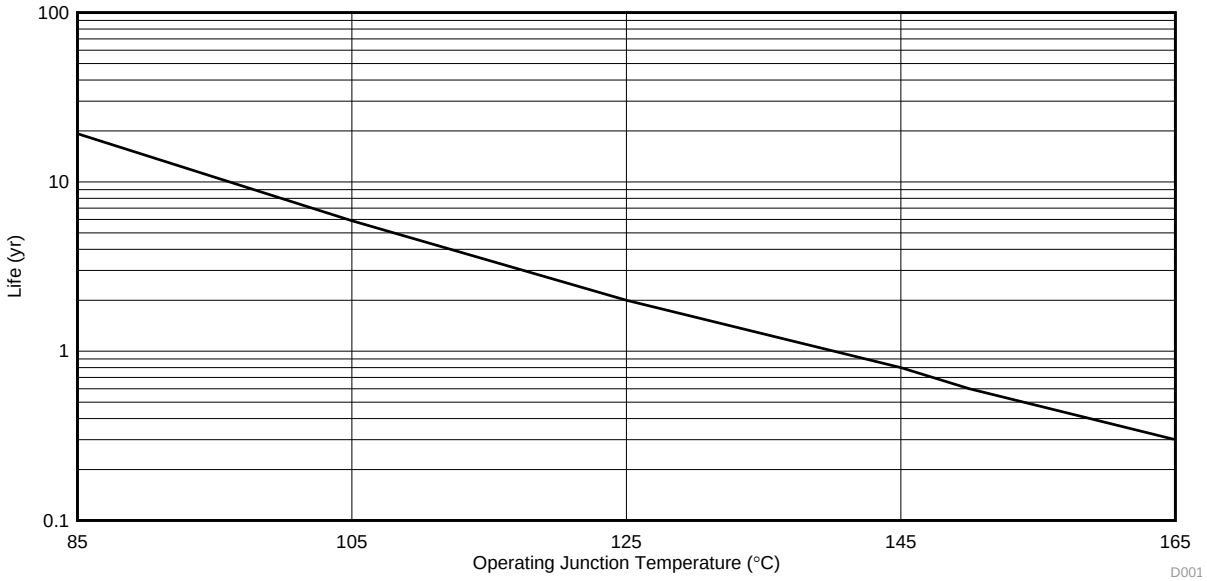
6.6 Switching Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Differential output voltage rise time	V_{ID} = –3 V to 3 V, See Figure 7		2	7	ns
t_f	Differential output voltage fall time			2	7	ns
t_{PLH}	Propagation delay time, low-to-high level output		8	12	18	ns
t_{PHL}	Propagation delay time, high-to-low level output		8	12	18	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 8		27	39	ns
t_{PHZ}	Propagation delay time, high-level-output-to-high impedance			7	24	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	See Figure 9		29	39	ns
t_{PLZ}	Propagation delay time, low-level-output-to-high impedance			12	18	ns
$t_{sk(p)}$	Pulse skew (|t_{PLH} – t_{PHL}|)			0.2	2	ns
$t_{sk(o)}$	Output skew(1)				3	ns
$t_{sk(pp)}$	Part-to-part skew(2)				3	ns

(1) Output skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
(2) Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

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(1) See data sheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) Enhanced plastic product disclaimer applies.

Figure 1. SN65LBC173A-EP Wirebond Life Derating Chart

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6.7 Typical Characteristics

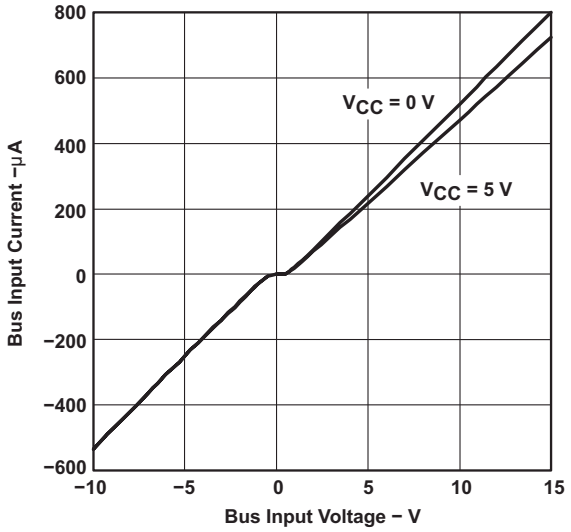


Figure 2. Bus Input Current vs Bus Input Voltage

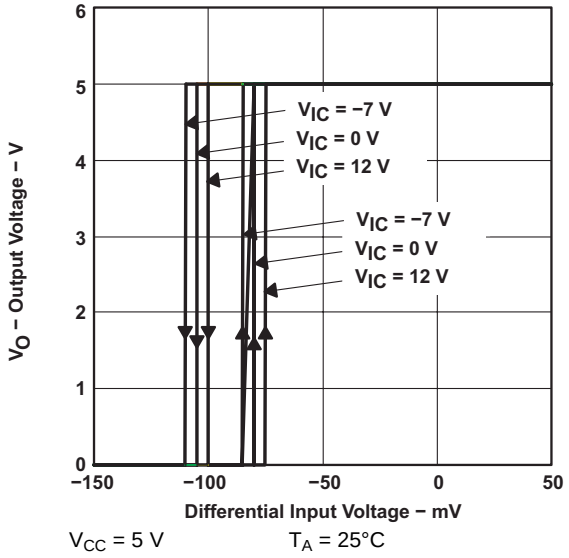


Figure 3. Output Voltage vs Differential Input Voltage

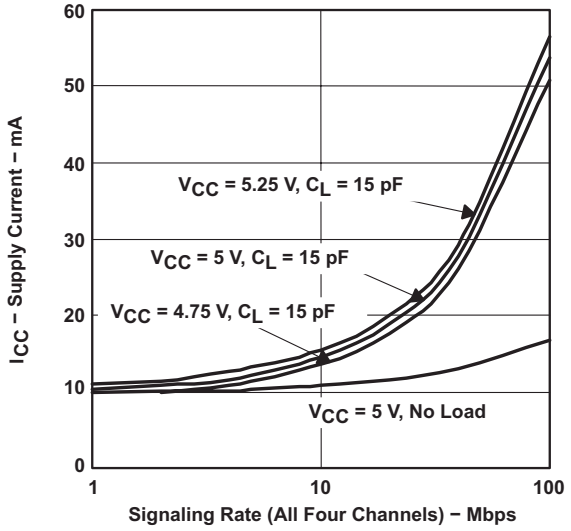


Figure 4. Supply Current vs Signaling Rate (All Four Channels)

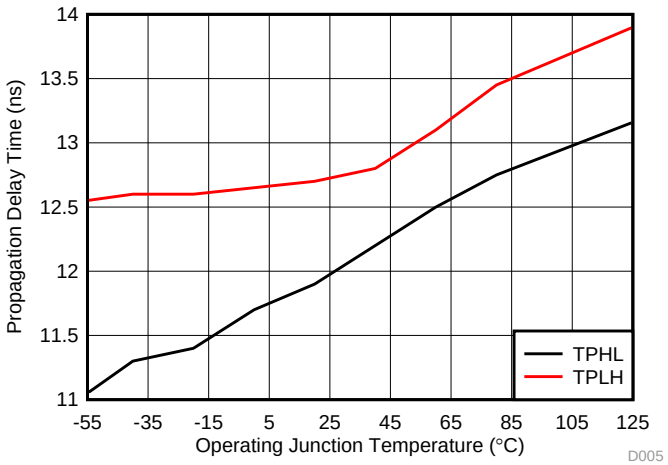


Figure 5. Propagation Delay Time vs Free-Air Temperature

7 Parameter Measurement Information

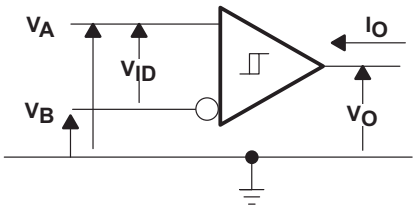
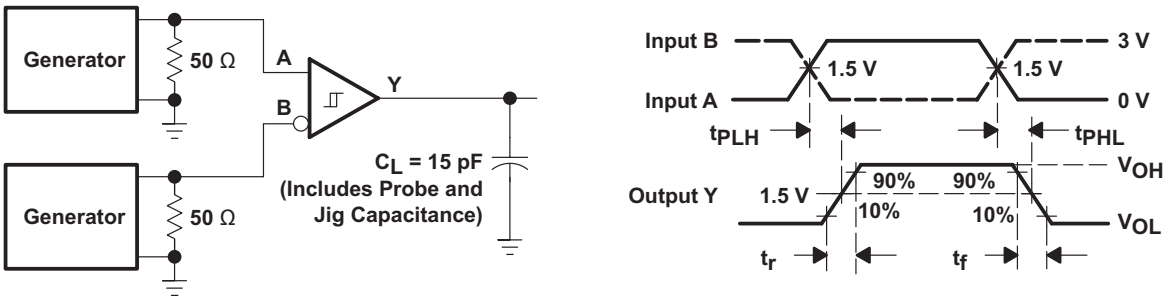
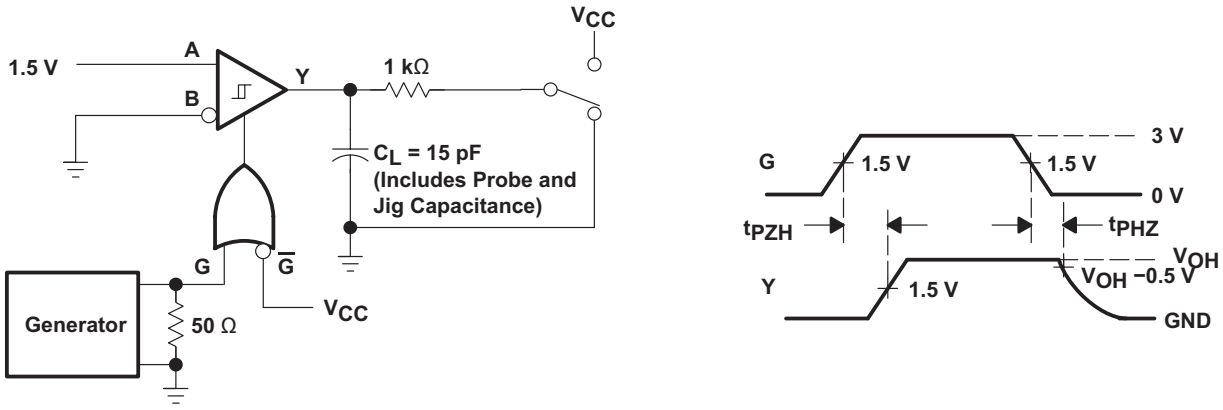


Figure 6. Voltage and Current Definitions



Generators: PRR = 1 MHz, 50% Duty Cycle,
t_r <6 ns, Z_O = 50 Ω

Figure 7. Switching Test Circuit and Waveforms

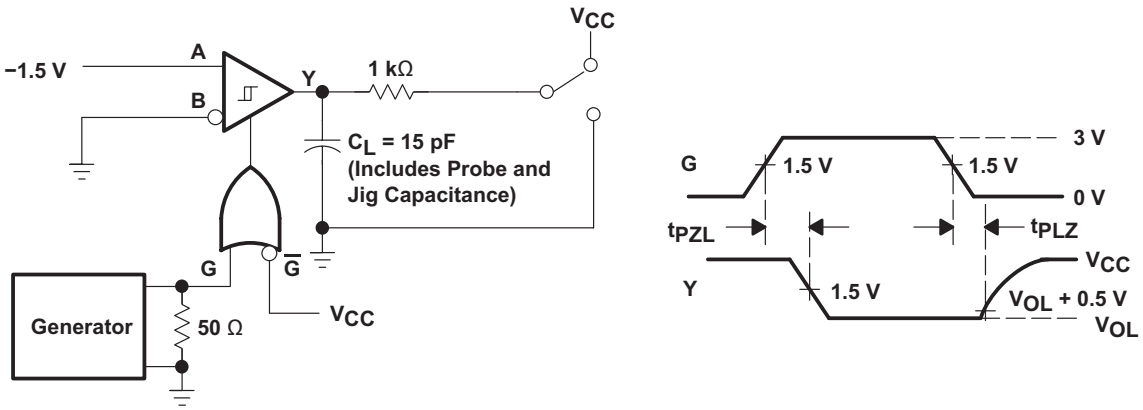


Generators: PRR = 1 MHz, 50% Duty Cycle,
t_r <6 ns, Z_O = 50 Ω

Figure 8. Test Circuit Waveforms, t_{PZH} and t_{PHZ}

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Parameter Measurement Information (continued)



Generators: PRR = 1 MHz, 50% Duty Cycle,
t_r <6 ns, Z_O = 50 Ω

Figure 9. Test Circuit Waveforms, t_{PZL} and t_{PLZ}

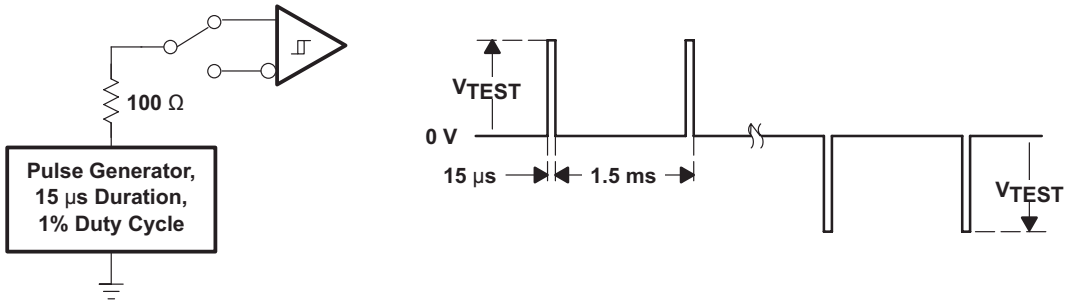


Figure 10. Test Circuit and Waveform, Transient Over-Voltage Test

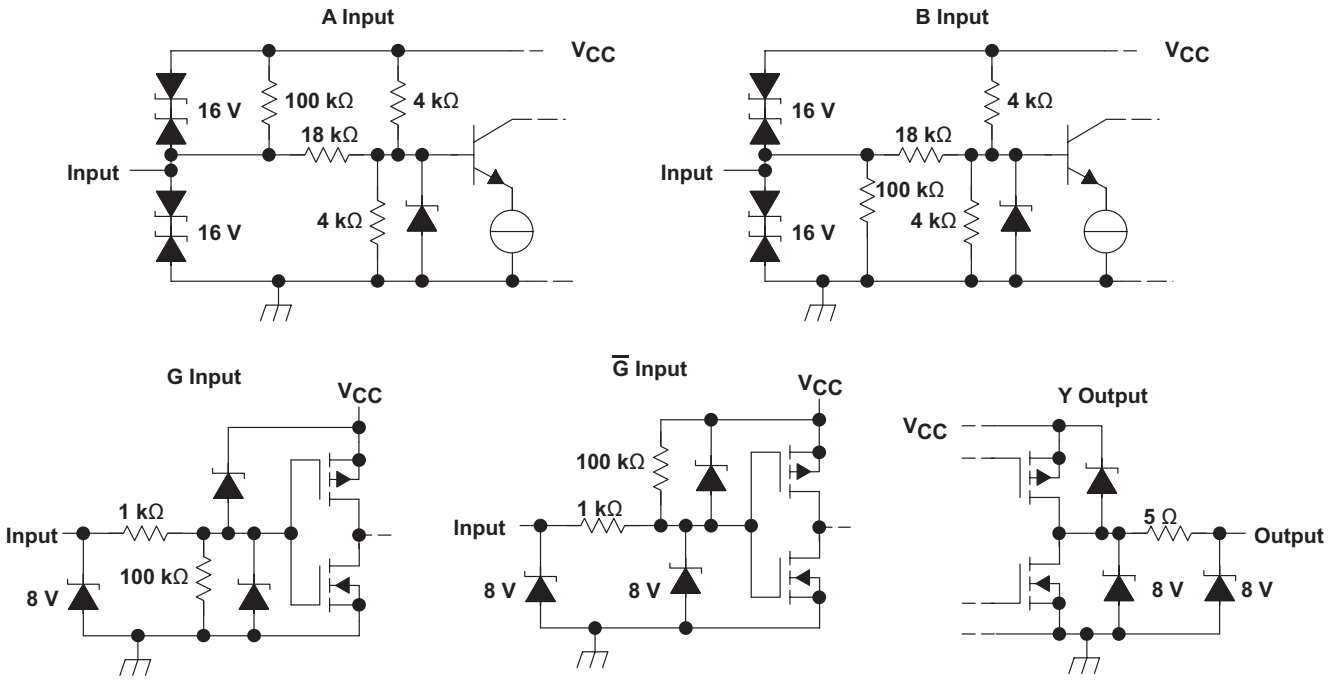


Figure 11. Equivalent Input and Output Schematic Diagrams

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8 Detailed Description

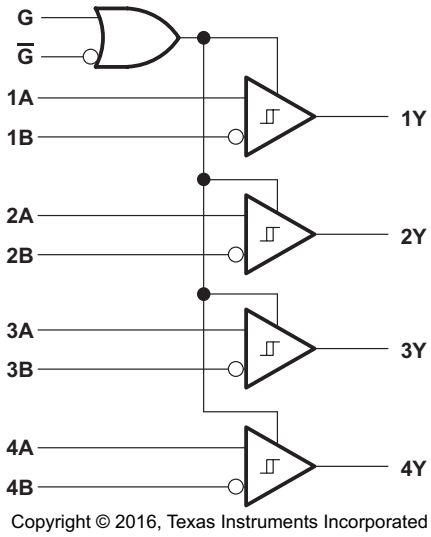
8.1 Overview

The SN65LBC173A is a quadruple differential line receiver with tri-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 (Euro RS-485) applications. This device is optimized for balanced multipoint bus communication at data rates up to and exceeding 50 million bits per second. The transmission media may be twisted-pair cables, printed-circuit board traces, or backplanes. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The receiver operates over a wide range of positive and negative common-mode input voltages, and features ESD protection to 6 kV, making it suitable for high-speed multipoint data transmission applications in harsh environments. These devices are designed using LinBiCMOS®, facilitating low-power consumption and robustness.

The G and $\overline{G}$ inputs provide enable control logic for either positive- or negative-logic enabling all four drivers. When disabled or powered off, the receiver inputs present a high-impedance to the bus for reduced system loading.

8.2 Functional Block Diagram



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8.3 Feature Description

The device can be configured using the G and $\overline{G}$ logic inputs to select receiver output. The high voltage or logic 1 on the G pin allows the device to operate on an active-high, and having a low voltage or logic 0 on the $\overline{G}$ enables active low operation. These are simple ways to configure the logic to match that of the receiving or transmitting controller or microprocessor.

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8.4 Device Functional Modes

The receivers implemented in these RS-485 device can be configured using the G and $\overline{G}$ logic pins to be enabled or disabled. This allows users to ignore or filter out transmissions as desired.

Table 1. Function Table(1)

INPUT	ENABLES		OUTPUT
A - B (V_{ID})	G	$\overline{G}$	Y
$V_{ID} \le -0.2$ V	H	X	L
	X	L	
-0.2 V < V_{ID} < -0.01 V	H	X	?
	X	L	
-0.01 V ≤ V_{ID}	H	X	H
	X	L	
X	L	H	Z
	OPEN	OPEN	
Short circuit	H	X	H
	X	L	
Open circuit	H	X	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

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9 Application and Implementation

NOTE

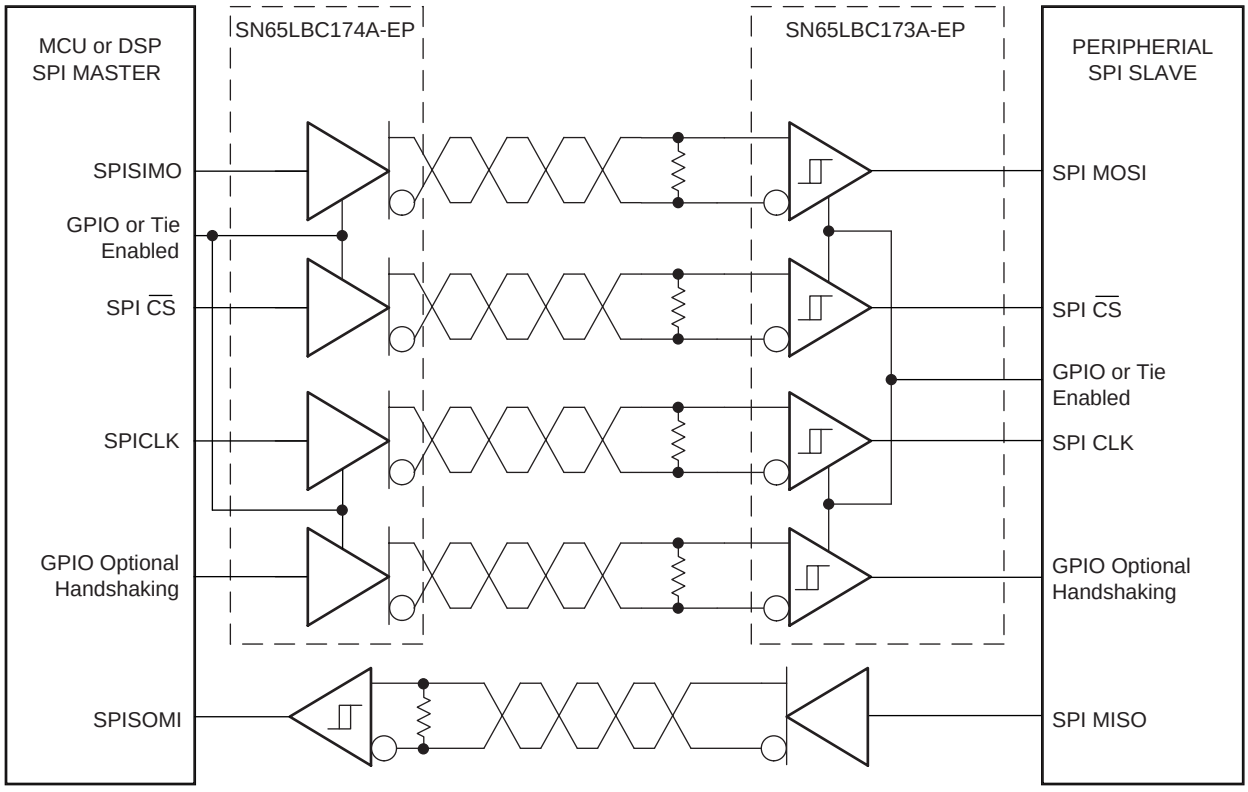
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Extending SPI operation over RS-485 link.

9.2 Typical Application

The following block diagram shows an MCU host connected via RS-485 to a SPI slave device. This device can be an ADC, DAC, MCU, or other SPI slave peripheral.



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Figure 12. DSP-to-DSP Link via Serial Peripheral Interface

9.2.1 Design Requirements

This application can be implemented using standard SPI protocol on DSP or MCU devices. The interface is independent of the specific frame or data requirements of the host or slave device. An additional but not required handshake bit is provided that can be used for customer purposes.

9.2.2 Detailed Design Procedure

The interface design requirements are fairly straight forward in this single source/destination scenario. Trace lengths and cable lengths need to be matched to maximize SPI timing. If there is a benefit to put the interface to sleep, GPIOs can be used to control the enable signals of the transmitter and receiver. If GPIOs are not available, or constant uptime needed, both the enables on transmit and receive can be hard tied enabled.

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Typical Application (continued)

The link shown can operate at up to 50 Mbps, well within the capability of most SPI links.

9.2.3 Application Curves

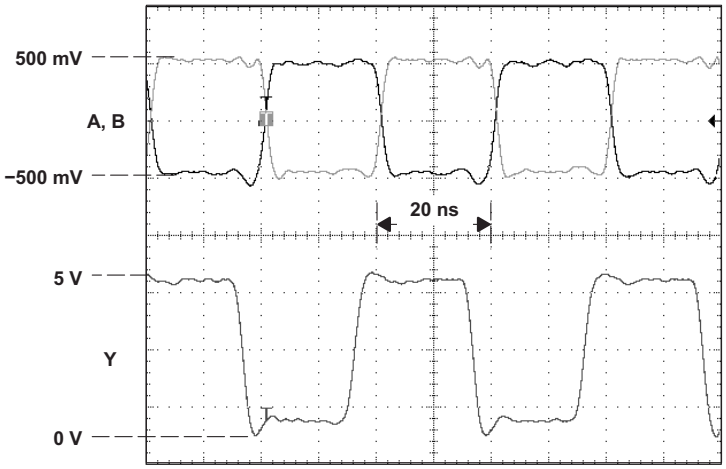


Figure 13. Receiver Inputs and Outputs, 50-Mbps Signaling Rate

10 Power Supply Recommendations

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible.
- Place termination resistor as close as possible to the input pins (if end point node).
- Keep trace lengths from input pins to buss as short as possible to reduce stub lengths and reflections on any nodes that are not end points of bus.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.

11.2 Layout Example

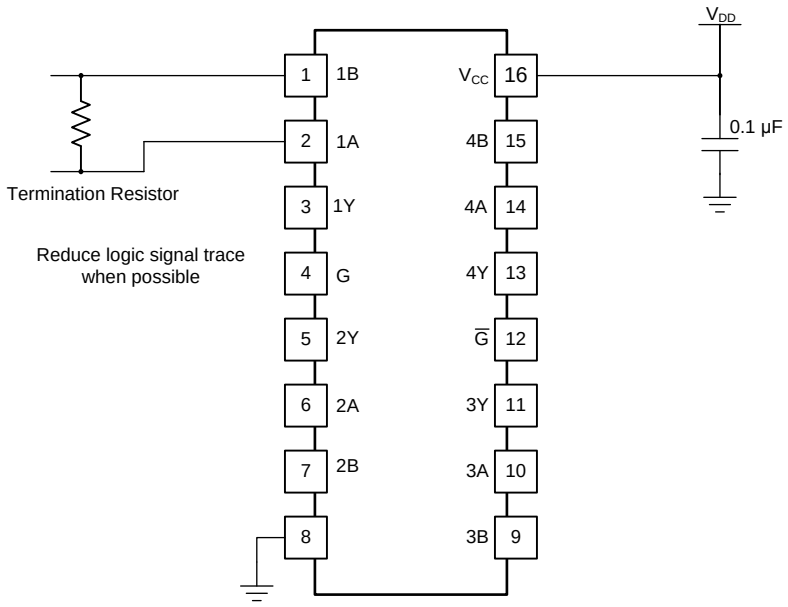


Figure 14. Layout with PCB Recommendations

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
LinBiCMOS is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC173AMDREP	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LBC173AEP	Samples
V62/13623-02XE	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LBC173AEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN65LBC173A-EP :

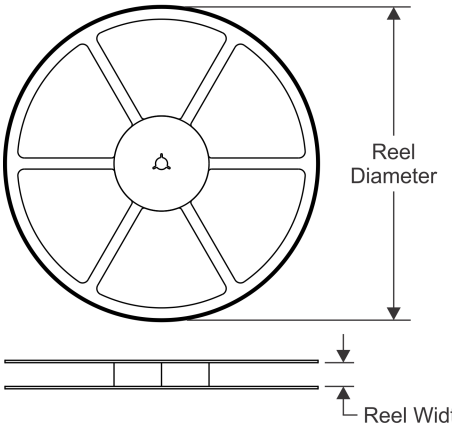
- Catalog: SN65LBC173A

NOTE: Qualified Version Definitions:

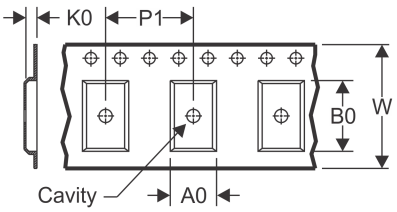
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

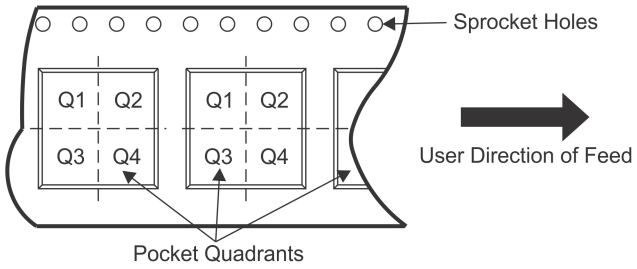


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

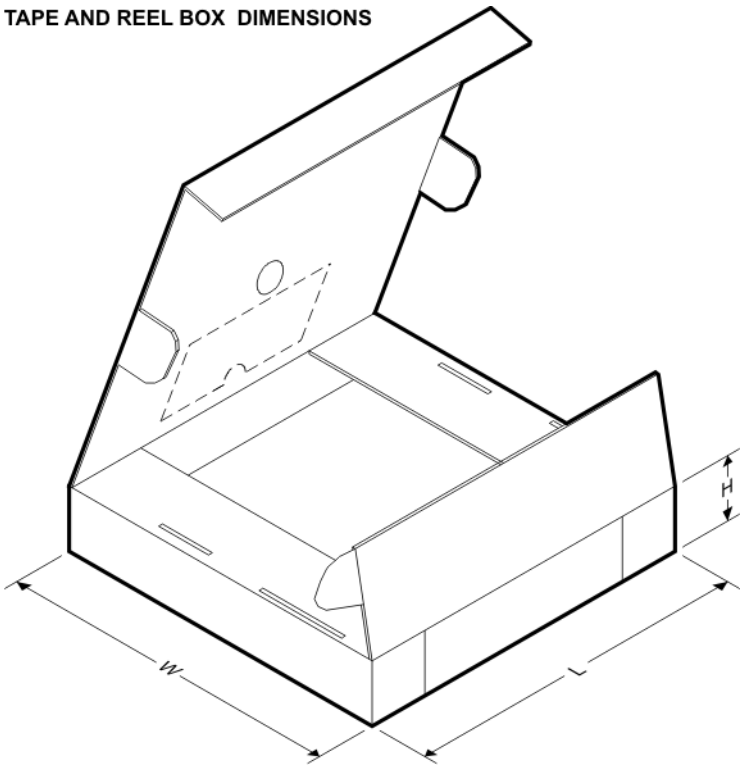
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC173AMDREP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

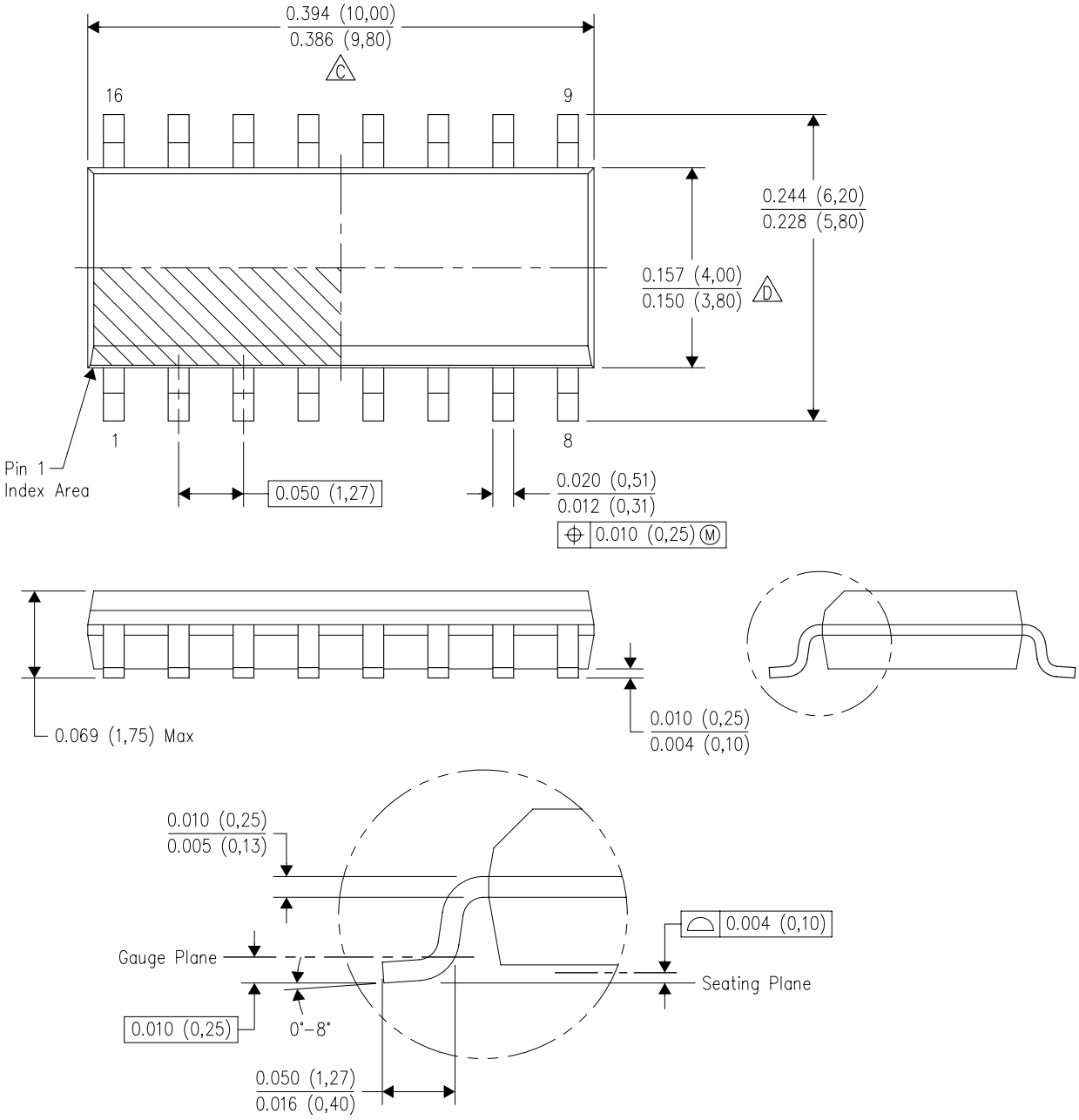
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

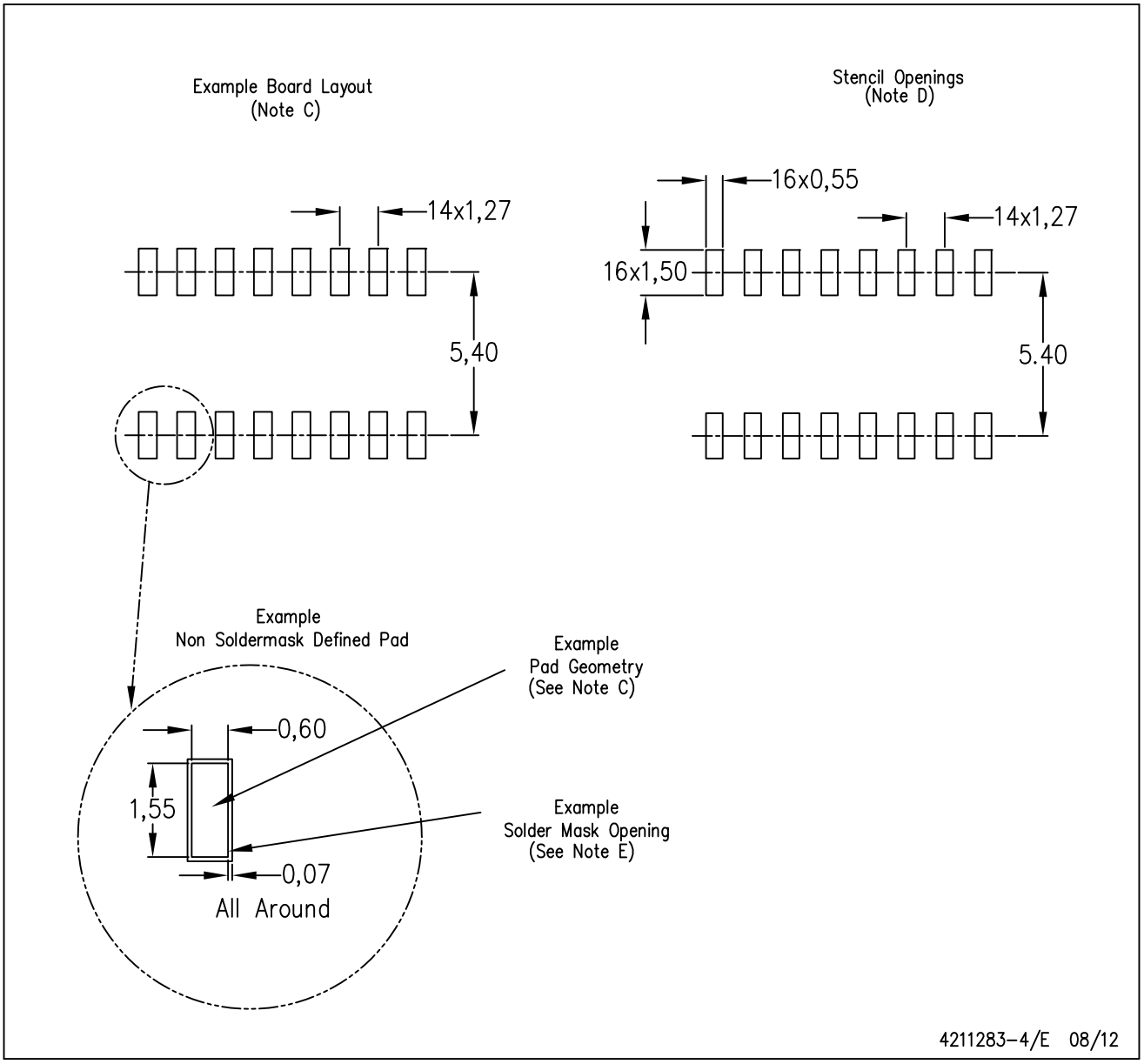
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC173AMDREP	SOIC	D	16	2500	333.2	345.9	28.6

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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