PIC16(L)F18324/18344

PIC16(L)F18324/18344 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F18324/18344 family devices that you have received conform functionally to the current Device Data Sheet (DS40001800**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F18324/18344 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A6**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F18324/18344 silicon revisions are shown in Table 1

.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A3	A4	A6
PIC16F18324	303Ah	2003h	2004h	2006h
PIC16LF18324	303Ch	2003h	2004h	2006h
PIC16F18344	303Bh	2003h	2004h	2006h
PIC16LF18344	303Dh	2003h	2004h	2006h

Note 1: The Device IDs (DEVID and DEVREV) are located at addresses 8006h and 8005h, respectively. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC16(L)F183XX Memory Programming Specification"* (DS40001738) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A3	A4	A6
Oscillators	Fail-Safe Clock Monitor (FSCM)	1.1	The FSCM may fail to trigger.	X	X	
Nonvolatile Memory (NVM) Control	NVMREG Access	2.1	Self-writes on LF devices below 2.2V at -40°C may not work.	X	X	
Nonvolatile Memory (NVM) Control	NVM WRRERR	2.2	Write Error (WRERR) bit is incorrectly set.	X	X	X
Electrical Specifications	Fixed Voltage Reference (FVR) Accuracy	3.1	Fixed Voltage Reference (FVR) output tolerance may be higher than specified at temperatures below -20°C.	X	X	X
Electrical Specifications	SMBus 2.0	3.2	The maximum V_{IL} level changes when V_{DD} is below 4.0V at 125°C.	X	X	
Electrical Specifications	NVM Access	3.3	NVM access on LF devices may not work at all specified voltage and temperature ranges.	X	X	X
Master Synchronous Serial Port (MSSP)	I^2C Communication	4.1	Acknowledge failure on LF devices only.	X	X	
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	4.2	SSPBUF transmit shift register may be corrupted under certain conditions	X	X	
Analog-to-Digital Converter (ADC)	Positive Voltage Reference	5.1	Using the FVR as the ADC positive voltage reference can cause missing codes.	X	X	
Analog-to-Digital Converter (ADC)	Auto-Conversion Trigger	5.2	Auto-trigger event does not begin a conversion while in Sleep.	X	X	X
Timer0	Clock Source	6.1	Operation of Timer0 is incorrect when F_{OSC}/4 is used as the clock source.	X	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A6**).

1. Module: Oscillators

1.1 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor may fail to trigger with the loss of the external clock signal when the 4x PLL is enabled. This includes all external clock modes: LP, XT, HS, ECL, ECM, and ECH.

Work around

None.

Affected Silicon Revisions

A3	A4	A6					
X	X						

2. Module: Nonvolatile Memory (NVM) Control

2.1 NVMREG Access

When performing self-writes through NVMREG access on the PIC16LF18324/18344 devices with VDD below 2.2V and at temperature of -40°C, the write operation may not work. This applies to both Program Flash Memory and EEPROM writes.

Work around

None.

Affected Silicon Revisions

A3	A4	A6					
X	X						

2.2 NVM WRERR

If a Reset occurs while a self-write operation is in progress, the Write Error (WRERR) bit is set. If the user clears the WRERR bit and another Reset occurs, even though no self-write is in progress, the WRERR bit will be incorrectly set again since the internal write latch has not been cleared.

Work around

A successful write operation will clear the WRERR condition.

Affected Silicon Revisions

A3	A4	A6					
X	X	X					

3. Module: Electrical Specifications

3.1 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate FVR only at temperatures above -20°.

Affected Silicon Revisions

A3	A4	A6					
X	X	X					

3.2 SMBus 2.0

At 125°C, when the VDD voltage level supplied to the device is 4.0V and above, the maximum SMBus 2.0 voltage level for the VIL parameter is 0.8V. When VDD drops below 4.0V, the maximum SMBus 2.0 voltage level for VIL drops to 0.7V. This issue applies to extended temperature devices only.

Work around

None.

Affected Silicon Revisions

A3	A4	A6					
X	X						

3.3 Nonvolatile Memory (NVM)

Nonvolatile memory (NVM) access on LF devices may not work when operating at temperatures between -40°C and +25°C and VDD levels below 2.0V.

Work around

None.

Affected Silicon Revisions

A3	A4	A6					
X	X	X					

4. Module: Master Synchronous Serial Port (MSSP)

4.1. I²C Communication

When using the MSSP to perform I²C communication and the voltage for VDD is above 3.0 volts, the Acknowledge signal (ACK) does not always occur after the second address byte is received, as expected. This issue exhibits itself when the MSSP is configured for either 7-bit or 10-bit addressing and in either Master or Slave mode.

The issue occurs more frequently when using 10-bit addressing in Slave mode and when the lower address bits (A7-A0) are transmitted by the Master on the SDA line.

Work around

Do not exceed 3.0 volts on VDD when using an LF device.

Affected Silicon Revisions

A3	A4	A6					
X	X						

4.2. SPI Slave Mode

When operating in SPI Slave mode, if the incoming SCK clock signal arrives during any of the conditions below, the SSPBUF transmit shift register may become corrupted. The transmitted slave byte cannot be assured to be correct, and the state of the WCOL bit may or may not indicate a write collision.

These conditions include:

- A write to an SFR
- A write to RAM following an SFR Read
- A write to RAM prior to an SFR Read.

Work around

Method 1 (Interrupt-based using $\overline{SS}$):

Connect the $\overline{SS}$ line to both the $\overline{SS}$ input and either an INT or IOC input pin.

1. Enable INT or IOC interrupts (interrupt on falling edge if available, otherwise check that $\overline{SS}$==0 when the interrupt occurs).
2. Load SSPBUF with the data to be transmitted.
3. Continue program execution.
4. When the Interrupt Service Routine (ISR) is invoked, do either of the following:
   - Add a delay that ensures the first SCK clock will be complete, or
   - Poll SSPSTAT.BF (while(BF==0)), and wait for the transmission/reception to complete.

   Once one of these two methods are complete, it is safe to return to program execution.

Method 2 (SS not available):

1. Load SSPBUF with the data to be transmitted.
2. Poll SSPSTAT.BF (while(BF==0)), and wait for the transmission or reception to complete.

Affected Silicon Revisions

A3	A4	A6					
X	X						

5. Module: Analog-to-Digital Converter (ADC)

5.1 Positive Voltage Reference

Using the Fixed Voltage Reference (FVR) as positive voltage reference for the ADC can cause an increase in missing codes.

Work around

Increase the bit conversion time, known as TAD, to 8 µs or higher.

Affected Silicon Revisions

A3	A4	A6					
X	X						

5.2 Auto-Conversion Trigger

When using the ADC in Sleep mode, an auto-conversion trigger event will not cause the ADC to begin a conversion.

Work around

None.

Affected Silicon Revisions

A3	A4	A6					
X	X	X					

6. Module: Timer0

6.1 Clock Source

Clearing the TMR0 Input Asynchronous Enable bit (T0ASYNC) of the T0CON1 register when Timer0 is configured to use FOSC/4 as its clock source may cause incorrect behavior.

Work around

Ensure that the T0ASYNC bit is set when using FOSC/4 as clock source.

Affected Silicon Revisions

A3	A4	A6					
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001800**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (09/2015)

Initial release of this document.

Rev B Document (01/2017)

Added Module 2: Nonvolatile Memory Control

Data Sheet Clarifications:

Removed Module 1 through Module 4; Added new Module 1: Comparator.

Rev C Document (07/2017)

Added Module 3: Electrical Specifications

Data Sheet Clarifications: Removed Modules 1 and 2. Other minor corrections.

Rev D Document (10/2018)

Added 2.2, 3.2, 3.3, 4, 5 and 6 Modules; Other minor corrections.

Note the following details of the code protection feature on Microchip devices:

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