

TVS2200 22-V Flat-Clamp Surge Protection Device

1 Features

- Protection Against ± 1 kV, 42 Ω IEC 61000-4-5 Surge Test for Industrial Signal Lines
- Max Clamping Voltage of 28.4 V at 40 A of 8/20 μ s Surge Current
- Standoff Voltage: 22 V
- Tiny 4 mm² Footprint
- Survives Over 5,000 Repetitive Strikes of 35 A 8/20 μ s Surge Current at 125°C
- Robust Surge Protection:
 - IEC 61000-4-5 (8/20 μ s): 40 A
 - IEC 61643-321 (10/1000 μ s): 5 A
- Low Leakage Current
 - 3.5 nA Typical at 27°C
 - 25 nA Typical at 85°C
- Low Capacitance: 105 pF
- Integrated Level 4 IEC 61000-4-2 ESD Protection

2 Applications

- Industrial Sensor I/O
- Medical Equipment
- USB Type-C V_{bus}
- PLC I/O Modules
- Appliances

3 Description

The TVS2200 robustly shunts up to 40 A of IEC 61000-4-5 fault current to protect systems from high power transients or lightning strikes. The device offers a solution to the common industrial signal line EMC requirement to survive up to ± 1 kV IEC 61000-4-5 open circuit voltage coupled through a 42 Ω impedance. The TVS2200 uses a unique feedback mechanism to ensure precise flat clamping during a fault, assuring system exposure below 30 V. The tight voltage regulation allows designers to confidently select system components with a lower voltage tolerance, lowering system costs and complexity without sacrificing robustness.

In addition, the TVS2200 is available in a small 2 mm $\times$ 2 mm SON footprint which is designed for space constrained applications, offering a 70 percent reduction in size compared to industry standard SMA and SMB packages. The extremely low device leakage and capacitance ensure a minimal effect on the protected line. To ensure robust protection over the lifetime of the product, TI tests the TVS2200 against 5,000 repetitive surge strikes at high temperature with no shift in device performance.

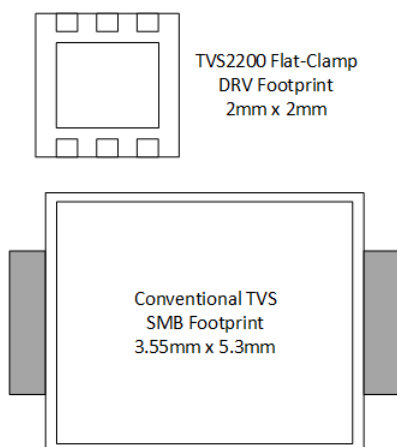
The TVS2200 is part of TI's Flat-Clamp family of surge devices. For more information on the other devices in the family, see the [Device Comparison Table](#).

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TVS2200	SON (6)	2.00 mm $\times$ 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Footprint Comparison



Voltage Clamp Response to 8/20 μ s Surge Event

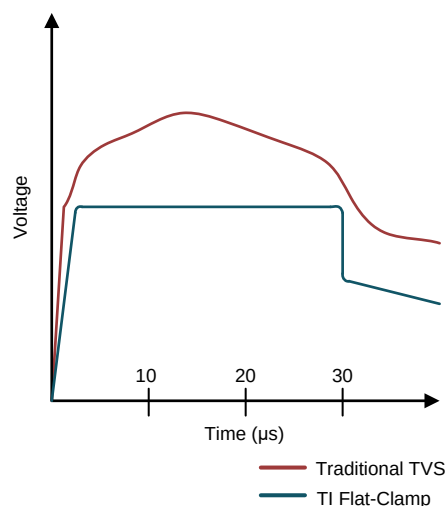


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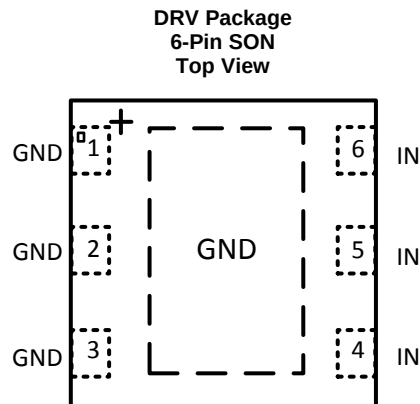
4 Revision History

Changes from Original (December 2017) to Revision A	Page
• Changed product status from Advance Information to Production Data	1

5 Device Comparison Table

Device	V_{rwm}	V_{clamp} at I_{pp}	I_{pp} (8/20 μs)	V_{rwm} leakage (nA)	Package Options	Polarity
TVS0500	5	9.2	43	0.07	SON	Unidirectional
TVS1400	14	18.4	43	2	SON	Unidirectional
TVS1800	18	22.8	40	0.5	SON	Unidirectional
TVS2200	22	27.7	40	3.2	SON	Unidirectional
TVS2700	27	32.5	40	1.7	SON	Unidirectional
TVS3300	33	38	35	19	WCSP, SON	Unidirectional

6 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	No.		
IN	4, 5, 6	I	ESD and surge protected channel
GND	1, 2, 3, exposed thermal pad	GND	Ground

7 Specifications

7.1 Absolute Maximum Ratings

 $T_A = 27^{\circ}\text{C}$ (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Maximum Surge	IEC 61000-4-5 Current (8/20 μs)		40	A
	IEC 61000-4-5 Power (8/20 μs)		1120	W
	IEC 61643-321 Current (10/1000 μs)		5	A
	IEC 61643-321 Power (10/1000 μs)		145	W
Maximum Forward Surge	IEC 61000-4-5 Current (8/20 μs)		50	A
	IEC 61000-4-5 Power (8/20 μs)		80	W
	IEC 61643-321 Current (10/1000 μs)		23	A
	IEC 61643-321 Power (10/1000 μs)		60	W
EFT	IEC 61000-4-4 EFT Protection		80	A
I_{BR}	DC Breakdown current		18	mA
I_F	DC Forward Current		500	mA
T_A	Ambient Operating Temperature	-40	125	$^{\circ}\text{C}$
T_{stg}	Storage Temperature	-65	150	$^{\circ}\text{C}$

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings - JEDEC

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	± 2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	± 500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings - IEC

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	IEC 61000-4-2 contact discharge	± 17	kV
	IEC 61000-4-2 air-gap discharge	± 30	

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	NOM	MAX	UNIT
V_{RWM} Reverse Stand-off Voltage		22		V

7.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TVS2200	UNIT
		DRV (SON)	
		6 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	70.4	$^{\circ}\text{C/W}$
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	73.7	$^{\circ}\text{C/W}$
R_{qJB}	Junction-to-board thermal resistance	40	$^{\circ}\text{C/W}$
Y_{JT}	Junction-to-top characterization parameter	2.2	$^{\circ}\text{C/W}$

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

TVS2200

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Thermal Information (continued)

THERMAL METRIC ⁽¹⁾		TVS2200	UNIT
		DRV (SON)	
		6 PINS	
Y_{JB}	Junction-to-board characterization parameter	40.3	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	11	°C/W

7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse Stand-off Voltage		-0.5		22	V
I_{LEAK}	Leakage Current	Measured at $V_{IN} = V_{RWM}$ $T_A = 27^{\circ}\text{C}$		3.5	62	nA
		Measured at $V_{IN} = V_{RWM}$ $T_A = 85^{\circ}\text{C}$		25	400	nA
		Measured at $V_{IN} = V_{RWM}$ $T_A = 105^{\circ}\text{C}$		80	1300	nA
V_F	Forward Voltage	$I_{IN} = 1\text{ mA}$ from GND to IO	0.25	0.5	0.65	V
V_{BR}	Break-down Voltage	$I_{IN} = 1\text{ mA}$ from IO to GND	24.6	25.9	27.6	V
V_{FCLAMP}	Forward Clamp Voltage	40 A IEC 61000-4-5 Surge (8/20 μs) from GND to IO, 27°C	1	2	5	V
V_{CLAMP}	Clamp Voltage	24 A IEC 61000-4-5 Surge (8/20 μs) from IO to GND, $V_{IN} = 0\text{ V}$ before surge, 27°C		27.2	27.7	V
		40 A IEC 61000-4-5 Surge (8/20 μs) from IO to GND, $V_{IN} = 0\text{ V}$ before surge, 27°C		27.6	28	V
		35 A IEC 61000-4-5 Surge (8/20 μs) from IO to GND, $V_{IN} = V_{RWM}$ before surge, $T_A = 125^{\circ}\text{C}$		27.8	28.35	V
R_{DYN}	8/20 μs surge dynamic resistance	Calculated from V_{CLAMP} at $.5 \cdot I_{pp}$ and I_{pp} surge current levels, 27°C		30		m Ω
C_{IN}	Input pin capacitance	$V_{IN} = V_{RWM}$, $f = 1\text{ MHz}$, 30 mV _{pp} , IO to GND		105		pF
SR	Maximum Slew Rate	0- V_{RWM} rising edge, sweep rise time and measure slew rate when $I_{PK} = 1\text{ mA}$, 27°C		2.5		V/ μs
		0- V_{RWM} rising edge, sweep rise time and measure slew rate when $I_{PK} = 1\text{ mA}$, 105°C		0.7		V/ μs

7.7 Typical Characteristics

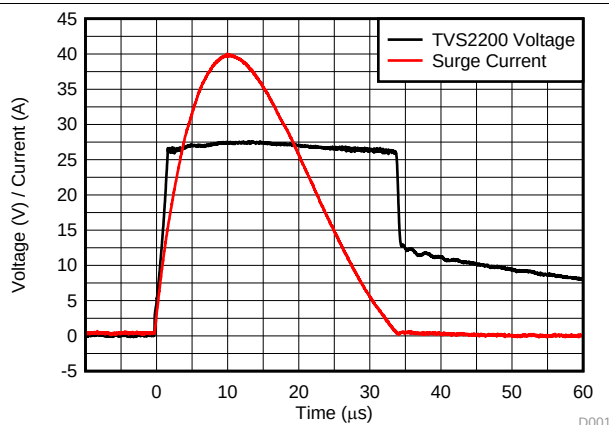


Figure 1. Surge Response at 40 A

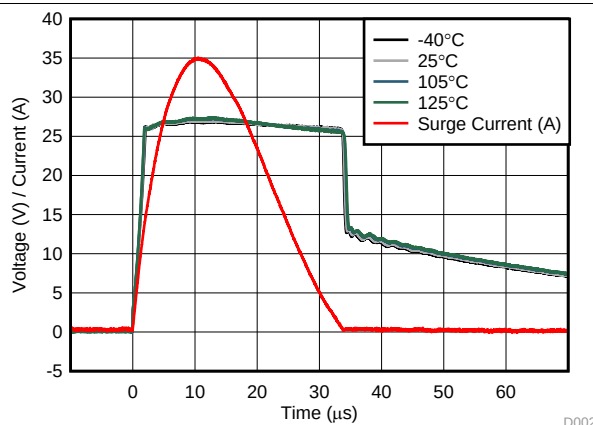


Figure 2. Surge Response at 35 A Across Temperature

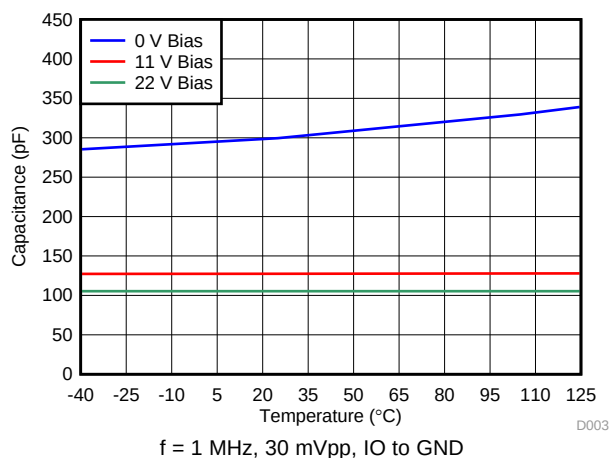


Figure 3. Capacitance vs Temperature Across Bias

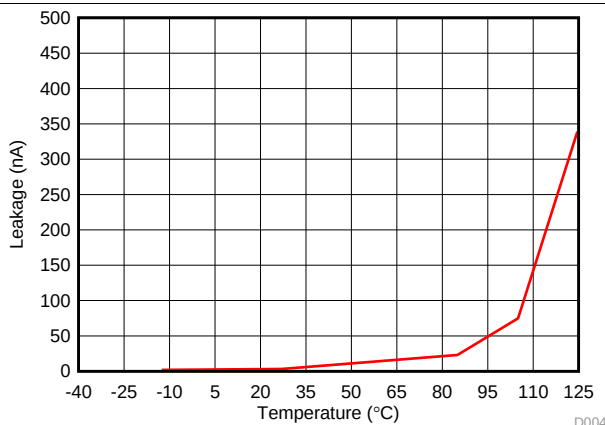


Figure 4. Leakage Current vs Temperature at 22 V

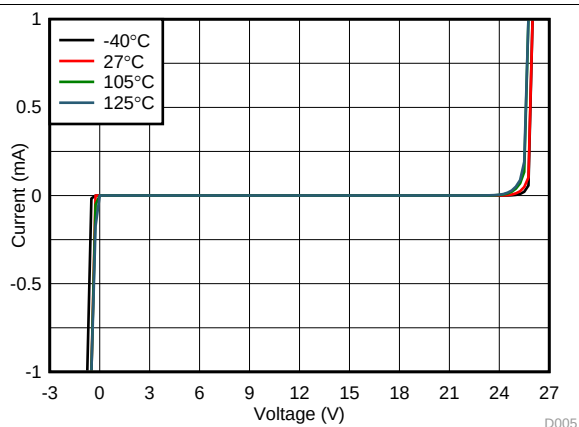


Figure 5. IV Across Temperature

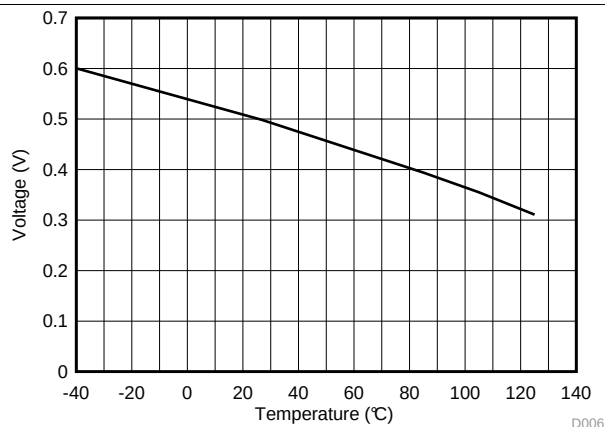


Figure 6. Forward Voltage vs Temperature Across Current

Typical Characteristics (continued)

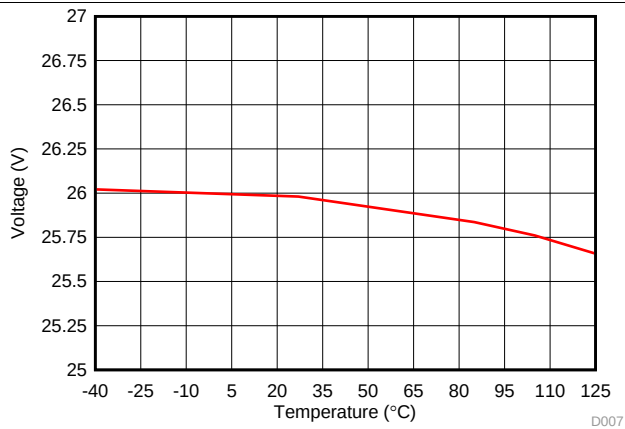


Figure 7. Breakdown Voltage at 1 mA vs Temperature

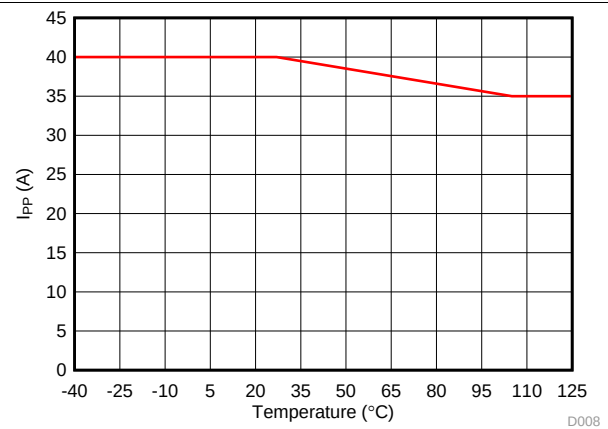


Figure 8. Max Surge Current (8/20 μ s) vs Temperature

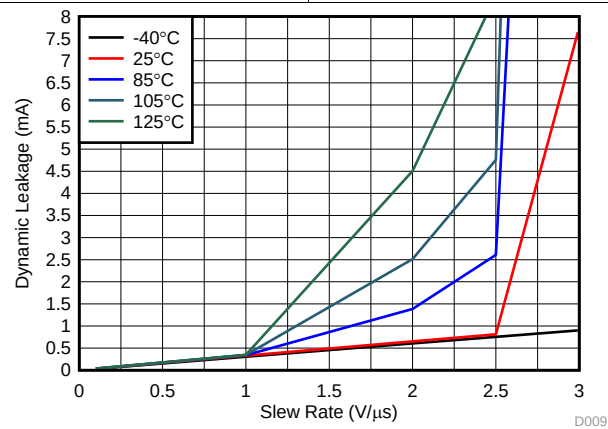


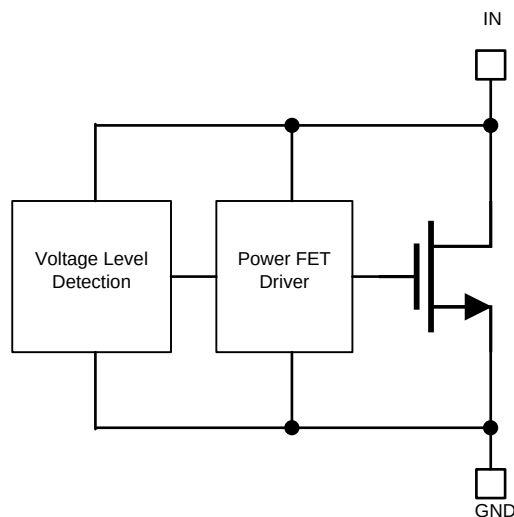
Figure 9. Maximum Leakage vs Signal Slew Rate across Temperature

8 Detailed Description

8.1 Overview

The TVS2200 is a precision clamp with a low, flat clamping voltage during transient overvoltage events like surge and protecting the system with zero voltage overshoot. For a detailed overview of the Flat-Clamp family of devices, please reference TI's [Flat-Clamp surge protection technology for efficient system protection](#) white paper. This document explains in detail the functional operation of the devices and how they impact and improve system design.

8.2 Functional Block Diagram



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8.3 Feature Description

The TVS2200 is a precision clamp that handles 40 A of IEC 61000-4-5 8/20 μ s surge pulse. The flat clamping feature helps keep the clamping voltage very low to keep the downstream circuits from being stressed. The flat clamping feature can also help end-equipment designers save cost by opening up the possibility to use lower-cost lower voltage tolerant downstream ICs. The TVS2200 has minimal leakage under the standoff voltage of 22 V, making it an ideal candidate for applications where low leakage and power dissipation is a necessity. IEC 61000-4-2 and IEC 61000-4-4 ratings make it a robust protection solution for ESD and EFT events. Wide ambient temperature range of -40°C to $+125^{\circ}\text{C}$ makes it a good candidate for most applications. Compact packages enable it to be used in small devices and save board area.

8.4 Reliability Testing

To ensure device reliability, the TVS2200 is characterized against 5000 repetitive pulses of 35 A IEC 61000-4-5 8/20 μ s surge pulses at 125°C . The test is performed with less than 10 seconds between each pulse at high temperature to simulate worst case scenarios for fault regulation. After each surge pulse, the TVS2200 clamping voltage, breakdown voltage, and leakage are recorded to ensure that there is no variation or performance degradation. By ensuring robust, reliable, high temperature protection, the TVS2200 enables fault protection in applications that must withstand years of continuous operation with no performance change.

8.5 Device Functional Modes

8.5.1 Protection Specifications

The TVS2200 is specified according to both the IEC 61000-4-5 and IEC 61643-321 standards. This enables usage in systems regardless of which standard is required in relevant product standards or best matches measured fault conditions. The IEC 61000-4-5 standard requires protection against a pulse with a rise time of 8 μs and a half length of 20 μs while the IEC 61643-321 standard requires protection against a much longer pulse with a rise time of 10 μs and a half length of 1000 μs .

The positive and negative surges are imposed to the TVS2200 by a combinational waveform generator (CWG) with a 2- Ω coupling resistor at different peak voltage levels. For powered on transient tests that need power supply bias, inductances are usually used to decouple the transient stress and protect the power supply. The TVS2200 is post tested by guaranteeing that there is no shift in device breakdown or leakage at V_{rwm} .

In addition, the TVS2200 has been tested according to IEC 61000-4-5 to pass a ± 1 kV surge test through a 42- Ω coupling resistor and a 0.5 μF capacitor. This test is a common test requirement for industrial signal I/O lines and the TVS2200 will serve an ideal protection solution for applications with that requirement.

The TVS2200 also integrates IEC 61000-4-2 Level 4 ESD Protection and 80 A of IEC 61000-4-4 EFT Protection. These combine to ensure that the device can protect against all transient conditions regardless of length or type.

For more information on TI's test methods for Surge, ESD, and EFT testing, reference [TI's IEC 61000-4-x Testing Application Note](#).

8.5.2 Minimal Derating

Unlike traditional diodes the TVS2200 has very little derating of max power dissipation and ensures robust performance up to 125°C shown in [Figure 8](#). Traditional TVS diodes lose up to 50% of their current carrying capability when at high temperatures, so a surge pulse above 85°C ambient can cause failures that are not seen at room temperature. The TVS2200 prevents this and ensures that you will see the same level of protection regardless of temperature.

8.5.3 Transient Performance

During large transient swings, the TVS2200 will begin clamping the input signal to protect downstream conditions. While this prevents damage during fault conditions, it can cause leakage when the intended input signal has a fast slew rate. In order to keep power dissipation low and remove the chance of signal distortion, it is recommended to keep the slew rate of any input signal on the TVS2200 below 2.5 V/ μs at room temperature and below 0.7 V/ μs at 125°C shown in [Figure 9](#). Faster slew rates will cause the device to clamp the input signal and draw current through the device for a few microseconds, increasing the rise time of the signal. This will not cause any harm to the system or to the device, however if the fast input voltage swings occur regularly it can cause device overheating.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TVS2200 can be used to protect any power, analog, or digital signal from transient fault conditions caused by the environment or other electrical components.

9.2 Typical Application

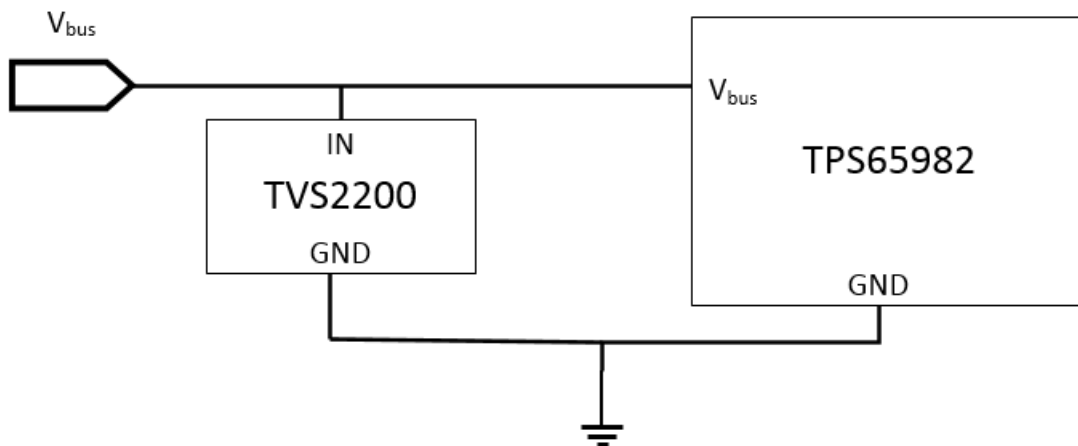


Figure 10. TVS2200 Application Schematic

9.2.1 Design Requirements

A typical operation for the TVS2200 would be protecting a USB Type-C V_{bus} input, with a nominal input voltage of 20 V and a required withstand of 22 V, shown in [Figure 10](#). In this example, a TVS2200 is protecting the input to a TPS65982 Type-C Port Controller. Without any input protection, if a surge event is caused by lightning, coupling, hot-swap ringing, or any other fault condition this input voltage will rise to hundreds of volts for multiple microseconds, violating the absolute maximum input voltage and harming the device.

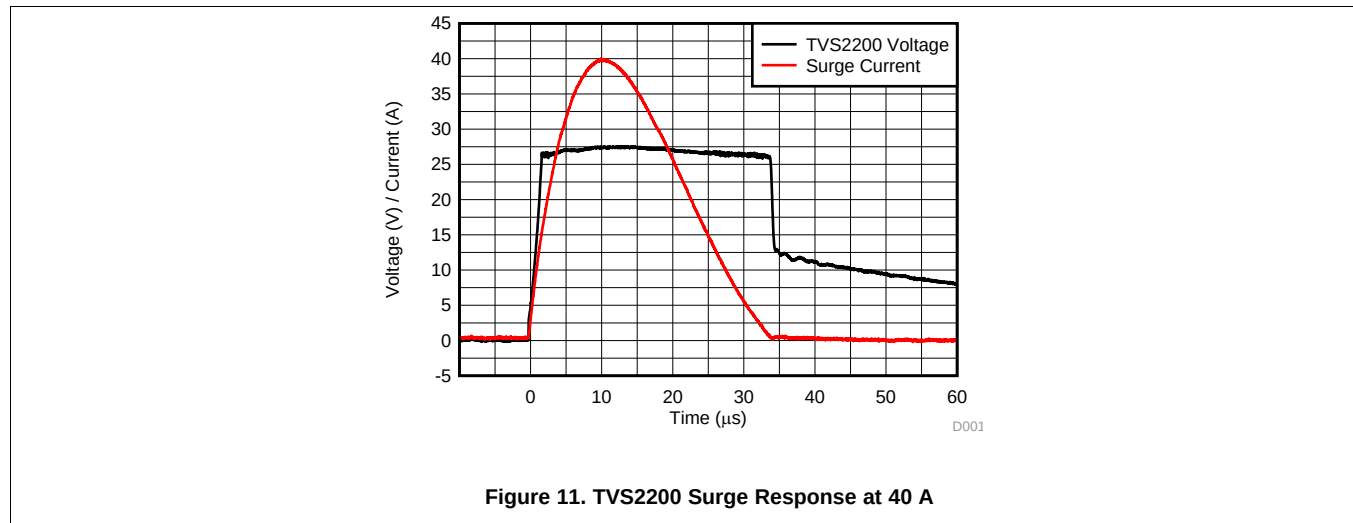
9.2.2 Detailed Design Procedure

If the TVS2200 is in place to protect the device, during a surge event the voltage will rise to the breakdown of the diode at 25.9 V, and then the TVS2200 will turn on, shunting the surge current to ground. With the low dynamic resistance of the TVS2200, even large amounts of surge current will have minimal impact on the clamping voltage. The dynamic resistance of the TVS2200 is around 30 m Ω , which means 40 A of surge current will cause a voltage raise of $40 \text{ A} \times 30 \text{ m}\Omega = 1.2 \text{ V}$. Because the device turns on at 25.9 V, this means the input will be exposed to a maximum of $25.9 \text{ V} + 1.2 \text{ V} = 27.1 \text{ V}$ during surge pulses, robustly protecting the USB Type-C port. This pulse is shown in [Figure 11](#) and ensures robust protection of the circuit.

Typical Application (continued)

Finally, the small size of the device also improves fault protection by lowering the effect of fault current coupling onto neighboring traces. The small form factor of the TVS2200 allows the device to be placed extremely close to the input connector, lowering the length of the path fault current will take through the system compared to larger protection solutions.

9.2.3 Application Curves



9.2.4 Configuration Options

The TVS2200 can be used in either unidirectional or bidirectional configuration. The TVS2200 shows unidirectional usage to protect an input. By placing two TVS2200's in series with reverse orientation, bidirectional operation can be used which will allow a working voltage of ± 22 V. TVS2200 operation in bidirectional will be similar to unidirectional operation, with a minor increase in breakdown voltage and clamping voltage. The TVS3300 bidirectional performance has been characterized in the [TVS3300 Configurations Characterization](#). While the TVS2200 in bidirectional configuration has not specifically been characterized, it will have similar relative changes to the TVS3300 in bidirectional configuration.

10 Power Supply Recommendations

The TVS2200 is a clamping device so there is no need to power it. Take care not to violate the recommended V_{IN} voltage range (0 V to 22 V) to ensure the device functions properly.

11 Layout

11.1 Layout Guidelines

The optimum placement is as close to the connector as possible. EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.

Route the protected traces as straight as possible.

Eliminate any sharp corners on the protected traces between the TVS2200 and the connector by using rounded corners with the largest radii possible. Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Example

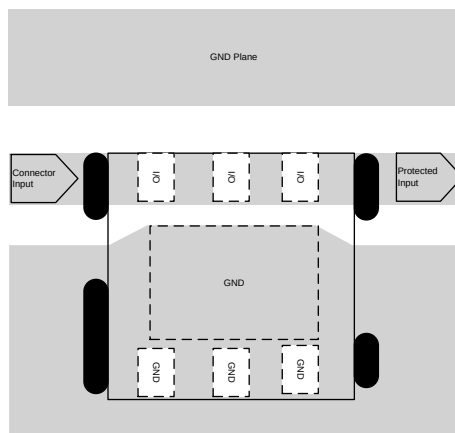


Figure 12. TVS2200 Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TVS2200DRVR	ACTIVE	WS0N	DRV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1HVH	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

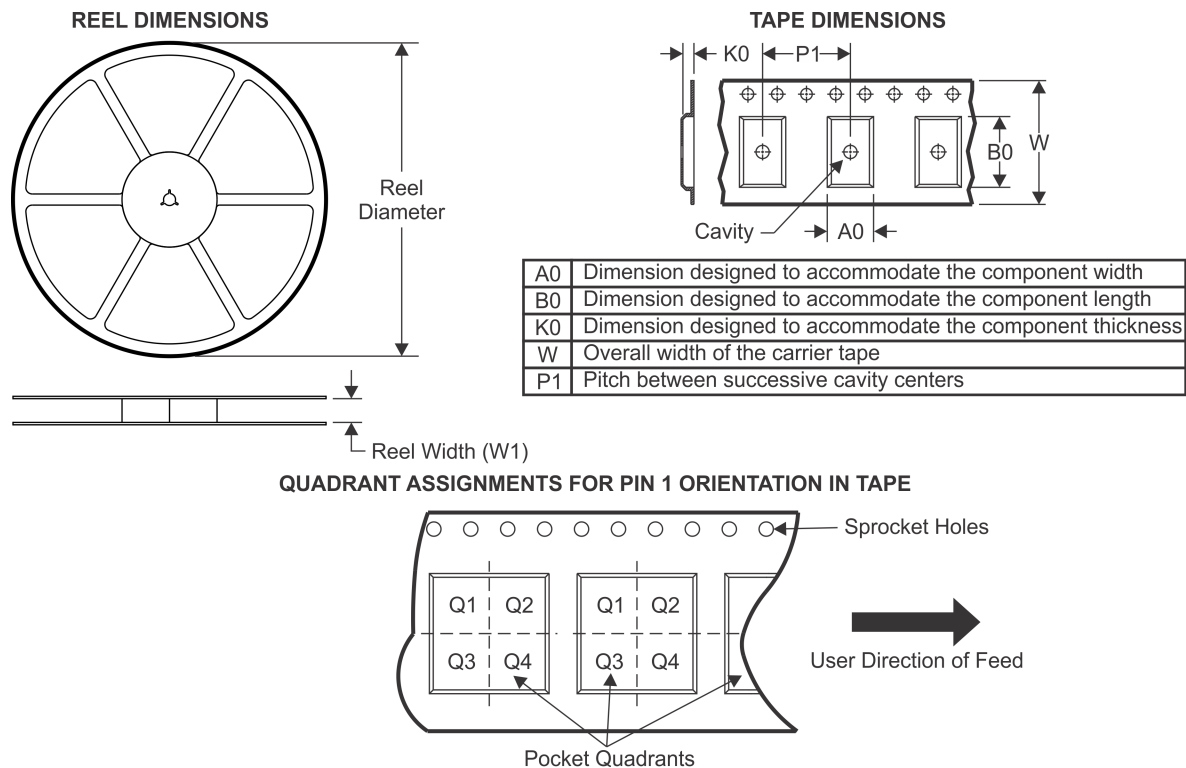
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

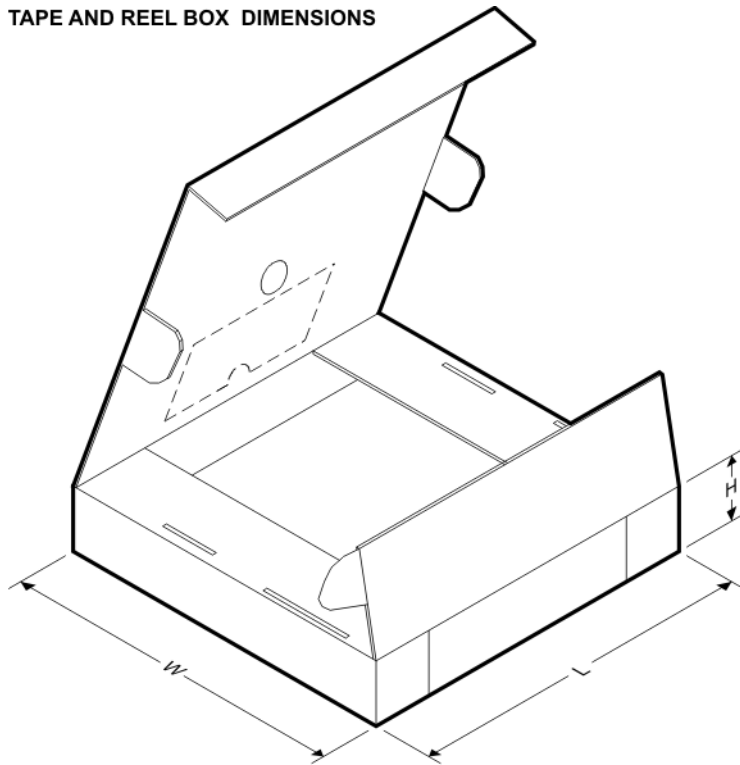
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

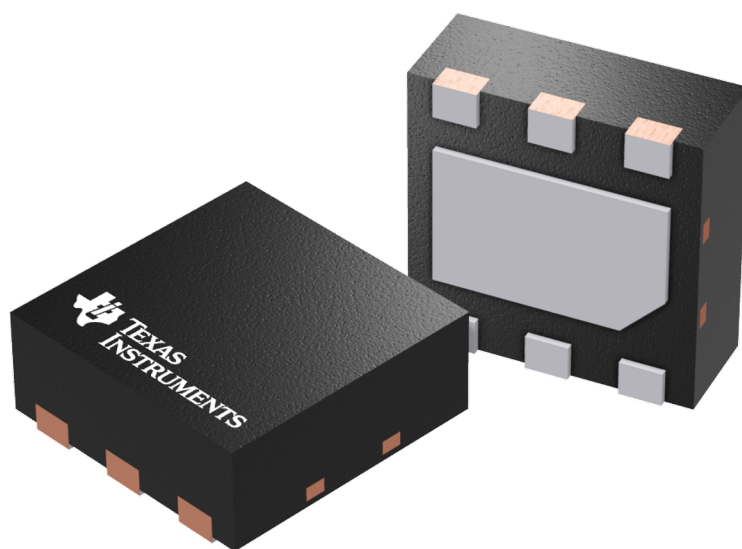
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TVS2200DRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

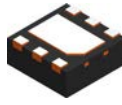
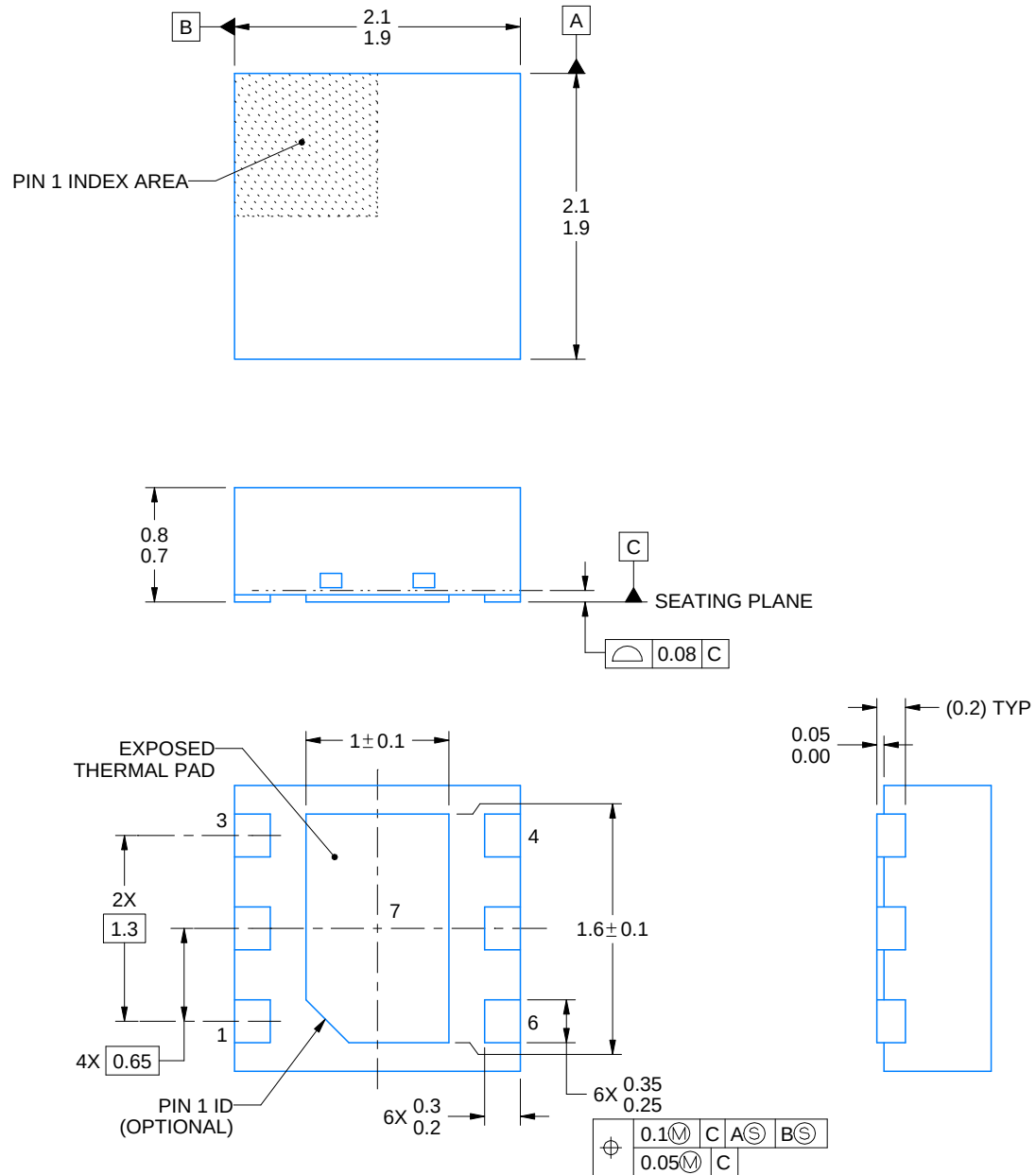


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TVS2200DRVR	WS0N	DRV	6	3000	210.0	185.0	35.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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NOTES:

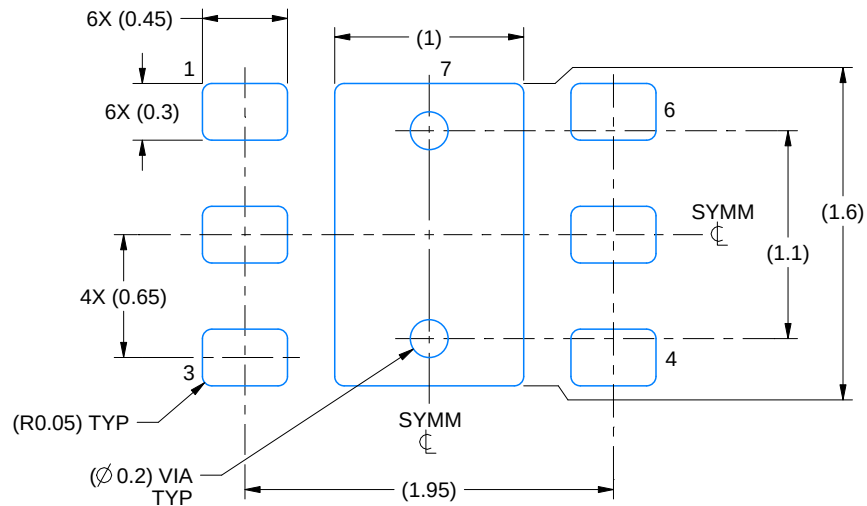
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

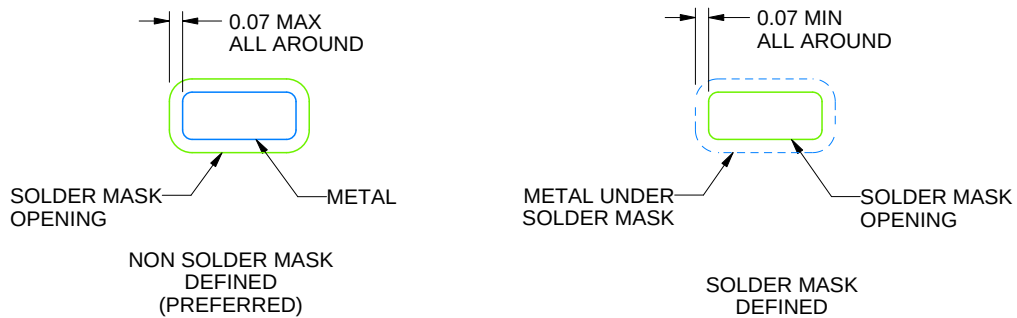
DRV0006A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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NOTES: (continued)

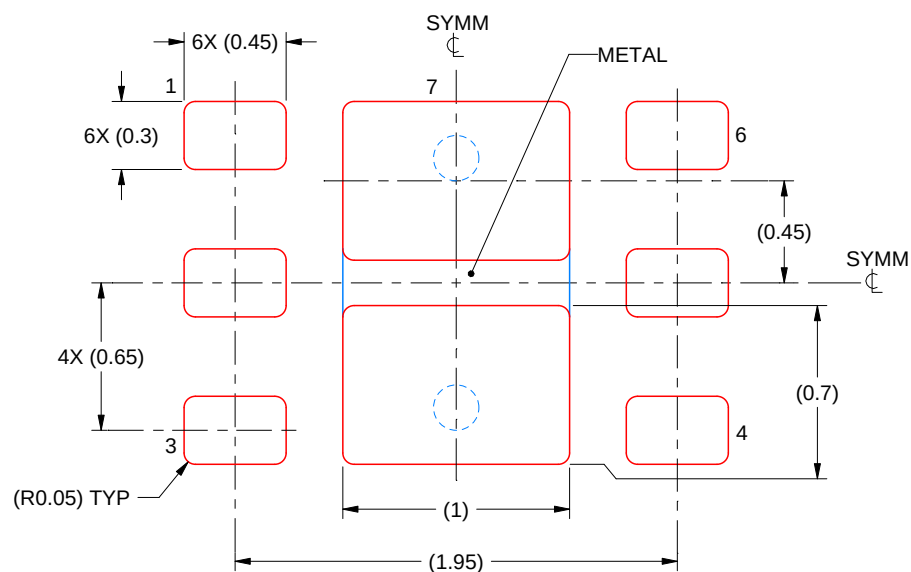
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sl原因271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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