MAX31953/MAX31963

Octal Industrial Digital Input with Isolated SPI Interface

General Description

The MAX31953/MAX31963 translates eight current-sinking, 12V, 24V, or 48V industrial inputs to a galvanically isolated, SPI-compatible, serial output that interfaces with 3V to 5.5V logic. The galvanic isolation is certified to $500V_{RMS}$ for 60 seconds, with creepage and clearance distances of 1.4 mm. The input side (field-side) of the device includes a 5V logic serial input for daisy-chaining data from other devices (such as the MAX31911/MAX31913) through the devices' isolated serial port, eliminating the need for additional isolators. The field-side of the devices requires a single 4.5V to 5.5V supply. This power is supplied either directly or through the integrated voltage regulator. The MAX31953 includes a linear voltage regulator, while the MAX31963 includes an efficient buck regulator that requires an external inductor. Both regulators accept input voltages from 7V to 36V. The logic-side of the devices operate from a single 3V to 5.5V supply, which also sets the SPI logic level.

Applications

- Programmable Logic Controllers
- Industrial Automation
- Process Automation
- Building Automation

Standard Compliance (Pending)

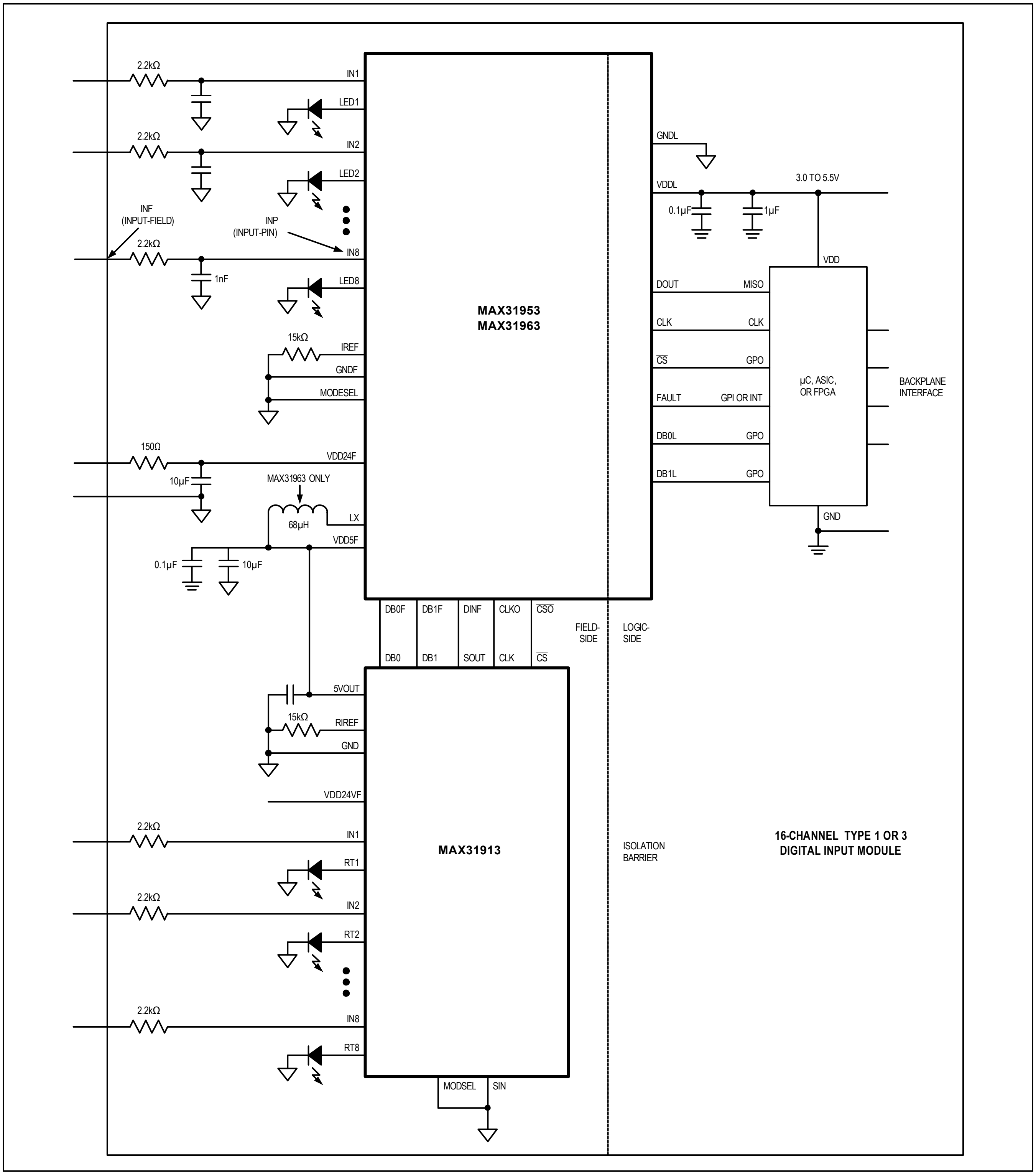
- UL1577

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Reduced Power and Heat Dissipation
  - Accurate Input-Current Limiters
  - Energyless Field-Side LED Drivers
  - Integrated Buck Regulator (MAX31963)
- Configurability Enables Wide Range of Standard and Custom Applications
  - Eight High-Voltage Input Channels (36V Max)
  - Configurable IEC 61131-2 Type 1, 2, 3 Inputs
  - Configurable Input Current-Limiting From 0.5mA to 6mA
  - Selectable 0, 25µs, 0.75ms, or 3ms Input Debounce Filtering
  - High-Speed, 2µs Update Rate
- High Integration Reduces BOM Count and Board Space
  - Integrated $500V_{RMS}$ Galvanic Isolation
  - Integrated 5V LDO (MAX31953)
  - Daisy-Chain Capability Eliminates Isolators
  - 48-Pin TSSOP Package
  - Integrated Overtemperature Monitor and Thermal Shutdown
  - Integrated Field-Supply Voltage Monitors
  - 5-Bit CRC Code Generation and Transmission For Error Detection
  - ±15kV ESD HBM Immunity on IN1–IN8
  - -40°C to +125°C Ambient Operating Temperature
- Operates Directly From Field Supply in 12V and 24V Systems
  - Integrated Voltage Regulator Accepts 7V to 36V
  - Option to Power Directly From a 5V Supply
- SPI Interface Flexibility
  - Compatible with 3.3V or 5V Logic
  - Daisy-Chain Data From the Field-Side

Typical Application Circuit



Absolute Maximum Ratings

VDDL to GNDL ....-0.3V to +6V
VDD5F to GNDF ....-0.3V to +6V
VDD24F to GNDF ....-0.3V to +45V
GNDL to GNDF for 1 min ....$500V_{RMS}$
DB0L, DB1L, $\overline{CS}$, CLK to GNDL............................-0.3V to +6V
DOUT, FAULT to GNDL..........................-0.3V to (VDDL + 0.3V)
Short-circuit duration FAULT, DOUT
to VDDL or GDL ....Continuous
DB0F, DB1F, DINF, MODESEL,
CLKO, $\overline{CSO}$, IREF to GNDF .... -0.3V to (VDD5F + 0.3V)
Short-circuit duration CLKO, $\overline{CSO}$
to VDD5F or GNDF ....Continuous
IN1–IN8 to GNDF ....0.3V to +45V
IN1–IN8 to GNDF with 2.2kΩ series resistor ....-45V to +45V
LED1 – LED8 to GNDF ....-0.3V to +6V
Continuous Power Dissipation (T_A = +70°C)
48-pin TSSOP
(derate at 54.2mW/°C above +70°C) 4333mW
Operating Temperature Range
Ambient Temperature ....+125°C
Junction Temperature ....+150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....18.46°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....1.82°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

DC Electrical Characteristics

V_{VDDL} - V_{GNDL} = +3.0V to +5.5V, V_{VDD5F} - V_{GNDF} = +4.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. C_L = 15pF. Typical values are at V_{VDDL} - V_{GNDL} = +3.3V, V_{VDD5F} - V_{GNDF} = +5V, VDD24F connected to VDD5F, V_{GNDL} - V_{GNDF} = 0V, and T_A = +25°C. (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Logic Supply Voltage	VDDL			3.0		5.5	V
Logic Supply Current	I_{VDDL}	$\overline{CS}$ = GNDL, CLK = 2MHz	$V_{VDDL} – V_{GNDL}$ = +3.3V		6.2	9.5	mA
			$V_{VDDL} – V_{GNDL}$ = +5V		7.2	11	
Field Supply Voltage	VDDL24F	When using the internal regulator in MAX31963.		7		36	V
	VDD24F	When using the internal regulator in MAX31953		7		36	V
	VDD5F	When powering the field-side directly from a 5V supply (Note 3)		4.5		5.5	V
Field Supply Current of VDD24F in MAX31963	I_{VDD24F}	VDD24F = 24V	IN1–IN8 = 24V, LED1–LED8 = GNDF, $\overline{CS}$ = GNDL, CLK = 2MHz, (DB0F, DB1F, $\overline{CSO}$, CLKO = unconnected, RIREF = 15kΩ.		3.2	7	mA
Field Supply Current of VDD24F in MAX31953	I_{VDD24F}				9.1	14	mA
Field Supply Current Powered From VDD5F	I_{VDD5F}	VDD5F = 5V			8.8	14	mA

DC Electrical Characteristics (continued)

V_{VDDL} - V_{GNDL} = +3.0V to +5.5V, V_{VDD5F} - V_{GNDF} = +4.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. C_L = 15pF. Typical values are at V_{VDDL} - V_{GNDL} = +3.3V, V_{VDD5F} - V_{GNDF} = +5V, VDD24F connected to VDD5F, V_{GNDL} - V_{GNDF} = 0V, and T_A = +25°C. (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VDD5F Undervoltage-Lockout Threshold	V_{UVLO5F}	VDD5F rising		3.5	4	4.5	V
VDD5F Undervoltage-Lockout-Threshold Hysteresis	$V_{UVHYST5F}$				0.4		V
MAX31953 Regulator Output Voltage	V_{VDD5FL}	Max I_{LOAD} = 50Ma	T_A = +25°C	4.5	5	5.5	V
			T_A = -40°C to 125°C	4.5	5	5.5	
MAX31963 Regulator Output Voltage	V_{VDD5FB}	Max I_{LOAD} = 50mA	T_A = +25°C	4.5	5	5.5	V
			T_A = -40°C to 125°C	4.5	5	5.5	
MAX31963 Regulator Efficiency		VDD24F = 24V, Load = 50mA Inductor = 68µH with R = 1.95Ω, T_A = 25°C (e.g., inductor part number SD3814-680R)			82		%
MAX31953 Line Regulation	$dVDD5F_{LINEL}$	I_{LOAD} = 50mA, including internal load, VDD24F = 7V to 24V			20		mV
MAX31963 Line Regulation	$dVDD5F_{LINEB}$	I_{LOAD} = 50mA, including internal load, VDD24F = 7V to 24V			14		mV
MAX31953 Load Regulation	$dVDD5F_{LOAD}$	I_{LOAD} = 1mA to 50mA C_{LOAD} = 4.7µF			20		mV
MAX31963 Load Regulation	$dVDD5F_{LOAD}$	I_{LOAD} = 5mA to 50mA C_{LOAD} = 4.7µF			25		mV
Buck Regulator Frequency	f_{BUCK}	VDD24F = 24V, I_{LOAD} = 50mA			469		kHz
VDD24F UV1 Alarm On/Off	$V_{ALRMOFFUV1}$	Rising VDD24F			9	10	V
VDD24F UV1 Alarm Off/On	$V_{ALRMONUV1}$	Falling VDD24F		7	8		V
VDD24F UV2 Alarm On/Off	$V_{ALRMOFFUV2}$	Rising VDD24F			16.6	18	V
VDD24F UV2 Alarm Off/On	$V_{ALRMONUV2}$	Falling VDD24F		14	15.7		V
Overtemperature Alarm	T_{ALRM}	Junction temperature			155		°C
Overtemperature Alarm Hysteresis	T_{ALRM_HYS}				7		°C
Thermal-Shutdown Threshold	TSHDN				165		°C
Thermal-Shutdown Hysteresis	TSHDN_HYS				10		°C
FIELD INPUTS							
LED On-State Current	I_{LEDON}	RIREF = 15kΩ, VDD24F = 18V to 30V			2.4		mA
Field-Input Threshold High-to-Low	V_{INF-}	2.2kΩ external series resistor		6.2	9.1		V
Field-Input Threshold Low-to-High	V_{INF+}	2.2kΩ external series resistor			10	10.82	V
Field-Input Threshold Hysteresis	V_{INFHYS}	2.2kΩ external series resistor			0.9		V

DC Electrical Characteristics (continued)

V_{VDDL} - V_{GNDL} = +3.0V to +5.5V, V_{VDD5F} - V_{GNDF} = +4.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. C_L = 15pF. Typical values are at V_{VDDL} - V_{GNDL} = +3.3V, V_{VDD5F} - V_{GNDF} = +5V, VDD24F connected to VDD5F, V_{GNDL} - V_{GNDF} = 0V, and T_A = +25°C. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Threshold High-to-Low (at IC pin)	V_{THP-}	IN1 – IN8	2.9	3.4		V
Input Threshold Low-to-High (at IC pin)	V_{THP+}	IN1 – IN8		4.2	4.8	V
Input Threshold Hysteresis (at IC pin)	V_{INPHYS}	IN1 – IN8		0.8		V
Field-Input Data Rate	f_{IN}			200		kHz
Current-Limit Setting Resistor	RIREF	Nominal value	4.99	15	62	kΩ
Field-Input Current Limit	I_{INLIM}	RIREF = 15k, V_{IN} = 18V to 30V, T_A = +25°C to +125°C (Note 4)	2.1	2.4	2.85	mA
Debounce Filter Time Constant (See Table 1)	t_{BOUNCE}	DB1L/DB0L = 0/0: no filtering		0		ms
		DB1L/DB0L = 0/1	0.008	0.025	0.038	
		DB1L/DB0L = 1/0	0.25	0.75	1.1	
		DB1L/DB0L = 1/1	1	3	4.5	
INTERFACE LOGIC						
Input Logic-High Voltage	V_{IH}	CLK, $\overline{CS}$ relative to GNDL	0.7 x V_{VDDL}			V
		DB0L, DB1L relative to GNDL	0.80			
		DINF, MODESEL relative to GNDF	0.7 x V_{VDD5F}			
Input Logic-Low Voltage	V_{IL}	CLK, $\overline{CS}$ relative to GNDL			0.8	V
		DB0L, DB1L relative to GNDL			0.5	
		DINF, MODESEL relative to GNDF			0.8	
Output Logic-High Voltage	V_{OH}	CLKO, $\overline{CSO}$ sourcing 4mA	V_{VDD5F} -0.4			V
		DOUT, FAULT sourcing 4mA	V_{VDDL} -0.4			V
Open-Drain Pullup Current		DB0F, DB1F (from VDD5F)		30		µA
Output Logic-Low Voltage	V_{OL}	CLKO, $\overline{CSO}$ sinking 4mA to GNDF			0.8	V
		DOUT, FAULT sinking 4mA to GNDL			0.8	
		DB0F, DB1F sinking 4mA to GNDF			0.8	
Logic-Input Leakage Current	I_{IL}	$\overline{CS}$, CLK	-1		1	µA
Logic Input Capacitance		$\overline{CS}$, CLK (capacitance to GNDL)		2		pF
DYNAMIC CHARACTERISTICS						
Common-Mode Transient Immunity	dV_{ISO}/dt	V_{IN} = $V_{VDD\_}$ or $V_{GND\_}$ (Note 6)		1.5		kV/µs

AC Electrical Characteristics

V_{VDDL} - V_{GNDL} = +3.0V to +5.5V, V_{VDD5F} - V_{GNDF} = +4.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. CL = 15pF. Typical values are at V_{VDDL} - V_{GNDL} = +3.3V, V_{VDD5F} - V_{GNDF} = +5V, VDD24F connected to VDD5F, V_{GNDL} - V_{GNDF} = 0V, and T_A = +25°C. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Detectable Field Input Pulse Width	t_{PW}	No external capacitors on pins IN1-IN8			1.3	µs
CLK Pulse Duration	t_{CLKPW}	See Figure 6	50			ns
$\overline{CS}$ Pulse Duration	t_{CSPW}	See Figure 3	50			ns
DINF-to-CLKO Setup Time	t_{SU1}	(Note 8) See Figure 4	5			ns
DINF-to-CLKO Hold Time	t_{H1}	(Note 8) See Figure 4	8			ns
$\overline{CS}$-to-CLK Setup Time	t_{SU2}	See Figure 5	12			ns
$\overline{CS}$-to-CLK Recovery Time	t_{REC}	See Figure 5	16			ns
Channel-to-Channel Skew		(Notes 7, 8)			5	ns
Clock Pulse Frequency	f_{CLK}	See Figure 6			10	MHz
Propagation Delay, CLK-to-DOUT	t_{P1}	See Figure 6			80	ns
Propagation Delay, $\overline{CS}$-to-DOUT	t_{P2}	See Figure 3			80	ns
Rise/Fall Time DOUT/FAULT	$t_{R/F}$	(Note 8) See Figure 6		7		ns
Propagation Delay $\overline{CS}$-to-$\overline{CSO}$					30	ns
Propagation Delay CLK-to-CLKO					30	ns

Note 2: All units are production tested at 25°C. Specifications over temperature are guaranteed by design and characterization. Typical values are not guaranteed. All voltages on the logic side are referenced to GNDL. All voltages on the field-side are referenced to GNDF.

Note 3: If a 24V supply is not available, the device can be powered through VDD5F. In this mode of operation, VDD24F must be connected to VDD5F. The field-supply UV1 and UV2 alarms will be activated (set to 1), indicating the absence of the 24V supply in this mode of operation. All other specifications remain identical.

Note 4: External resistor RIREF is selected to set any desired current limit between 0.5mA and 6mA.

Note 5: The isolation voltage is guaranteed for t = 60s, and tested at 120% of the guaranteed value for 1s.

Note 6: Common mode voltage (V_{CM}) = 250V. Guaranteed by design and characterization, not production tested.

Note 7: Channel-to-channel difference in the time between assertion of $\overline{CS}$ and the input state being latched.

Note 8: Design guaranteed by bench characterization. Limits are not production tested.

Insulation Characteristics

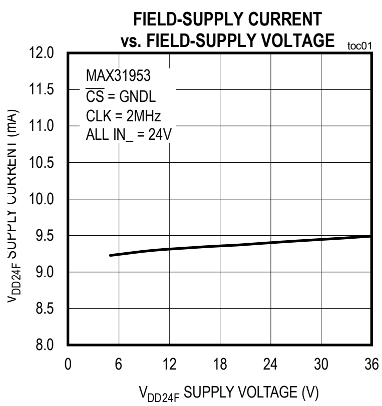
PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Maximum Repetitive Peak Isolation Voltage	V_{IORM}		283	V_P
Maximum Working Isolation Voltage	V_{IOWM}		200	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s	840	V_P
Maximum Withstand Isolation Voltage	V_{ISO}	f = 60Hz, duration = 60s	500	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Basic insulation	1	kV
Insulation Resistance	R_S	T_A = +150°C V_{IO} = 500V	10^9	Ω
Barrier Capacitance Input to Output	CIO	f = 1MHz	12	pF
Minimum Creepage Distance	CPG		1.4	mm
Minimum Clearance Distance	CLR		1.4	mm
Internal Clearance		Distance through insulation	0.0026	mm
Comparative Tracking Resistance Index	CTI	Material Group II (IEC 60112)	550	
Climatic Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

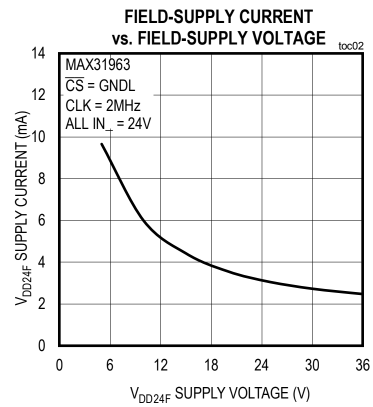
ESD Protection

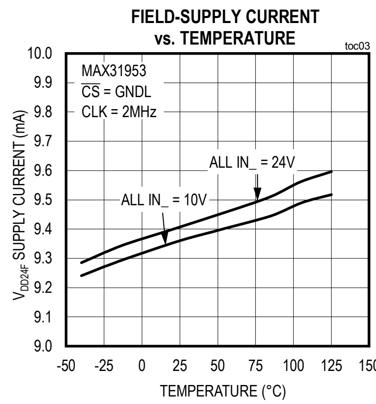
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD		Human Body Model, all pins		±2		kV
		Human Body Model, IN1-IN8 with respect to GNDF		±15		

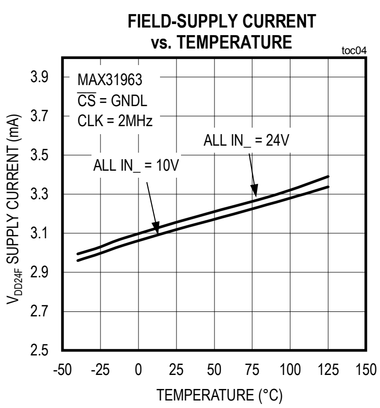
Typical Operating Characteristics

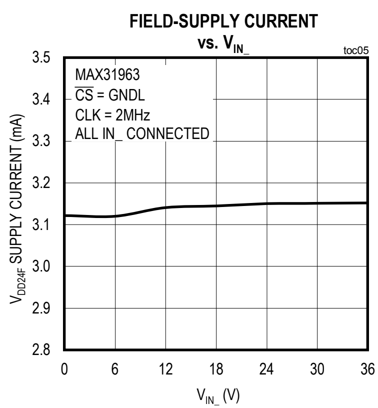
(T_A = +25°C, RIREF = 15kΩ, unless otherwise noted.)

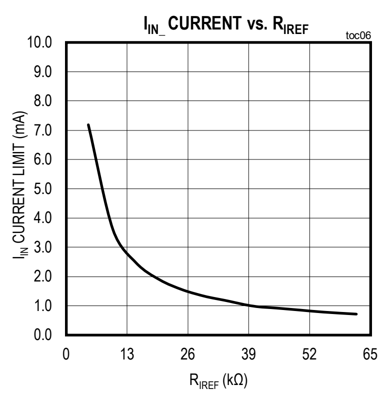


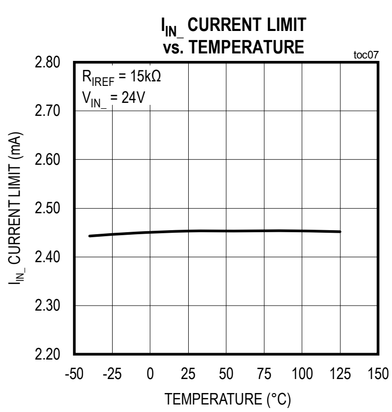


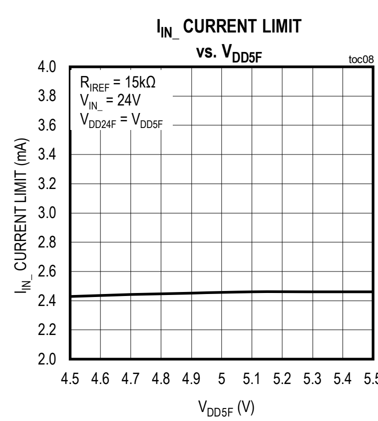






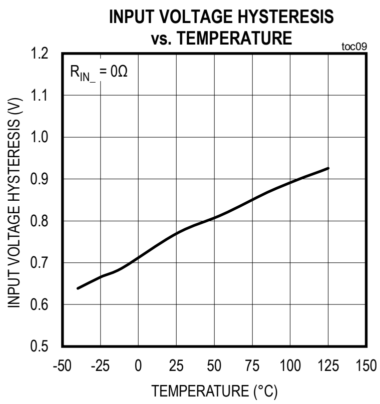


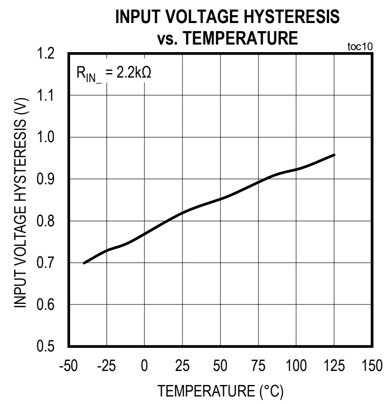


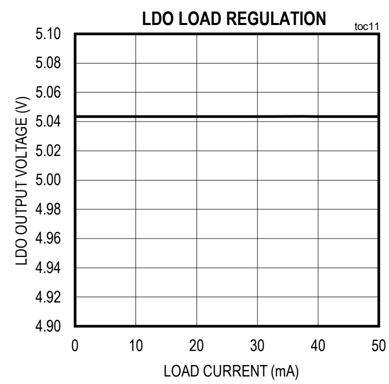


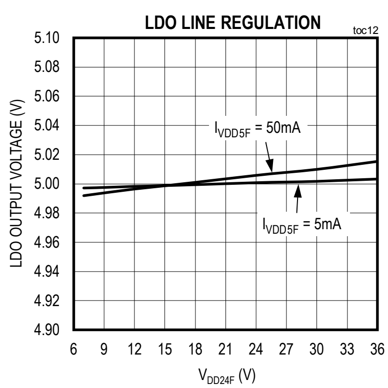
Typical Operating Characteristics (continued)

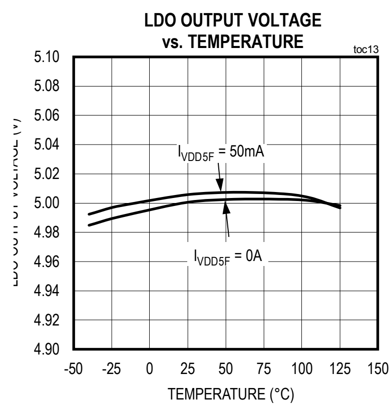
(T_A = +25°C, RIREF = 15kΩ, unless otherwise noted.)

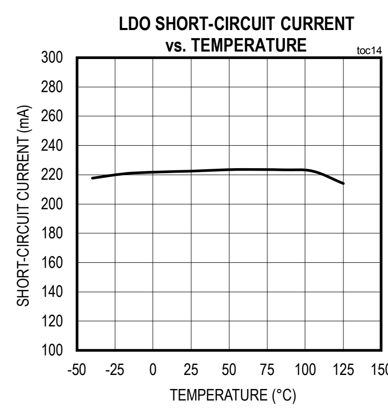


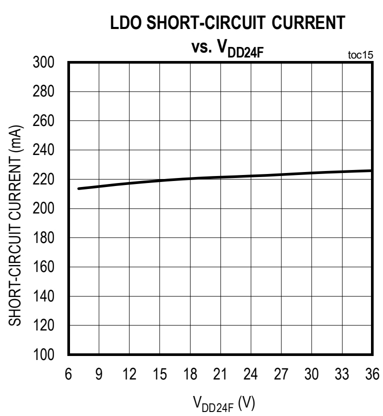


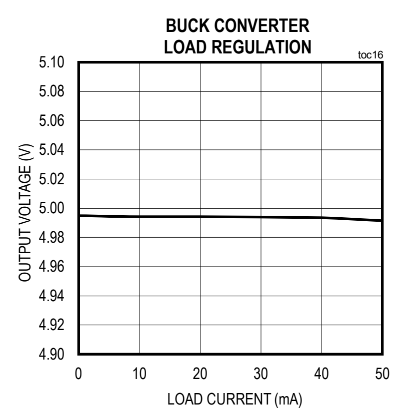






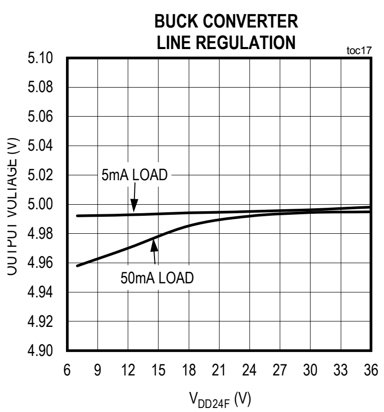


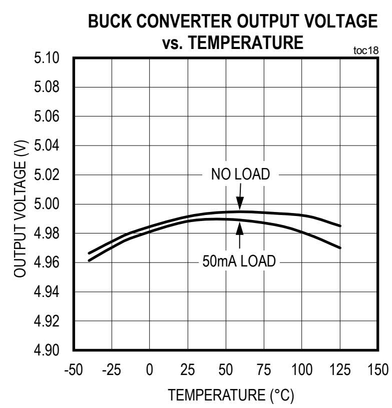


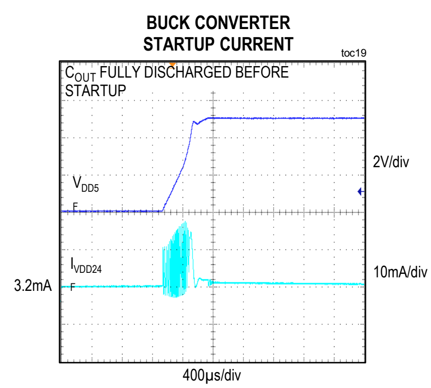


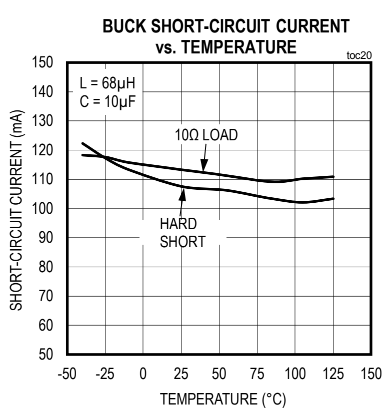
Typical Operating Characteristics (continued)

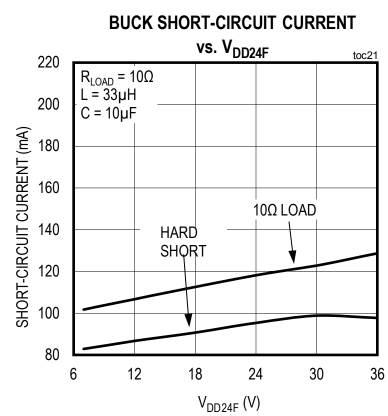
(T_A = +25°C, RIREF = 15kΩ, unless otherwise noted.)

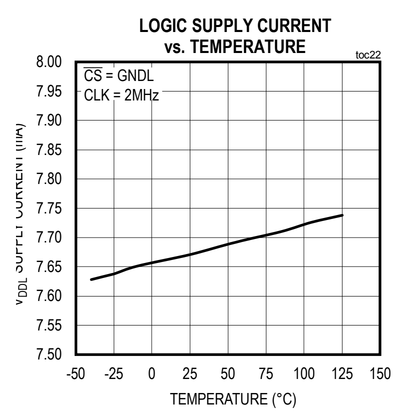


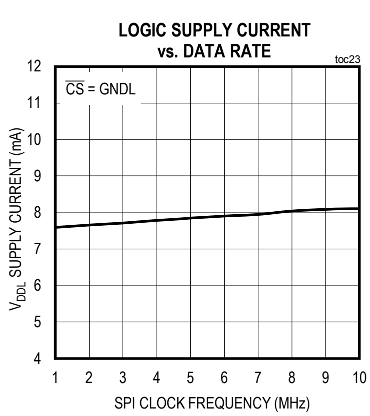


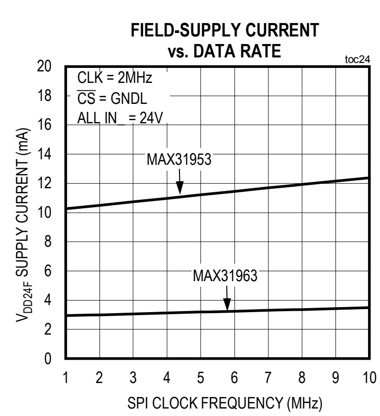






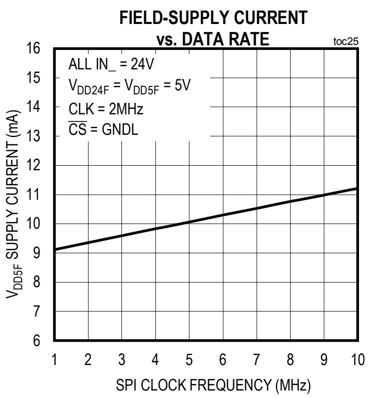


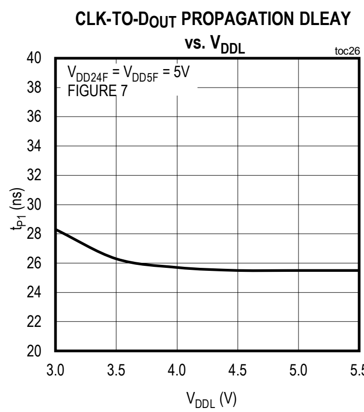


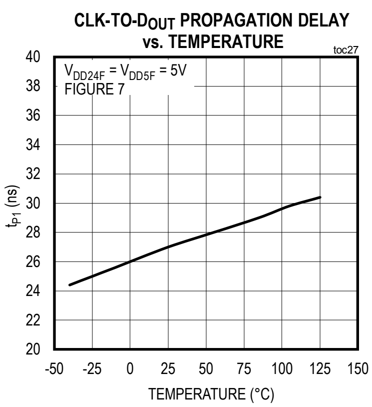


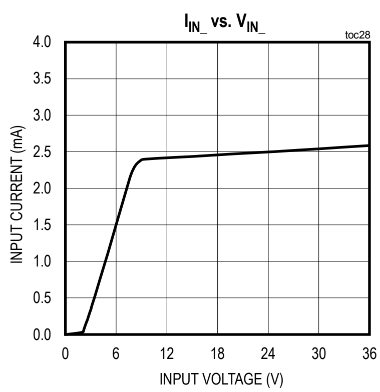
Typical Operating Characteristics (continued)

(T_A = +25°C, RIREF = 15kΩ, unless otherwise noted.)

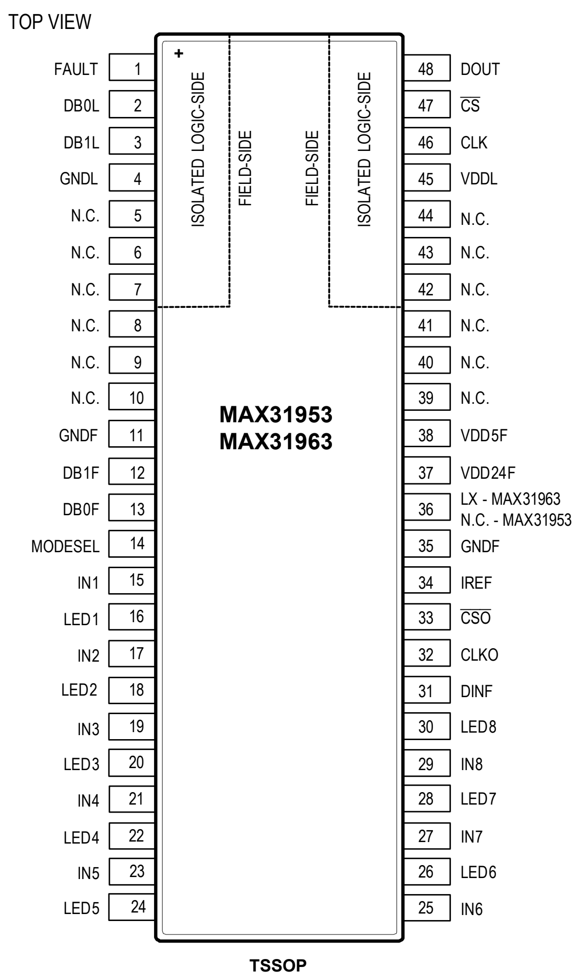








Pin Configurations



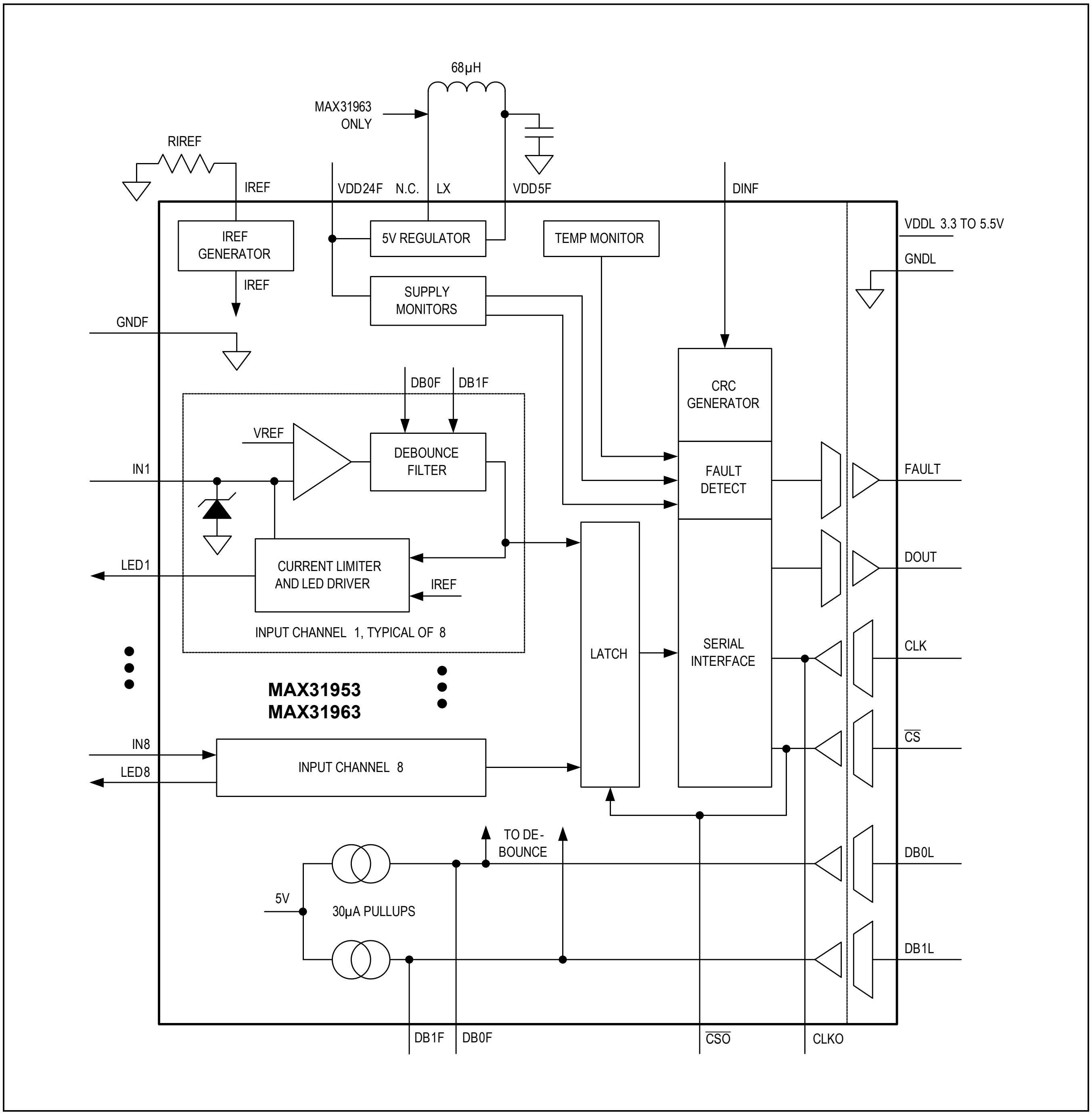
Pin Description

PIN	NAME	FUNCTION
LOGIC-SIDE PINS		
1	FAULT	Active-High Fault Indicator. A high state indicates low field-side supply voltage or an overtemperature condition. Read status bits for cause of fault.
2	DB0L	This input controls debounce filter in conjunction with DB1L. See Table 1.
3	DB1L	This input controls debounce filter in conjunction with DB0L. See Table 1.
4	GNDL	Logic-Side Ground for Power and Signals
45	VDDL	Logic-Side Supply
46	CLK	Serial-Clock Input for the SPI interface
47	$\overline{CS}$	Chip-Select Input. Assert low to enable the SPI interface.
48	DOUT	Serial Data Output of the SPI Interface. When $\overline{CS}$ is high DOUT is high.

Pin Description (continued)

PIN	NAME	FUNCTION
ISOLATION/CREEPAGE PINS		
5-10, 39-44	N.C.	Not Connected. The space between these pins provides necessary creepage and clearance. The PWB area between these pins should be clear of traces.
FIELD-SIDE PINS		
11, 35	GNDF	Field-Side Ground. Ground return for all data inputs and the field power supply
12	DB1F	Isolated Open-drain Output of DB1L. Controls debounce filter in conjunction with DB0L. See Table 1. If daisy-chaining to MAX31911 or MAX31913, connect to DB1 of daisy-chained devices to control their debounce filter.
13	DB0F	Isolated Open-Drain Output of DB0L. Controls debounce filter in conjunction with DB1L. See Table 1. If daisy-chaining to MAX31911 or MAX31913, connect to DB0 of daisy-chained devices to control their debounce filter.
14	MODESEL	SPI Mode-Select Input. Tie MODESEL high for 8-bit data (IN1-IN8 states only). Tie MODESEL low for 16-bit data (IN1-IN8 plus CRC and status bits).
15, 17, 19, 21, 23, 25, 27, 28	IN1 – IN8, respectively	Field inputs. For 24V type 1 and type 3 inputs, place a 2.2kΩ resistor between the field input and IN_.
16, 18, 20, 22, 24, 26, 28, 30	LED1 – LED8, respectively	Energyless LED Driver Outputs. Connect to GNDF if LEDs are not used.
31	DINF	Serial Data Input Field-Side. Data input for daisy-chaining.
32	CLKO	Isolated SPI Clock Output for Daisy-Chain Applications. Connect to CLK input of all devices in the chain.
33	$\overline{\text{CSO}}$	Isolated Chip-Select Output for Daisy-Chain Applications. Connect to $\overline{\text{CS}}$ of all devices in the chain.
34	IREF	Current-Limit Reference Resistor. For 24V Type 1 and Type 3 inputs, place a 15kΩ resistor from IREF to GNDF.
36	LX	(MAX31963) When using internal buck converter, connect 68FH inductor between LX and VDD5F. Connect a 10µF capacitor in parallel with a 0.1µF capacitor from VDD5F to GNDF.
	N.C.	(MAX31953) No connect.
37	VDD24F	MAX31954 Field-Side Power Input for LDO. Connect to 24V field supply. MAX31963 Field-side Power Input for Buck Converter. Connect to 24V field supply.
38	VDD5F	Output of Buck Converter or LDO. Power input for field-side circuit. Bypass to GNDF with 4.7µF capacitor. If the integrated regulator is not used and if the field-side is powered using a 5V supply, connect an external 5V supply to VDD5F and VDD24F.
EP	—	Exposed Pad. Connect to GNDF. Solder entire exposed pad area (EP = exposed pad on back of package) to ground plane for best thermal performance.

Functional (or Block) Diagram



Detailed Description

The MAX31953/MAX31963 senses the state (on, high or off, low) of eight digital inputs. The input data is serialized and sent across the isolation barrier to an SPI interface. For compliance with IEC 61131-2 Type 1 and Type 3 digital inputs, a 15k current-setting resistor is connected from IREF to GNDF and a resistor (RINx) placed between each field input and the corresponding INx pin. Under these conditions, the current into INx rises linearly with an input voltage up to approximately 2.4mA and then remains constant. This constant-current mode significantly reduces power dissipation while maintaining compliance with the IEC61131-2 standard for digital inputs. The nominal thresholds plus the additional voltage drop across a 2.2k series resistor provides system thresholds that are compatible with both Type 1 and Type 3 inputs.

Input current and system threshold voltage can be changed by changing the value of resistor RIREF and the value of the series input resistor (RINx). The input current limit is set by the value of RIREF and is adjustable over a range of 0.5mA to 6mA. I_{IN} = 36/RIREF, where I_{IN} is the nominal input current in mA and RIREF is the resistor value in kΩ. RIREF sets the current limit for all eight inputs. The nominal threshold voltage at INx is not affected by changes in the input current. However, system threshold voltages will be affected due to the voltage drop across the series input resistor RINx. The following equation provides the transition threshold at the field input (RINx input).

$$V_{INF} = V_{THP} + RINx \times 31.2/RIREF$$

where,

V_{INF} is the field input threshold voltage,

V_{THP} is the devices' threshold (V_{THP+} for rising inputs and V_{THP-} for falling inputs, as shown in the *Electrical Characteristics* table), RINx is the kΩ value of the resistor between the field input and the INx pin of the devices, and RIREF is the resistor from IREF to GNDF.

Energyless LED Drivers

When INx is determined to be on, its input current is diverted to the LEDx pin and flows from that pin to GNDF. Placing an LED between LEDx and GNDF provides an indication of the input state without increasing overall power dissipation. If the indicator LEDs are not used, connect LEDx to GNDF.

Fault Detection and Monitoring

The devices continually monitors die temperature and VDD24F. There are two alarm levels for VDD24F. The upper-voltage alarm clears the SPI flag UV2 to 0 when VDD24F drops below $V_{ALRMONUV2}$. This indicates a problem with the 24V supply. It is not an indication that the devices is close to its functional limit. UV2 does not assert the FAULT pin. When VDD24F rises above $V_{ALRMOFFUV2}$, the UV2 flag is set again to 1. The lower VDD24F alarm (UV1) trips when VDD24F falls below $V_{ALRMONUV1}$ and indicates that VDD24F is approaching the dropout voltage of the VDD5F regulator. The alarm clears the SPI flag UV1 to 0 and asserts the FAULT pin. The SPI flag is set again to 1 and the FAULT pin de-asserted when VDD24F rises above $V_{ALRMOFFUV1}$.

The overtemperature alarm trips when the nominal die temperature rises above T_{ALRM}. This sets the SPI flag OT to 1 and asserts the FAULT pin. The OT flag is cleared to 0 and the FAULT pin de-asserts when the die temperature drops below the alarm threshold and a hysteresis margin of T_{ALRM_HYS}. If the temperature continues to rise, thermal shutdown will occur above a die temperature of T_{SHDN}. At this point, the device shuts down and all internal functions of the device are disabled, including the serializer and the LDO or the buck regulator.

When powering the devices directly from a 5V supply, connect VDD24F directly to VDD5F. This is an automatic undervoltage condition for VDD24F, so both UV flags will be active and the FAULT pin asserts. The OT flag is still valid, but the FAULT output is no longer meaningful. See Figure 1 for a typical circuit powered using VDD5F on the field side.

Consult the Electrical Characteristics table for detailed information on alarm thresholds.

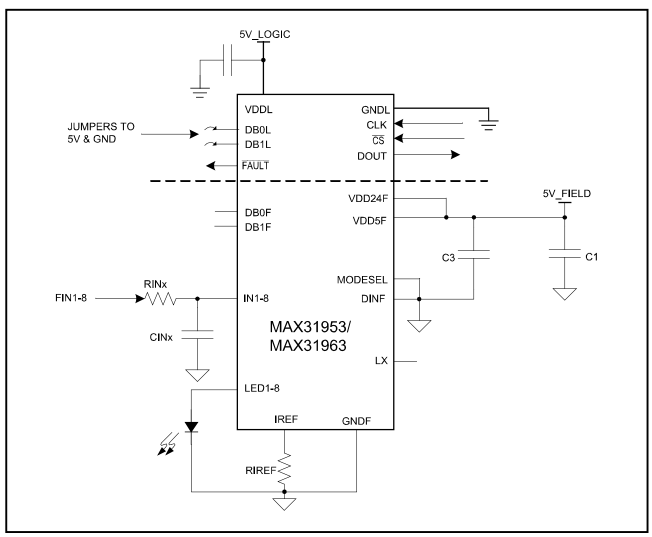


Figure 1. Powering Using VDD5F

CRC generation

The CRC code can be used to check data integrity during transfer from the device to an external microcontroller. In applications where the integrity of data transferred is not of concern, the CRC bits can be ignored. The CRC uses the following polynomial:

$$P(x) = x^5 + x^4 + x^2 + x^0$$

Glitch Filter

A digital glitch filter provides debouncing and filtering of noisy sensor signals. There are two galvanically isolated control inputs (DB0L and DB1L) that control the time-constant of a debounce filter. The time-constant of this filter is programmable from 0 to 3ms. The same time-constant is applied to all eight inputs. See Table 1 for debounce settings.

To provide the digital glitch filter, the device checks to see if an input is stable for at least three clock cycles. The duration of a clock cycle is 1/3 of the selected debounce time. If the input is not stable for at least three clock cycles, the input change is not sent to the internal shift register.

SPI Interface

The state of each input is read from an SPI interface that is galvanically isolated from the field inputs. Asserting $\overline{\text{CS}}$ latches the state of all inputs and enables the SPI interface. CLK clocks data out in either the 8-bit or 16-bit format, depending on the state of the MODESEL input. If MODESEL is high, only the states of the eight inputs are clocked-out as an 8-bit word. If MODESEL is low, then a 16-bit word is clocked out. The first 8 bits indicate the state of each input, while the last 8 bits contain three diagnostic flags (two undervoltage levels and overtemperature) plus a 5-bit CRC code to verify data integrity.

SPI Waveforms

The serial output of the device adheres to the SPI protocol, running with CPHA = 0 and CPOL = 0. Input states on IN1–IN8 are latched in on the falling-edge of $\overline{\text{CS}}$. The transfer of data out of the slave output (DOUT) starts

Table 1. Debounce Settings

DB0L	DB1L	BINARY VALUE	NOMINAL DEBOUNCE TIME
0	0	0	0
0	1	1	25µs
1	0	2	0.75ms
1	1	3	3ms

See Electrical Characteristics table for timing tolerance.

Table 2. MODESEL Settings

MODESEL SETTING	SPI DATA
0	16-bit output; [IN8–IN1] [CRC (5 bit)] [UV1] [OT] [UV2]
1	8-bit output; [IN8–IN1]

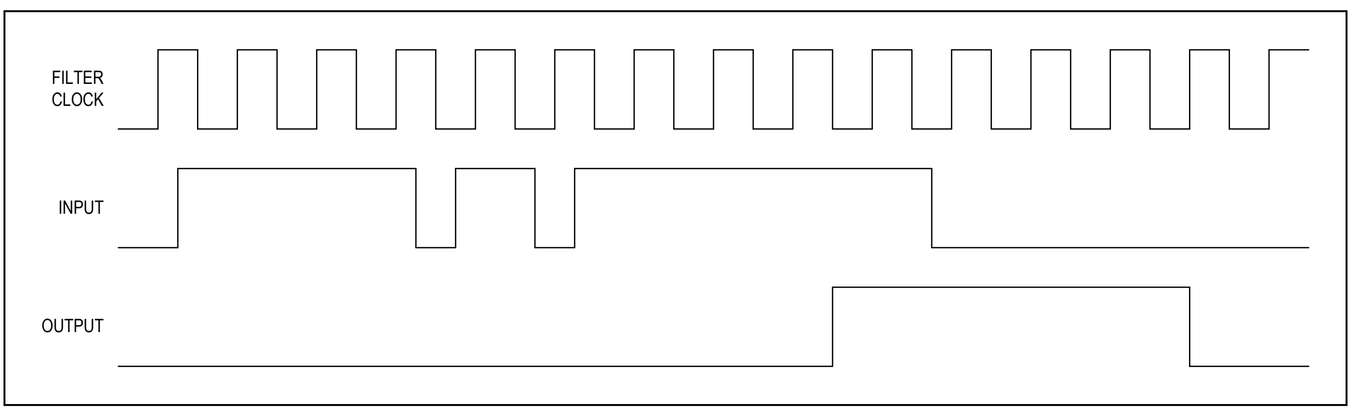


Figure 2. Debounce filter Example

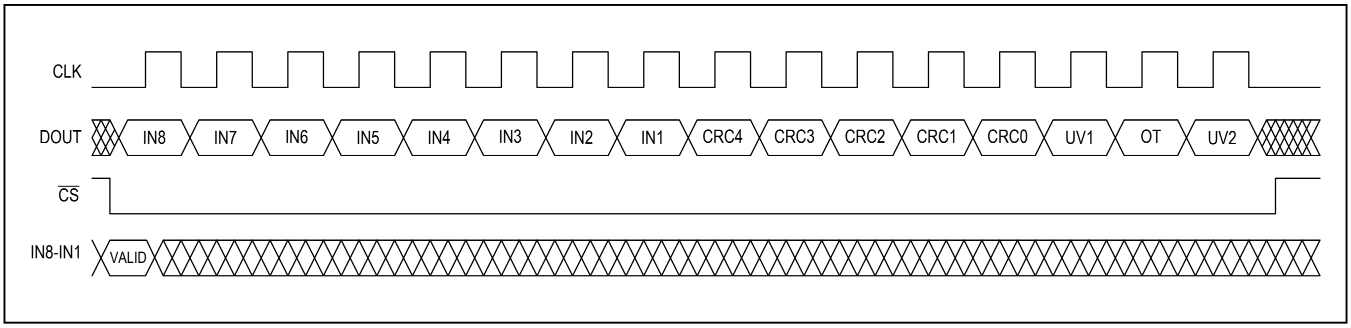


Figure 3. SPI Communication Example

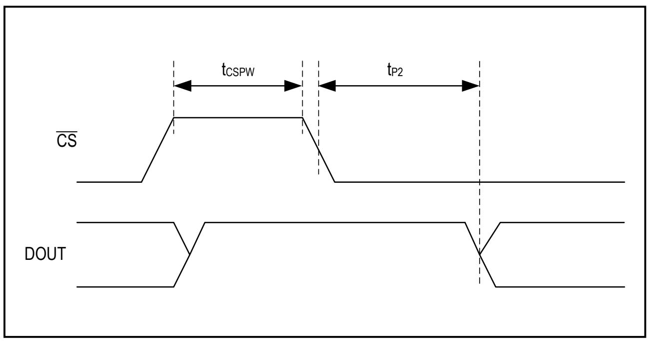


Figure 4. SPI Timing Diagram 1

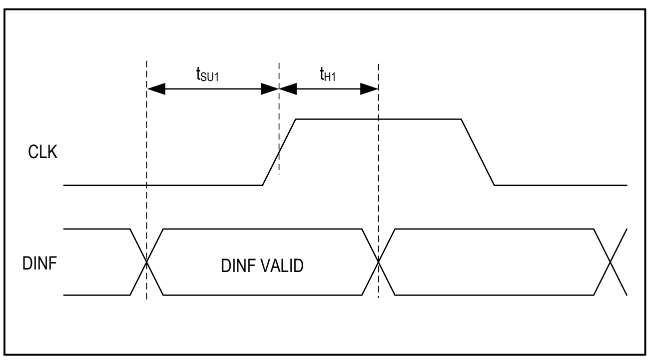


Figure 5. SPI Timing Diagram 2

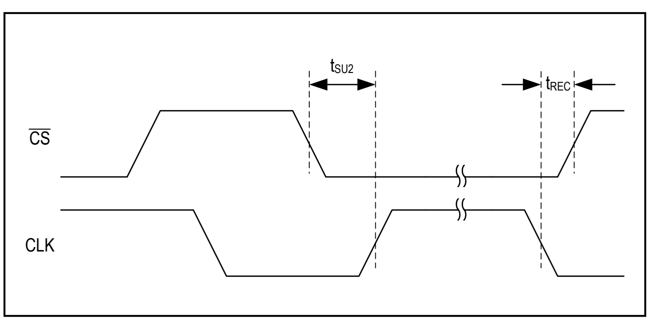


Figure 6. SPI Timing Diagram 3

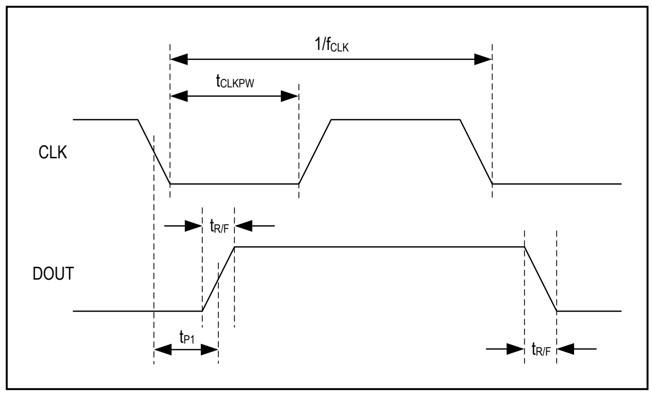


Figure 7. SPI Timing Diagram 4

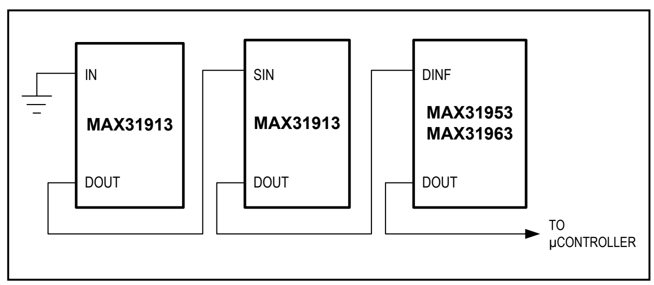


Figure 8. Daisy Chaining

immediately when $\overline{CS}$ is asserted (i.e., MSB is output onto DOUT independent of CLK). The remaining data bits are shifted out on the falling-edge of CLK. The data bits are shifted out through the output DOUT MSB first. When $\overline{CS}$ is high, DOUT is high. The resultant timing is shown in Figure 3. Note that all bits after IN1 are invalid if the 8-bit operation mode is selected using the MODESEL input. Figure 4 through Figure 7 illustrate the SPI timing specifications.

Daisy Chaining

For systems with more than eight sensor inputs, multiple devices can be daisy-chained to allow access to all data inputs through a single serial port. When using a daisy-chain configuration, connect DOUT of one of the devices to the SIN/DINF input of another upstream device. $\overline{CS}$ and CLK of all devices in the chain should be connected together in parallel (see Figure 4). In a daisy-chain configuration, external components used to enhance EMC robustness do not need to be duplicated for each device of a circuit board. Figure 5 illustrates a 24-input application.

Applications Information

EMC Standard Compliance

The external components shown in Figure 9 allow the device to operate in harsh industrial environments.

Components were chosen to assist in suppression of voltage burst and surge transients, allowing the system to meet or exceed international EMC requirements. Table 3 lists an example device for each component in Figure 9. The system shown in Figure 9, using the components shown in Table 3, is designed to be robust against IEC Fast Transient Burst, surge, RFI specifications, and ESD specifications (IEC 61000-4-4, -5, -6, and -2).

The recommendations in Figure 8 also apply to the MAX31963.

Power Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass VDDL, VDD24F, and VDD5F with 0.1µF ceramic capacitors to GNDL and GNDF, respectively. Place the bypass capacitors as close as possible to the power supply input pins.

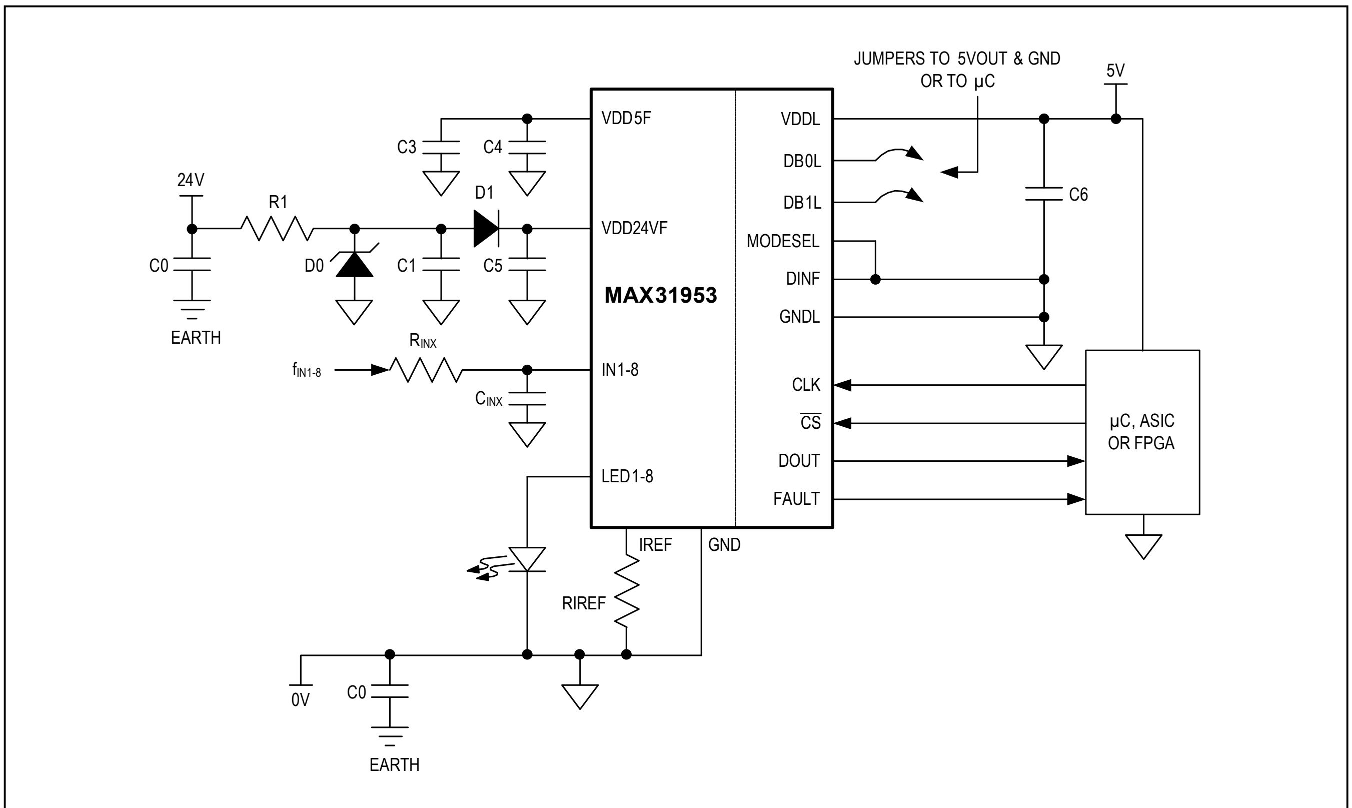


Figure 9. Typical EMC Protection Circuitry for the MAX319153

Table 3. Recommended Components

COMPONENT	DESCRIPTION	REQUIRED/RECOMMENDED/OPTIONAL
C0	4,7nF, 2kV polypropylene capacitor	Recommended
C1	10µF, 60V ceramic capacitor	Required
C3	100nF, 10V ceramic capacitor	Recommended
C4	4,7µF, 10V low ESR ceramic capacitor	Required
C5	100nF, 100V ceramic capacitor	Recommended
CINX	1nF, 100V ceramic capacitor	Required
C6	100nF, 10V ceramic capacitor	Required
D0	36V fast zener diode (ZSMB36)	Recommended
D1	General-purpose rectifier (IN4007)	Optional: For reverse-polarity protection. This diode can alternatively be placed in series with the field supply (24V)
LED1–LED8	LEDs for visual input status indication	Optional
R1	150Ω, 1/3W MELF resistor	Required
RINX	2,2kΩ, 1/4W MELF resistor	Required
RIREF	15kΩ, 1/8W resistor	Required

Ordering Information

PART	REGULATOR TYPE	TEMP RANGE	PIN-PACKAGE	CARRIER
MAX31953AUM+	LINEAR	-40°C to +125°C	48 TSSOP-EP	Bulk
MAX31953AUM+T	LINEAR	-40°C to +125°C	48 TSSOP-EP	Tape and Reel
MAX31963AUM+	BUCK	-40°C to +125°C	48 TSSOP-EP	Bulk
MAX31963AUM+T	BUCK	-40°C to +125°C	48 TSSOP-EP	Tape and Reel

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

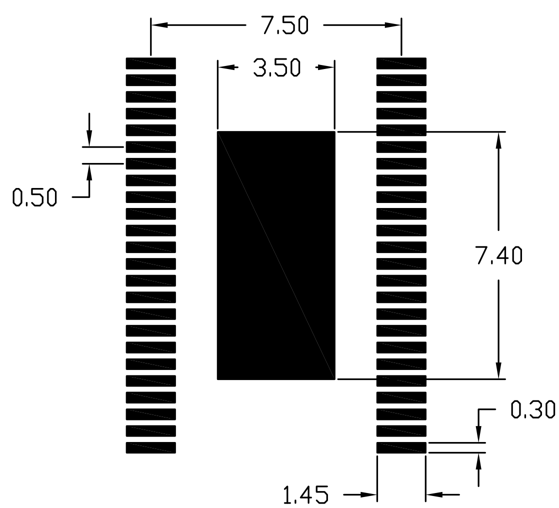
Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TSSOP	U48EM+3	21-0767	90-100004



NOTES:
1. REFERENCE PKG. OUTLINE: 21-0767
2. LAND PATTERN COMPLIES TO: IPC7351A.
3. TOLERANCE: +/- 0.02 MM.
4. ALL DIMENSIONS APPLY TO PbFREE (+) PKG. CODE ONLY.
5. ALL DIMENSIONS IN MM.

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TITLE: PACKAGE LAND PATTERN, [U48EM+3] TSSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	90-100004	A	1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/15	Initial release	—

