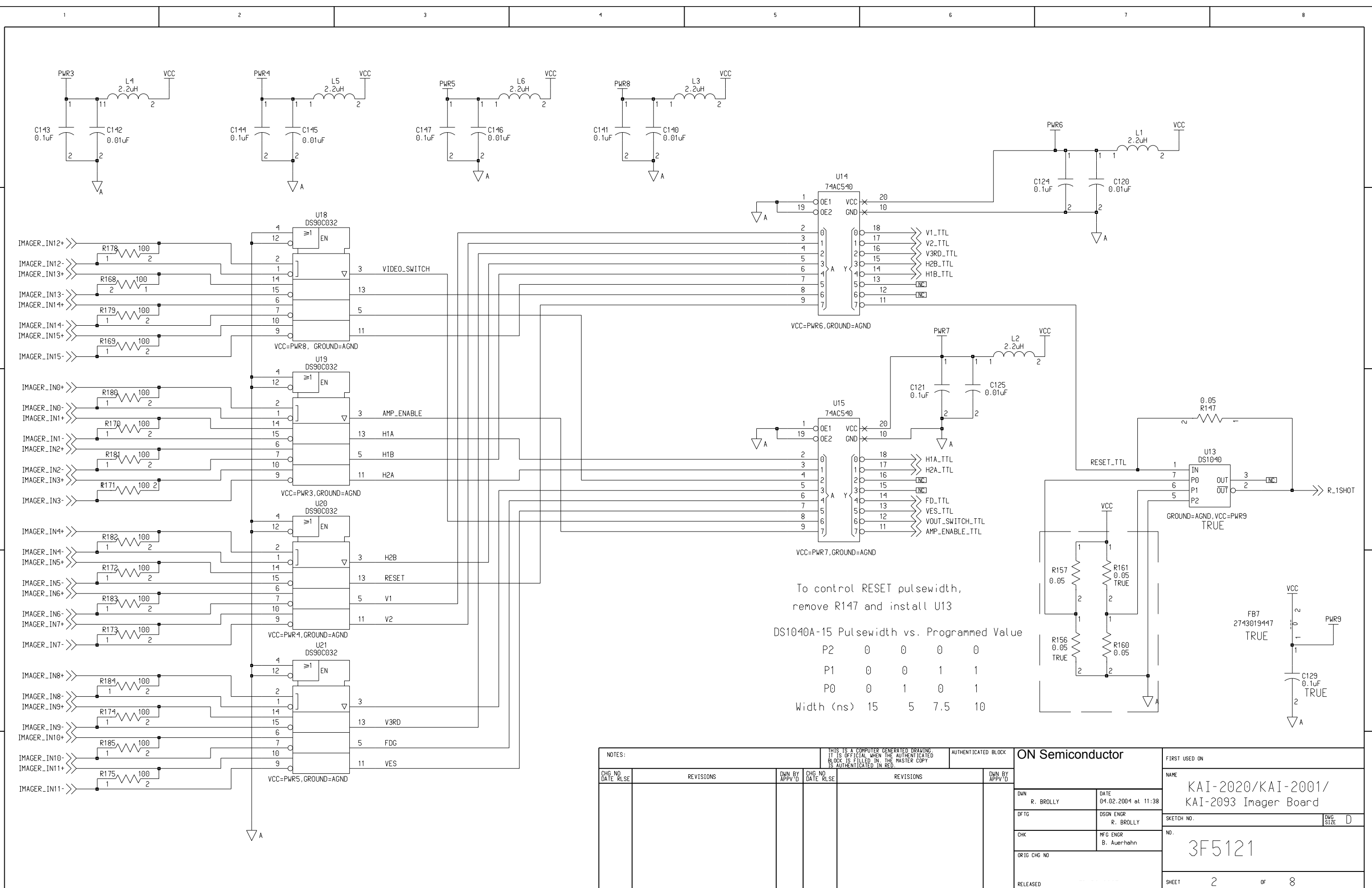


CHG NO		REVISIONS		DWN BY		CHG NO		REVISIONS		DWN BY		ON Semiconductor		FIRST USED ON	
DATE	RLSE			APPRV'D	DATE	RLSE			APPRV'D	DATE	RLSE	DATE	TIME	NAME	NO.
												10.14.2004	09:43	KAI-2020/KAI-2001/ KAI-2093 Imager Board	1
															3F5121
															1
															8

NOTES:		THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.		AUTHENTICATED BLOCK	
DWN R. BROLLY		DATE 10.14.2004 at 09:43		DFTG NONE	
DFTG NONE		DSGN ENGR R. BROLLY		CHK NONE	
CHK NONE		MFG ENGR B. Auerhahn		ORIG CHG NO BRDN	
MTD/PS-0687, Rev 4		PS-0122, Rev 1			

NAME		KAI-2020/KAI-2001/ KAI-2093 Imager Board	
SKETCH NO.		1	
NO.		3F5121	
SHEET		1 of 8	

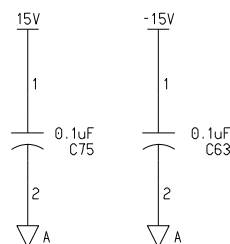
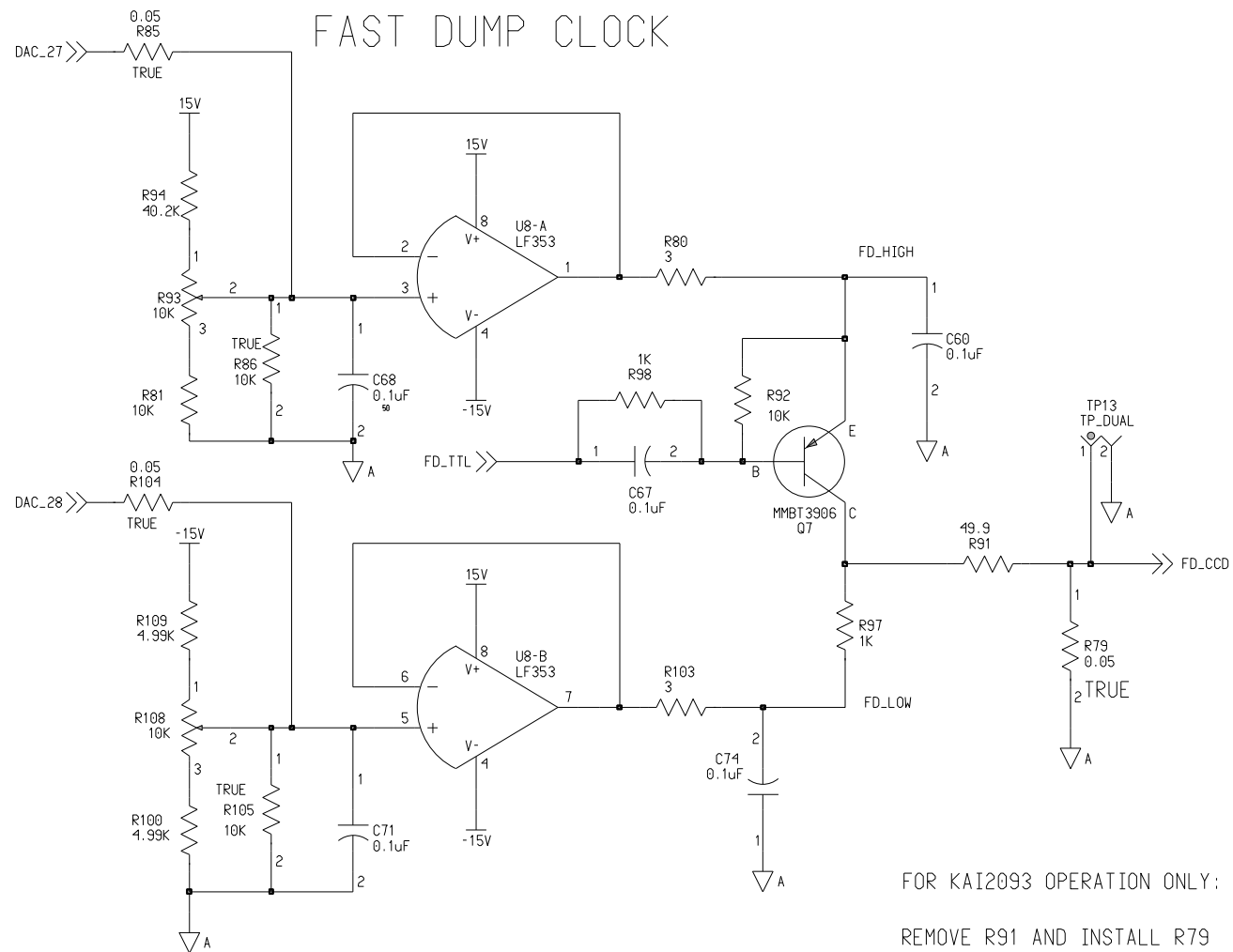


To control RESET pulsewidth,
remove R147 and install U13

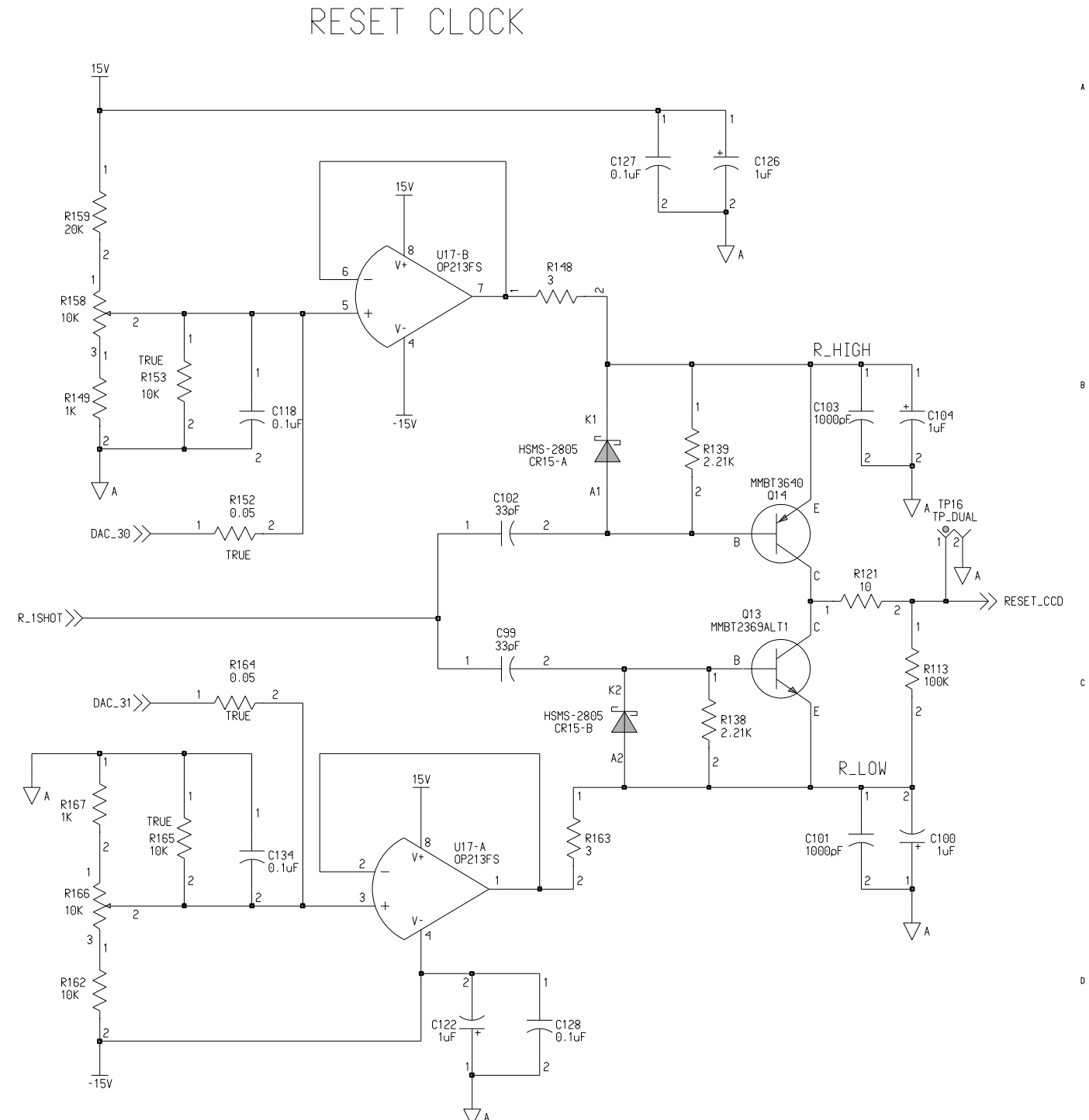
DS1040A-15 Pulsewidth vs. Programmed Value

P2	0	0	0	0
P1	0	0	1	1
P0	0	1	0	1
Width (ns)	15	5	7.5	10

NOTES:				THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.				AUTHENTICATED BLOCK		ON Semiconductor		FIRST USED ON	
CHG NO	DATE	REVISIONS	DWN BY	CHG NO	DATE	REVISIONS	DWN BY	R. BROLLY		DATE		NAME	
			APPR'D				APPR'D	R. BROLLY		04.02.2004 at 11:38		KAI-2020/KAI-2001/ KAI-2093 Imager Board	
								DFTG		DSGN ENGR		SKETCH NO.	
								CHK		MFG ENGR		NO.	
								ORIG CHG NO		B. Auerhahn		3F5121	
								RELEASED				SHEET 2 OF 8	

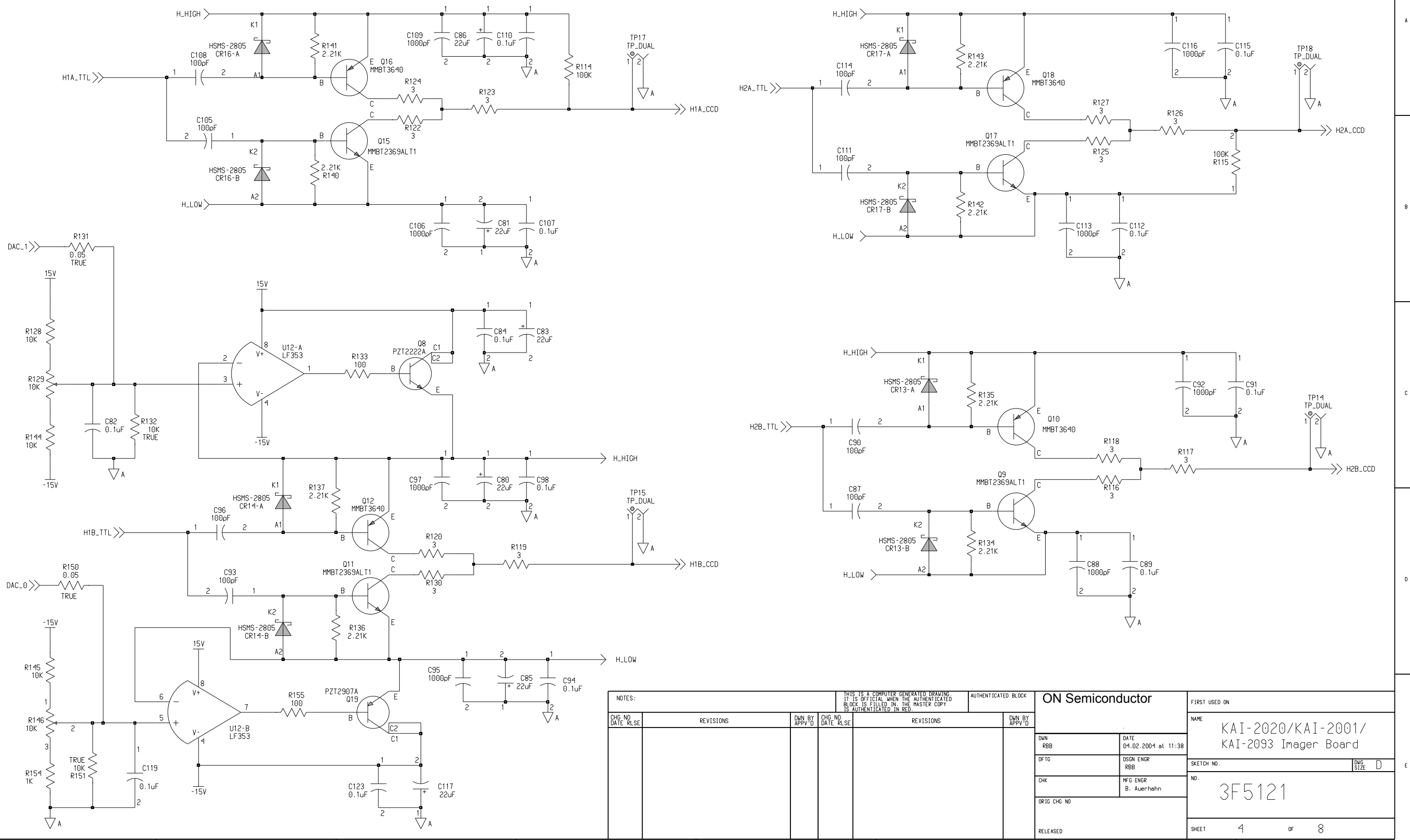


U8 Decoupling Caps

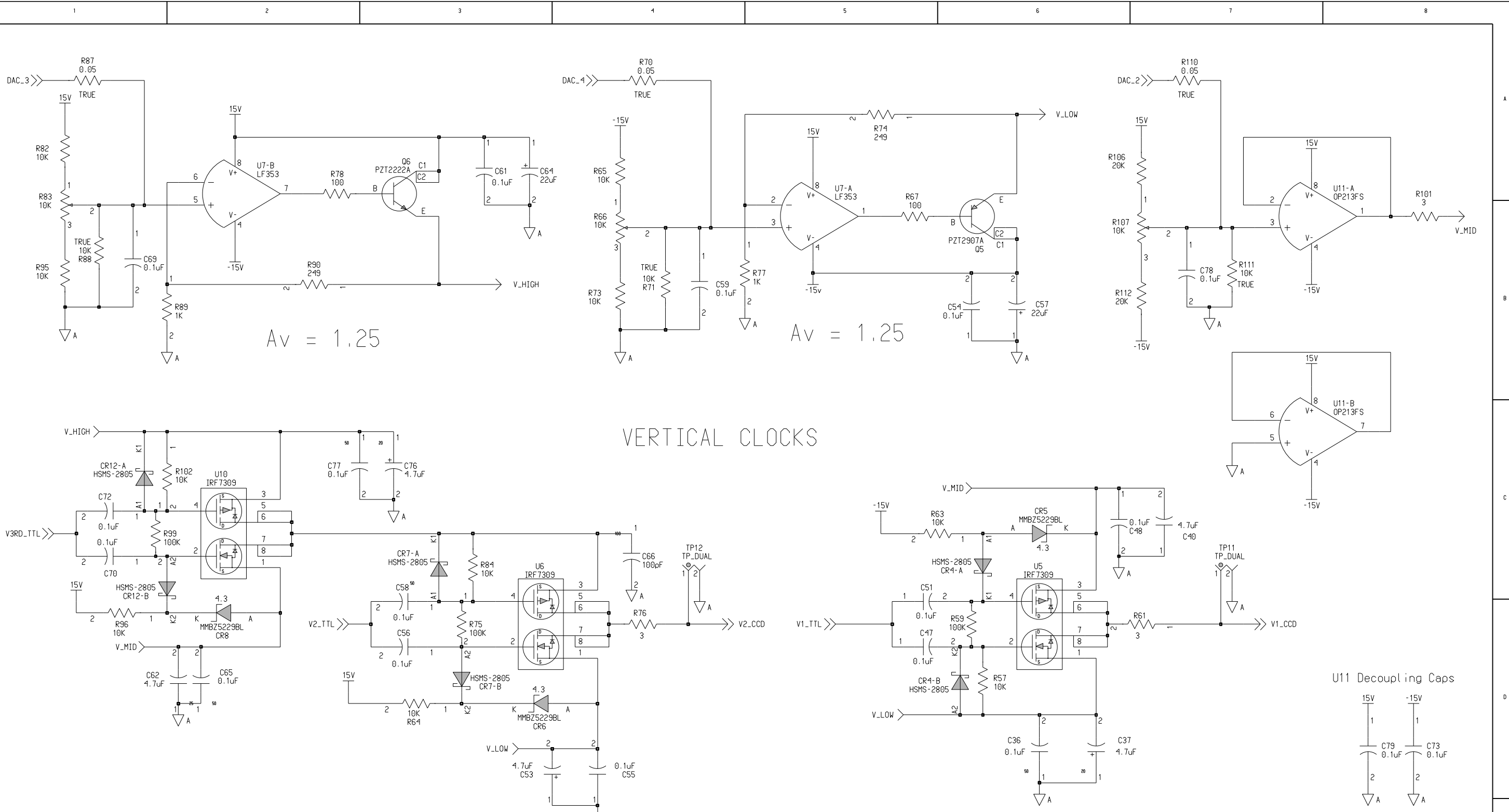


NOTES:				THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.				AUTHENTICATED BLOCK		ON Semiconductor		FIRST USED ON					
CHG NO	DATE	RELS	REVISIONS	DWN BY	DATE	RELS	CHG NO	DATE	RELS	REVISIONS	DWN BY	DATE	RELS				
DWN RBB												DATE: 04.02.2004 at 11:38					
DFTG												DSGN ENGR: RBB		SKETCH NO.		DWG SIZE: D	
CHK												MFG ENGR: B. Auerhahn		NO.		3F5121	
ORIG CHG NO																	
RELEASED														SHEET 3 OF 8			

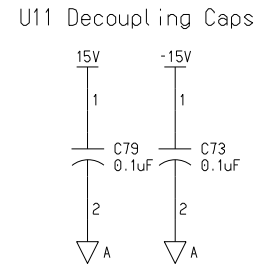
HORIZONTAL CLOCKS

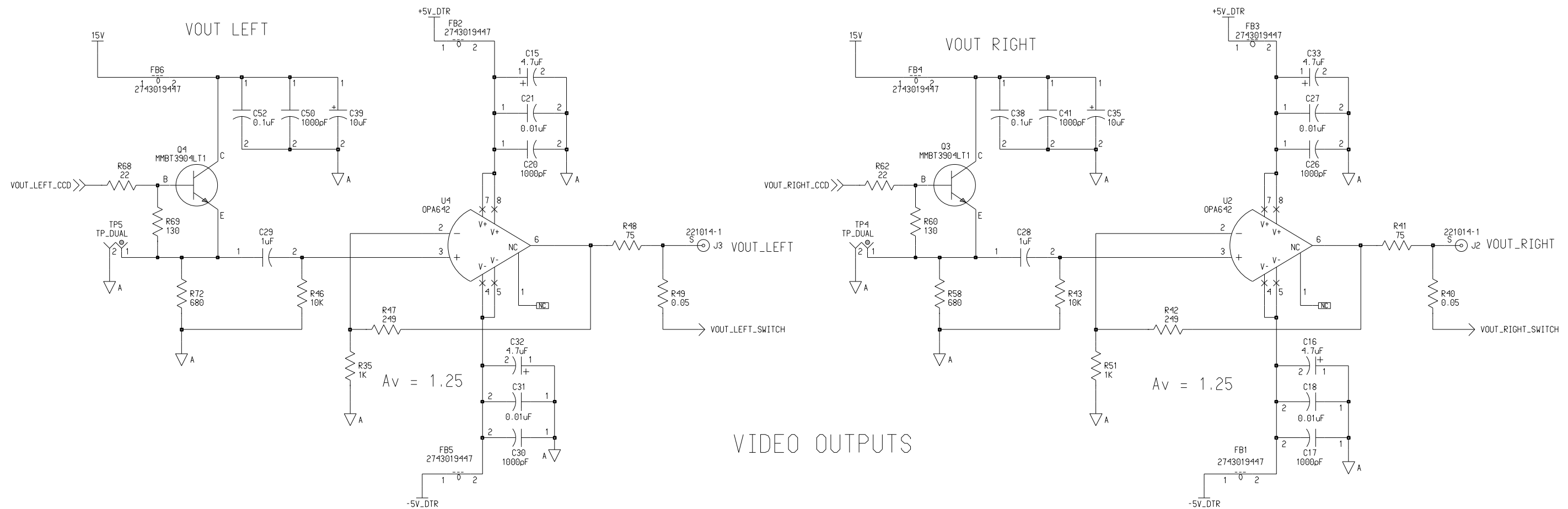


CHG NO		REVISIONS		DWN BY		CHG NO		REVISIONS		DWN BY		ON Semiconductor		FIRST USED ON	
DATE	RLSE			APPRV'D		DATE	RLSE			APPRV'D		DATE	NAME		
												04.02.2004	KAI-2020/KAI-2001/ KAI-2093 Imager Board		
													SKETCH NO. DWG SIZE D		
													NO. 3F5121		
													SHEET 4 OF 8		

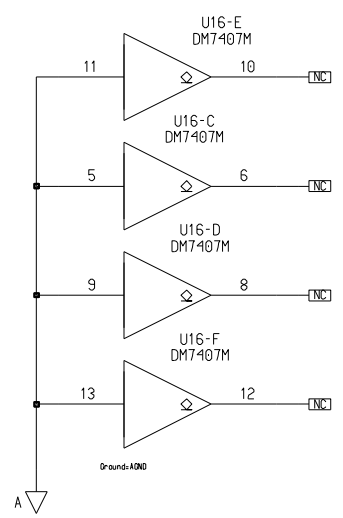
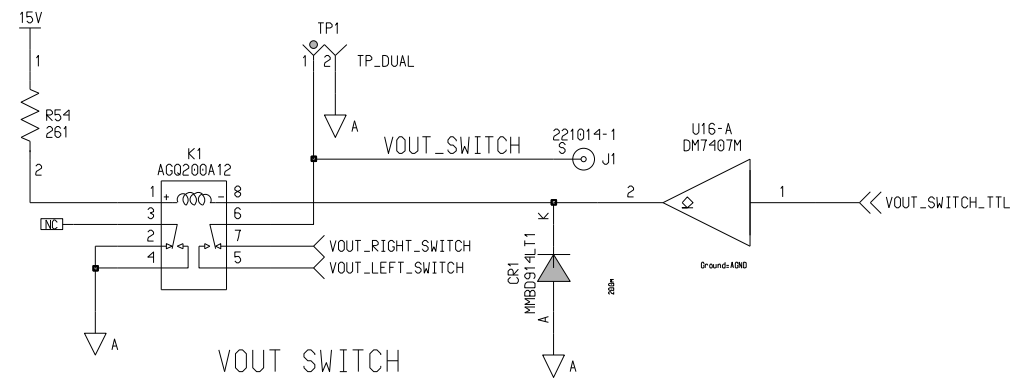


NOTES:				THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.				AUTHENTICATED BLOCK		ON Semiconductor		FIRST USED ON	
CHG NO	DATE	REVISIONS	DWN BY	CHG NO	DATE	REVISIONS	DWN BY			NAME		KAI-2020/KAI-2001/ KAI-2093 Imager Board	
										DATE		04.02.2004 at 11:38	
										DFTG		DSGN ENGR RBB	
										CHK		MFG ENGR B. Auerhahn	
										ORIG CHG NO		NO.	
										RELEASED		NO.	
										SHEET		5 OF 8	



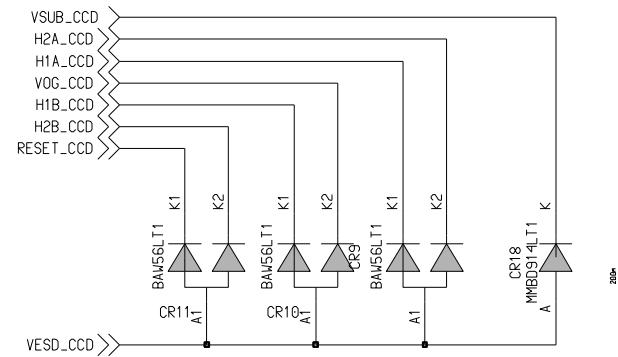


VIDEO OUTPUTS

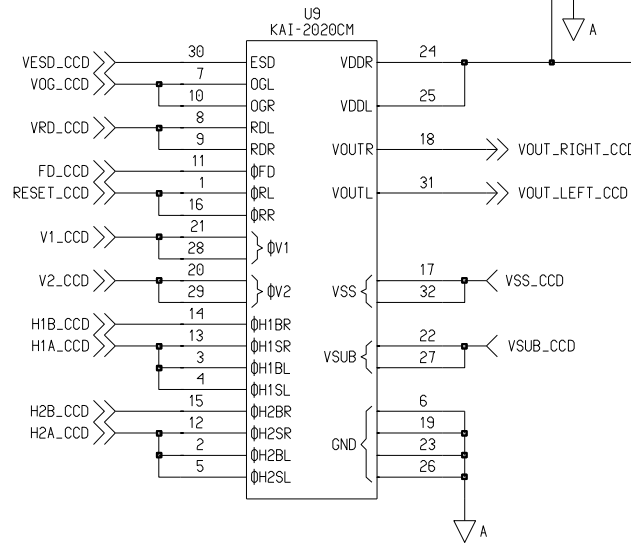


NOTES:				THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.				AUTHENTICATED BLOCK		ON Semiconductor		FIRST USED ON	
CHG NO	DATE	REVISIONS	DWN BY	CHG NO	DATE	REVISIONS	DWN BY	DATE		NAME		NO.	
								04.02.2004 at 11:39		KAI-2020/KAI-2001/ KAI-2093 Imager Board		D	
								DATE		SKETCH NO.		D	
								DATE		NO.		3F5121	
								DATE		SHEET		6 OF 8	

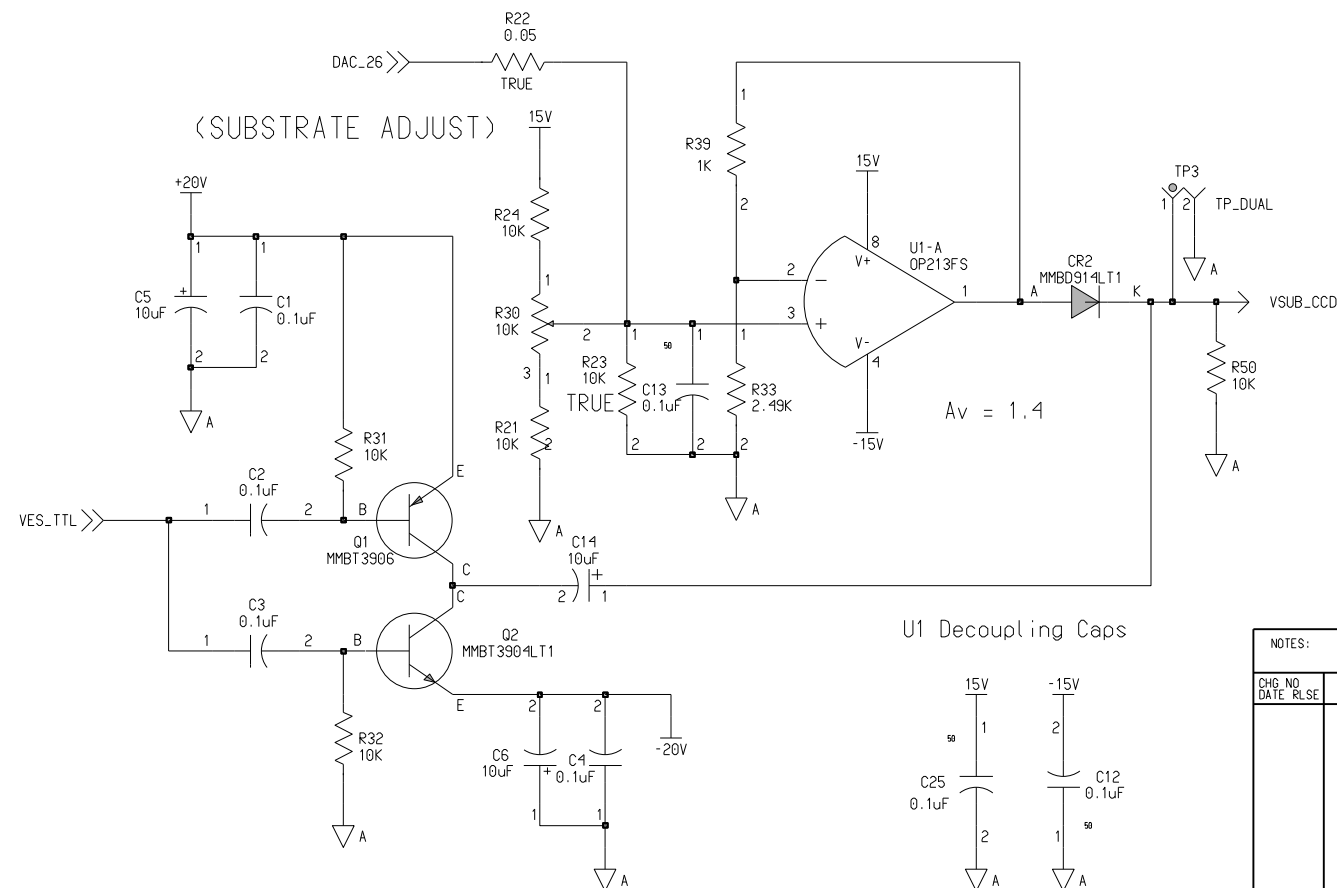
KAI-2001/KAI-2020 CCD IMAGER



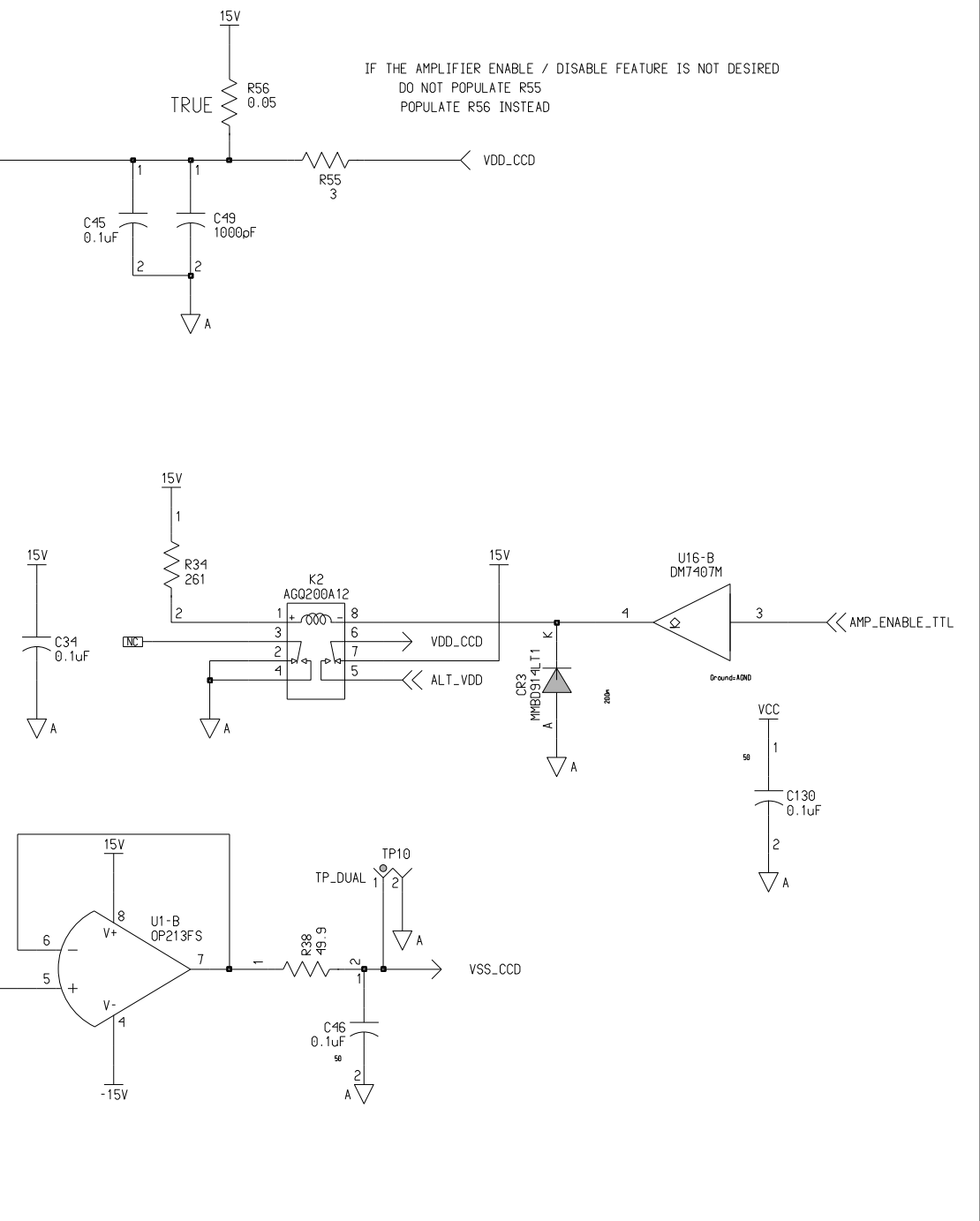
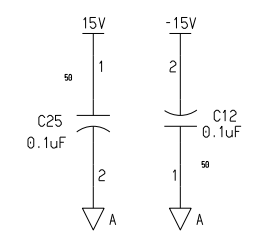
ESD PROTECTION CIRCUITRY



ELECTRONIC SHUTTER CIRCUIT



U1 Decoupling Caps

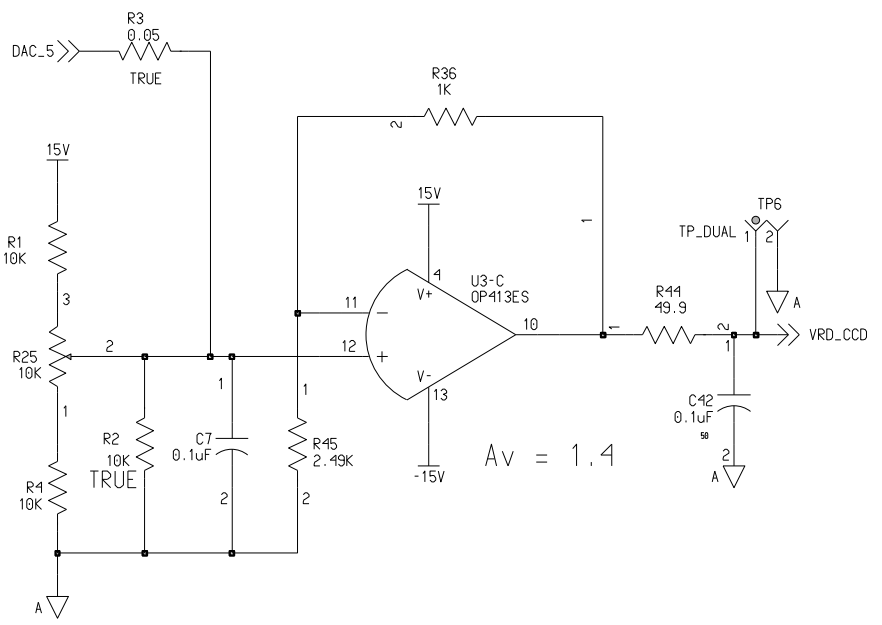
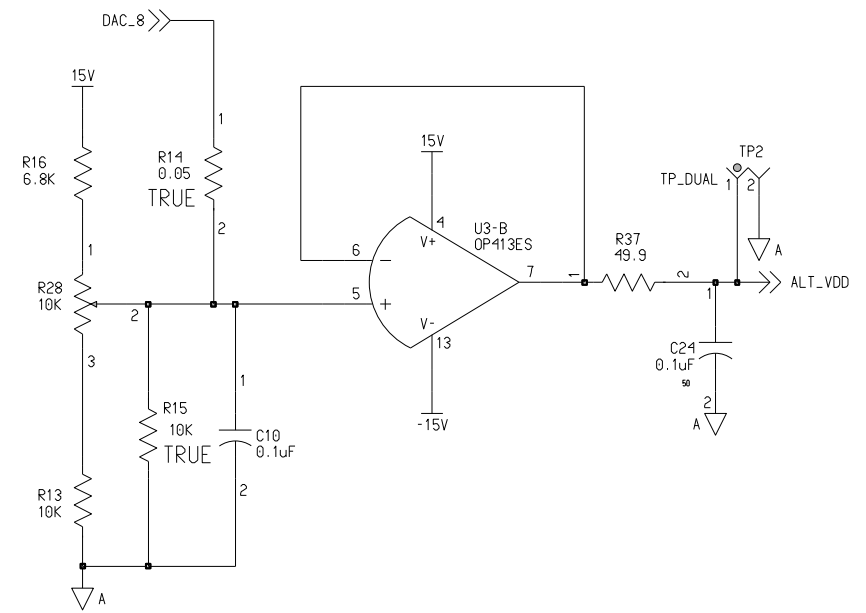
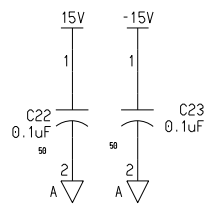
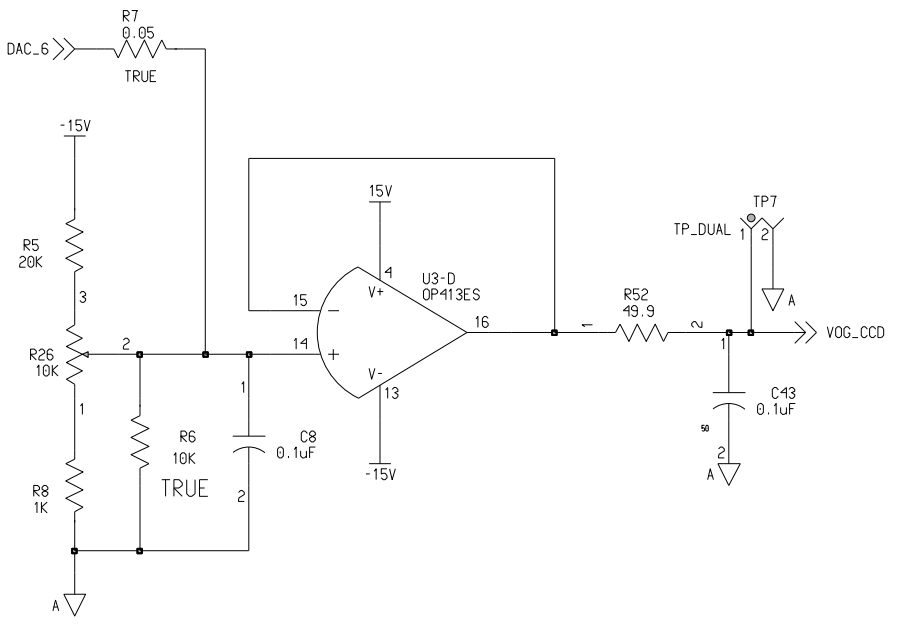
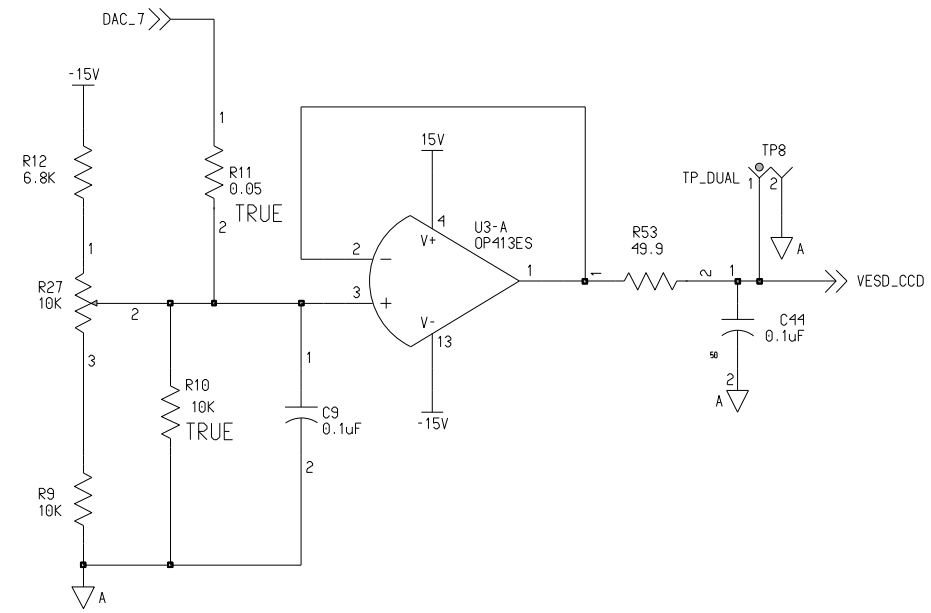


IF THE AMPLIFIER ENABLE / DISABLE FEATURE IS NOT DESIRED
DO NOT POPULATE R55
POPULATE R56 INSTEAD

NOTES:				THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.		AUTHENTICATED BLOCK		ON Semiconductor		FIRST USED ON	
CHG NO DATE	REVISIONS	DWN BY APPR'D	CHG NO DATE	REVISIONS	DWN BY APPR'D	DWN	DATE	NAME KAI-2020/KAI-2001/ KAI-2093 Imager Board			
						R. BROLLY	04.02.2004 at 11:39	SKETCH NO.			
						DFTG	R. BROLLY	NO. 3F5121			
						CHK	B. Auerhahn	DWG SIZE D			
						ORIG CHG NO		SHEET 7 OF 8			
						RELEASED					

DAC CONNECTOR

104549-9	P1-1	1	→	DAC_0
	P1-2	2	→	DAC_1
	P1-3	3	→	DAC_2
	P1-4	4	→	DAC_3
	P1-5	5	→	DAC_4
	P1-6	6	→	DAC_5
	P1-7	7	→	DAC_6
	P1-8	8	→	DAC_7
	P1-9	9	→	DAC_8
	P1-10	10	→	DAC_9
	P1-11	11	→	DAC_10
	P1-12	12	→	DAC_11
	P1-13	13	→	DAC_12
	P1-14	14	→	DAC_13
	P1-15	15	→	DAC_14
	P1-16	16	→	DAC_15
	P1-17	17	→	DAC_16
	P1-18	18	→	DAC_17
	P1-19	19	→	DAC_18
	P1-20	20	→	DAC_19
	P1-21	21	→	DAC_20
	P1-22	22	→	DAC_21
	P1-23	23	→	DAC_22
	P1-24	24	→	DAC_23
	P1-25	25	→	DAC_24
	P1-26	26	→	DAC_25
	P1-27	27	→	DAC_26
	P1-28	28	→	DAC_27
	P1-29	29	→	DAC_28
	P1-30	30	→	DAC_29
	P1-31	31	→	DAC_30
	P1-32	32	→	DAC_31
	P1-33	33	→	[NC]
	P1-34	34	→	[NC]
	P1-35	35	→	[NC]
	P1-36	36	→	[NC]
	P1-37	37	→	[NC]
	P1-38	38	→	[NC]
	P1-39	39	→	[NC]
	P1-40	40	→	[NC]
	P1-41	41	→	[NC]
	P1-42	42	→	[NC]
	P1-43	43	→	[NC]
	P1-44	44	→	[NC]
	P1-45	45	→	[NC]
	P1-46	46	→	[NC]
	P1-47	47	→	[NC]
	P1-48	48	→	[NC]
	P1-49	49	→	DAC_16
	P1-50	50	→	DAC_17
	P1-51	51	→	DAC_18
	P1-52	52	→	DAC_19
	P1-53	53	→	DAC_20
	P1-54	54	→	DAC_21
	P1-55	55	→	DAC_22
	P1-56	56	→	DAC_23
	P1-57	57	→	DAC_24
	P1-58	58	→	DAC_25
	P1-59	59	→	DAC_26
	P1-60	60	→	DAC_27
	P1-61	61	→	DAC_28
	P1-62	62	→	DAC_29
	P1-63	63	→	DAC_30
	P1-64	64	→	DAC_31
	P1-65	65	→	DAC_24
	P1-66	66	→	DAC_25
	P1-67	67	→	DAC_26
	P1-68	68	→	DAC_27
	P1-69	69	→	DAC_28
	P1-70	70	→	DAC_29
	P1-71	71	→	DAC_30
	P1-72	72	→	DAC_31
	P1-73	73	→	DAC_28
	P1-74	74	→	DAC_29
	P1-75	75	→	DAC_30
	P1-76	76	→	DAC_31
	P1-77	77	→	DAC_30
	P1-78	78	→	DAC_31
	P1-79	79	→	DAC_31
	P1-80	80	→	DAC_31



NOTES:				THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.				AUTHENTICATED BLOCK		ON Semiconductor		FIRST USED ON	
CHG NO	DATE	REVISIONS	DWN BY	CHG NO	DATE	REVISIONS	DWN BY	R. BROLLY		DATE		NAME	
								R. BROLLY		04.02.2004 at 11:39		KAI-2020/KAI-2001/ KAI-2093 Imager Board	
								DFTG		DSGN ENGR		SKETCH NO.	
								CHK		MFG ENGR		NO.	
								ORIG CHG NO		B. Auerhahn		3F5121	
								RELEASED				SHEET 8 OF 8	

Components
For Circuit Board Assembly

NO. 3F5121

SHEET 1

NEXT SHEET 2

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description	CHG. NO DATE	REVISIONS	DR. BY APPS.
1	3F5120	HW-T-1	BRD1	1		BARE BOARD REV 1			
2	785076	TOP-2 BOT-5	C126 C163 C100 C104 C122 C131 C162	7	case_a_h.075	1uF_25V_.20 ELECTROLYTIC, TANTALUM	REV 1	INITIAL RELEASE	BPF
3	4B4495	TOP-6 BOT-1	C15 C16 C32 C33 C53 C76 C37	7	case_b_h.085	4.7uF_20V_.20 ELECTROLYTIC TANTALUM CHIP	REV 2	ECO D0748	BPF
4	254471	TOP-20 BOT-4	C17 C20 C26 C30 C41 C49 C50 C88 C92 C95 C97 C101 C103 C106 C109 C113 C116 C153 C155 C166 C133 C148 C151 C164	24	0805_h.055	1000pF_50V_.05 MONOLITHIC, CERAMIC CHIP	REV 3	ECO D0754	BPF
5	980646	TOP-6 BOT-4	C18 C21 C27 C31 C120 C125 C140 C142 C145 C146	10	0805_h.055	0.01uF_50V_.10 MONOLITHIC, CERAMIC CHIP	REV 4	ECO D0774	BPF
6	7B9716	TOP-51 BOT-30	C2 C3 C7 C8 C9 C10 C11 C12 C13 C25 C34 C38 C42 C43 C44 C45 C46 C47 C51 C52 C54 C55 C56 C58 C59 C60 C65 C67 C68 C69 C70 C71 C72 C73 C74 C77 C78 C79 C82 C118 C119 C121 C124 C127 C130 C134 C139 C149 C154 C157 C158 C1 C4 C19 C22 C23 C24 C36 C48 C61 C63 C75 C84 C89 C91 C94 C98 C107 C110 C112 C115 C123 C128 C132 C136 C141 C143 C144 C147 C152 C165	81	0805_h.055	0.1uF_50V_.10 Ceramic Monolithic Chip			
7	7B9655	TOP-2	C28 C29	2	1206_h.060	1uF_16V_.20 MONOLITHIC, CERAMIC			

Notes: 1. REFER TO CIRCUIT DIAGRAM 3F5121

SEE SHEET		FOR ADD'L REVISIONS	
ON Semiconductor		FIRST USED ON	
		NAME CIRCUIT BOARD ASSEMBLY	
DR. XXXX	DATE 1/18/05	KAI-2020 IMAGER BOARD	
DES. ENG. R. BROLLY	PKG. MATL.	SKETCH NO.	DWG. SIZE B
CK. BPF	MFG. ENG. R. BROLLY	3F5121	
ORIG. CHG. NO. RELEASED		SHEET 1	NEXT SHEET 2

Components
For Circuit Board Assembly

NO. 3F5121

SHEET 2

NEXT SHEET 3

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description	CHG. NO DATE	REVISIONS	DR. BY APPS.
8	258541	TOP-5 BOT-4	C35 C39 C156 C160 C161 C135 C138 C150 C167	9	case_c_h.110	CHIP 10uF_20V_.20 ELECTROLYTIC TANTALUM CHIP	REV 1	INITIAL RELEASE	BPF
9	770251	TOP-5	C5 C6 C14 C137 C159	5	case_d_h.130	10uF_35V_.10 ELECTROLYTIC, TANTALUM	REV 2	ECO D0748	BPF
10	7E7251	TOP-1 BOT-1	C62 C40	2	1210_h.100	4.7uF_25V_.10 SMT CERAMIC CHIP	REV 3	ECO D0754	BPF
11	2B1595	TOP-9	C66 C87 C90 C93 C96 C105 C108 C111 C114	9	0805_h.055	100pF_100V_.10 CAPACITOR-CERAMIC MONOLITHIC CHIP (PF)	REV 4	ECO D0774	BPF
12	8B0987	TOP-4 BOT-4	C80 C81 C85 C86 C57 C64 C83 C117	8	case_c_h.110	22uF_20V_.20 ELECTROLYTIC TANTALUM CHIP			
13	4B3897	TOP-2	C99 C102	2	0805_h.055	33pF_50V_.05 CAPACITOR-CERAMIC MONOLITHIC CHIP (PF)			
14	616293	TOP-3 BOT-1	CR1 CR2 CR18 CR3	4	sot23_akn_sp	MMBD914LT1 DIODE, SWITCHING, 100V, 200mA			
15	902510	TOP-5 BOT-3	CR13 CR14 CR15 CR16 CR17 CR4 CR7 CR12	8	sot143_kkaa_	HSMS-2805 DIODE, SCHOTTKY BARRIER, DUAL, 70V, 15mA			
16	717944	TOP-1 BOT-2	CR6 CR5 CR8	3	zener_sot23_	MMBZ5229BL DIODE, ZENER, 4.3V, 225mW			
17	237522	TOP-3	CR9 CR10 CR11	3	sot23_kak_sp	BAW56LT1 DIODE, SWITCHING, DUAL, COM ANODE, 70V, 100mA			
18	233152	TOP-8 BOT-8	FB4 FB6 FB10 FB11 FB13 FB15 FB16 FB17 FB1 FB2 FB3 FB5 FB8 FB9 FB12 FB14	16	fb_274301944	2743019447 - FERRITE, SMT BEADS			
19	911244	TOP-3	J1 J2 J3	3	j01ra_221014	221014-1 SMB, R/A RF COAXIAL JACK, 75 OHM			

SEE SHEET FOR ADD'L REVISIONS

Notes: 1. REFER TO CIRCUIT DIAGRAM 3F5121

ON Semiconductor		FIRST USED ON	
		NAME CIRCUIT BOARD ASSEMBLY	
DR. XXXX	DATE 1/18/05	KAI-2020 IMAGER BOARD	
DES. ENG. R. BROLLY	PKG. MATL.	SKETCH NO.	DWG. SIZE B
CK. DATE BPF	MFG. ENG. R. BROLLY	3F5121	
ORIG. CHG. NO. RELEASED		SHEET 2	NEXT SHEET 3

Components
For Circuit Board Assembly

NO. 3F5121

SHEET 3

NEXT SHEET 4

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description	CHG. NO DATE	REVISIONS	DR. BY APPS.
20	999979	TOP-1	J4	1	p80s_104549-	104549-9 SMT, AMPMODU, SHROUDED HEADER CONNECTOR	REV 1	INITIAL RELEASE	BPF
21	5F0204	TOP-1 BOT-1	K1 K2	2	k_agq200a12_	AGQ200A12 DPDT RELAY, DPDT, 12V	REV 2	ECO D0748	BPF
22	1E1112	TOP-2 BOT-4	L1 L2 L3 L4 L5 L6	6	ind_1008cs_h	2.2uH SMT WIREWOUND ENCAPSULATED	REV 3	ECO D0754	BPF
23	233838	TOP-2	Q1 Q7	2	sot23_bce_sp	MMBT3906 TRANSISTOR, PNP, 40V, GENERAL PURPOSE	REV 4	ECO D0774	BPF
24	236307	TOP-5	Q10 Q12 Q14 Q16 Q18	5	sot23_bce_sp	MMBT3640 TRANSISTOR, PNP, 12V, SWITCHING			
25	616292	TOP-3	Q2 Q3 Q4	3	sot23_bce_sp	MMBT3904LT1 TRANSISTOR, NPN, 40V, GENERAL PURPOSE			
26	960471	TOP-2	Q5 Q19	2	sot223_bce_s	PZT2907A TRANSISTOR, PNP, 60V, GENERAL PURPOSE			
27	960472	TOP-2	Q6 Q8	2	sot223_bce_s	PZT2222A TRANSISTOR, NPN, 40V, GENERAL PURPOSE			
28	4B4317	TOP-5	Q9 Q11 Q13 Q15 Q17	5	sot23_bce_sp	MMBT2369ALT1 TRANSISTOR, NPN, 15V, SWITCHING			
29	233981	TOP-22 BOT-5	R1 R4 R9 R13 R21 R24 R43 R46 R50 R57 R64 R65 R73 R81 R82 R84 R95 R102 R128 R144 R145 R162 R31 R32 R63 R92 R96	27	0805_h.025	10K 0hms .100W .01 FLAT, THICK METAL FILM CHIP			
30	992875	TOP-2	R100 R109	2	0805_h.030	4.99K 0hms .100W .001 SMT CHIP FLAT THIN METAL FILM			
31	954557	TOP-2	R12 R16	2	0805_h.030	6.8K 0hms .100W .05 SMT CHIP FLAT THICK METAL FILM			
32	232841	TOP-1	R121	1	0805_h.030	10 0hms .100W .05 FLAT, THICK METAL FILM, CHIP			

SEE SHEET FOR ADD'L REVISIONS

Notes: 1. REFER TO CIRCUIT DIAGRAM 3F5121

ON Semiconductor		FIRST USED ON	
		NAME CIRCUIT BOARD ASSEMBLY	
DR. XXXX	DATE 1/18/05	KAI-2020 IMAGER BOARD	
DES. ENG. R. BROLLY	PKG. MATL.	SKETCH NO.	DWG. SIZE B
CK. BPF	MFG. ENG. R. BROLLY	3F5121	
ORIG. CHG. NO. RELEASED		SHEET 3	NEXT SHEET 4

Components
For Circuit Board Assembly

NO. **3F5121**
SHEET 4 NEXT SHEET 5

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description	CHG. NO DATE	REVISIONS	DR. BY APPS.
33	901770	B0T-12	R134 R135 R136 R137 R138 R139 R140 R141 R142 R143 R177 R187	12	0805_h.030	2.21K 0hms .100W .01 FLAT, THICK METAL FILM, CHIP	REV 1	INITIAL RELEASE	BPF
34	783957	B0T-2	R176 R186	2	0805_h.030	200 0hms .100W .01 FLAT, THICK METAL FILM, CHTP	REV 2	ECO D0748	BPF
35	770026	TOP-15	R25 R26 R27 R28 R29 R30 R66 R83 R93 R107 R108 R129 R146 R158 R166	15	pot_3266w_h.	10K POT, MULTI-TURN	REV 3	ECO D0754	BPF
36	901801	TOP-6	R37 R38 R44 R52 R53 R91	6	0805_h.030	49.9 0hms .100W .01 SMT CHIP FLAT THICK METAL FILM	REV 4	ECO D0774	BPF
37	257516	B0T-5	R40 R49 R147 R157 R160	5	0805_h.030	0.05 0hms .100W_- ZERO OHM CHIP JUMPER			
38	954554	TOP-2	R41 R48	2	0805_h.030	75 0hms .100W .01 SMT CHIP FLAT THICK METAL FILM			
39	902504	B0T-4	R42 R47 R74 R90	4	0805_h.030	249 0hms .100W .01 SMT CHIP FLAT THICK METAL FILM			
40	902942	TOP-1 B0T-1	R45 R33	2	0805_h.030	2.49K 0hms .100W .01 SMT CHIP FLAT THICK METAL FILM			
41	253955	TOP-5	R5 R17 R106 R112 R159	5	0805_h.030	20K 0hms .100W .05 FLAT, THICK METAL FILM, CHTP			
42	7B8769	TOP-1 B0T-1	R54 R34	2	0805_h.030	261 0hms .100W .01 SMT CHIP FLAT THICK METAL FILM			
43	903960	TOP-20	R55 R61 R76 R80 R101 R103 R116 R117 R118 R119 R120 R122 R123 R124 R125 R126 R127 R130 R148 R163	20	0805_h.030	3 0hms .100W .05 FLAT, THICK METAL FILM, CHIP			
44	739757	TOP-2	R58 R72	2	1210_h.025	680 0hms .250W .05 FLAT, THICK METAL FILM, CHTP			

SEE SHEET		FOR ADD'L REVISIONS	
ON Semiconductor		FIRST USED ON	
		NAME CIRCUIT BOARD ASSEMBLY	
DR. XXXX	DATE 1/18/05	KAI-2020 IMAGER BOARD	
DES. ENG. R. BROLLY	PKG. MATL.	SKETCH NO.	DWG. SIZE B
CK. DATE BPF	MFG. ENG. R. BROLLY	3F5121	
ORIG. CHG. NO. RELEASED		SHEET 4	NEXT SHEET 5

Notes: 1. REFER TO CIRCUIT DIAGRAM 3F5121

BOARD

Components
For Circuit Board Assembly

NO. 3F5121
SHEET 5 NEXT SHEET 6

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description	CHG. NO DATE	REVISIONS	DR. BY APPS.
45	254478	TOP-6	R59 R75 R99 R113 R114 R115	6	0805_h.030	100K Ohms .100W .05 FLAT, THICK METAL FILM, CHIP	REV 1	INITIAL RELEASE	BPF
46	941226	TOP-2	R60 R69	2	0805_h.030	130 Ohms .100W .01 SMT CHIP FLAT THICK METAL FILM	REV 2	ECO D0748	BPF
47	255345	TOP-2	R62 R68	2	0805_h.030	22 Ohms .100W .05 FLAT, THICK METAL FILM, CHIP	REV 3	ECO D0754	BPF
48	980690	TOP-20	R67 R78 R133 R155 R168 R169 R170 R171 R172 R173 R174 R175 R178 R179 R180 R181 R182 R183 R184 R185	20	0805_h.030	100 Ohms .100W .005 SMT CHIP FLAT THIN METAL FILM	REV 4	ECO D0774	BPF
49	902564	TOP-8 BOT-5	R8 R20 R36 R97 R98 R149 R154 R167 R35 R39 R51 R77 R89	13	0805_h.025	1K Ohms .100W .01 FLAT, THICK METAL FILM CHIP			
50	2B4344	TOP-1	R94	1	0805_h.030	40.2K Ohms .100W .01 SMT CHIP FLAT THICK METAL FILM			
51	TPDUAL	TOP-18	TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18	18	tpdual_.1_p4	TP_DUAL DUAL TEST PADS (THRU HOLE)			
52	901614	TOP-4	TP19 TP20 TP21 TP23	4	tp_tp104_h.2	TP-104-01-02 PRESS MOUNT TERMINAL - RED			
53	901613	TOP-2	TP22 TP24	2	tp_tp104_h.2	TP-104-01-00 PRESS MOUNT TERMINAL - BLACK			
54	7B8486	TOP-3	U1 U11 U17	3	so08_.200_h.	OP213FS OPAMP, DUAL, BIPOLAR, SINGLE-SUPPLY, LOW-NOISE			
55	5E6841	TOP-2	U14 U15	2	so120_.375_h	74AC540 BUFFER/DRIVER, OCTAL, W/ 3-STATE OUTPUT, INVERTING			
56	263517	TOP-1	U16	1	so14_.210_h.	DM7407M BUFFER, HEX, W/ OPEN-COLLECTOR OUTPUT			

SEE SHEET		FOR ADD'L REVISIONS	
ON Semiconductor		FIRST USED ON	
		NAME CIRCUIT BOARD ASSEMBLY	
DR. XXXX	DATE 1/18/05	KAI-2020 IMAGER BOARD	
DES. ENG. R. BROLLY	PKG. MATL.	SKETCH NO.	DWG. SIZE B
CK. BPF	MFG. ENG. R. BROLLY	3F5121	
ORIG. CHG. NO. RELEASED		SHEET 5	NEXT SHEET 6

Notes: 1. REFER TO CIRCUIT DIAGRAM 3F5121

BOARD

Components
For Circuit Board Assembly

NO. 3F5121

SHEET 6

NEXT SHEET 7

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description	CHG. NO DATE	REVISIONS	DR. BY APPS.
57	691935	TOP-4	U18 U19 U20 U21	4	so16_.210_h.	DS90C032 DIFFERENTIAL LINE RECEIVER, QUAD	REV 1	INITIAL RELEASE	BPF
58	5C2040	TOP-2	U2 U4	2	so08_.210_h.	OPA642 OPAMP, SINGLE, BIPOLAR, WIDEBAND, LOW-DISTORTION	REV 2	ECO D0748	BPF
59	G10861	TOP-1	U3	1	so116_.375_h	OP413ES LOW NOISE & DRIFT, SINGLE SUPPLY OPAMP	REV 3	ECO D0754	BPF
60	5F1246	TOP-3	U5 U6 U10	3	so08_.200_h.	IRF7309 TRANSISTOR, DUAL N & P CHANNEL, 30V, MOSFET	REV 4	ECO D0774	BPF
61	734408	TOP-3	U7 U8 U12	3	so08_.210_h.	LF353 OPAMP, DUAL, BIPOLAR, JFET-INPUT			
62	241054	TOP-1	VR1	1	to220_aio_pd	LM337T 1.5A -40V -1.2 to -37V VOLTAGE REGULATOR, NEG ADJ, 1.5A,			
63	498310	TOP-1	VR2	1	to220_aoi_pd	LM317T 1.5A 4.2-40V 1.2-37V VOLTAGE REGULATOR, ADJ, 1.5A, 3-TE			
64	5E6702	HW-B-2	XU9 XU9	2	HDWR	SOCKET 714-93-116-31-018000 MILL-MAX For U9			
65	7B9716	BOT-1	C129	1NL	0805_h.055	NO LOAD 0.1uF_50V_.10 Ceramic Monolithic Chip			
66	233152	BOT-1	FB7	1NL	fb_274301944	NO LOAD 2743019447 - FERRITE, SMT BEADS			
67	999979	TOP-1	P1	1NL	p80s_104549-	NO LOAD 104549-9 SMT, AMPMODU, SHROUDED HEADER CONNECTOR			
68	233981	BOT-15	R2 R6 R10 R15 R18 R23 R71 R86 R88 R105 R111 R132 R151 R153 R165	15NL	0805_h.025	NO LOAD 10K 0hms_.100W_.01 FLAT, THICK METAL FILM CHIP			
69	257516	TOP-17 BOT-2	R3 R7 R11 R14 R19 R22 R56 R70 R79 R85 R87 R104 R110 R131 R150 R152 R164 R156 R161	19NL	0805_h.030	NO LOAD 0.05 0hms_.100W_- ZERO OHM CHIP JUMPER			

SEE SHEET FOR ADD'L REVISIONS

Notes: 1. REFER TO CIRCUIT DIAGRAM 3F5121

ON Semiconductor		FIRST USED ON	
		NAME CIRCUIT BOARD ASSEMBLY	
DR. XXXX	DATE 1/18/05	KAI-2020 IMAGER BOARD	
DES. ENG. R. BROLLY	PKG. MATL.	SKETCH NO.	DWG. SIZE B
CK. BPF	MFG. ENG. R. BROLLY	3F5121	
ORIG. CHG. NO. RELEASED		SHEET 6	NEXT SHEET 7

Components
For Circuit Board Assembly

NO. 3F5121

SHEET 7

NEXT SHEET 8

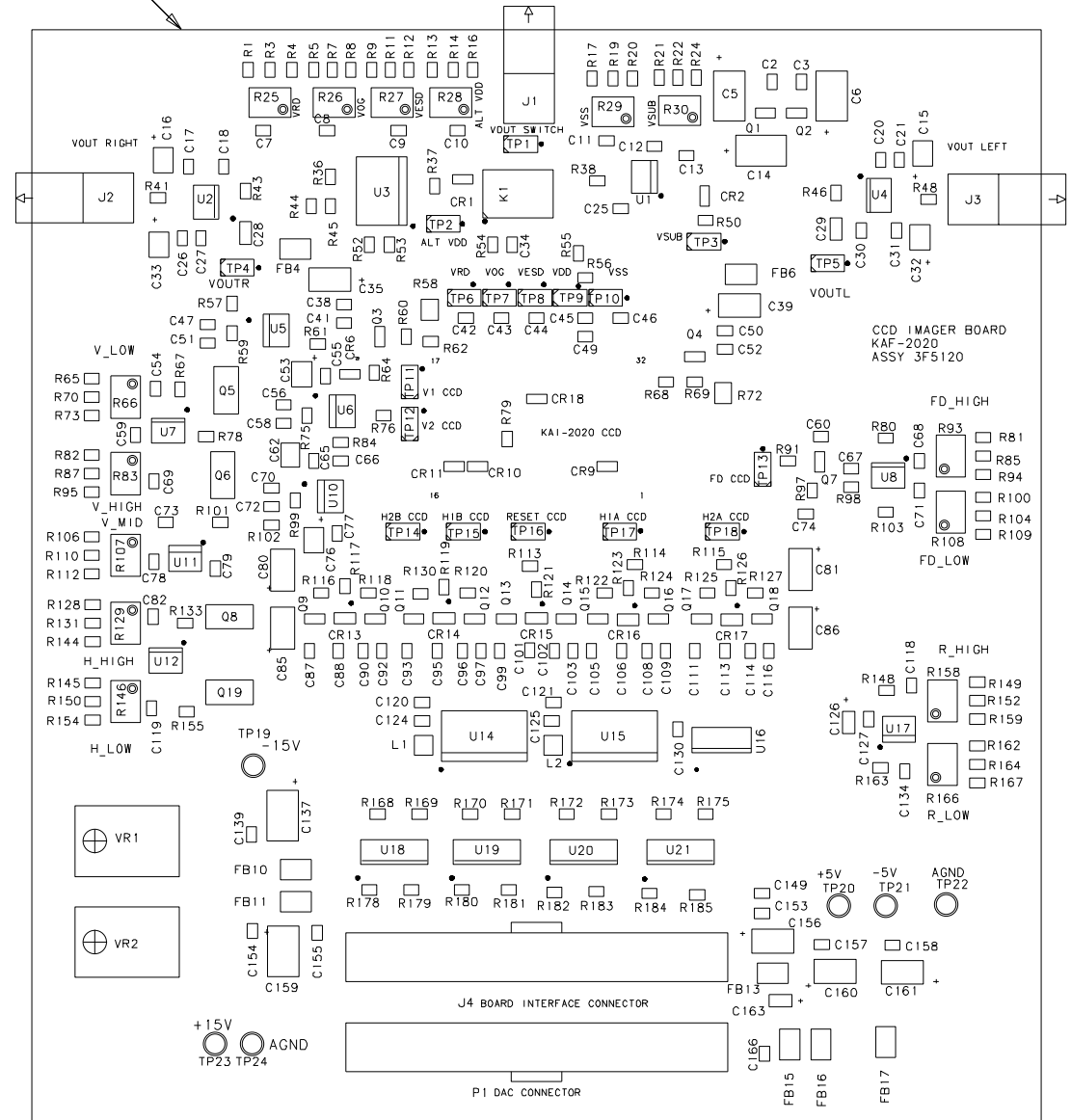
Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description	CHG. NO DATE	REVISIONS	DR. BY APPS.
70	5C2045	B0T-1	U13	1NL	so08_.210_h.	NO LOAD DS1040 PULSE GENERATOR, PROGRAMMABLE ONE-SHOT	REV 1	INITIAL RELEASE	BPF
71	4H0459	B0T-1	U9	1NL	socsensor_5E	NO LOAD KAI-2020CM CCD 1600x1200	REV 2	ECO D0748	BPF
							REV 3	ECO D0754	BPF
							REV 4	ECO D0774	BPF

SEE SHEET FOR ADD'L REVISIONS

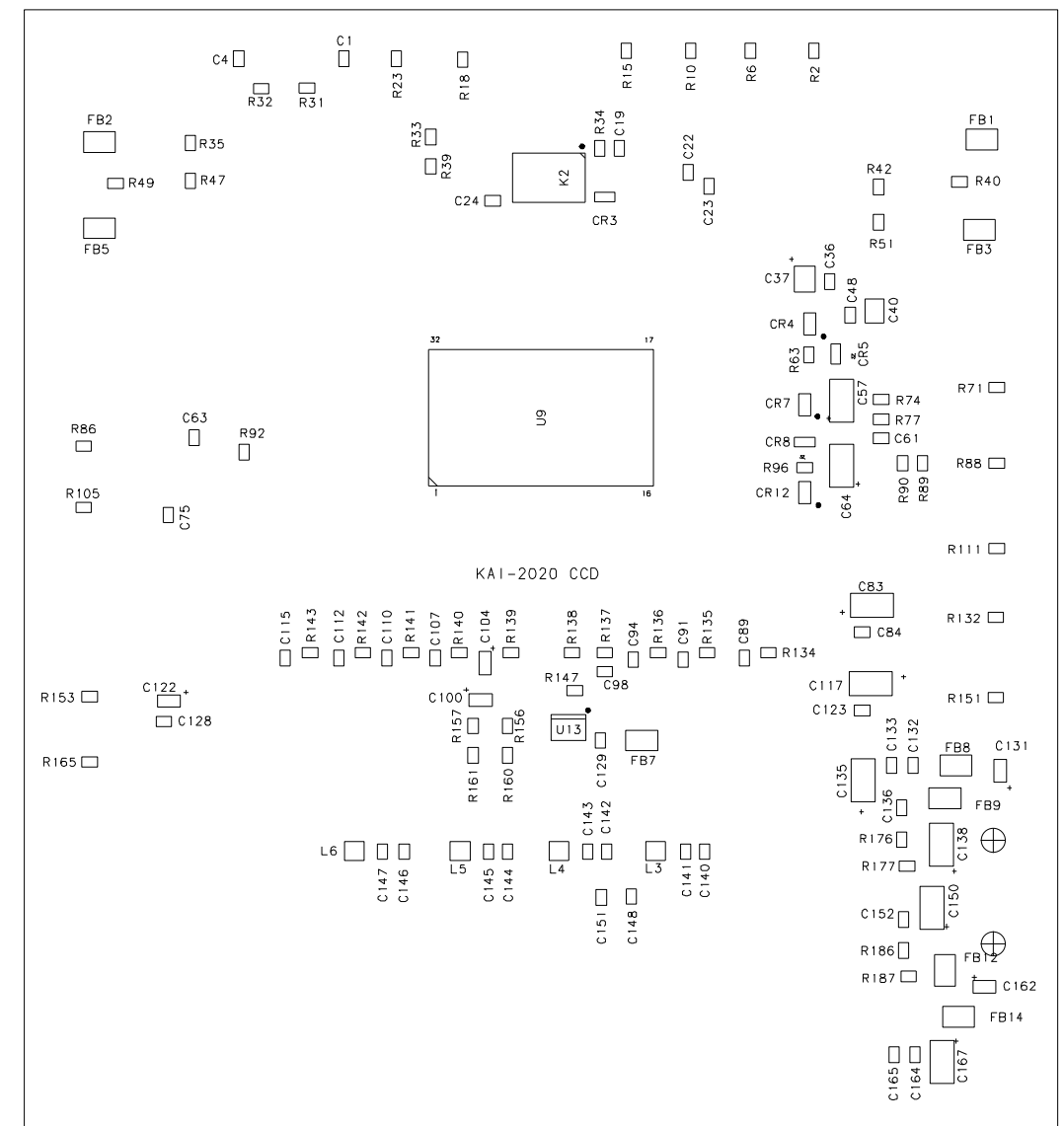
Notes: 1. REFER TO CIRCUIT DIAGRAM 3F5121

ON Semiconductor		FIRST USED ON	
		NAME CIRCUIT BOARD ASSEMBLY	
DR. XXXX	DATE 1/18/05	KAI-2020 IMAGER BOARD	
DES. ENG. R. BROLLY	PKG. MATL.	SKETCH NO.	DWG. SIZE B
CK. BPF	MFG. ENG. R. BROLLY	3F5121	
ORIG. CHG. NO. RELEASED		SHEET 7	NEXT SHEET 8

REVISION BLOCK				
ZONE	REV.	DESCRIPTION	ESC./DATE	APVD/OWN



PRIMARY SIDE



SECONDARY SIDE

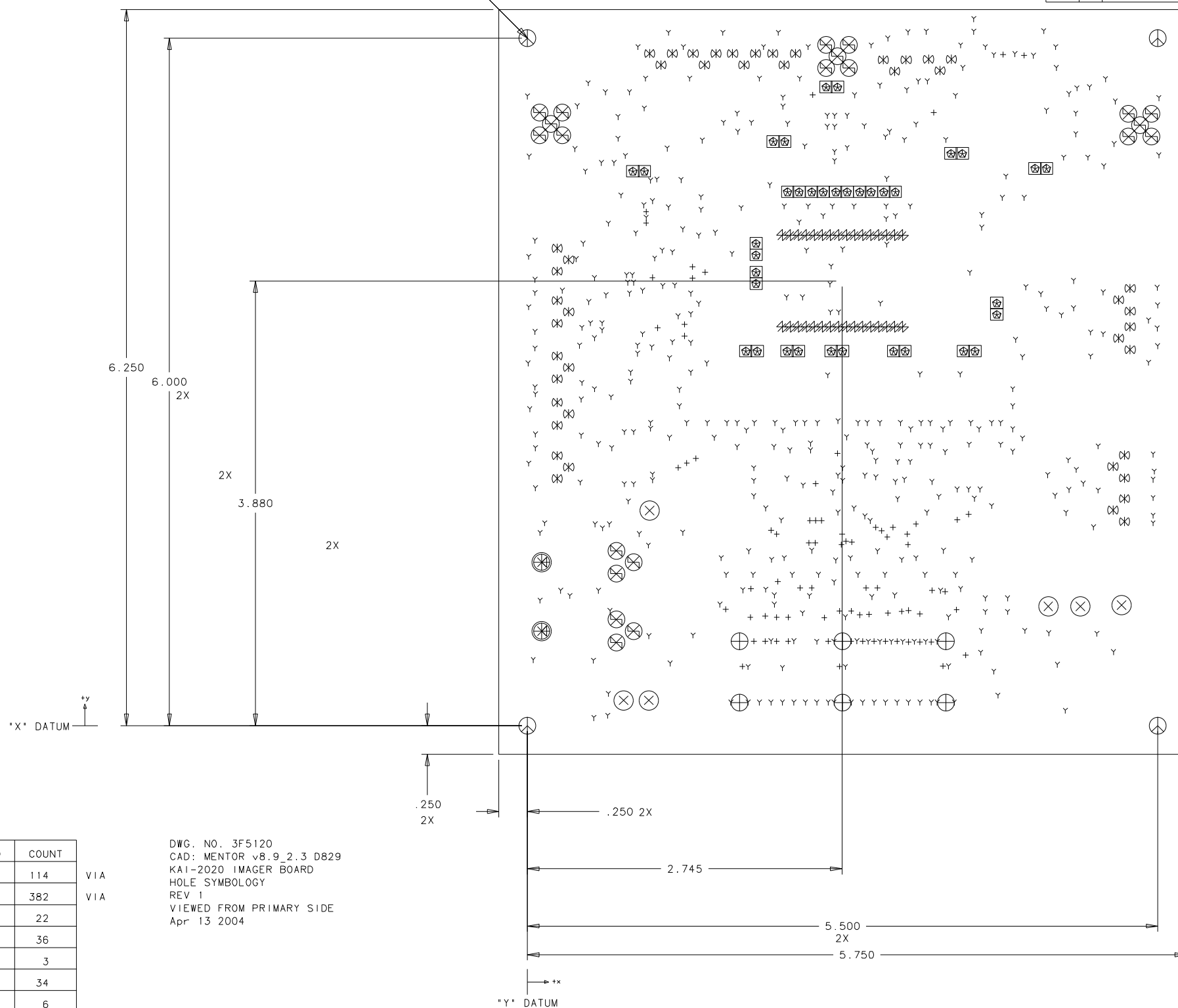
REF: DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.	MATERIAL:	DWN	ON Semiconductor
DIMENSIONS APPLY AFTER FINISH WHERE TOTAL TOLERANCE IS .001 INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.	UNLESS OTHERWISE SPECIFIED	DFTC	
DEVIATIONS FROM INTENDED SHAPE (FLATNESS, ROUNDNESS, SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES	DATUM PRECEDENCE PRI A SEC B TER C	ENGR	TITLE
	DIMENSIONS ARE IN INCHES	CHK	ASSY, KAI-2001/KAI-2020 IMAGER BOARD
	TOLERANCES	APVD	SIZE
	ANGLES ± 5°	APVD	ITEM NO
	1 PL ± N/A	APVD	3F5121
	2 PL ± .010	APVD	REV
	3 PL ± .005	CONTRACT #	4
			CODE
			WT
			SCALE 2X
			SH 8 OF 8

NOTES:

1. PERFORMANCE CLASS
 - 1.1 MANUFACTURE BOARD IN ACCORDANCE WITH IPC-6011 & 6012, CLASS 2.
2. MATERIAL SPECIFICATIONS:
 - 2.1 CORE MATERIAL: FR-4, SIZE AND CONSTRUCTION PER DETAIL A.
 - 2.2 PRE-PREG MATERIAL: FR-4 B STAGE, SIZE AND CONSTRUCTION PER DETAIL A.
 - 2.3 MODIFICATIONS TO THE LAYER STACKUP AS SHOWN IN DETAIL A ARE PERMISSIBLE WITH THE FOLLOWING CONSTRAINTS:
 - 2.3.1 CONDUCTIVE LAYERS SHALL BE EVENLY SPACED THROUGHOUT.
 - 2.3.2 OVERALL THICKNESS SHALL BE UNCHANGED.
3. COPPER PLATE:
 - 3.1 HOLES: COPPER PLATING ON WALL OF HOLES SHALL BE 0.0015 MIN. UNLESS OTHERWISE SPECIFIED
4. FINISH PLATE:
 - 4.1 SURFACE AND HOLES: EXPOSED LANDS AND LINES, EXCLUDING CONTACT FINGERS, SHALL BE TIN-LEAD COATED IN ACCORDANCE WITH THE SOLDERABILITY REQUIREMENTS OF J-STD-003.
5. CONDUCTOR WIDTH AND SPACING:
 - 5.1 WIDTH: 0.005 MIN
 - 5.2 SPACING: 0.005 MIN
 - 5.3 DESIGN FABRICATION PATTERN ALIGNMENT ALLOWANCE IS 0.015.
6. HOLE REQUIREMENTS:
 - 6.1 ANNULAR RING: 0.002 MIN
 - 6.2 HOLE LOCATIONS TO BE 0.003 (DTP - DIAMETRICAL TRUE POSITION)
 - 6.3 HOLE SIZES APPLY AFTER SOLDER PLATING, REFLOW OR DEPOSITION
7. SOLDERMASK:
 - 7.1 SOLDERMASKING OF PRIMARY AND SECONDARY SIDES OF THE BOARD SHALL BE PER MASKING ARTWORK OVER BARE COPPER (SMOBC) USING LIQUID PHOTOIMAGEABLE SOLDER MASK MATERIAL PER IPC-SM-840.
 - 7.2 RESIZING FOR MINIMAL LAND TO MASK CLEARANCE PERMISSIBLE.
8. MARKING:
 - 8.1 MARKING OF PRIMARY AND SECONDARY SIDES SHALL BE PER MARKING ARTWORK USING WHITE NON-CONDUCTIVE EPOXY INK.
9. BOARD WARPAGE:
 - 9.1 BOARD WARPAGE 0.75% MAX.
10. TESTING:
 - 10.1 BOARDS SHALL BE TESTED USING CAD SUPPLIED IPC-D-356 FORMAT NET LIST. ELECTRICAL TESTING SHALL FOLLOW GUIDELINES ESTABLISHED BY IPC-9252.
11. SIGNAL INTEGRITY / IMPEDANCE REQUIREMENTS
 - 11.1 NONE REQUIRED
12. MISCELLANEOUS NOTES:
 - 12.1 X,Y DATUMS INDICATE DRILL ORIGIN
 - 12.2 TEST COUPONS TO BE MADE AVAILABLE UPON REQUEST

4 MOUNTING HOLES
DIA = 0.125

REVISION BLOCK				
ZONE	REV.	DESCRIPTION	ESG/DATE	APVD/OWN



BOARD'S DRILL SCHEDULE

DRILL SIZE	DRILL SYMBOL	PLATED	COUNT
.013	+	YES	114
.015	γ	YES	382
.032	⊗	YES	22
.034	⊗	YES	36
.038	⊗	YES	3
.042	⊕	YES	34
.050	⊗	YES	6
.054	⊗	YES	21
.065	⊗	YES	6
.100	⊕	YES	4
.125	⊕	YES	4
.144	⊗	NO	2

TOTAL DRILL COUNT ON BOARD: 634

DWG. NO. 3F5120
CAD: MENTOR v8.9.2.3 D829
KAI-200 IMAGER BOARD
HOLE SYMBOLOLOGY
REV 1
VIEWED FROM PRIMARY SIDE
Apr 13 2004

REF: DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.	MATERIAL:	DWN B.FORD 08-15-03	ON Semiconductor
DIMENSIONS APPLY AFTER FINISH WHERE TOTAL TOLERANCE IS .001 INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.	UNLESS OTHERWISE SPECIFIED	DFTG B.NOEL 08-15-03	TITLE PCB, KAI-2001/KAI-2020 IMAGER
DEVIATIONS FROM INTENDED SHAPE (FLATNESS, ROUNDNESS, SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES	DATUM PRECEDENCE PRI A SEC B TER C	ENGR B.FORD 08-15-03	SIZE D
	DIMENSIONS ARE IN INCHES	ENGR X.XXXXXX XX-XX-XX	ITEM NO 3F5120
	TOLERANCES	CHK X.XXXXXX XX-XX-XX	REV 1
	ANGLES ± 5° 1 PL ± N/A	APVD X.XXXXXX XX-XX-XX	CODE
	2 PL ± .010 3 PL ± .005	APVD X.XXXXXX XX-XX-XX	WT
		CONTRACT #	SCALE 2X
			SH 1 OF 4