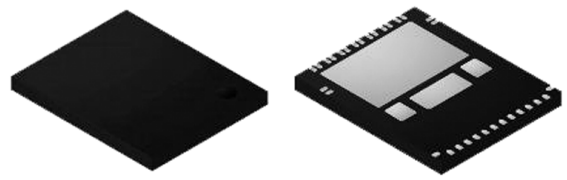
ISO8200BQ

Galvanic isolated octal high-side smart power solid state-relay

Datasheet - production data



TFQFPN32

Features

- V_{demag} = V_{CC} - 45 V (per channel)
- $R_{DS(on)}$ = 0.12 Ω (per channel)
- I_{OUT} = 0.7 A (per channel)
- V_{CC} = 45 V
- Parallel input interface
- Direct and synchronous control mode
- High common mode transient immunity
- Short-circuit protection
- Channel overtemperature protection
- Thermal independence of separate channels
- Common output disable pin
- Case overtemperature protection
- Loss of GND_{CC} and V_{CC} protection
- Undervoltage shutdown with auto-restart and hysteresis
- Overvoltage protection (V_{CC} clamping)
- Very low supply current
- Common fault open-drain output
- 5 V and 3.3 V TTL/CMOS compatible I/Os
- Fast demagnetization of inductive loads
- Reset function for IC output disable
- ESD protection
- Designed to meet IEC 61000-4-2, IEC 61000-4-4, IEC 61000-4-5 and IEC 61000-4-8
- UL1577 and UL508 certified
- Safety Limits as per VDE0884-11

Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- Drivers for all types of loads (resistive, capacitive, inductive)

Description

The ISO8200BQ is a galvanic isolated 8-channel driver featuring a very low supply current. It contains 2 independent galvanic isolated voltage domains (V_{CC} for the power stage and V_{DD} for the digital stage). Additional embedded functions are: loss of GND protection, undervoltage shutdown with hysteresis, and reset function for immediate power output shutdown.

IC is intended to drive any kind of load with one side connected to ground. Active channel current limitation combined with thermal shutdown, (independent for each channel), and automatic restart, protect the device against overload and short-circuit. In overload conditions, if junction temperature overtakes threshold, the channel involved is turned off and on again automatically after the IC temperature decreases below a reset threshold. If this condition causes case temperature to reach TCR limit threshold, the overloaded channel is turned off and it only restarts when case and junction temperature decrease down to the reset thresholds. Non-overloaded channels continue operating normally. An internal circuit provides an OR-wired non-latched common $\overline{FAULT}$ indicator signaling the channel OVT. The $\overline{FAULT}$ pin is an open-drain active low fault indication pin.

This is information on a product in full production. www.st.com

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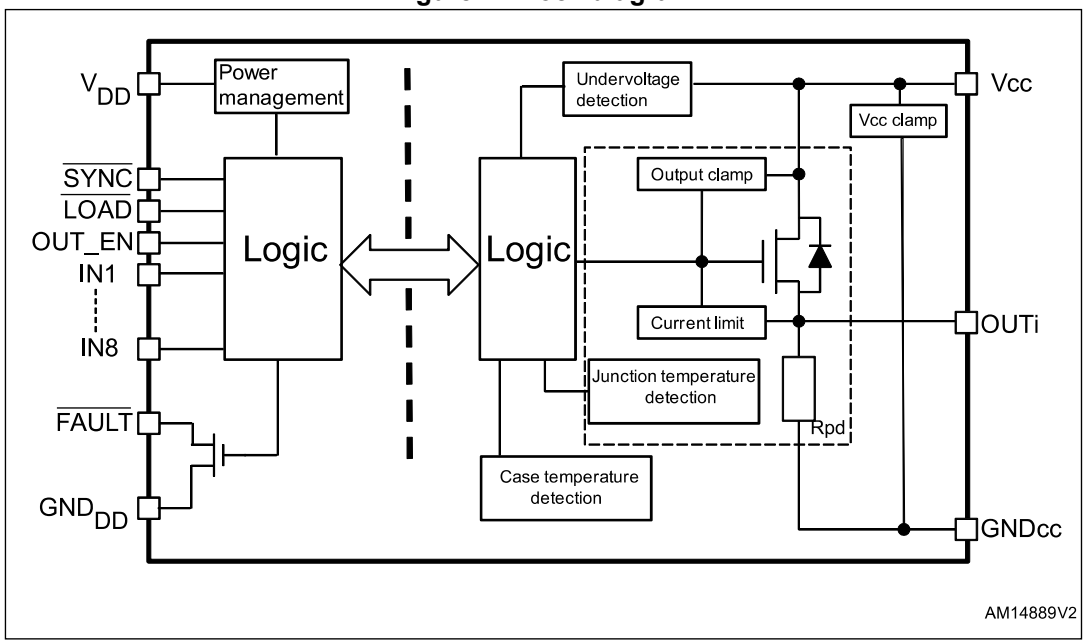
1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Pin connection (top through view)

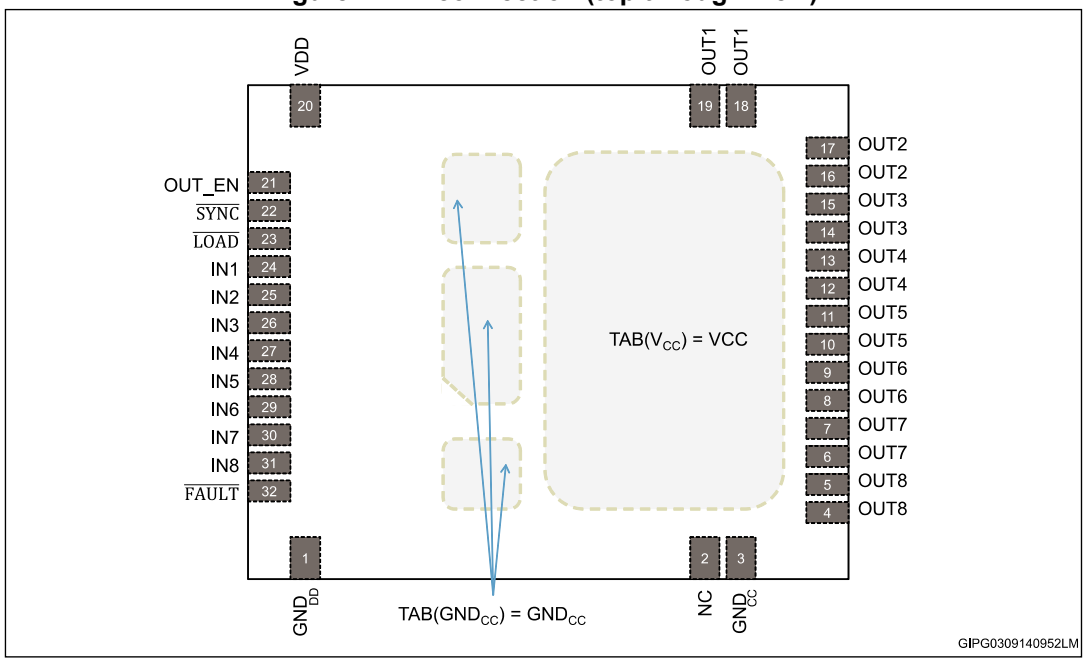


Table 1. Pin description

Pin	Name	Description
1	GND_{DD}	Input logic ground, negative logic supply
2	NC	Not connected
3	GND_{CC}	Output power ground
4	OUT8	Channel 8 power output
5	OUT8	
6	OUT7	Channel 7 power output
7	OUT7	
8	OUT6	Channel 6 power output
9	OUT6	
10	OUT5	Channel 5 power output
11	OUT5	
12	OUT4	Channel 4 power output
13	OUT4	
14	OUT3	Channel 3 power output
15	OUT3	
16	OUT2	Channel 2 power output
17	OUT2	

Table 1. Pin description (continued)

Pin	Name	Description
18	OUT1	Channel 1 power output
19	OUT1	
20	V_{DD}	Positive logic supply
21	OUT_EN	Output enable
22	$\overline{SYNC}$	Input-to-output synchronization signal. Active low, see *Section 6.3: Synchronous control mode (SCM) on page 21*.
23	$\overline{LOAD}$	Load input data signal. Active low, see *Section 6.3*
24	IN1	Channel 1 input
25	IN2	Channel 2 input
26	IN3	Channel 3 input
27	IN4	Channel 4 input
28	IN5	Channel 5 input
29	IN6	Channel 6 input
30	IN7	Channel 7 input
31	IN8	Channel 8 input
32	$\overline{FAULT}$	Common fault indication, active low
TAB(V_{CC})	V_{CC}	Exposed tab internally connected to V_{CC}, positive power supply voltage
TAB(GND_{CC})	GND_{CC}	Exposed tab internally connected to GND_{CC}

3 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Power supply voltage	-0.3	45	V
V_{DD}	Digital supply voltage	-0.3	6.5	V
V_{IN}	DC input pin voltage (INx, OUT_EN, $\overline{LOAD}$, $S\overline{YNC}$)	-0.3	+6.5	V
V_{FAULT}	Fault pin voltage	-0.3	+6.5	V
I_{GNDDD}	DC digital ground reverse current	-	-25	mA
I_{OUT}	Channel output current (continuous)	-	Internally limited	A
I_{GNDcc}	DC power ground reverse current	-	-250	mA
$-I_{OUT}$	Reverse output current (single channel)	-	-5	A
I_{IN}	DC input pin current (INx, OUT_EN, $\overline{LOAD}$, $S\overline{YNC}$)	-10	+ 10	mA
I_{FAULT}	Fault pin current	-10	+ 10	mA
V_{ESD}	Electrostatic discharge with human body model (R = 1.5 kΩ; C = 100 pF)	-	2000	V
E_{AS}	Single pulse avalanche energy per channel not simultaneously at $_{Tamb}$= 125 °C, I_{OUT} = 0.5 A	-	1.8	J
	Single pulse avalanche energy per channel, all channels driven simultaneously at $_{Tamb}$ = 125 °C, I_{OUT} = 0.5 A	-	0.35	
P_{TOT}	Power dissipation at Tc = 25 °C	-	Internally limited(1)	W
T_J	Junction operating temperature	-	Internally limited(1)	°C
T_{STG}	Storage temperature	-	-55 to 150	°C

1. Protection functions are intended to avoid IC damage in fault conditions and are not intended for continuous operation. Continuous or repetitive operations of protection functions may reduce the IC lifetime.

4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj\text{-}case}$	Thermal resistance, junction-case((1)	2	°C/W
$R_{thj\text{-}amb}$	Thermal resistance, junction-ambient(2)	15	°C/W

1. For each channel.
2. TFQFPN32 mounted on the product evaluation board (FR4, 4 layers, 8 cm^2 for each layer, copper thickness 35 mm).

5 Electrical characteristics

(10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C, unless otherwise specified)

Table 4. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC(THON)}$	V_{CC} undervoltage turn-ON threshold	-	-	9.5	10.5	V
$V_{CC(THOFF)}$	V_{CC} undervoltage turn-OFF threshold	-	8	9	-	V
$V_{CC(hys)}$	V_{CC} undervoltage hysteresis	-	0.25	0.5	-	V
$V_{CCclamp}$	Clamp on V_{CC} pin	I_{clamp} = 20 mA	45	50	52	V
$R_{DS(on)}$	On-state resistance(1)	I_{OUT} = 0.5 A, T_J = 25 °C I_{OUT} = 0.5 A T_J = 125 °C	-	0.12 0.24		Ω
R_{pd}	Output pull-down resistor		-	210	-	kΩ
I_{CC}	Power supply current	All channels in OFF-state All channels in ON-state	-	5 9	-	mA
I_{LGND}	Ground disconnection output current	V_{CC} = V_{GND} = 0 V V_{OUT} = -24 V	-	-	500	µA
$V_{OUT(OFF)}$	Off-state output voltage	Channel OFF and I_{OUT} = 0 A	-	-	1	V
$I_{OUT(OFF)}$	Off-state output current	Channel OFF and V_{OUT} = 0 V	-	-	5	µA

1. See *Figure 3: RDS(on) measurement*.

Table 5. Digital supply voltage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-	2.75	-	5.5	V
$V_{DD(THON)}$	V_{DD} undervoltage turn-ON threshold	-	2.55	-	2.75	V
$V_{DD(THOFF)}$	V_{DD} undervoltage turn-OFF threshold	-	2.45	-	2.65	V
$V_{DD(hys)}$	V_{DD} undervoltage hysteresis	-	0.04	0.1	-	V
I_{DD}	I_{DD} supply current	V_{DD} = 5 V and input channel with a steady logic level V_{DD} = 3.3 V and input channel with a steady logic level	- -	4.5 4.4	6 5.9	mA mA

Table 6. Diagnostic pin and output protection function

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{FAULT}	$\overline{FAULT}$ pin open-drain voltage output low	I_{FAULT} = 10 mA	-	-	0.4	V
I_{LFAULT}	$\overline{FAULT}$ output leakage current	V_{FAULT} = 5 V	-	-	1	µA
I_{PEAK}	Maximum DC output current before limitation	V_{CC} = 24 V R_{LOAD} = 0 Ω	-	1.6	-	A
I_{LIM}	Short-circuit current limitation	-	0.7	1.3	1.9	A
H_{yst}	ILIM tracking limits	-	-	0.3	-	A
T_{JSD}	Junction shutdown temperature	-	150	170	-	°C
T_{JR}	Junction reset temperature	-	-	150	-	°C
T_{HIST}	Junction thermal hysteresis	-	-	20	-	°C
T_{CSD}	Case shutdown temperature	-	115	130	145	°C
T_{CR}	Case reset temperature	-	-	110	-	°C
T_{CHYST}	Case thermal hysteresis	-	-	20	-	°C
V_{demag}	Output voltage at turn-OFF	I_{OUT} = 0.5 A I_{LOAD} > = 1 mH	V_{CC} -45	V_{CC} -50	V_{CC} -52	V

Table 7. Power switching characteristics (VCC = 24 V; -40 °C < TJ < 125 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
dV/dt(ON)	Turn-ON voltage slope	I_{OUT} = 0.5 A, resistive load 48 Ω	-	5.6	-	V/µs
dV/dt(OFF)	Turn-OFF voltage slope	I_{OUT} = 0.5 A, resistive load 48 Ω	-	2.81	-	V/µs
t_d(ON)	Turn-ON delay time(1)	I_{OUT} = 0.5 A, resistive load 48 Ω	-	17	22	µs
t_d(OFF)	Turn-OFF delay time(1)	I_{OUT} = 0.5 A, resistive load 48 Ω	-	22	40	µs
t_f	Fall time(1)	I_{OUT} = 0.5 A, resistive load 48 Ω	-	5	-	µs
t_r	Rise time(1)	I_{OUT} = 0.5 A, resistive load 48 Ω	-	5	-	µs

1. See *Figure 3: RDS(on) measurement* , *Figure 4: dV/dT* and *Figure 6: td(ON) - td(OFF) direct control mode*.

Figure 3. $R_{DS(on)}$ measurement

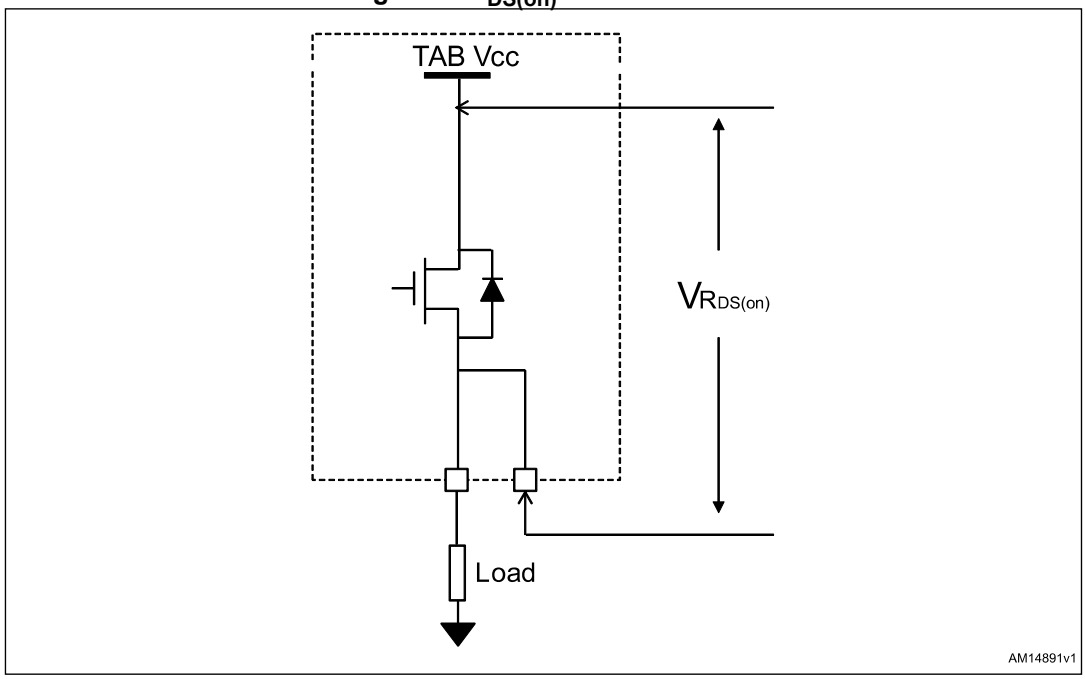


Figure 4. dV/dT

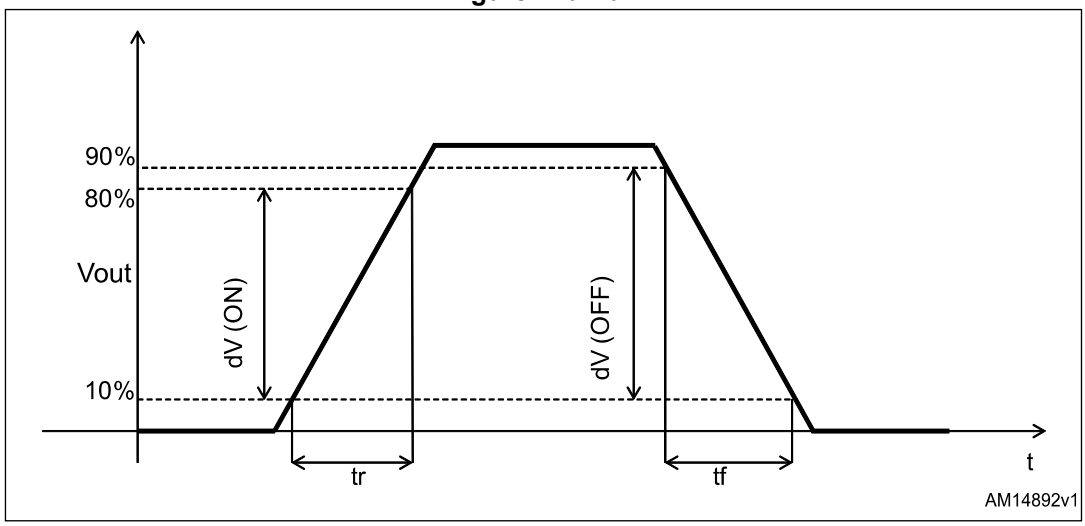


Figure 5. $t_{d(ON)}$ - $t_{d(OFF)}$ synchronous mode

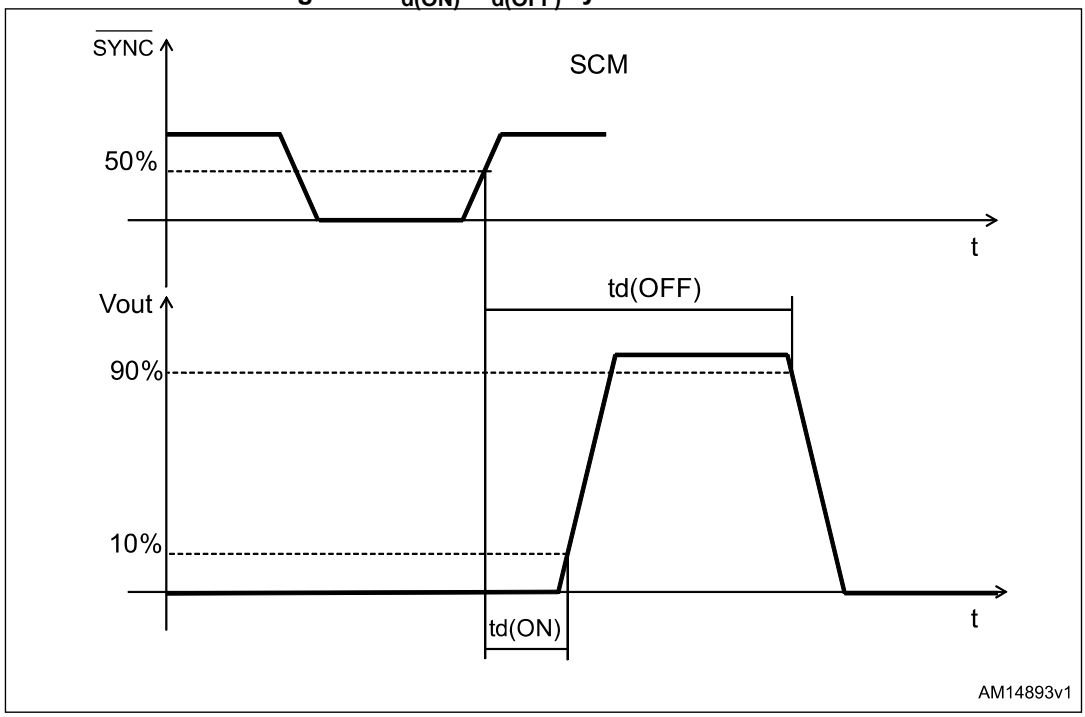


Figure 6. $t_{d(ON)}$ - $t_{d(OFF)}$ direct control mode

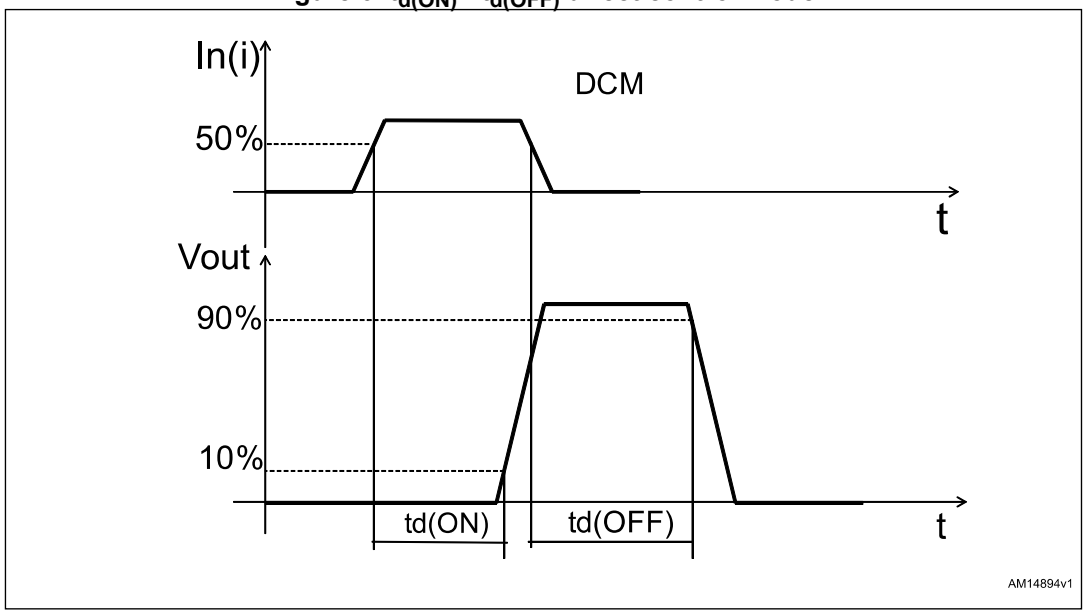


Table 8. Logic input and output

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Logic input pin low level voltage (INx, OUT_EN, $\overline{LOAD}$, $\overline{SYNC}$)	-	-0.3		0.3 x V_{DD}	V
V_{IH}	Logic input pin high level voltage (INx, OUT_EN, $\overline{LOAD}$, $\overline{SYNC}$)	-	0.7 x V_{DD}		V_{DD} + 0.3	V
$V_{I(HYST)}$	Logic input hysteresis voltage (INx, OUT_EN, $\overline{LOAD}$, $\overline{SYNC}$)	V_{DD} = 5 V	-	100	-	mV
I_{IN}	Logic input pin current (INx, OUT_EN, $\overline{LOAD}$, $\overline{SYNC}$)	V_{IN} = 5 V	10	-	-	µA
t_{WM}	Power side watchdog time	-	272	320	400	µs

Table 9. Parallel interface timings (VDD = 5 V; VCC = 24 V; -40 °C < TJ < 125 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{dis(SYNC)}$	$\overline{SYNC}$ disable time	Sync. control mode	10	-	-	µs
$t_{dis(DCM)}$	$\overline{SYNC}$, $\overline{LOAD}$ disable time	Direct control mode	80	-	-	ns
$t_{w(SYNC)}$	$\overline{SYNC}$ negative pulse width	Sync. control mode	20	-	195	µs
$t_{su(LOAD)}$	$\overline{LOAD}$ setup time	Sync. control mode	80	-	-	ns
$t_{h(LOAD)}$	$\overline{LOAD}$ hold time	Sync. control mode	400	-	-	ns
$t_{w(LOAD)}$	$\overline{LOAD}$ pulse width	Sync. control mode	240	-	-	ns
$t_{su(IN)}$	Input setup time	-	80	-	-	ns
$t_{h(IN)}$	Input hold time	-	10	-	-	ns
$t_{w(IN)}$	Input pulse width	Sync. control mode	160	-	-	ns
		Direct control mode	20	-	-	µs
t_{INLD}	IN to $\overline{LOAD}$ time	Direct control mode From IN variation to $\overline{LOAD}$ falling edge	80	-	-	ns
t_{LDIN}	$\overline{LOAD}$ to IN time	Direct control mode From $\overline{LOAD}$ falling edge to IN variation	400	-	-	ns
$t_{w(OUT_EN)}$	OUT_EN pulse width	-	150	-	-	ns
$t_{p(OUT_EN)}$	OUT_EN propagation delay	-	-	22	40	µs
$t_{jitter(SCM)}$	Jitter on single channel	Sync. mode	-	-	6	µs
$t_{jitter(DCM)}$		Direct mode	-	-	20	
$f_{refresh}$	Refresh delay	-	-	15	-	kHz

Table 10. Insulation and safety-related specifications

Symbol	Parameter	Test conditions	Value	Unit
CLR	Clearance (minimum external air gap)	Measured from input terminals to output terminals, the shortest distance through air	3.3	mm
CPG	Creepage (minimum external tracking)	Measured from input terminals to output terminals, the shortest distance path along body	3.3	mm
CTI	Comparative tracking index (tracking resistance)	DIN IEC 112/VDE 0303 part 1	≥ 600	V
	Isolation group	Material group (DIN VDE 0110, 1/89, Table 1)	I	-

Table 11. Insulation characteristics

Symbol	Parameter	Test conditions	Value	Unit
IEC 60747-5-5				
V_{IORM}	Maximum working isolation	-	937	V_{PEAK}
V_{PR}	Input to output test voltage	Method a, type test, $V_{PR} = V_{IORM}$ x 1.6, tm = 10s partial discharge < 5 pC	1500	V_{PEAK}
		Method b, 100% production test, $V_{PR} = V_{IORM}$ x 1.875, tm = 1s partial discharge < 5 pC	1758	V_{PEAK}
V_{IOTM}	Transient overvoltage	Type test t_{ini} = 60 s	4245	V_{PEAK}
V_{IOSM}	Maximum surge insulation voltage	Type test	4245	V_{PEAK}
R_{IO}	Insulation resistance	V_{IO} = 500 V at t_s	$>10^9$	Ω
UL1577				
V_{ISO}	Insulation withstand voltage	1 min. type test	2500/3536	V_{rms}/V_{PEAK}
$V_{ISO\ test}$	Insulation withstand test	1 s 100% production	3000/4245	V_{rms}/V_{PEAK}

Table 12. Safety limits

Parameter	Description	Test Condition	Limit value	Unit
Input safety, Logic side				
T_{si}	Safety temperature of Logic side	-	150	^{o}C
P_{si}	Safety power of Logic side	$V_{DD} \leq 6.5V$, $V_{LOGIC(x)} \leq 6.5V$, $I_{LOGIC(x)} \leq 10mA$, $T_J \leq Tsi$	0.9	W
Output safety, Process side				
T_{so}	Safety temperature of Process side	-	150	^{o}C
P_{so}	Safety power of Process side	$V_{CC} \leq 36V$, $I_{OUT(x)} \leq 1.5A$, $T_J \leq Tso$	4.5	W

Note: The above limits are measured according to VDE 0884-11. Respecting above limits prevents potential damage potential damage to the isolation barrier upon failure on logic or process side circuitry. User can use these values to protect the IC and consequently guarantee the safety of the embedded isolation barrier.

LOGIC(X) stands for "any pin of logic side".

OUT(X) stands for "any of the 8 output pins of process side".

6 Functional description

6.1 Parallel interface

Smart parallel interface built-in ISO8200BQ offers three interfacing signals easily managed by a microcontroller.

The $\overline{\text{LOAD}}$ signal enables the input buffer storing the value of the channel inputs.

The $\overline{\text{SYNC}}$ signal copies the input buffer value into the transmission buffer and manages the synchronization between low voltage side and the channel outputs on the isolated side. The OUT_EN signal enables the channel outputs.

An internal refresh signal updates the configuration of the channel outputs with a $f_{refresh}$ frequency. This signal can be disabled forcing low the $\overline{\text{SYNC}}$ input when $\overline{\text{LOAD}}$ is high.

$\overline{\text{SYNC}}$ and $\overline{\text{LOAD}}$ pins can be in direct control mode (DCM) or synchronous control mode (SCM).

The operation of these two signals is described as follows:

Table 13. Interface signal operation (general)

$\overline{\text{LOAD}}$	$\overline{\text{SYNC}}$	OUT_EN	Device behavior
Don't care	Don't care	Low(1)	The outputs are disabled (turned off)
High	High	High	The outputs are left unchanged
Low	High	High	The input buffer is enabled The outputs are left unchanged
High	Low	High	The internal refresh signal is disabled The transmission buffer is updated The outputs are left unchanged
Low	Low	High	The device operates in direct control mode as described in *Section 6.2: Direct control mode (DCM)*

1. The outputs are turned off on OUT_EN falling edge and they are kept disabled as long as it is low.

6.1.1 Input signals (IN1 to IN8)

Inputs from IN1 to IN8 are the driving signals of the corresponding OUT1 to OUT8 outputs. Data are direct loaded on related outputs if $\overline{\text{SYNC}}$ and $\overline{\text{LOAD}}$ inputs are low (DCM operation) or stored into input buffer when $\overline{\text{LOAD}}$ is low and $\overline{\text{SYNC}}$ is high.

6.1.2 Load input data ($\overline{\text{LOAD}}$)

The input is active low; it stores the data from IN1 to IN8 into the input buffer.

6.1.3 Output synchronization ($\overline{\text{SYNC}}$)

The input is active low; it enables the ISO8200BQ transmission buffer loading input buffer data and manages the transmission between the two isolated sides of the device.

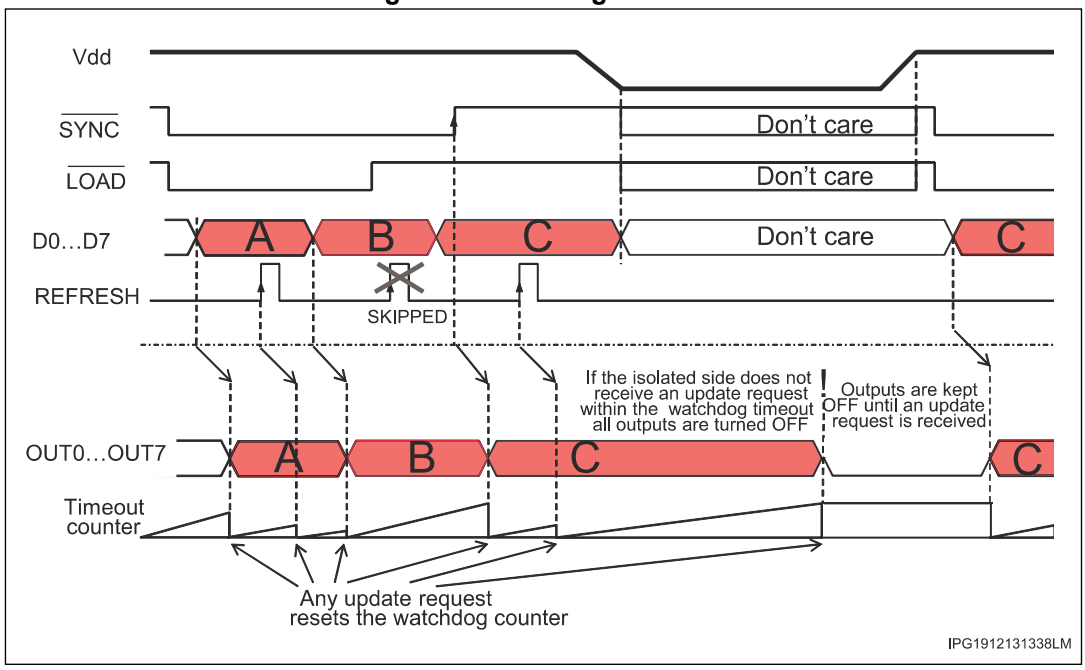
6.1.4 Watchdog

The isolated side of the device provides a watchdog function in order to guarantee a safe condition when V_{DD} supply voltage is missing.

If the logic side does not update the output status within t_{WD}, all outputs are disabled until a new update request is received.

The refresh signal is also considered a valid update signal, so the isolated side watchdog does not protect the system from a failure of the host controller (MCU freezing).

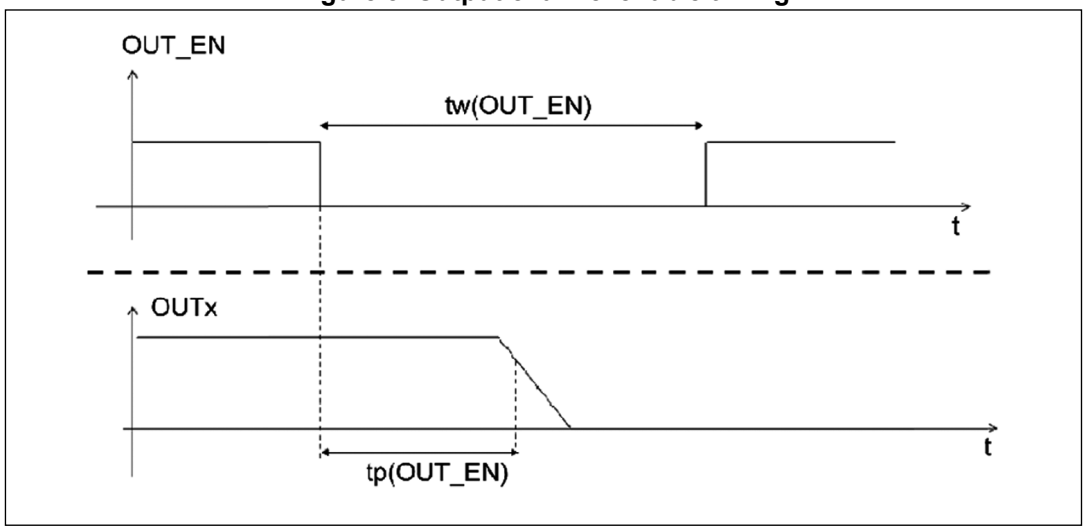
Figure 7. Watchdog behavior



6.1.5 Output enable (OUT_EN)

This pin provides a fast way to disable all outputs simultaneously. When the OUT_EN pin is driven low the outputs are disabled. To enable the output stage, the OUT_EN pin has to be raised. This timing execution is compatible with an external reset push, safety requirement, and allows, in a PLC system, the microcontroller polling to obtain all internal information during a reset procedure.

Figure 8. Output channel enable timing



6.2 Direct control mode (DCM)

When $\overline{\text{SYNC}}$ and $\overline{\text{LOAD}}$ inputs are driven by the same signal, the device operates in direct control mode (DCM).

In DCM the $\overline{\text{SYNC}}$ / $\overline{\text{LOAD}}$ signal operates as an active low input enable:

- When the signal is high, the current output configuration is kept regardless the input values
- When the signal is low, each channel input directly drives the respective output

This operation mode can also be set shorting both signals to the digital ground; in this case the channel outputs are always directly driven by the inputs except when OUT_EN is low (outputs disabled).

Table 14. Interface signal operation in direct control mode

$\overline{\text{SYNC}}$ / $\overline{\text{LOAD}}$	OUT_EN	Device behavior
Don't care	Low (1)	The outputs are disabled (turned off)
High	High	The outputs are left unchanged
Low	High	The channel inputs drive the outputs

1. The outputs are turned off on OUT_EN falling edge and they are kept disabled as long as it is low.

Figure 9. Direct control mode IC configuration

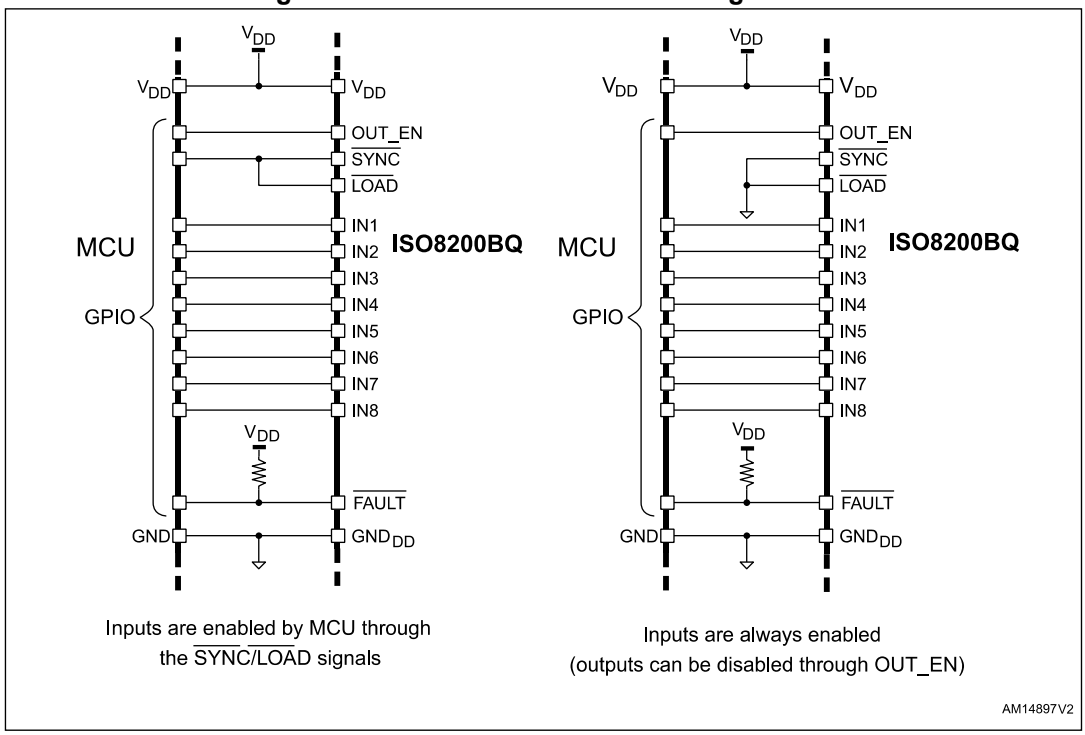
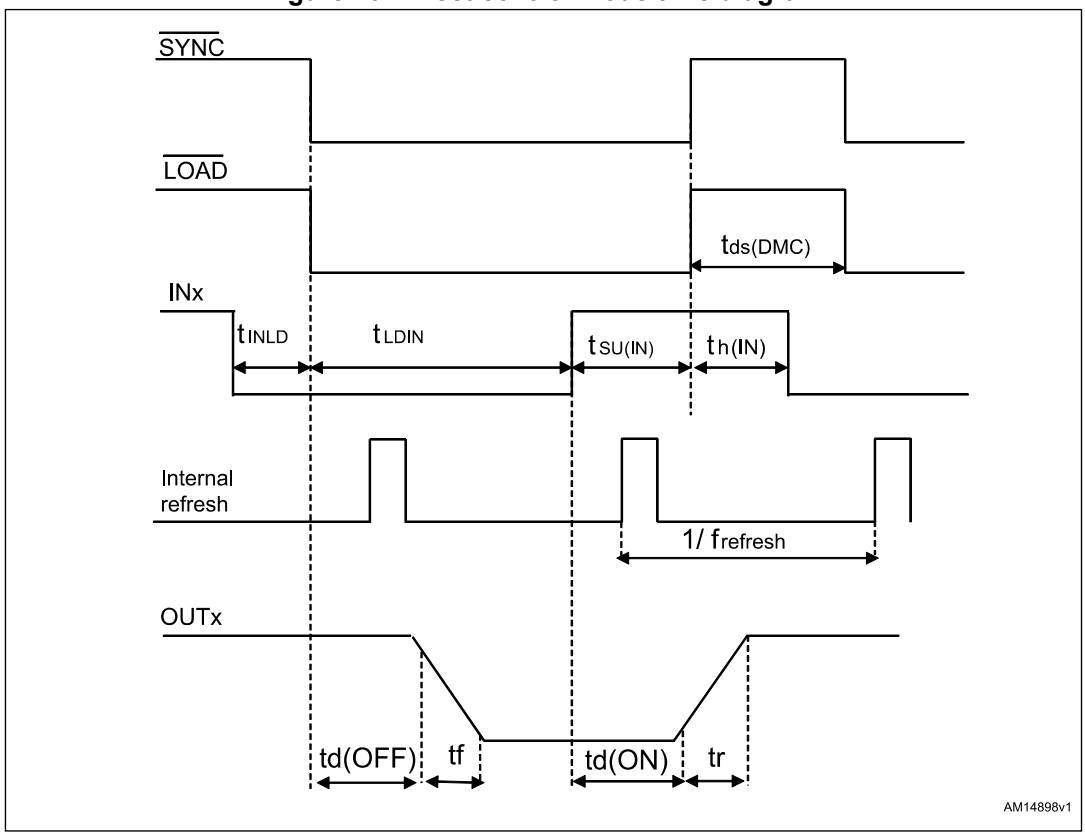


Figure 10. Direct control mode time diagram



6.3 Synchronous control mode (SCM)

When $\overline{SYNC}$ and $\overline{LOAD}$ inputs are independently driven, the device can operate in synchronous control mode (SCM). The SCM is used to reduce the jittering of the outputs and to drive all outputs of different devices at the same time.

In SCM the $\overline{LOAD}$ signal is forced low to update the input buffer while the $\overline{SYNC}$ signal is high. The $\overline{LOAD}$ signal is raised and the $\overline{SYNC}$ one is forced low for at least $t_{SYNC(SCM)}$. During this period, the internal refresh is disabled and any pending transmission between the low voltage and the isolated side is completed. When the $\overline{SYNC}$ signal is raised the channel output configuration is changed according to the one stored in the input.

If the $t_{SYNC(SCM)}$ limit is met, the maximum jitter of the channel outputs is t_{jitter}(SCM).

If more devices share the same $\overline{SYNC}$ signal, all device outputs change simultaneously with a maximum jitter related to maximum delay and maximum jitter for single device.

Table 15. Interface signal operation in synchronous control mode

$\overline{LOAD}$	$\overline{SYNC}$	OUT_EN	Device behavior
Don't care	Don't care	Low(1)	The outputs are disabled (turned off)
High	High	High	The outputs are left unchanged
Low	High	High	The input buffer is enabled. The outputs are left unchanged.
High	Low	High	The internal refresh signal is disabled. The transmission buffer is updated. The outputs are left unchanged.
High	Rising edge	High	The outputs are updated according to the current transmission buffer value
Low	Low	High	Should be avoided (DCM operation only)

1. The outputs are turned off on OUT_EN falling edge and they are kept disabled as long as it is low.

Figure 11. Synchronous control mode IC configuration

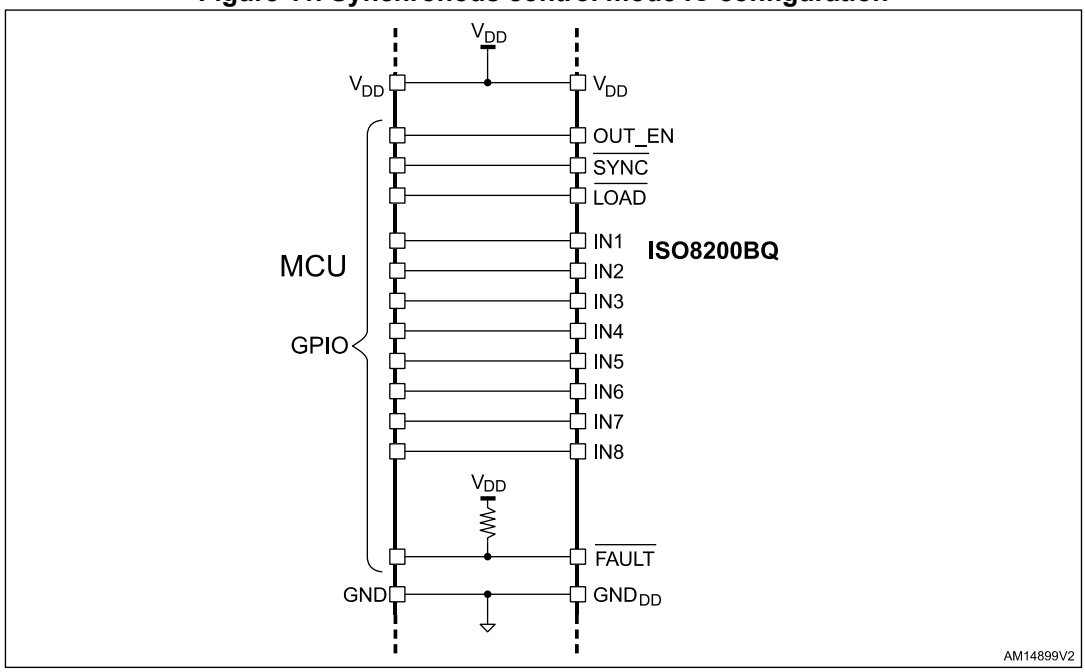


Figure 12. Synchronous control mode time diagram

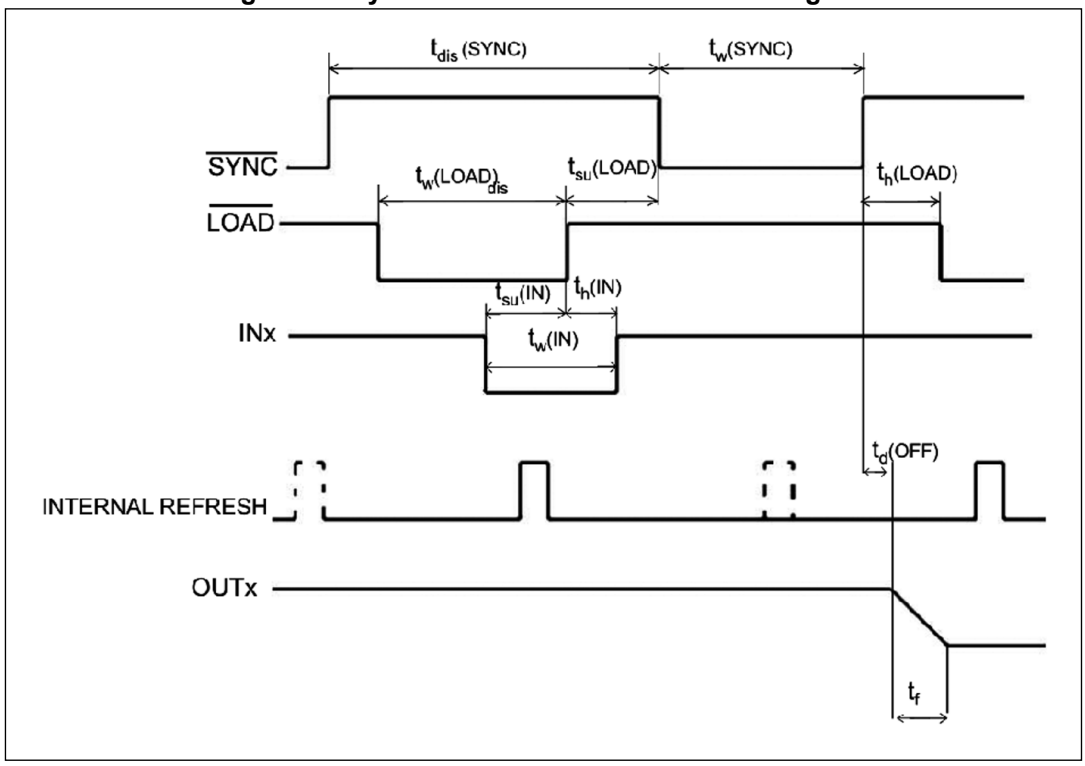
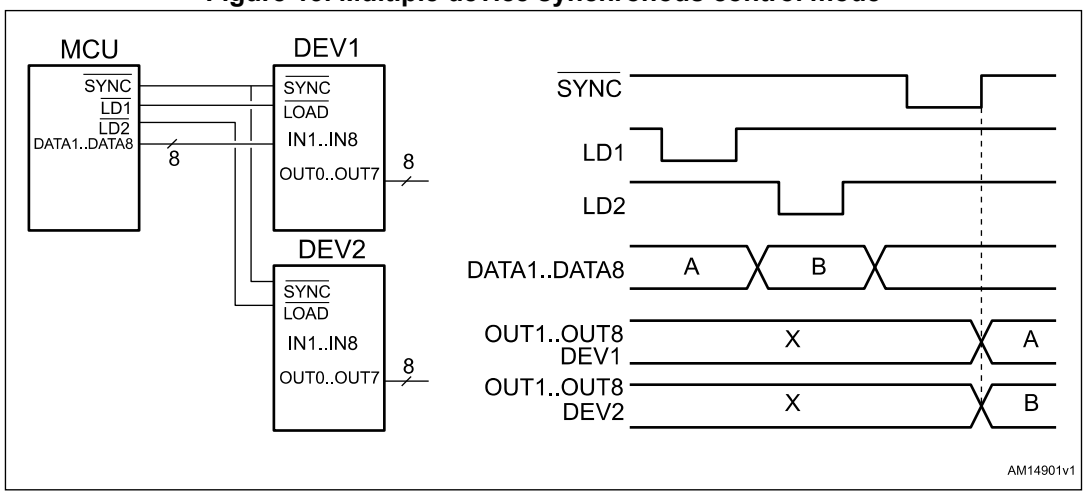


Figure 13. Multiple device synchronous control mode



6.4 Fault indication

The $\overline{FAULT}$ pin is an active low open-drain output indicating fault conditions. This pin is active when at least one of the following conditions occurs:

- Junction overtemperature of one or more channels ($T_J > T_{TJSD}$)
- Communication error

The communication error is intended as an internal data corruption event in the data transfer through isolation. In case of communication error the outputs are initially kept in the previous status and then reset (turned off) at the first communication error during data transfer of the refresh signal.

6.4.1 Junction overtemperature and case overtemperature

The thermal status of the device is updated during each transmission sequence between the two isolated sides.

In SCM operation, when the $\overline{LOAD}$ signal is high and the $\overline{SYNC}$ one is low, the communication is disabled. In this case the thermal status of the device cannot be updated and the $\overline{FAULT}$ indication can be different from the current status.

In any case, the thermal protection of the channel outputs is always operative.

Figure 14. Thermal status update (DCM)

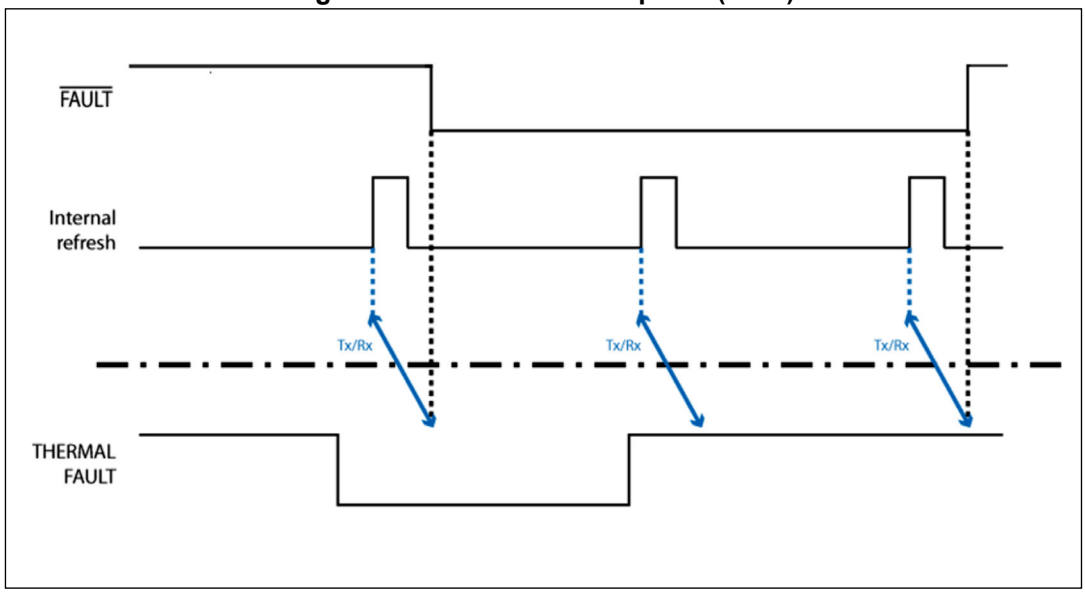
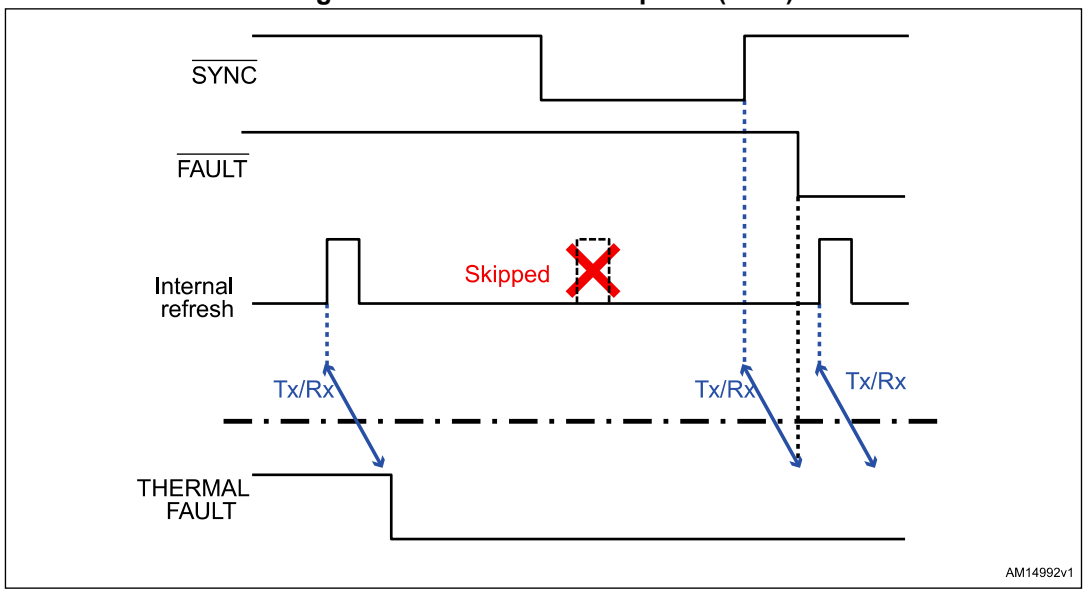


Figure 15. Thermal status update (SCM)



7 Power section

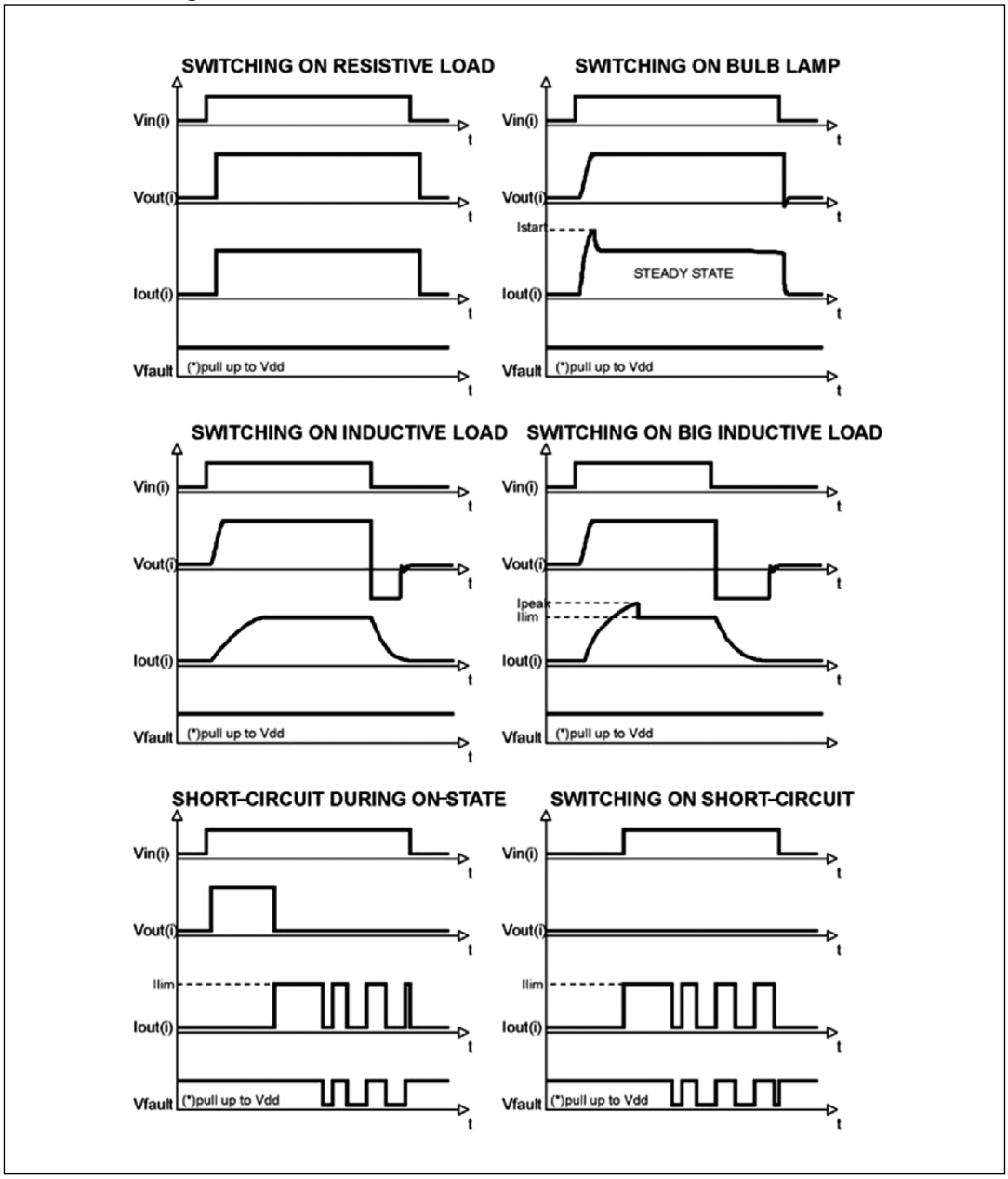
7.1 Current limitation

The current limitation process is active when the current sense connected on the output stage measures a current value, which is higher than a fixed threshold.

When this condition is verified the gate voltage is modulated to avoid the increase of the output current over the limitation value.

Figure 16 shows typical output current waveforms with different load conditions.

Figure 16. Current limitation with different load conditions



7.2 Thermal protection

The device is protected against overheating in case of overload conditions. During the driving period, if the output is overloaded, the device suffers two different thermal stresses, the former related to the junction, and the latter related to the case.

The two faults have different trigger thresholds: the junction protection threshold is higher than the case protection one; generally the first protection, that is active in thermal stress conditions, is the junction thermal shutdown. The output is turned off when the temperature is higher than the related threshold and turned back on when it goes below the reset threshold. This behavior continues until the fault on the output is present.

If the thermal protection is active and the temperature of the package increases over the fixed case protection threshold, the case protection is activated and the output is switched off and back on when the junction temperature of each channel in fault and case temperature is below the respective reset thresholds.

Figure 17 shows the thermal protection behavior, while *Figure 18* reports typical temperature trends and output vs. input state.

Figure 17. Thermal protection flowchart

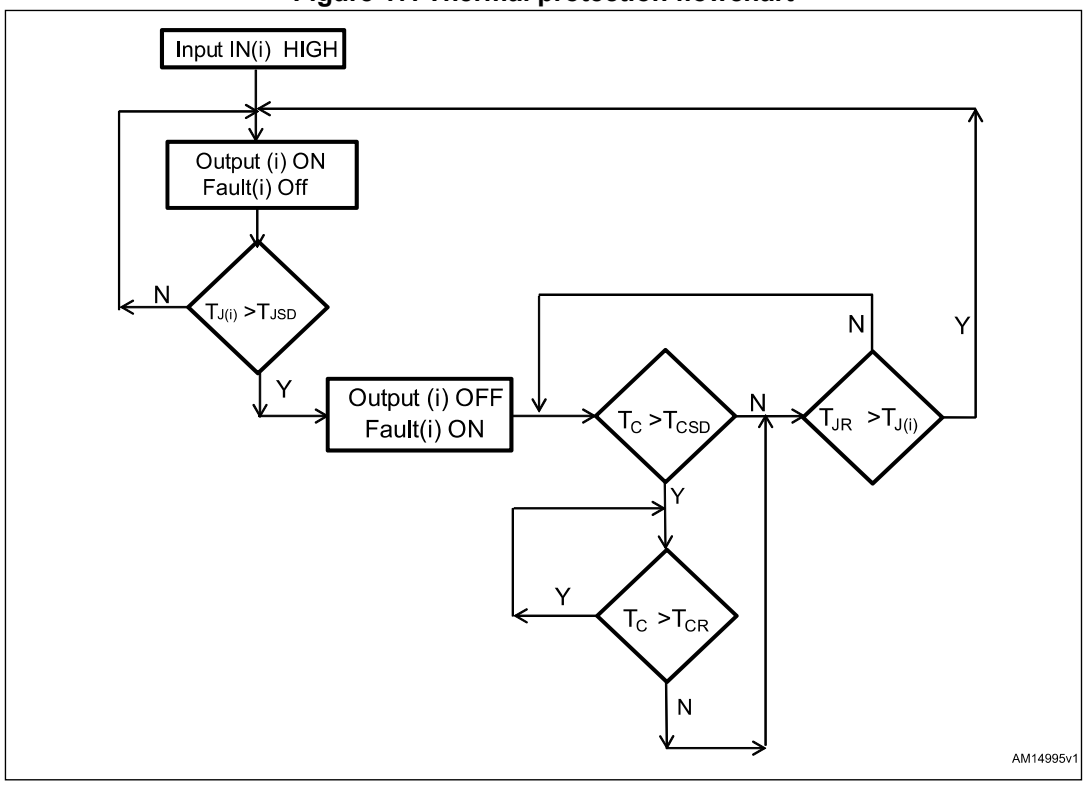
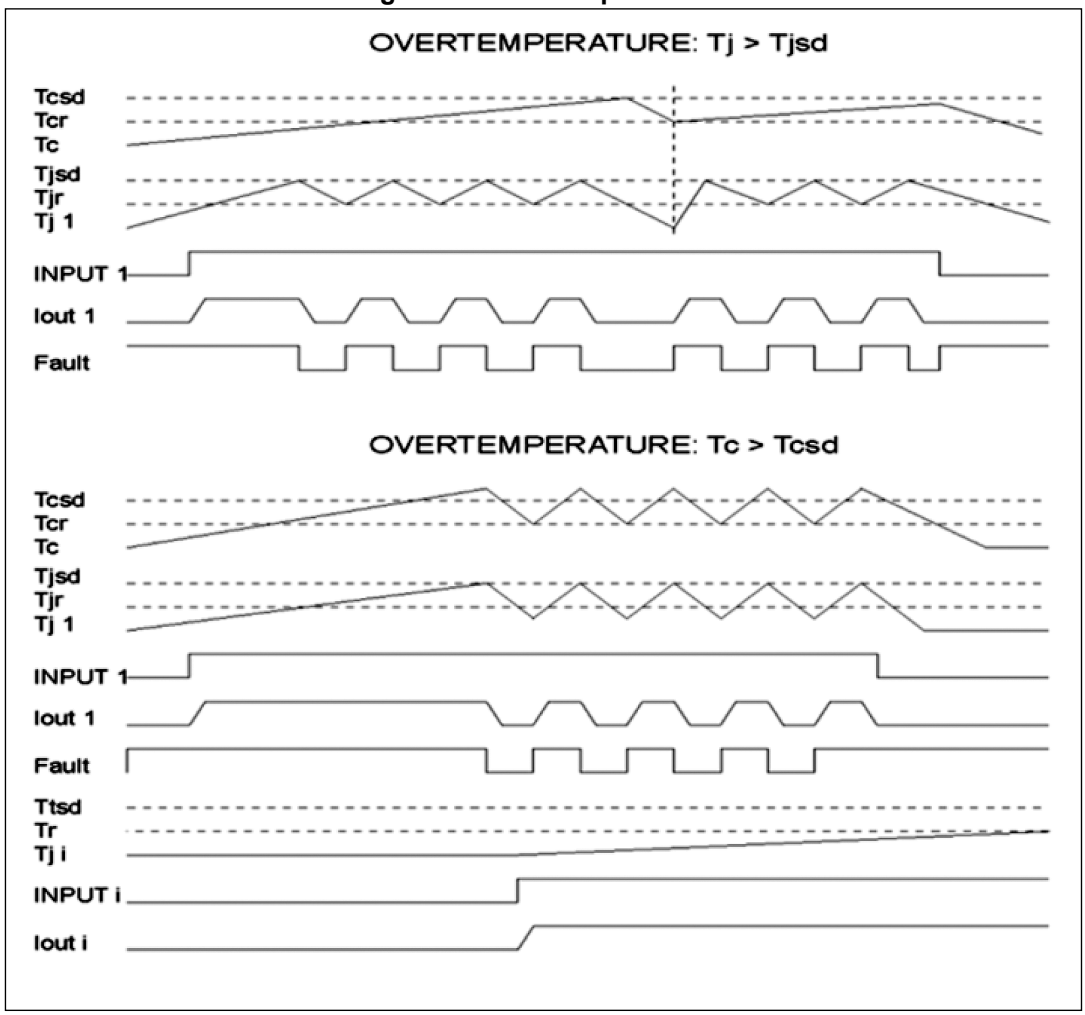


Figure 18. Thermal protection



8 Reverse polarity protection

Reverse polarity protection can be implemented on board using two different solutions:

1. Placing a resistor (R_{GND}) between IC GND pin and load GND
2. Placing a diode in parallel to a resistor between IC GND pin and load GND

If option 1 is selected, the minimum resistance value has to be selected according to *Equation 1*:

Equation 1

$$R_{GND} \geq V_{CC}/I_{GNDcc}$$

where I_{GNDcc} is the DC reverse ground pin current and can be found in *Section 3: Absolute maximum ratings on page 9*.

Power dissipated by RGND during reverse polarity situations is:

Equation 2

$$P_D = (V_{CC})^2/R_{GND}$$

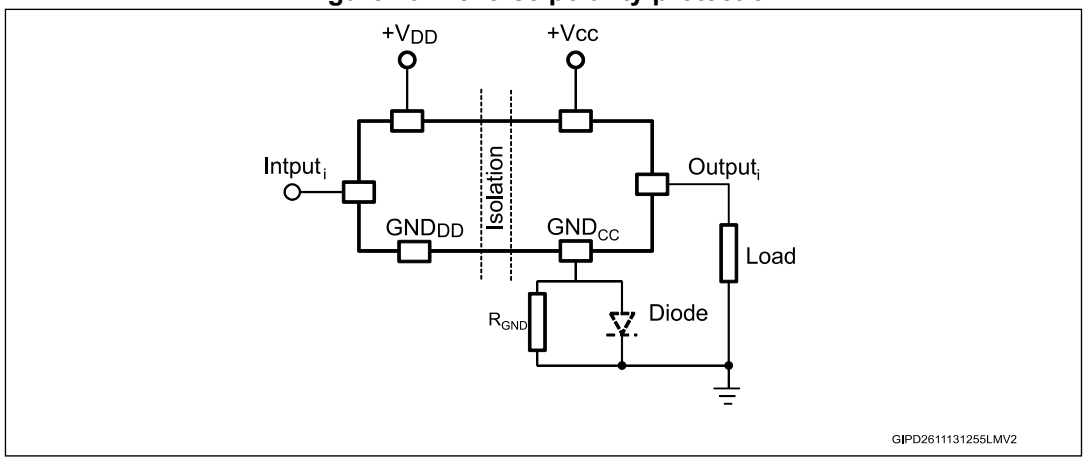
If option 2 is selected, the diode has to be chosen by taking into account VRRM > $|V_{CC}|$ and its power dissipation capability:

Equation 3

$$P_D \geq I_S * V_F$$

*Note: In normal operation (no reverse polarity), there is a voltage drop (ΔV) between GND of the device and GND of the system. Using option 1, ΔV = Rgnd * Icc. Using option 2, ΔV = $VF_{@(IF)}$.*

Figure 19. Reverse polarity protection



This schematic can be used with any type of load.

9 Reverse polarity on V_{DD}

The reverse polarity on V_{DD} can be implemented on board by placing a diode between GND_{DD} pin and GND digital ground.

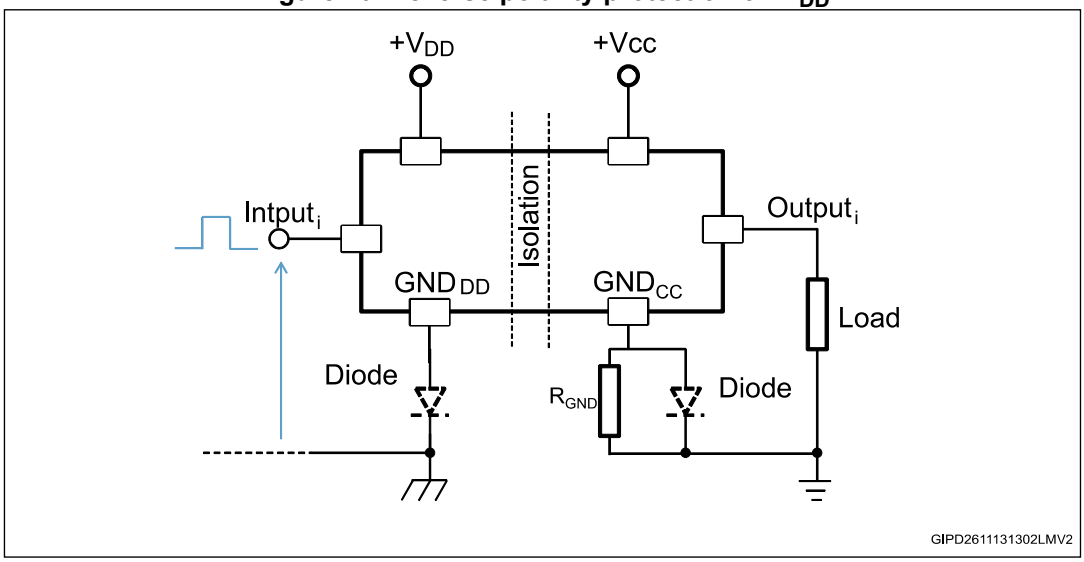
The diode has to be chosen by taking into account VRRM > $|V_{DD}|$ and its power dissipation capability:

Equation 4

$$P_D \geq I_{DD} * V_F$$

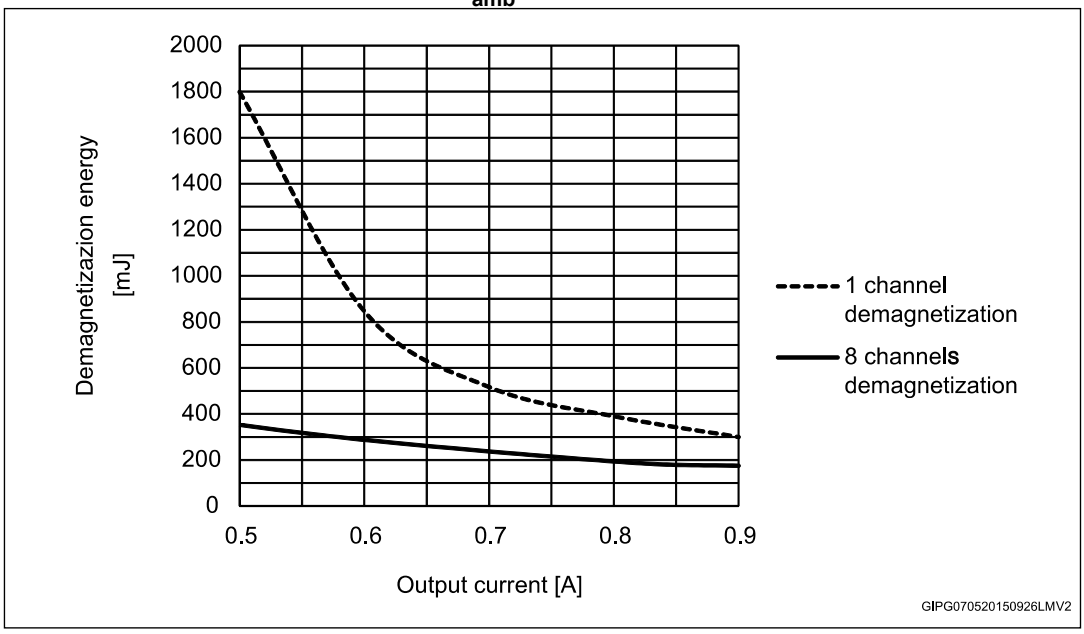
Note: In normal operation (no reverse polarity), there is a voltage drop (ΔV = VF@(Idd)) between GNDDD of the device and digital ground of the system.
In order to guarantee to proper triggering of the input signal, ΔV(max.) must result lower than $V_{IH(MIN)}$.

Figure 20. Reverse polarity protection on V_{DD}



10 Demagnetization energy

Figure 21. Maximum demagnetization energy vs. load current, typical values T_{amb} = 125 °C

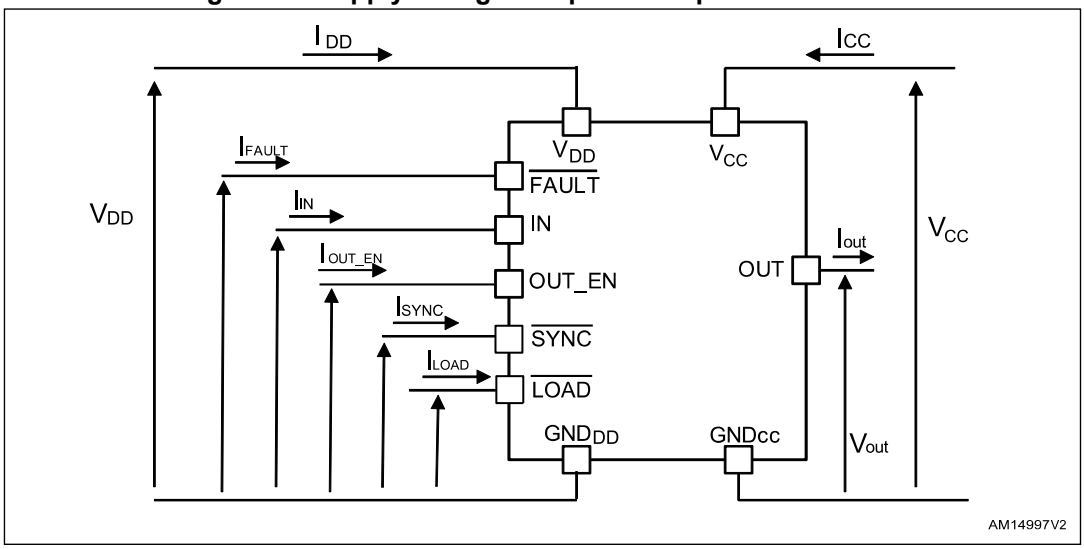


11 Conventions

Supply voltage and power output conventions

Figure 22 shows the convention used in this paper for voltage and current usage.

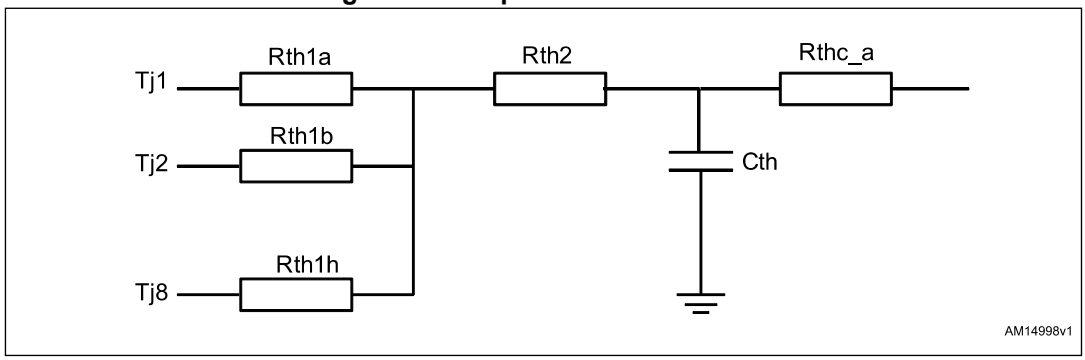
Figure 22. Supply voltage and power output conventions



12 Thermal information

Thermal impedance

Figure 23. Simplified thermal model



13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

13.1 TFQFPN32 package information

Figure 24. TFQFPN32 package outline

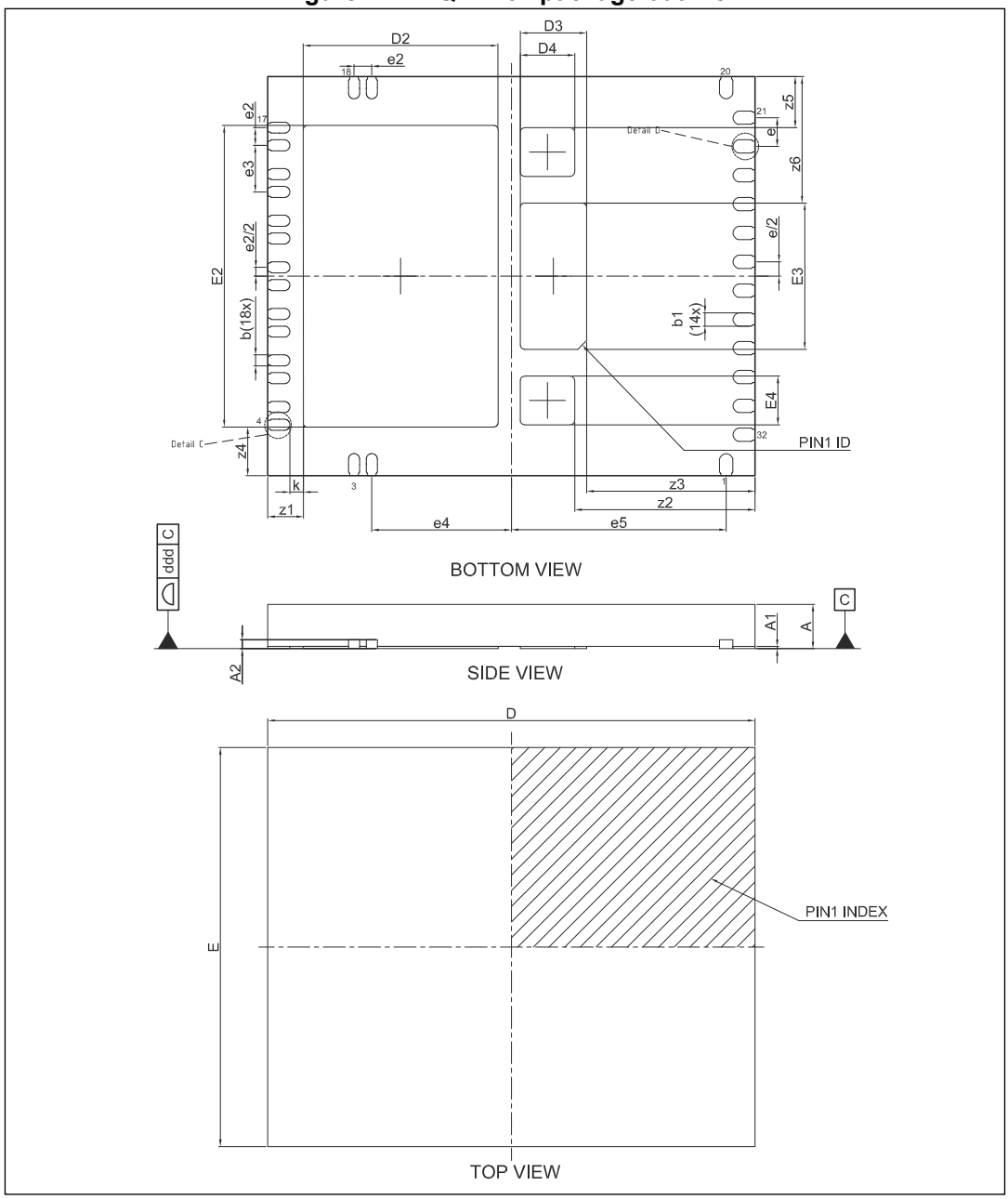


Figure 25. TFQFPN32 package detail outline

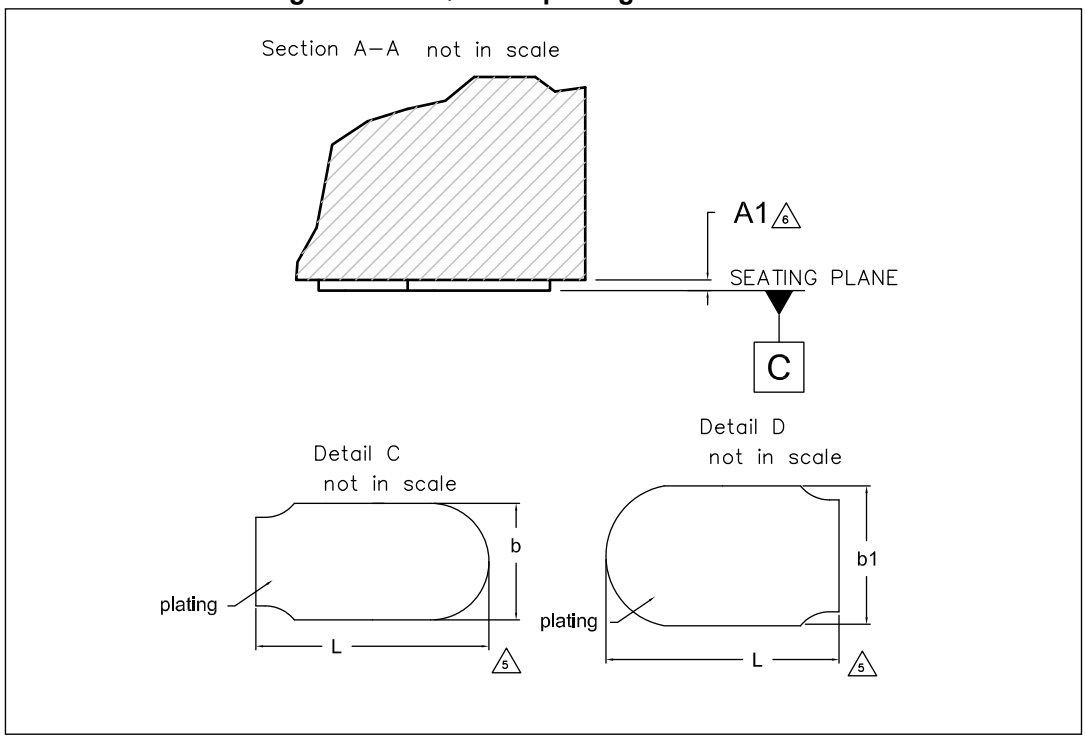


Figure 26. TFQFPN32 suggested footprint (measured in mm)

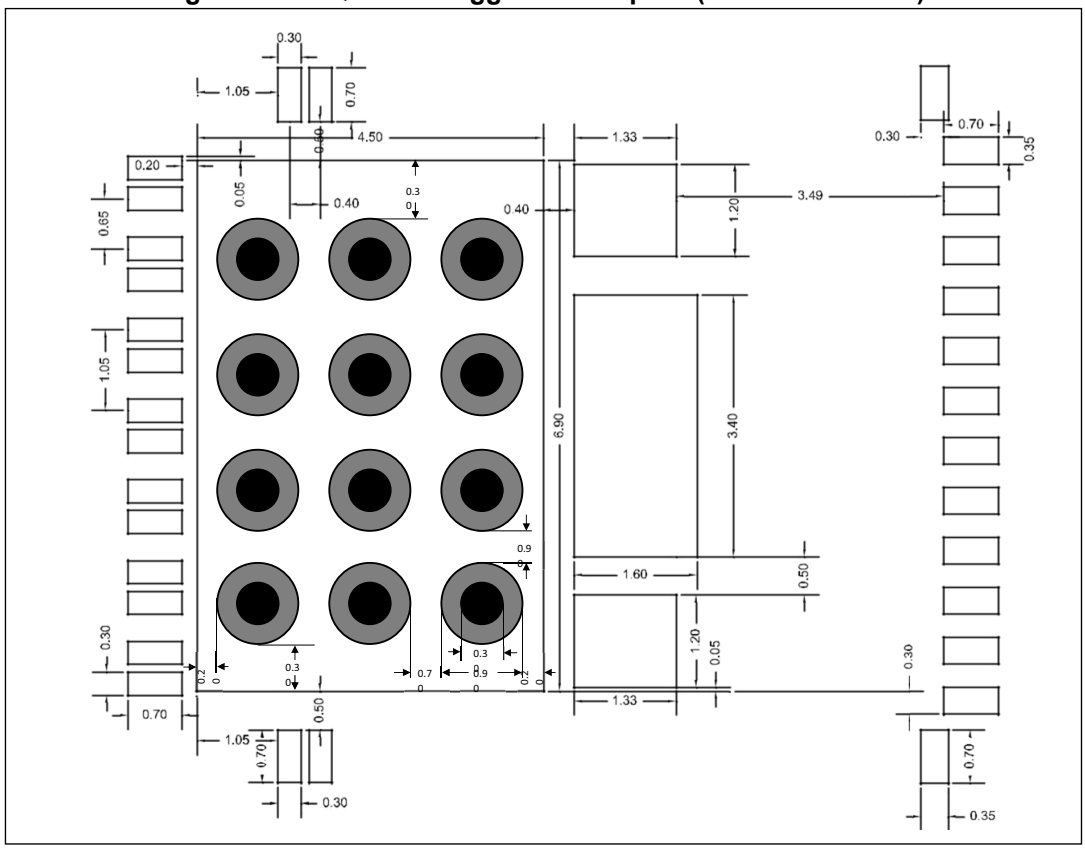


Table 16. TFQFPN32 package mechanical data

Symbol	Dimensions (mm]		
	Min.	Typ.	Max.
A	0.95	1.00	1.05
A1	0	-	0.05
A2	-	0.20 REF	-
b(1)	0.20	0.25	0.30
b1(1)	0.25	0.30	0.35
D	10.90	11.0	11.10
E(1)	8.90	9.00	9.10
D2	4.30	4.40	4.50
E2	6.70	6.80	6.90
D3	1.40	1.50	1.60
E3	3.20	3.30	3.40
D4	1.13	1.23	1.33
E4	1.00	1.10	1.20
e	-	0.65	-
e2	-	0.40	-
e3	-	1.05	-
e4	-	3.15	-
e5	-	4.85	-
k	0	0.30	-
z1	-	0.80	-
z2	-	4.07	-
z3	-	3.80	-
z4	-	1.10	-
z5	-	1.15	-
z6	-	2.85	-
L(1)	0.45	0.50	0.55

1. Dimensions “b” and “L” are measured on terminal plating surface.

Table 17. Tolerance of form and position

Symbol	Tolerance of form and position	Definition	Notes
aaa	0.15	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	
bbb	0.10	The tolerance that controls the position of the entire terminal pattern with respect to datum's A and B. The center of the tolerance zone for each terminal is defined by the basic dimension "e" as related to datum's A and B.	
ccc	0.10	The tolerance located parallel to the seating plane in which the top surface of the package must be located.	
ddd	0.08	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension "e".	This tolerance is normally compounded with tolerance zone defined by bbb.
eee	0.08	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly known as the “coplanarity” of the package terminals.
fff	0.10	The tolerance that controls the position of the exposed metal heat feature. The center of the tolerance zone will be datum's defined by the centerlines of the package body.	
REF	-	-	No tolerance for A2

14 Packing information

14.1 TFQFPN32 packing information

14.1.1 TFQFPN32 packing method concept

Figure 27. TFQFPN32 packing method concept

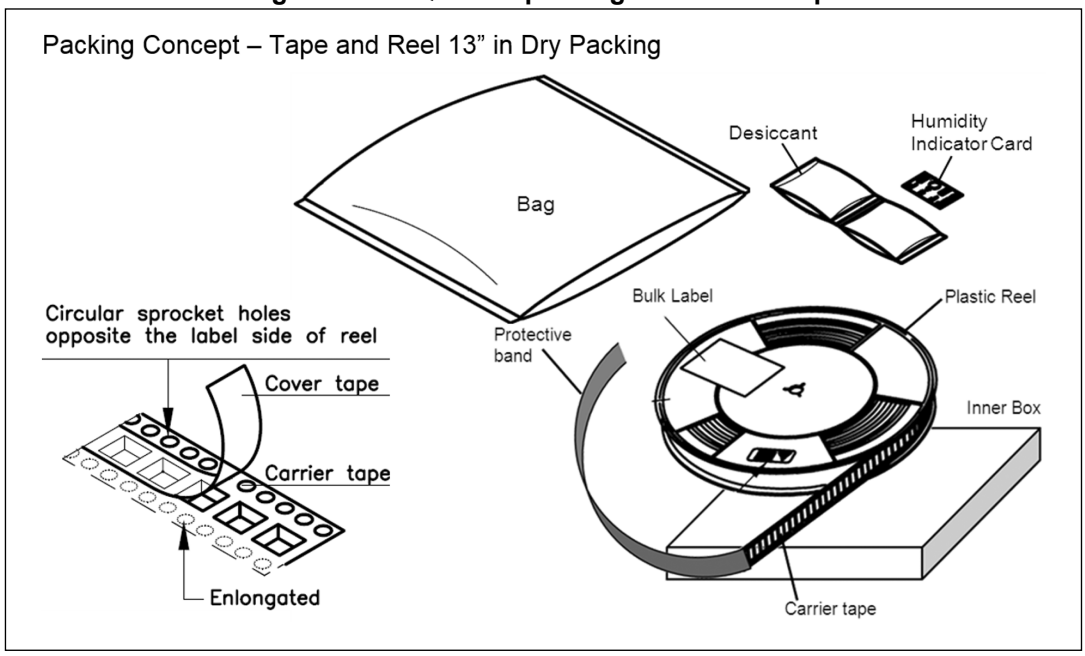
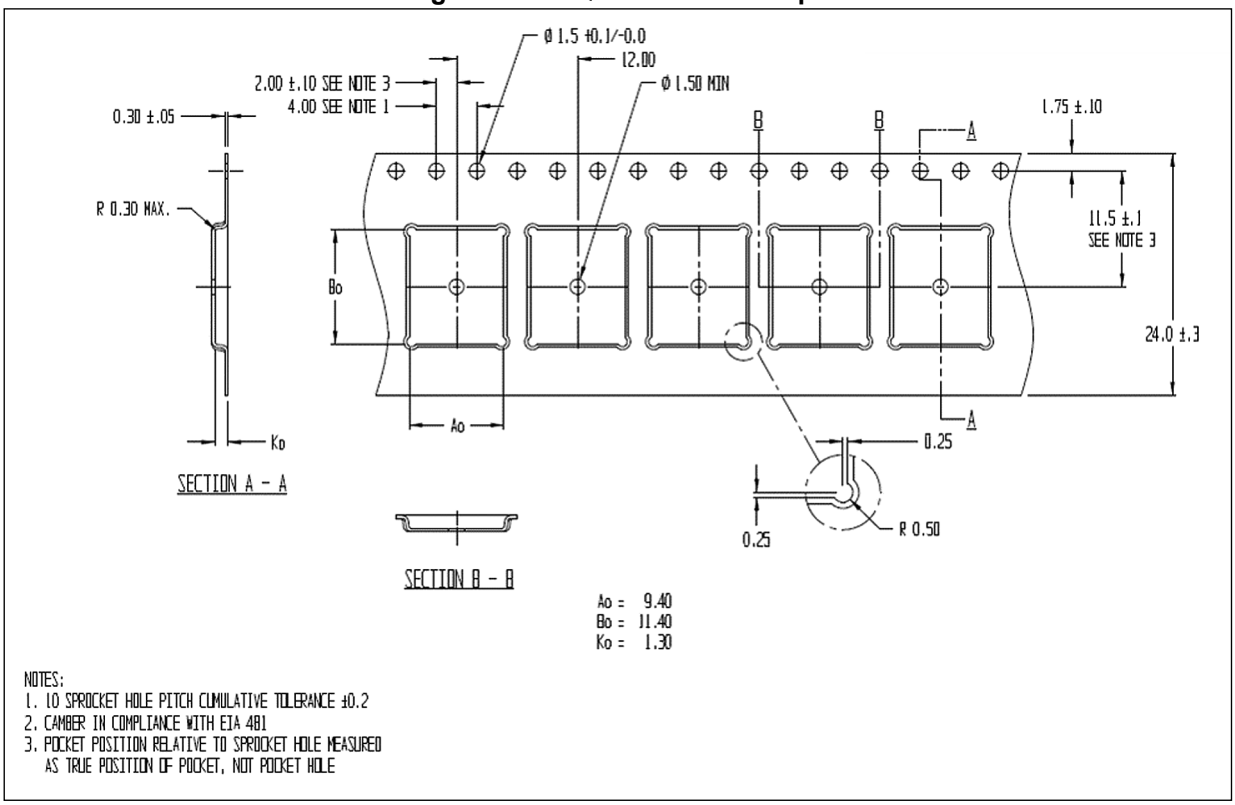
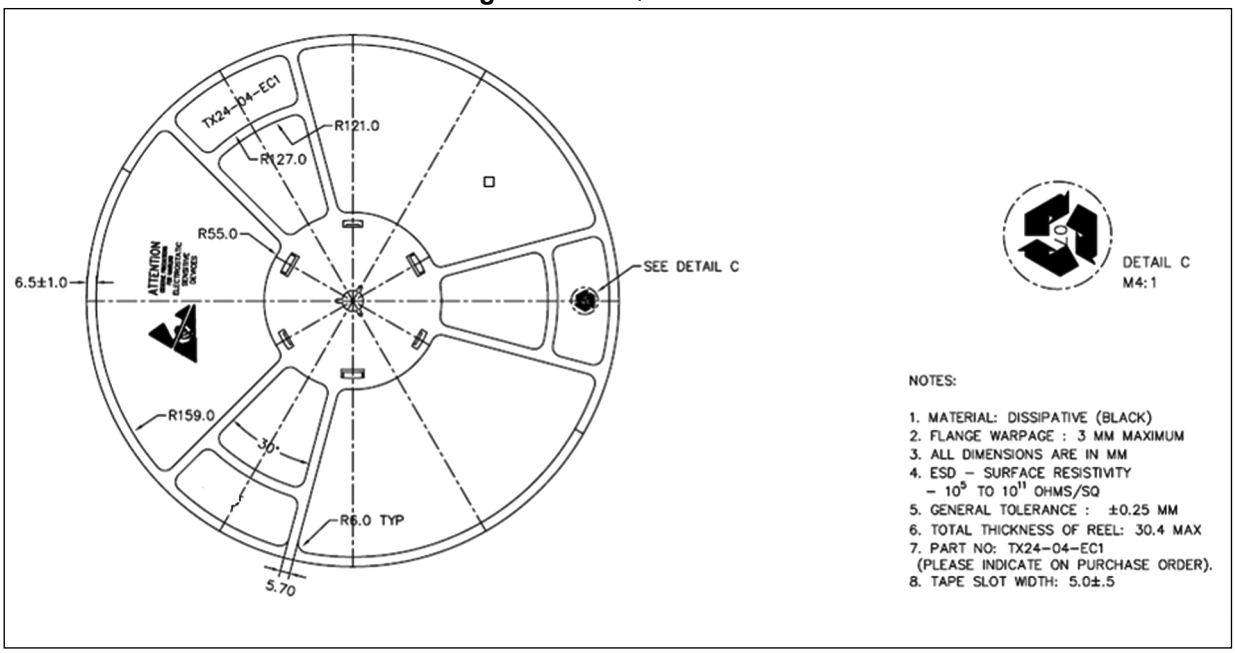


Figure 28. TFQFPN32 carrier tape



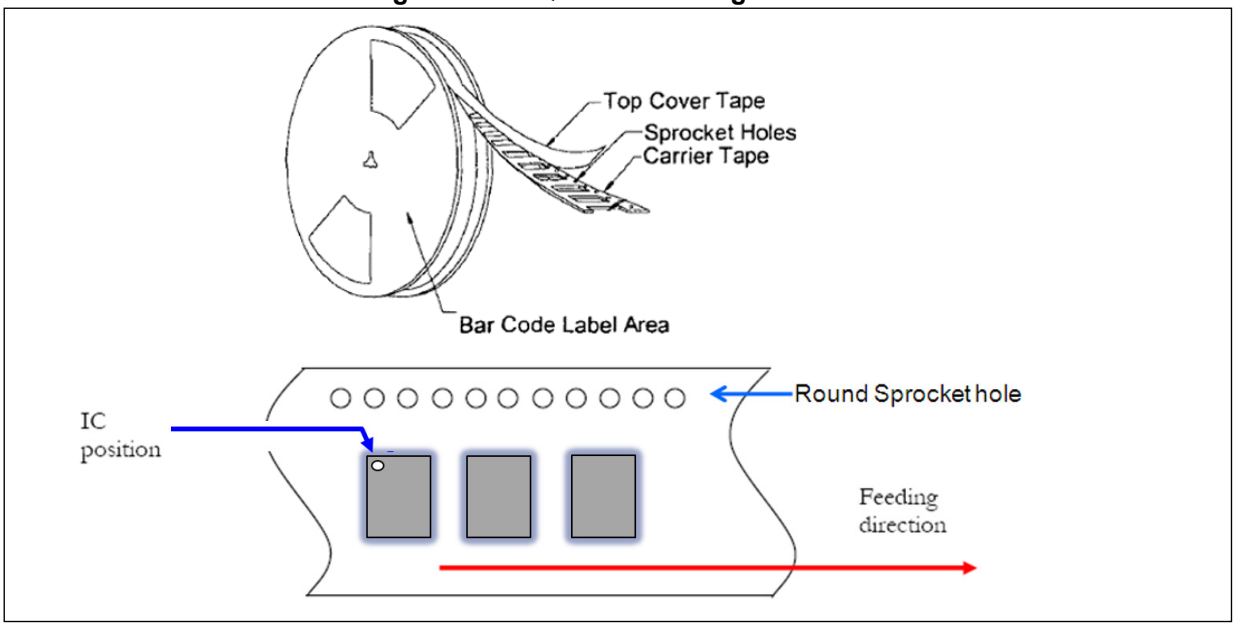
Reel – 330 mm diameter x 101 mm hub x 24 mm width

Figure 29. TFQFPN32 reel



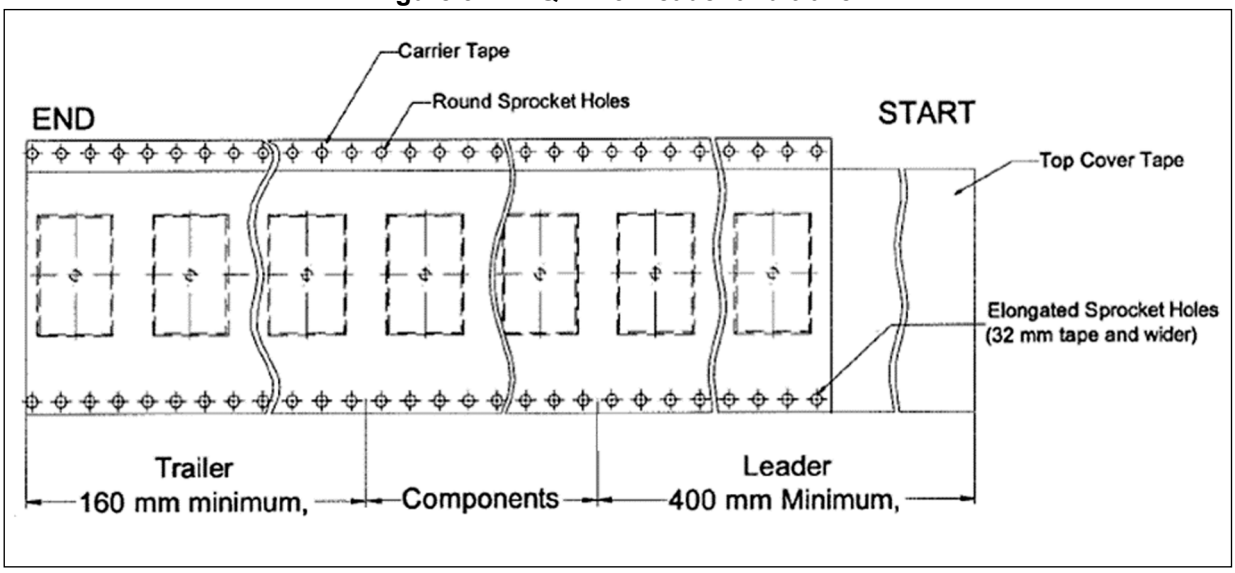
14.1.2 TFQFPN32 winding direction

Figure 30. TFQFPN32 winding direction



14.1.3 TFQFPN32 leader and trailer

Figure 31. TFQFPN32 leader and trailer



Note: Leader and trailer length as per EAI-481specification.

15 Ordering information

Table 18. Ordering information

Order code	Package	Packing
ISO8200BQ	TFQFPN32	Tube
ISO8200BQTR	TFQFPN32	Tape and reel

16 Revision history

Table 19. Document revision history

Date	Revision	Changes
17-Nov-2016	3	Datasheet promoted from preliminary to production data. Updated *Table 6: Diagnostic pin and output protection function*.
21-Apr-2017	4	Updated *Table 10:* "*Insulation and safety-related specifications*". Minor text changes.
05-Oct-2017	5	Updated *Table 11: "IEC 60747-5-2 insulation characteristics"*.
18-May-2018	6	Updated *Section : Features on page 1*. Replaced Vdd by V_{DD} in whole document. Updated titles of *Table 7 on page 11* and *Table 9 on page 14* . Updated titles of *Figure 3 on page 12*, *Figure 5 on page 13*, *Figure 6 on page 13*, *Figure 20 on page 29* and *Figure 21 on page 30* . Added cross-reference to *Section 6.2* in *Table 13 on page 17*. Updated *Figure 9 on page 20* and *Figure 11 on page 21* (replaced ISO8200B by ISO8200BQ). Added *Section on page 34*. Minor modifications throughout document.
24-Apr-2019	7	Added *Table 12: Safety limits on page 15*, Updated *Table 2: Absolute maximum ratings on page 9* Updated *Section : Features on page 1*. Minor text changes.
18-Oct-2019	8	Updated *Section : Features on page 1*.
08-May-2020	9	*Table 4*, *11* and *16* updated. *Figure 24* replaced. *Table 17* added.

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