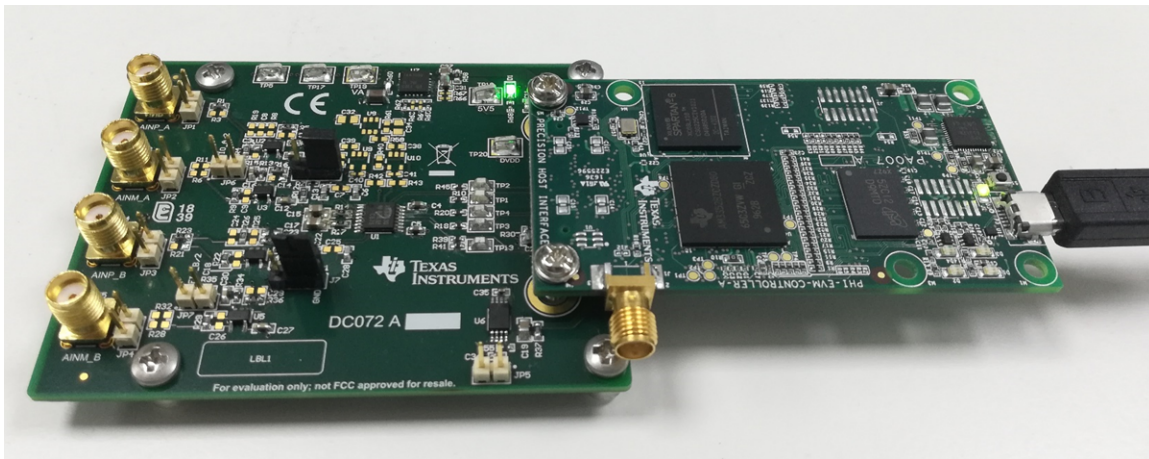


ADS8353Q1EVM-PDK Evaluation module

This user's guide describes the characteristics, operation, and use of the ADS8353-Q1 evaluation module (EVM) performance demonstration kit (PDK). This kit is an evaluation platform for the ADS8353-Q1 device, which is a 16-bit, dual-channel, simultaneous-sampling, 600-kSPS, single-ended and pseudo-differential analog input, successive approximation register (SAR) analog-to-digital converter (ADC) that features an easy-to-use serial programming interface (SPI). The ADS8353Q1EVM-PDK eases evaluation with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials (BOM).



The following related documents are available through the [Texas Instruments](https://www.ti.com) website.

Table 1. Related Documentation

Device	Literature Number
ADS8353-Q1	SBAS931
OPA320-Q1	SLOS884
TPS7A47-Q1	SBVS118
REF34-Q1	SBAS901A

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1 Overview

The ADS8353Q1EVM-PDK evaluation kit includes the ADS8353-Q1EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over the USB for data capture and analysis.

The ADS8353-Q1EVM board includes the ADS8353-Q1 SAR ADC, all the peripheral analog circuits, and the components required to achieve optimum performance from the ADC.

The PHI controller board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS8353-Q1 device
- Supplies power to all active circuitry on the ADS8353-Q1EVM board

Along with the ADS8353-Q1EVM and PHI controller board, this evaluation kit includes an A-to-micro-B USB cable to connect to a computer.

1.1 ADS8353Q1EVM-PDK Features

The ADS8353Q1EVM-PDK showcases the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS8353-Q1 ADC
- USB powered—no external power supply is required
- The PHI controller board provides a convenient communication interface to the ADS8353-Q1 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output
- Easy-to-use evaluation software for Microsoft® Windows® 7, 64-bit operating systems

1.2 ADS8353-Q1EVM Features

The ADS8353-Q1EVM showcases the following features:

- Onboard low-noise, low-distortion ADC input drivers optimized to meet ADC performance
- Onboard ultra-low noise, low-dropout (LDO) regulators, to generate supplies for the operation amplifier and ADC

2 Analog Interface

The ADS8353-Q1 is a low-power, dual-channel, simultaneous-sampling ADC that supports single-ended and pseudo-differential analog inputs. The ADS8353-Q1EVM uses an OPA320-Q1 to drive the analog inputs (AINP and AINM) of the ADC. The ADS8353-Q1EVM is designed for easy interfacing to analog sources. This section describes the front-end driver circuitry details, including jumper configurations for the analog input signal source.

2.1 Connectors for Analog Inputs

The ADS8353-Q1EVM has two 16-bit, simultaneous-sampling ADCs. The ADS8353-Q1EVM GUI can either be configured for individual ADC data sampling or simultaneous sampling with both ADCs. The ADS8353-Q1EVM is designed to interface to an external, analog source through either subminiature version A (SMA) connectors or 100-mil headers. Jumpers J2, J3, J4, and J5 are the SMA connectors that allow for analog signal source connectivity through coaxial cables. Alternatively, 100-mil jumper cables or mini-grabbers can be used to connect analog sources to pin 1 of connectors JP1, JP2, JP3, and JP4. [Table 2](#) lists the analog input connectors for the individual ADCs.

Table 2. Analog Input Connector Description

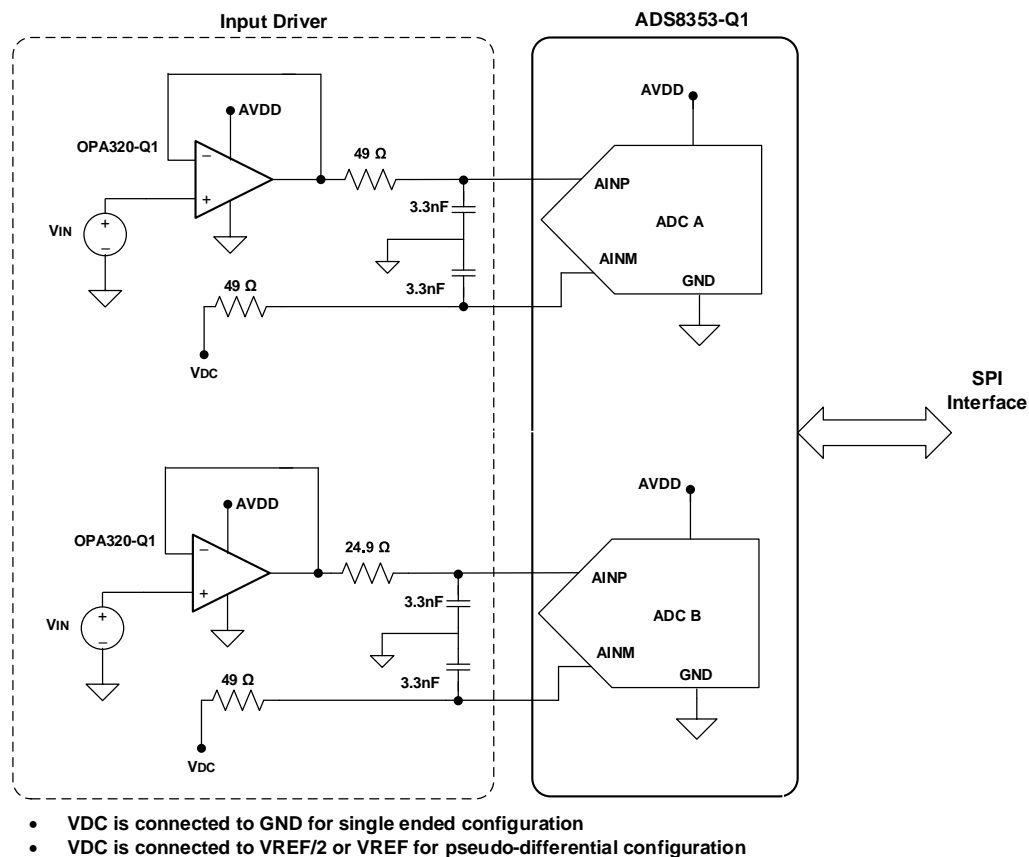
Pin Number	Signal	Description
J2 and J3	INP	Analog inputs provided at the SMA for ADC A
JP1:1 and JP2:1	INP	Alternate location to provide the analog inputs for ADC A
J4 and J5	INP	Analog inputs provided at the SMA for ADC B
JP3:1 and JP4:1	INP	Alternate location to provide the analog inputs for ADC B

2.2 ADC Input Signal Driver

The SAR ADC inputs terminate in switched-capacitor networks that create large instantaneous current loads when the switches are closed, which effectively makes the ADC inputs dynamically low impedance. The analog inputs of the ADC are therefore driven by an OPA320-Q1 used in a unity-gain buffer configuration to maintain ADC performance with maximum loading at full device throughput of the ADS8353-Q1 of 600 kSPS.

2.2.1 Input Signal Path

Figure 1 shows the signal path for the analog inputs applied to the ADS8353-Q1EVM. A separate OPA320-Q1 amplifier is used in a unity-gain buffer configuration to drive the individual analog inputs (AINP and AINM) of each ADC. There is onboard provisioning that enables configuring the OPA320-Q1 driver circuit to drive either single-ended ADC inputs or pseudo-differential ADC inputs. An RC filter with values of 49 Ω and 3.3 nF was selected to achieve a SINAD greater than 83 dB and a THD less than -100 dB for a 2-kHz sine-wave input at full throughput of the ADS8353-Q1 of 600 kSPS.


Figure 1. ADS8353-Q1EVM Analog Input Path

3 Digital Interfaces

As discussed in [Section 1](#), the ADS8353-Q1EVM interfaces with the PHI, which in turn communicates with the computer over the USB. The three devices on the EVM that the PHI communicates with are the two ADS8353-Q1 ADCs (over the SPI) and the EEPROM (over the I²C interface). The electrically erasable programmable read-only memory (EEPROM) comes preprogrammed with the information required to configure and initialize the ADS8353Q1EVM-PDK platform. When the hardware is initialized, the EEPROM is no longer used.

3.1 SPI for the ADC Digital I/O

The ADS8353Q1EVM-PDK supports the interface and ADC input modes detailed in the [ADS8353-Q1 datasheet](#). The PHI is capable of operating at a 3.3-V logic level and is directly connected to the digital I/O lines of the ADC.

4 Power Supplies

The ADS8353-Q1 supports a wide range of operation on its analog supplies. The AVDD operates from 4.5 V to 5.5 V. The DVDD operates from 1.65 V to 5.5 V, independent of the AVDD supply. The analog portion of the ADS8353-Q1EVM operates from a 5.3-V supply (VA) generated using the TPS7A47-Q1 low-noise, low-dropout regulator. The same supply is used to power the OPA320-Q1 front-end driver amplifiers.

The TPS7A47-Q1 regulator can be configured to generate a VA supply other than 5.3 V through programmable pin settings. For more information, see the *Detailed Description* section of the TPS7A47-Q1 device datasheet.

The digital portion of the ADC operates from a 3.3-V EVM_DVDD supply from the PHI.

4.1 ADC Input Driver Configuration

The ADS8353-Q1 supports modes where the ADC inputs can be configured as single-ended or pseudo-differential. The ADS8353-Q1 EVM allows the user to configure the ADC input driver amplifier either to drive single-ended ADC inputs or pseudo-differential ADC inputs. In the single-ended configuration, the individual ADC AINM pins are connected to ground and a unipolar signal is applied to AINP. In the pseudo-differential configuration, the individual ADC AINM pins are driven with a DC voltage of either $V_{REF} / 2$ (0 V to V_{REF} range) or V_{REF} (0 V to $2 \times V_{REF}$ range). For various analog input full-scale ranges supported by the ADS8353-Q1 in either single-ended or pseudo-differential mode, see the [ADS8353-Q1 datasheet](#). [Table 3](#) shows the jumper configurations required for the single-ended and pseudo-differential configurations.

Table 3. Jumper Settings for ADC Input Driver Configuration

ADC Input Type	ADC Input Full-Scale Range	Jumpers	Default Setting	Required Setting
Single-ended analog inputs	0 V to V_{REF} and 0 V to $2 \times V_{REF}$	J6 and J7	Open (all pins)	Short pins 2 and 3 of J6 and J7 (J6:2 ,J6:3 and J7:2, J7:3)
		JP6 and JP7	Open	Open
Pseudo-differential analog inputs	0 V to V_{REF}	J6 and J7	Open (all pins)	Short pins 1 and 2 of J6 and J7 (J6:1 ,J6:2 and J7:1, J7:2)
		JP6 and JP7	Open	Short pins 1 and 2 of jumpers JP6 and JP7
	0 V to $2 \times V_{REF}$	J6 and J7	Open (all pins)	Short pins 1 and 2 of J6 and J7 (J6:1 ,J6:2 and J7:1, J7:2)
		JP6 and JP7	Open	Open

4.2 ADC Voltage Reference Configuration

The ADS8353-Q1 has a low-noise, low-drift, 2.5-V internal voltage reference. By default, the ADS8353-Q1 EVM is configured to work with the ADC internal reference voltage of 2.5 V. The same reference voltage is brought on pin 1 of jumpers JP6 and JP7 that can be used to drive the ADC AINM pin when used in pseudo-differential configuration (either in 0 V to V_{REF} or 0 V to $2 \times V_{REF}$ analog input range).

There is also a provision for using an external voltage reference for the ADC. The external reference voltage can be generated by populating the REF34-Q1 (U8) and biasing components around U8. By default, the external reference and biasing circuit around U8 is not populated on the board. When using an external reference, the ADS8353-Q1 internal voltage reference must be disabled and the device must be programmed to accept the external reference voltage on its REFIO_x pins.

5 ADS8353Q1EVM-PDK Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for proper operation of the ADS8353Q1EVM-PDK.

5.1 Default Jumper Settings

Figure 2 shows the silkscreen plot, which details the jumper locations for the ADS8353Q1EVM-PDK.

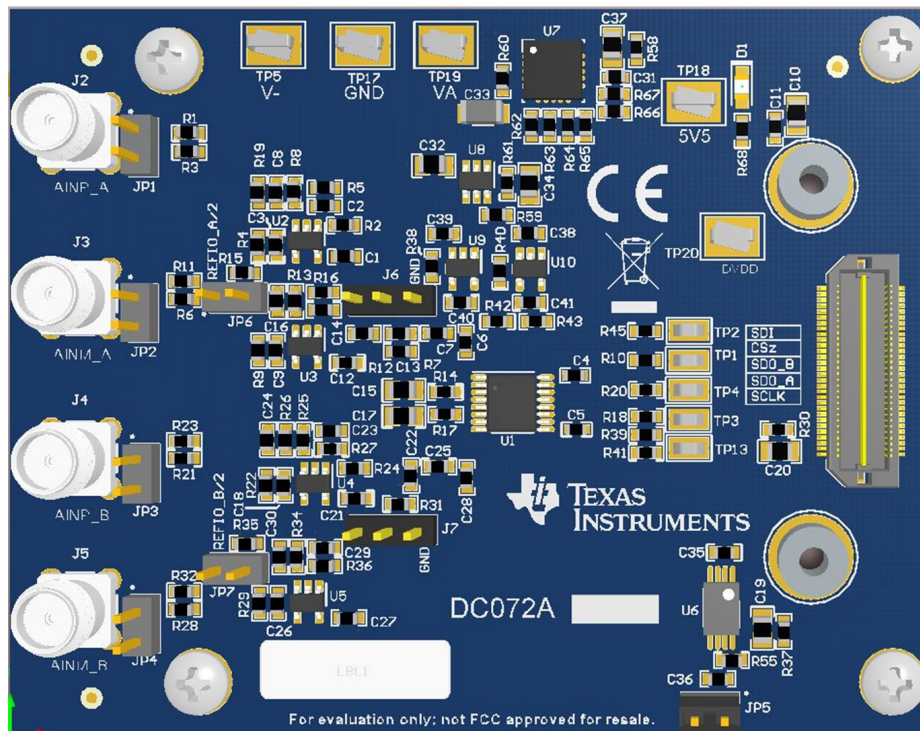


Figure 2. ADS8353Q1EVM-PDK Jumper Locations

Table 4 lists the functionality and default configuration of each jumper.

Table 4. Default Jumper Configurations

Reference Designator	Default Configuration	Description
JP1, JP2, JP3, JP4	Open	Use pin 1 of these jumpers as an alternate location to provide the analog input to ADC A and ADC B of the ADS8353-Q1.
JP5	Open	Connect this jumper to disable EEPROM write protection.
JP6, JP7	Open	Jumpers to feed either V_{REF} or $V_{REF} / 2$ to the OPA320-Q1 input driving the AINM pin of the ADC. See Section 7.3 for more details.
J6, J7	Open	Jumpers to configure the ADC inputs as single-ended or pseudo-differential. See Section 7.3 for more details.

5.2 EVM Graphical User Interface Software Installation

The following steps describe how to install the software for the ADS8353-Q1 EVM graphical user interface (GUI).

1. Download the latest version of the EVM GUI installer from the *Software* section of the [ADS8353Q1EVM-PDK Tool Folder](#), and run the GUI installer to install the EVM GUI software on your computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Failure to disable antivirus software, depending on the antivirus settings, may cause an error message to appear or the *installer.exe* file may be deleted.

2. Accept the license agreements (Figure 3) and follow the on-screen instructions to complete the installation.

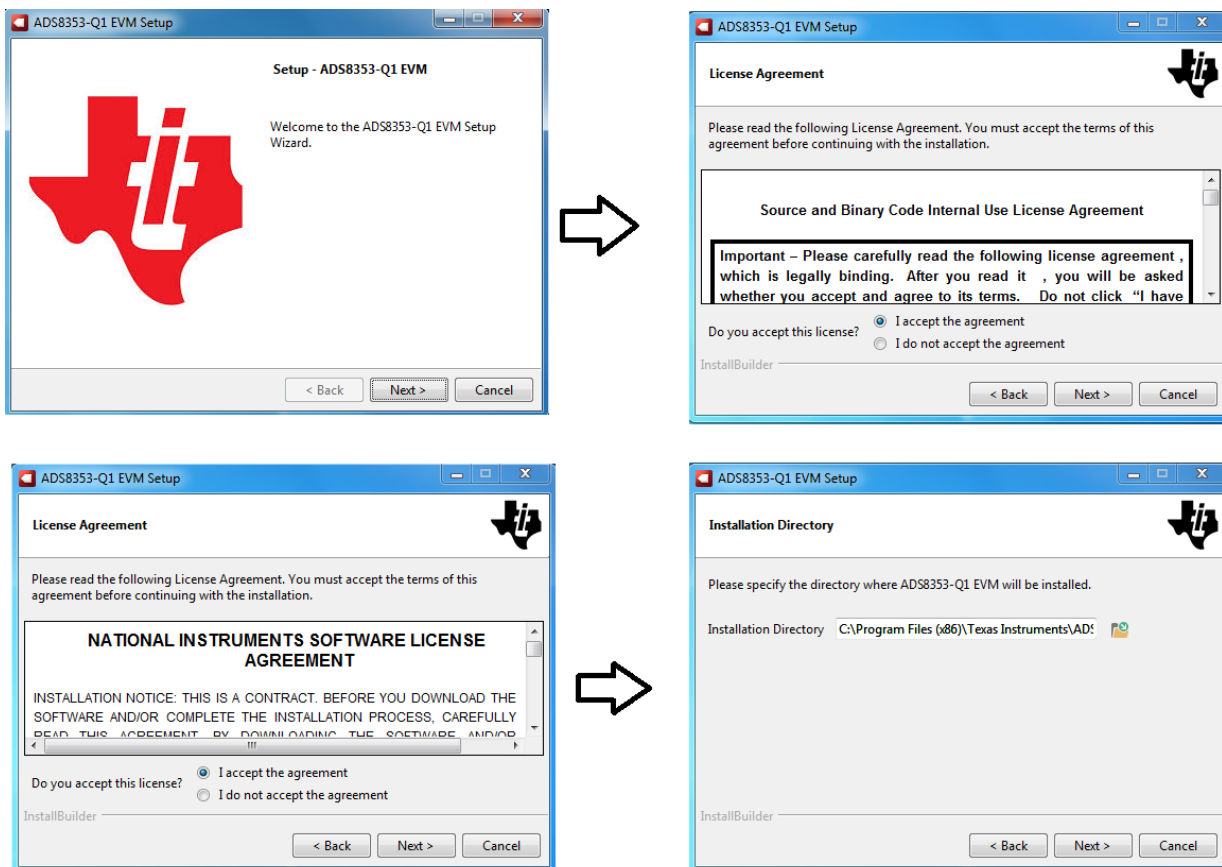


Figure 3. ADS8353-Q1EVM Software Installation Prompts

- As a part of the ADS8353-Q1EVM GUI installation, a prompt with a Device Driver Installation Wizard (Figure 4) appears on the screen. Click the *Next* button to proceed, then click the *Finish* button when the installation is complete.

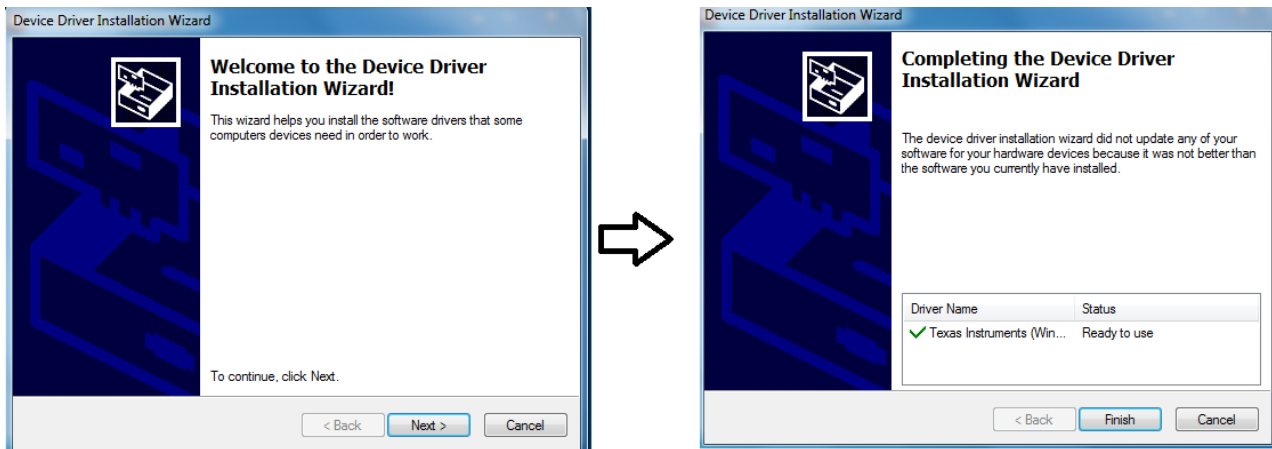


Figure 4. Device Driver Installation Wizard Prompts

NOTE: A notice may appear on the screen stating that Windows cannot verify the publisher of this driver software. Select the *Install this driver software anyway* option.

The device requires the LabVIEW™ Run-Time Engine (see Figure 5) and may prompt for the installation of this software, if not already installed.

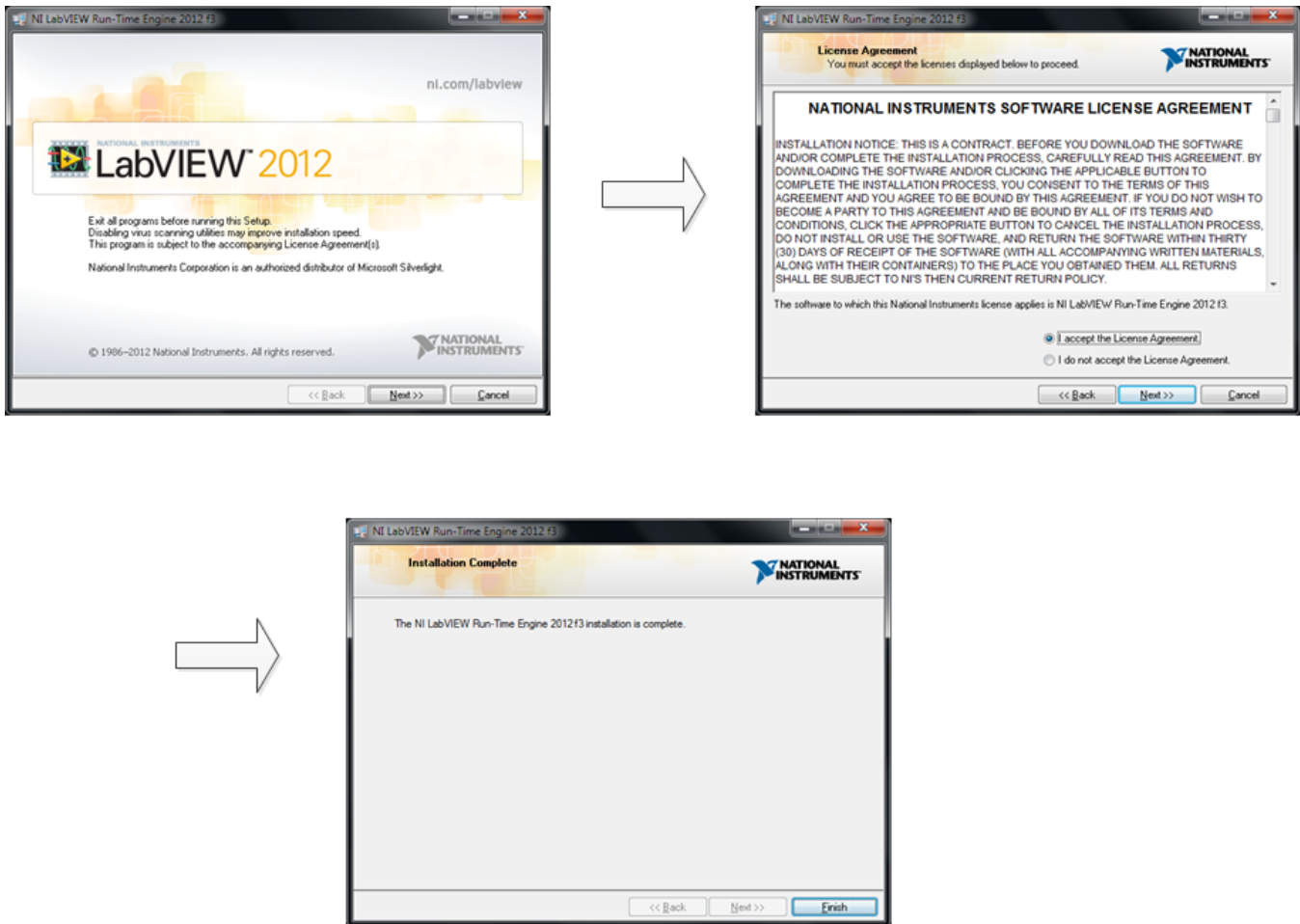


Figure 5. LabVIEW Run-Time Engine Installation

4. Check the *Create Desktop Shortcut* box, as [Figure 6](#) shows, after these installations.

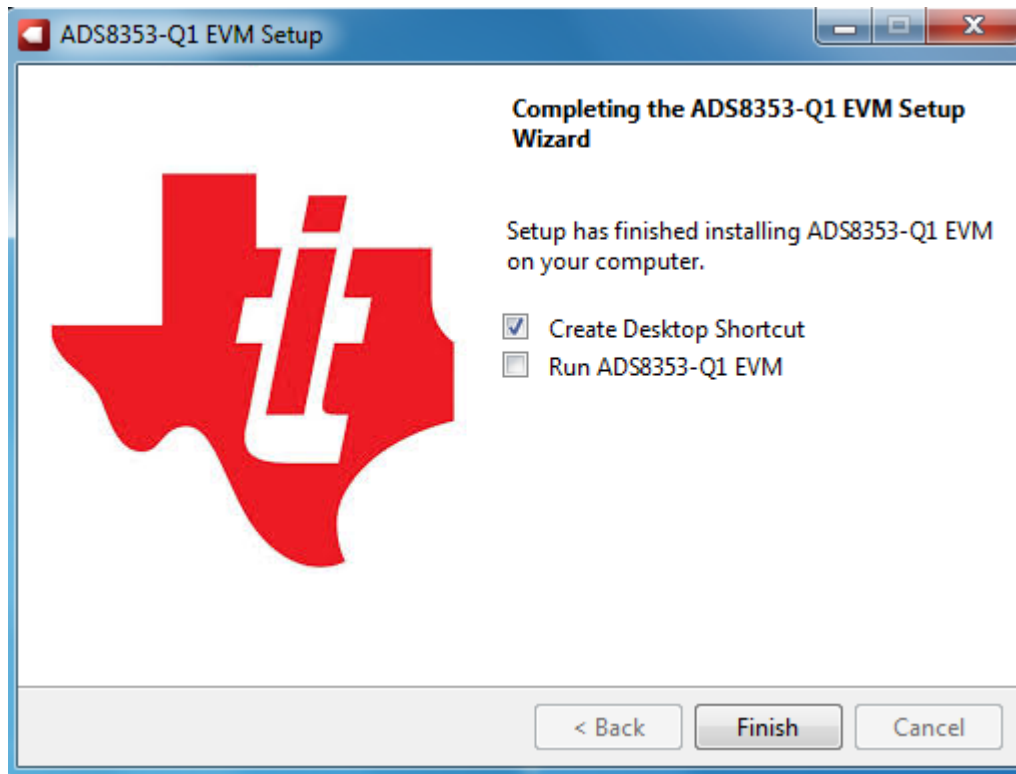


Figure 6. ADS8353Q1EVM-PDK Installation Final Step

6 ADS8353Q1EVM-PDK Operation

The following instructions are a step-by-step guide for connecting the device to a computer and evaluating the performance of the device.

1. Connect the device EVM to the PHI board. [Figure 7](#) indicates where two screws are to be installed.
2. Use the provided USB cable to connect the PHI to the computer.
 - LED D5 on the PHI lights up, indicating that the PHI is powered up.
 - LEDs D1 and D2 on the PHI start flashing, indicating that the PHI is booted up and communicating with the PC.

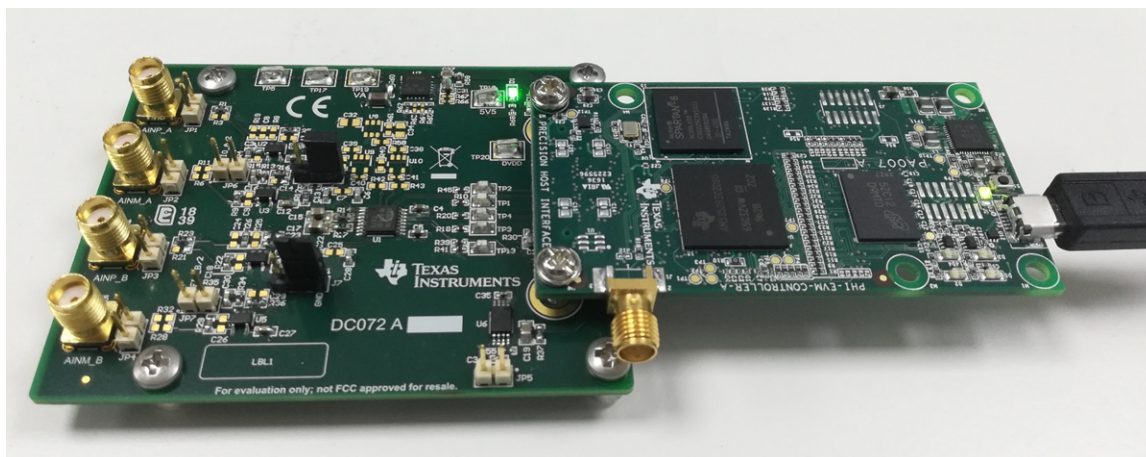


Figure 7. EVM-PDK Hardware Setup and LED Indicators

3. Launch the device EVM GUI software from the installed path, as [Figure 8](#) shows, or by using the desktop shortcut created during installation.

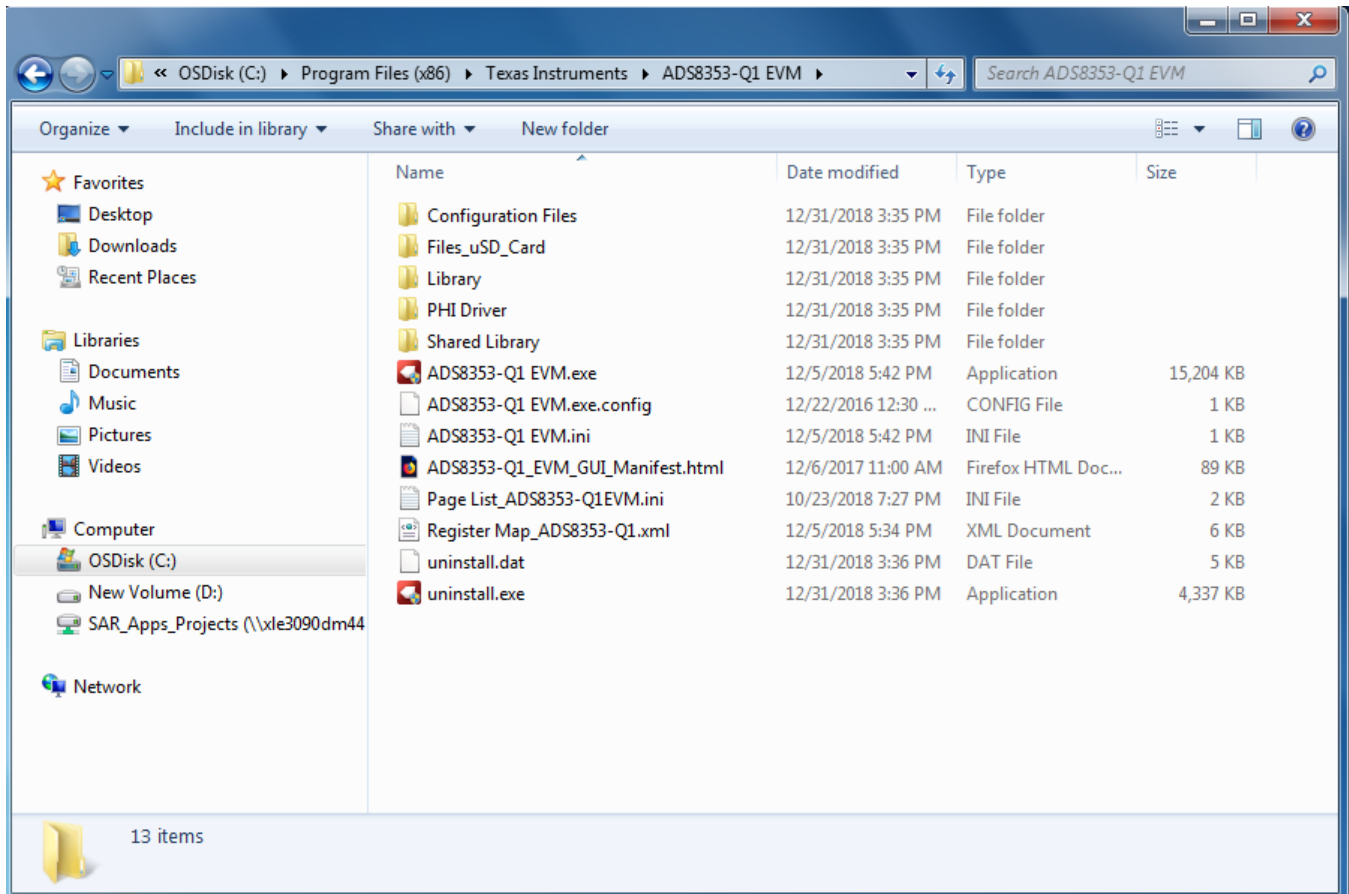


Figure 8. Launch the EVM GUI Software

6.1 EVM GUI Global Settings for ADC Control

Figure 9 shows the input parameters of the GUI (as well as their default values), through which the various functions of the ADS8353Q1EVM-PDK can be exercised. These settings are global and persist across the GUI tools listed in the top left pane (or from one page to another).

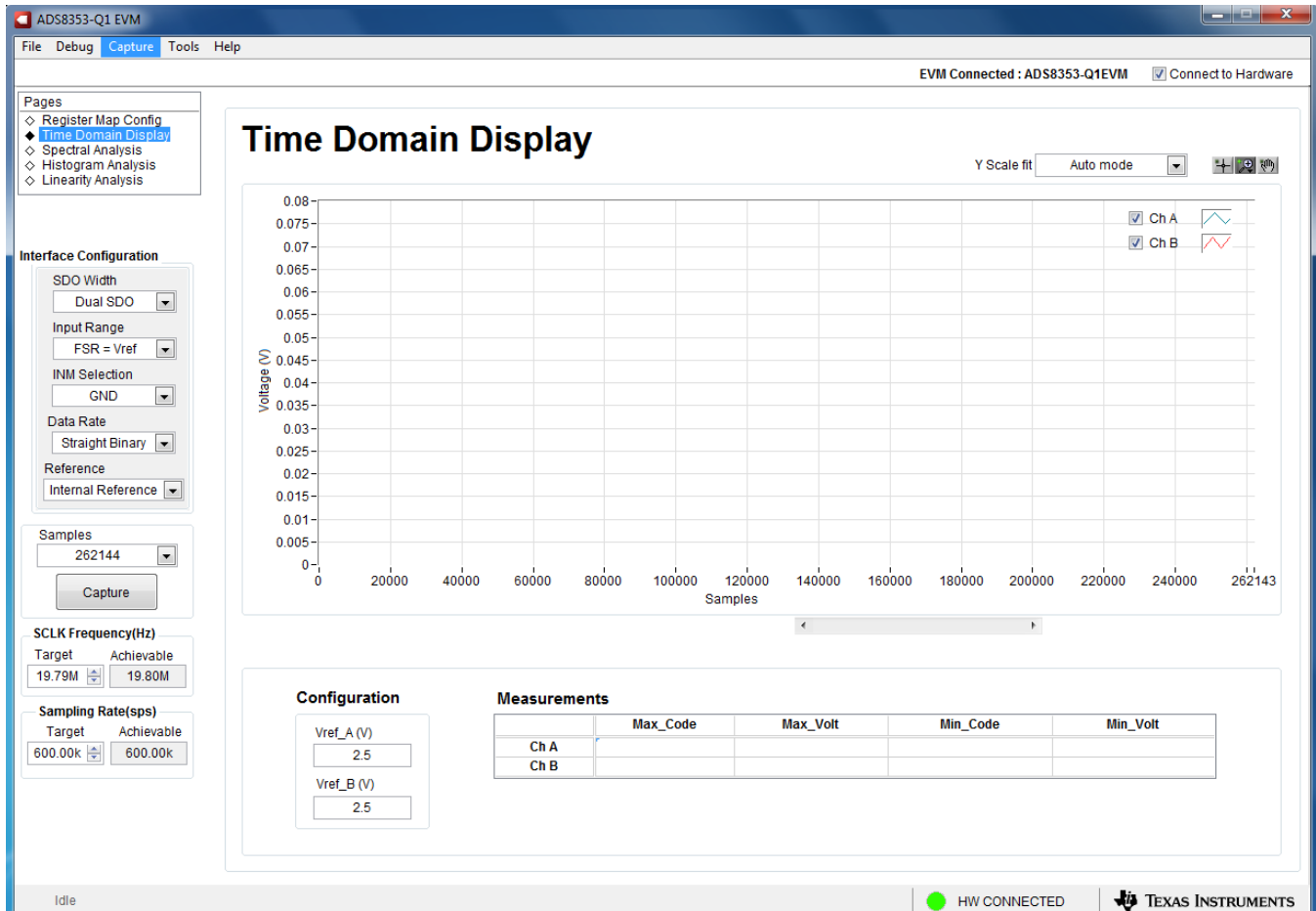


Figure 9. EVM GUI Global Input Parameters

The ADS8353-Q1 interface configurations can be selected on this page. The GUI lets the user select the ADC input range, ADC input configuration (single-ended or pseudo-differential), ADC voltage reference, and ADC data format using a drop-down menu.

The *SCLK Frequency* and *Sampling Rate* are selected on this page. The GUI lets the user enter the target values for these two parameters, and the GUI computes the closest value that can be achieved, considering the timing constraints of the device.

Select either one of the ADCs or both of the ADCs if they are configured in the simultaneous sampling scheme described in Section 2.1 by clicking on the drop-down menu titled *Channel Modes*. Specify a target SCLK frequency (Hz) and the GUI tries to match this frequency as closely as possible by changing the PHI PLL settings; however, the achievable frequency may differ from the target value entered. Similarly, the sampling rate of the ADC can be adjusted by modifying the *Target Sampling Rate* argument (Hz). The achievable ADC sampling rate can differ from the target value, depending on the applied SCLK frequency and the closest match achievable is displayed. This page, therefore, allows various settings available on the device to be tested in a repetitive fashion until arriving at the best settings for the corresponding test scenario.

6.2 Time Domain Display Tool

The *Time Domain Display* tool provides a visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or front-end drive circuits.

As per the selected interface mode settings using the *Capture* button indicated in Figure 10, the user can trigger a data capture of the selected number of samples from the ADS8353Q1EVM-PDK. The sample indices are on the x-axis, and two y-axes show the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the analysis tools described in the subsequent sections triggers calculations to be performed on the same set of data.

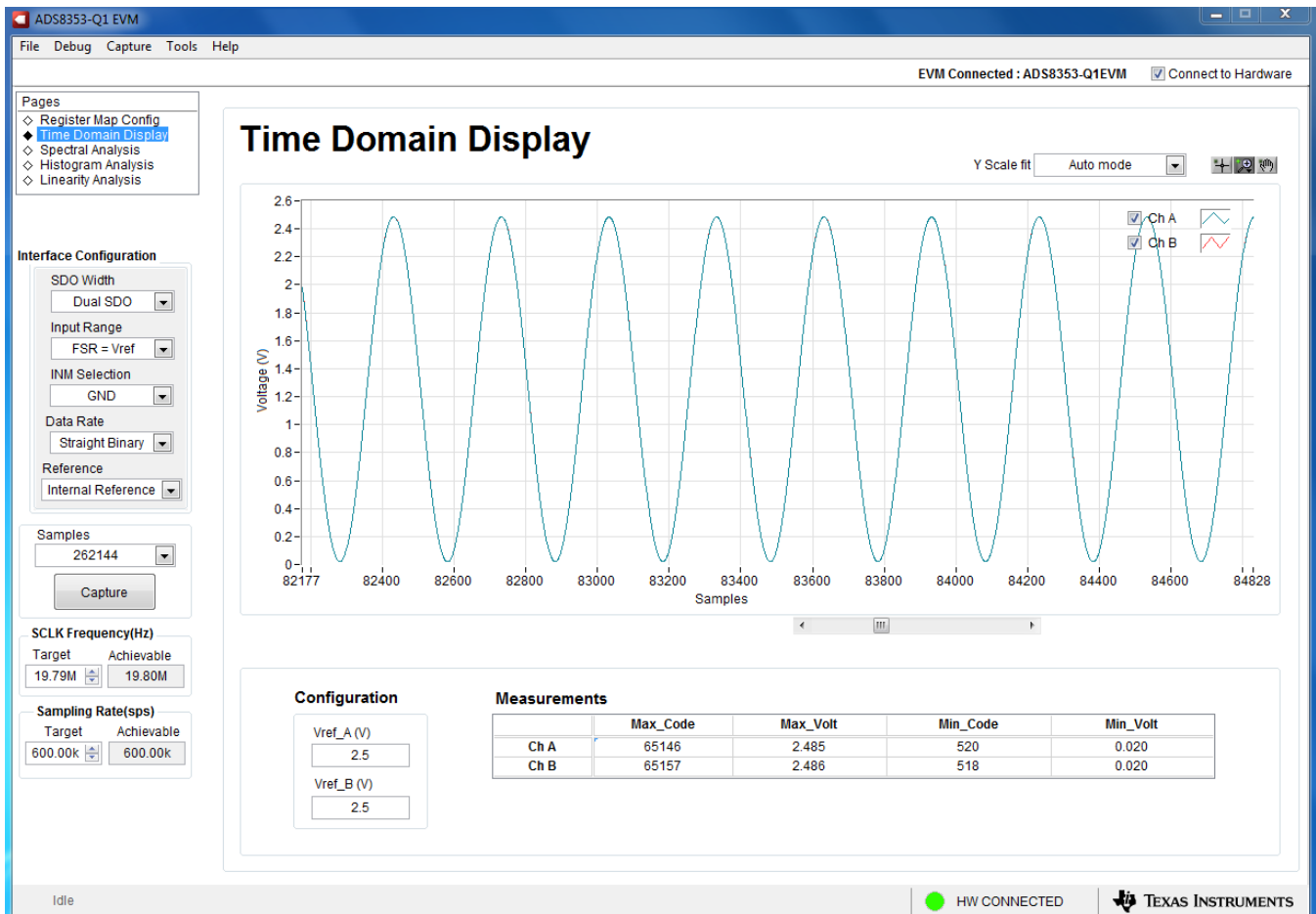


Figure 10. Time Domain Display Tool Options

6.3 Spectral Analysis Tool

The *Spectral Analysis* tool (Figure 11) is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS8353-Q1 SAR ADC through the use of a single-tone, sinusoidal signal FFT analysis, using the 7-term Blackman-Harris window setting. Alternatively, the window setting of *None* can be used to search for noise spurs over frequency in DC inputs.

For dynamic performance evaluation, the external, single-ended source must have better specifications than the ADC to ensure that the measured system performance is not limited by the performance of the signal source. Therefore, the external reference source must meet the source requirements listed in Table 5. Alternately, the user can use the [Precision Signal Injector EVM](#) that provides a low-distortion, low-noise, 2-kHz input signal for driving the input of the ADC, and pairs with most of the TI SAR ADC evaluation modules (EVMs). The board is powered over a USB, which also provides a user-interface connection to a PC.

Table 5. External Source Requirements for Device Evaluation (SNR and THD)

Specification Description	Specification Value
Signal frequency	2 kHz
External source type	Single-ended
External source common-mode	1.65 V
Minimum SNR	90 dB
Minimum THD	-115 dB

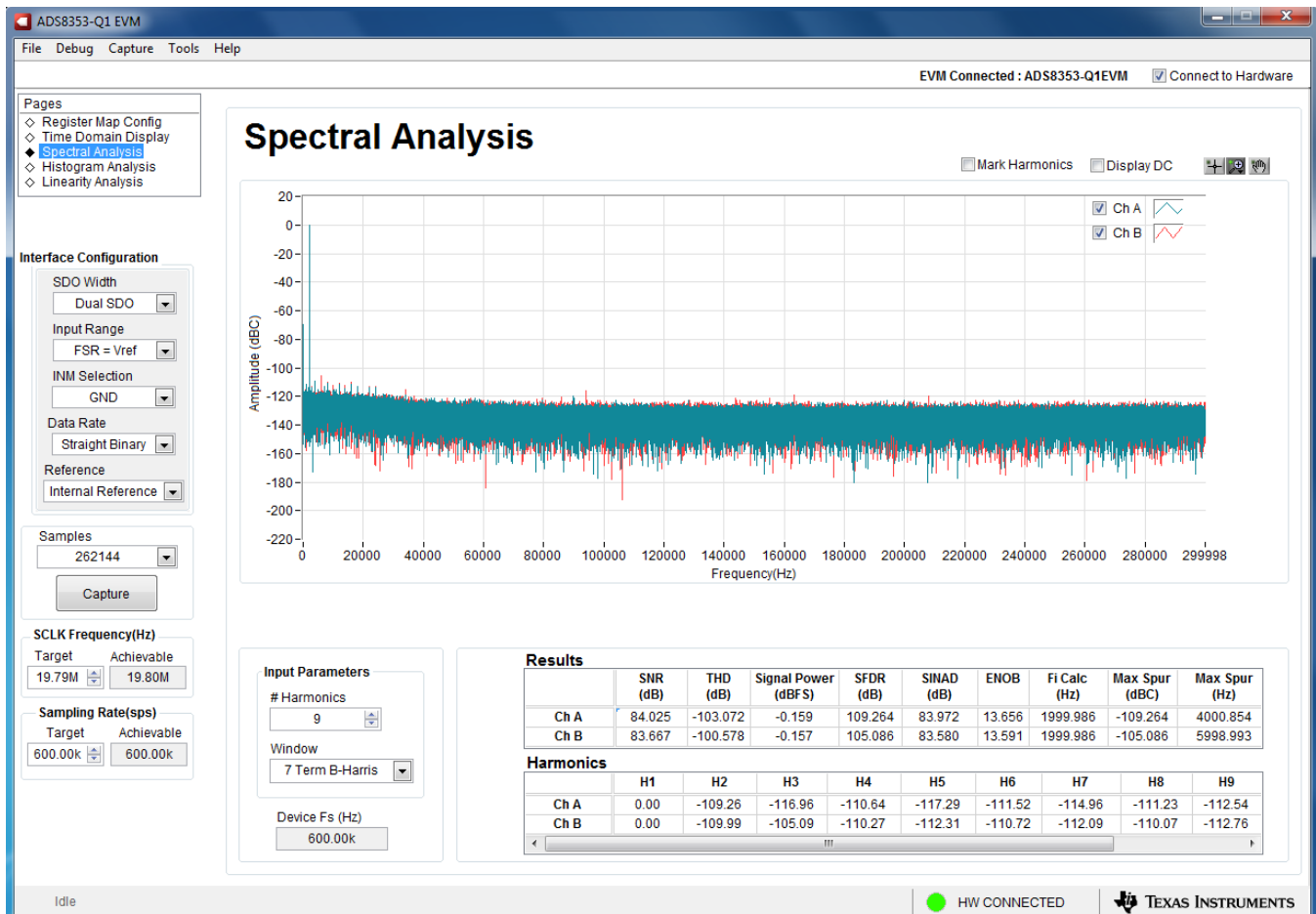


Figure 11. Spectral Analysis Tool

6.4 Histogram Analysis Tool

The *Histogram Analysis* tool can be used to estimate the effective resolution of the ADC resulting from performance degradation caused by noise. Effective resolution is an indicator of the number of bits of ADC measurement resolution resulting from performance losses caused by noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output (from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself) is reflected in the standard deviation of the ADC output code histogram obtained by performing multiple conversions of a DC input applied to a given channel.

The histogram corresponding to a DC input is displayed by clicking the *Capture* button. The example capture shown in [Figure 12](#) is captured with the ADC configured in single-ended, 0 V to 2 × V_{REF} mode and with the AINP pin driven with the V_{REF} input voltage.

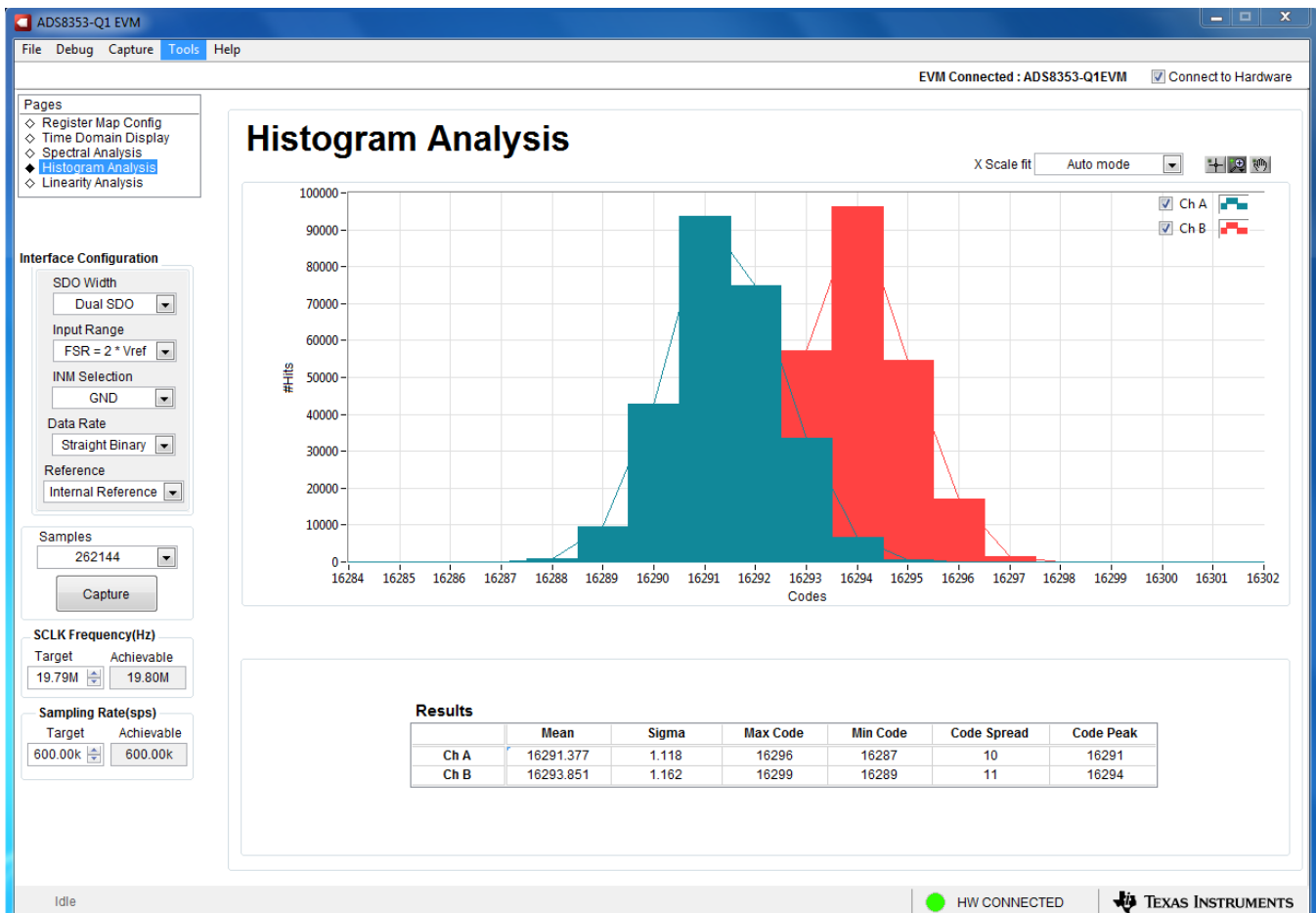


Figure 12. Histogram Analysis Tool

7 Bill of Materials, Printed-Circuit Board Layout, and Schematics

This section contains the ADS8353-Q1EVM bill of materials (BOM), printed-circuit board (PCB) layout, and schematics.

7.1 Bill of Materials

Table 6 lists the ADS8353-Q1EVM BOM.

Table 6. ADS8353-Q1EVM Bill of Materials

Manufacturer Part Number	Quantity	Reference Designators	Manufacturer	Description
DC072	1	PCB	Any	Printed Circuit Board
0603ZC103KAT2A	4	C1, C12, C21, C27	AVX	CAP, CERM, 0.01 uF, 10 V, +/- 10%, X7R, 0603
1891	4	@H1, @H2, @H3, @H4	Keystone	Hex Standoff, #4-40, Aluminum, 1/4"
RM3X4MM 2701	2	@H5, @H6	APM HEXSEAL	Machine Screw Pan PHILLIPS M3
GRM188R71E105KA12D	3	C4, C5, C31	Murata	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603
GRM1885C1H332JA01D	4	C6, C13, C22, C28	Murata	CAP, CERM, 3300 pF, 50 V, +/- 5%, C0G/NP0, 0603
GRM188R71C104KA01D	10	C8, C16, C24, C30, C35, C36, C38, C39, C40, C41	Murata	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0603
GRM21BR71A106KE51L	6	C10, C15, C17, C19, C20, C37	Murata	CAP, CERM, 10 uF, 10 V, +/- 10%, X7R, 0805
GRM1885C1H102FA01J	1	C11	Murata	CAP, CERM, 1000 pF, 50 V, +/- 1%, C0G/NP0, 0603
C3216X5R1E476M160AC	1	C33	TDK	CAP, CERM, 47 uF, 25 V, +/- 20%, X5R, 1206_190
APT2012LZGCK	1	D1	Kingbright	LED, Green, SMD
GRM155R71E104KE14D	2	C19, C38	Murata	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0402
GRM155R61A104KA01D	1	C23	Murata	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X5R, 0402
PMSSS 440 0025 PH	4	H1, H2, H3, H4	B&F Fastener Supply	MACHINE SCREW PAN PHILLIPS 4-40
9774050360R	2	H5, H6	Würth Elektronik	ROUND STANDOFF M3 STEEL 5MM
5-1814832-1	4	J2, J3, J4, J5	TE Connectivity	SMA Straight PCB Socket Die Cast, 50 Ohm, TH
PBC03SAAN	2	J6, J7	Sullins Connector Solutions	Header, 100mil, 3x1, Gold, TH
QTH-030-01-L-D-A	1	J4	Samtec	Header(Shrouded), 19.7mil, 30x2, Gold, SMT
HTSW-102-07-G-S	7	JP1, JP2, JP3, JP4, JP5, JP6, JP7	Samtec	Header, 100mil, 2x1, Gold, TH
RMCF0603ZT0R00	8	R1, R5, R14, R16, R17, R23, R27, R36	Stackpole Electronics Inc	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
ERJ-3EKF49R9V	4	R2, R7, R24, R31	Panasonic	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
ERJ-3GEY0R00V	10	R10, R18, R20, R37, R39, R41, R45, R58, R62, R65	Panasonic	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603
RT0603BRD071KL	4	R4, R9, R22, R29	Yageo America	RES, 1.00 k, 0.1%, 0.1 W, 0603
RT0603BRD07100KL	2	R12, R26	Yageo America	RES, 100 k, 0.1%, 0.1 W, 0603
RMCF0603FT10K0	6	R13, R15, R34, R35, R55, R68	Stackpole Electronics Inc	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
CRCW06035R11FKEA	1	R30	Vishay-Dale	RES, 5.11, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
ERJ-3RSFR10V	1	R60	Panasonic	RES, 0.1, 1%, 0.1 W, 0603
881545-2	1	SH-J1	TE Connectivity	Shunt, 100mil, Gold plated, Black
5015	1	TP1, TP2, TP3, TP4, TP13	Keystone	Test Point, Miniature, SMT
5016	1	TP5, TP17, TP18, TP19, TP20	Keystone	Test Point, Compact, SMT
ADS8353QPWRQ1	1	U1	Texas Instruments	SAR ADC, Dual, 600 kSPS, 16 Bit, Simultaneous Sampling ADC
OPA320AQBVRQ1	3	U2, U3, U4	Texas Instruments	Automotive Qualified Precision, Zero-Crossover, 20MHz, 0.9pA Ib, RRIO, CMOS Operational Amplifier, DBV0005A (SOT-23-5)
BR24G32FVT-3AGE2	1	U6	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8

Table 6. ADS8353-Q1EVM Bill of Materials (continued)

Manufacturer Part Number	Quantity	Reference Designators	Manufacturer	Description
TPS7A4701QRGWTQ1	1	U7	Texas Instruments	Automotive 35V, 1A, 4.2μVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)
0603ZC103KAT2A	0	C2, C14, C23, C29	AVX	CAP, CERM, 0.01 uF, 10 V, +/- 10%, X7R, 0603
06035A101FAT2A	0	C3, C9, C18, C26	AVX	CAP, CERM, 100 pF, 50 V, +/- 1%, C0G/NP0, 0603
GRM1885C1H332JA01D	0	C7, C25	Murata	CAP, CERM, 3300 pF, 50 V, +/- 5%, C0G/NP0, 0603
0805ZC105KAT2A	0	C32	AVX	CAP, CERM, 1 uF, 10 V, +/- 10%, X7R, 0805
GRM21BR71A106KE51L	0	C34	Murata	CAP, CERM, 10 uF, 10 V, +/- 10%, X7R, 0805
102-1092-BL-00100	0	H5	CnC Tech	Cable, USB-A to micro USB-B, 1 m
RT0603BRD071KL	0	R3, R6, R21, R28	Yageo America	RES, 1.00 k, 0.1%, 0.1 W, 0603
RC0603FR-07100RL	0	R8, R25	Yageo America	RES, 100, 1%, 0.1 W, 0603
RMCF0603ZT0R00	0	R11, R32, R38, R40, R42, R43	Stackpole Electronics Inc	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
RT0603BRD07100KL	0	R19	Yageo America	RES, 100 k, 0.1%, 0.1 W, 0603
CRCW06031K00FKEA	0	R59	Vishay-Dale	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
ERJ-3RQFR22V	0	R61	Panasonic	RES, 0.22, 1%, 0.1 W, 0603
ERJ-3GEY0R00V	0	R63, R64, R66, R67	Panasonic	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603
OPA320AQDBVRQ1	0	U5, U9, U10	Texas Instruments	Automotive Qualified Precision, Zero-Crossover, 20MHz, 0.9pA Ib, RRIO, CMOS Operational Amplifier, DBV0005A (SOT-23-5)
REF3425IDBVR	0	U8	Texas Instruments	2.5V Low-Drift Low-Power Small-Footprint Series Voltage Reference, DBV0006A (SOT-23-6)

7.2 PCB Layout

Figure 13 through Figure 16 show the EVM PCB layout.

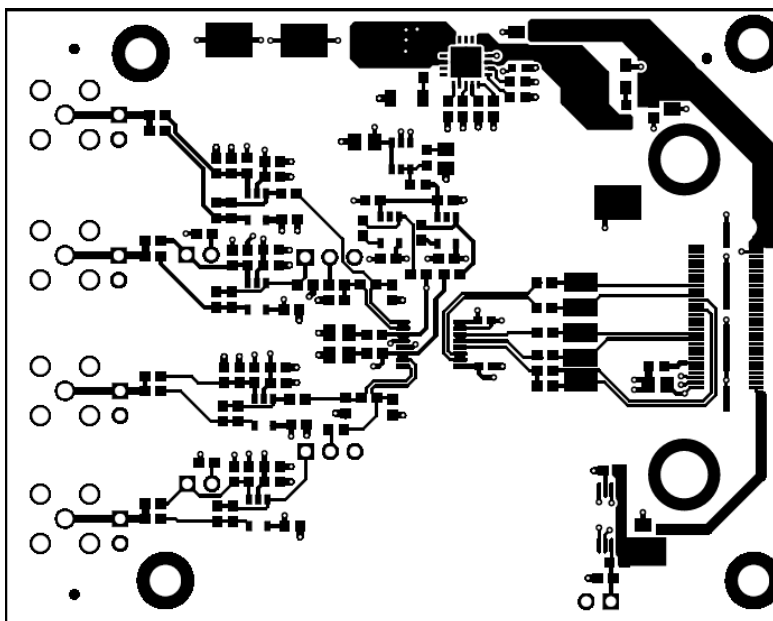


Figure 13. ADS8353-Q1EVM PCB Layer 1: Top Layer

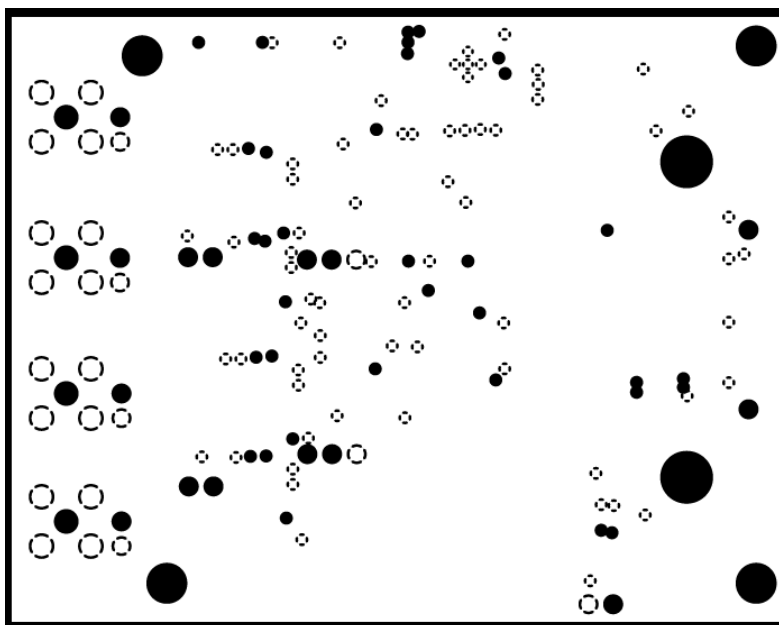


Figure 14. ADS8353-Q1EVM PCB Layer 2: GND Plane

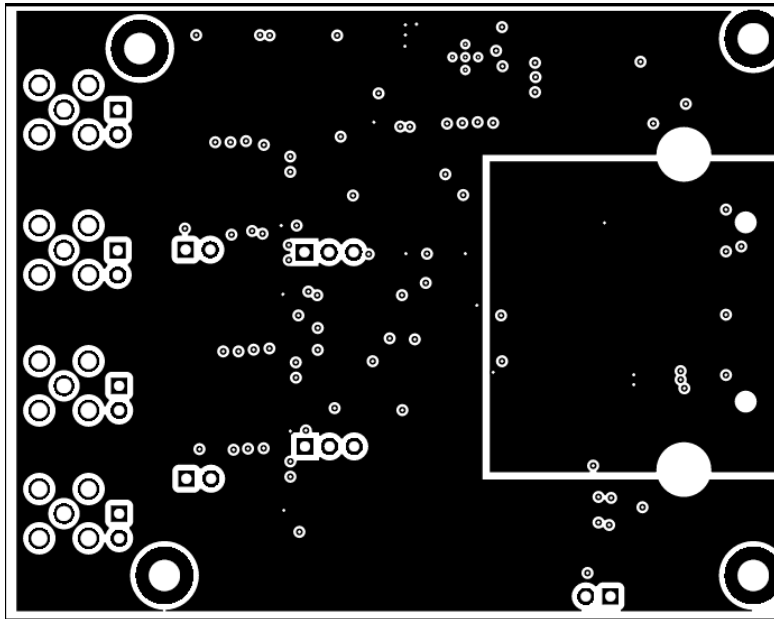


Figure 15. ADS8353-Q1EVM PCB Layer 3: Power Planes

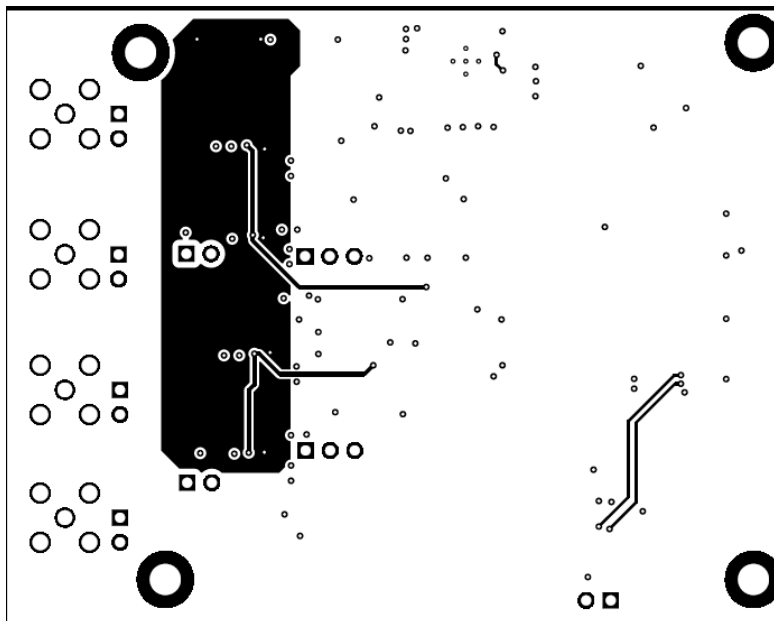


Figure 16. ADS8353-Q1EVM PCB Layer 4: Bottom Layer

7.3 Schematics

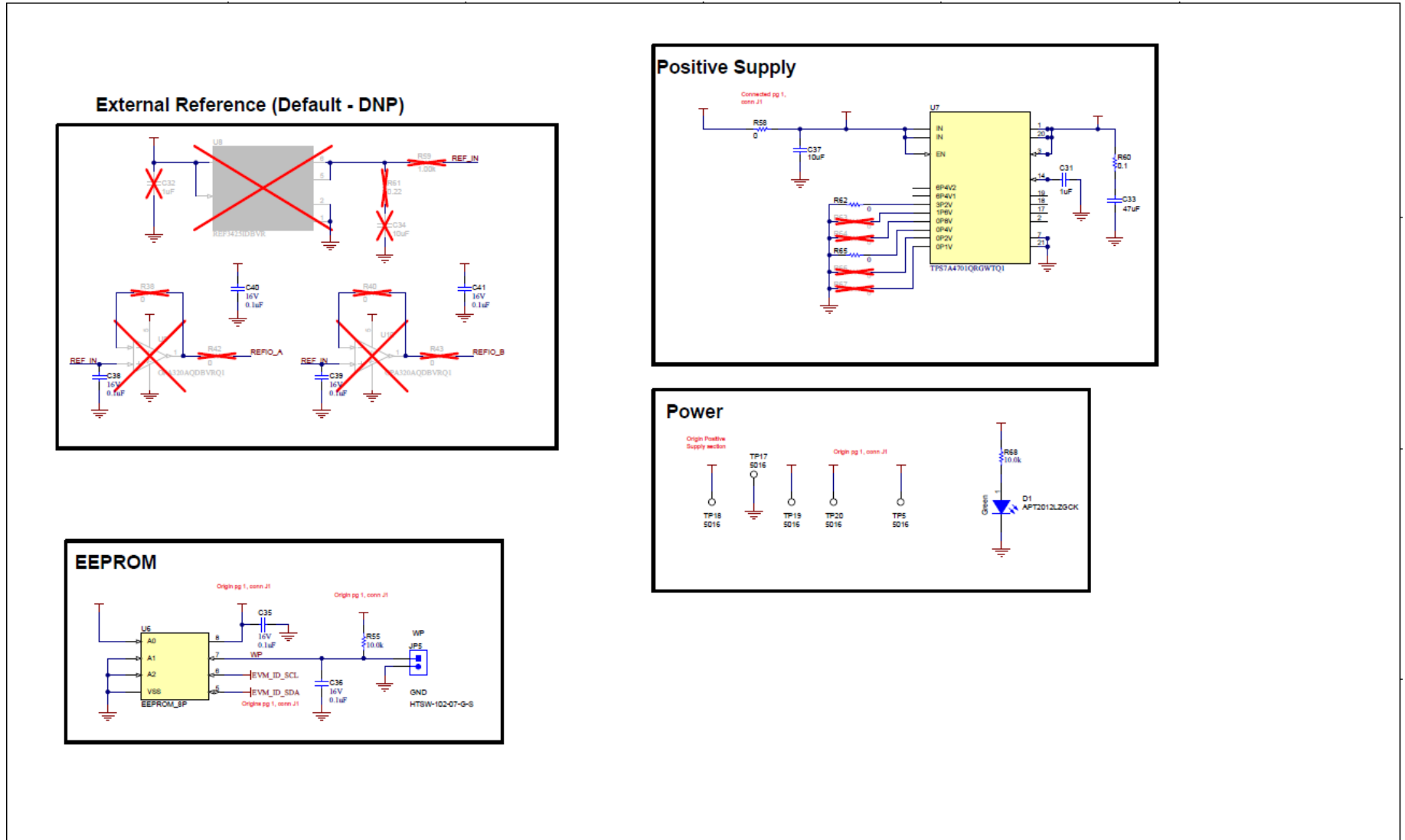


Figure 17. Schematic Diagram (Page 1) of the ADS8353-Q1EVM PCB

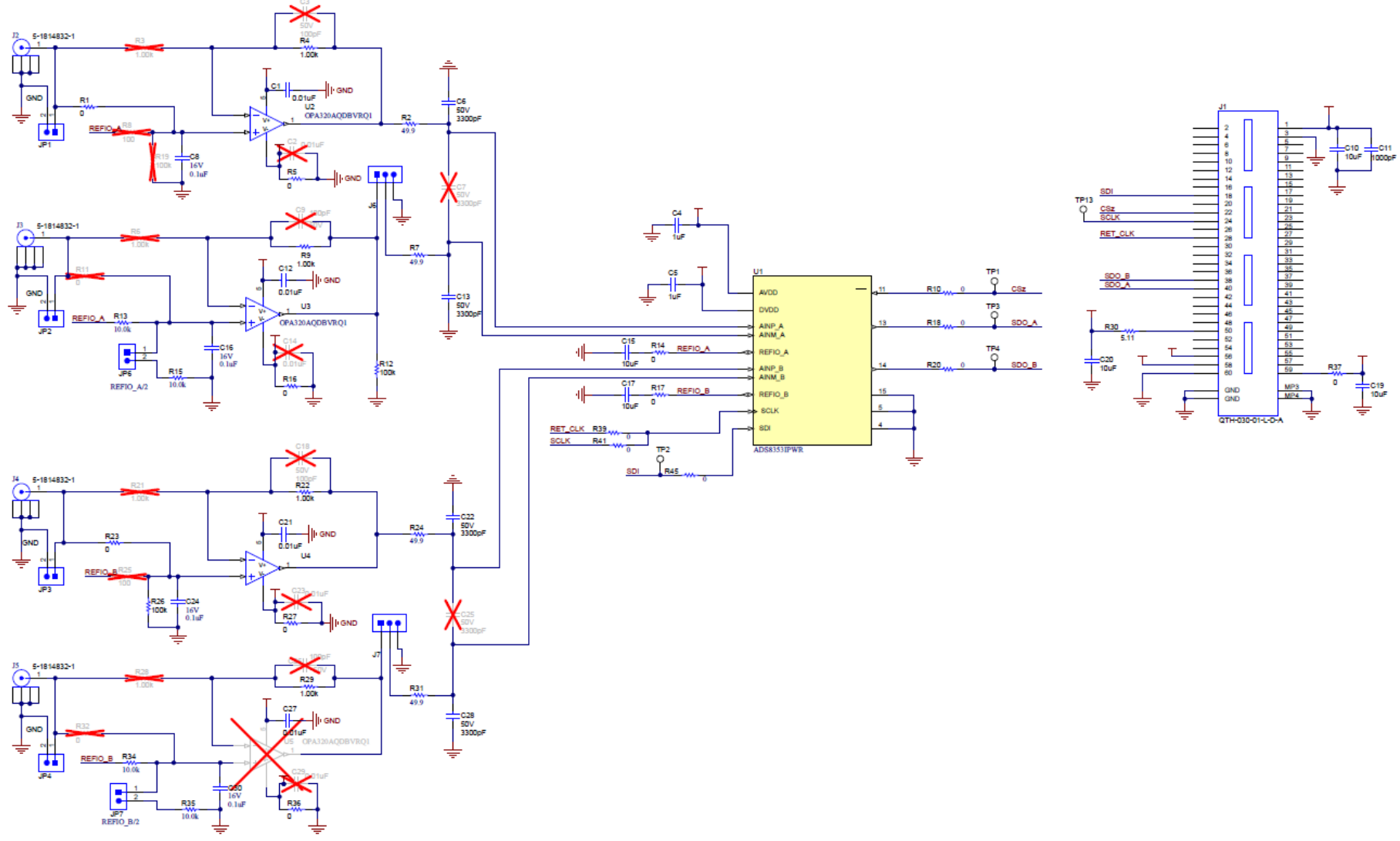
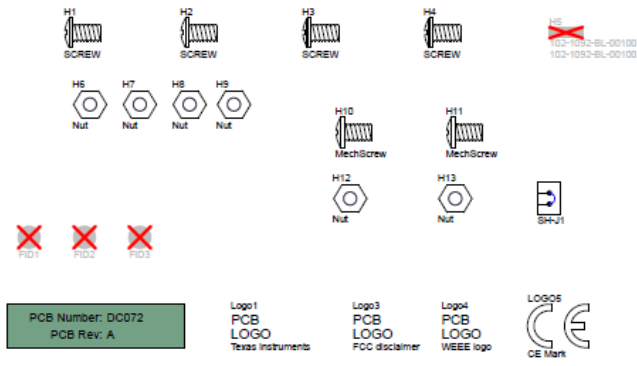


Figure 18. Schematic Diagram (Page 2) of the ADS8353-Q1EVM PCB



BL1
PCB Label
THP-14-423-16
Size: 0.65" x 0.20"

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

Variant/Label Table	
Variant	Label Text
001	ADS8353Q1EVM-PDK

ZZ2
Assembly Note
These assemblies are ESD sensitive. ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Figure 19. Schematic Diagram (Page 3) of the ADS8353-Q1EVM PCB

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1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
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 - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
2. *Limited Warranty and Related Remedies/Disclaimers:*
 - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
 - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.
 - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.
3. *Regulatory Notices:*
 - 3.1 *United States*
 - 3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.
 - 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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西新宿三井ビル

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3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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