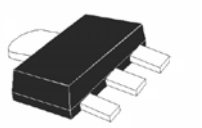
START499D

NPN RF silicon transistor

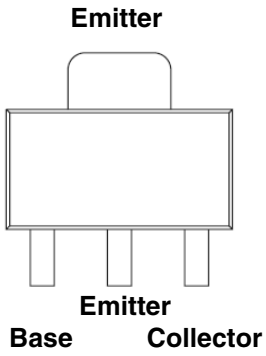
Features

- High efficiency
- Common emitter configuration
- Broadband performances P_{OUT} = 29 dBm with 14 dB gain @ 900 MHz
- Plastic package
- Linear and non linear operation
- Supplied in tape and reel
- In compliance with the 2002/95/EC european directive



SOT-89

Figure 1. Pin connection



Description

The START499D provide the market with a Si state-of-art RF process. Manufactured with ST 3rd generation bipolar process, it offers the highest power, gain and efficiency in SOT-89 for given breakdown voltage (BVCEo). START499D is suitable for a wide range of application up to 1 GHz.

Obsolete Product(s) - Obsolete Product(s)

Table 1. Device summary

Order code	Marking	Package	Packaging
START499D	D499	SOT-89	Tape and reel

Contents

1 **Electrical data** 3
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1.2 Thermal data 3

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7 **Revision history** 17

Obsolete Product(s) - Obsolete Product(s)

1 Electrical data

1.1 Maximum ratings

Table 2. Absolute maximum ratings (T_{CASE} = +25 °C)

Symbol	Parameter	Value	Unit
V_{CEO}	Collector - emitter voltage	4.5	V
V_{EBO}	Emitter - base voltage	1.5	V
I_C	Collectorcurrent	1.0	A
P_{DISS}	Power dissipation	1.7	W
T_J	Max. operating junction temperature	150	°C
T_{STG}	Storage temperature	-65 to +150	°C

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	75	°C/W

Obsolete Product(s) - Obsolete Product(s)

2 Electrical characteristics

2.1 Static

Table 4. Static T_{CASE} = +25 °C

Symbol	Test conditions	Min.	Typ.	Max.	Unit
I_{CBO}	V_{CB} = 15 V			5	µA
I_{EBO}	V_{EB} = 1.2 V			250	µA
BV_{CES}	I_C = 200 µA	15	20		V
h_{FE}	V_{CE} = 3 V I_C = 0.16 A		150		

2.2 Dynamic

Table 5. Dynamic

Symbol	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	V_{CC} = 3.6 V, I_{CQ} = 30 mA, P_{IN} = 15 dBm, f = 900 MHz	28	29		dBm
G_P		13	14		dB
h_D		55	65		%
Load mismatch	V_{CC} = 3.6 V, I_{CQ} = 30 mA, P_{OUT} = 28 dBm, f = 900 MHz All phase angles	3:1			VSWR

Obsolete Product(s) - Obsolete Product(s)

3 Impedance

Figure 2. Current conventions

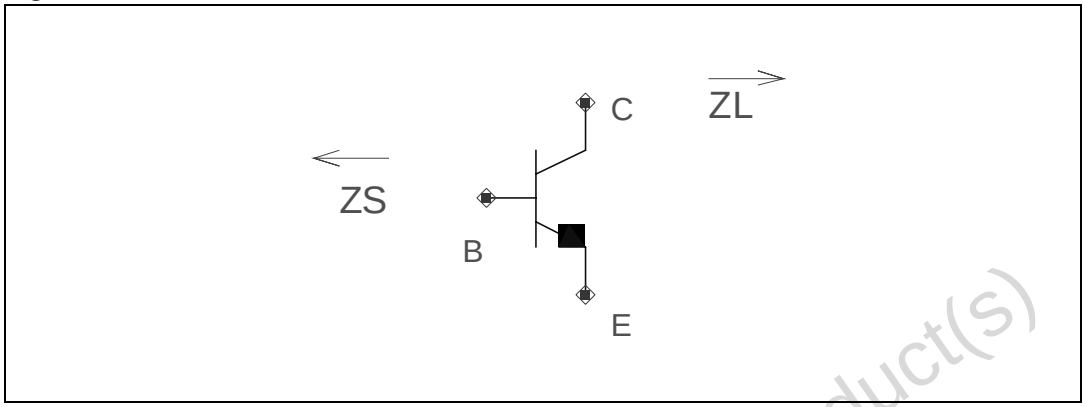


Table 6. Impedance data

Frequency (MHz)	Z_{BS} (Ω)	Z_{CL}(Ω)
800	16.58 - j4.04	17.95 - j5.49
820	15.81 - j3.81	16.28 - j5.11
840	15.04 - j3.53	14.77 - j4.67
860	14.31 - j3.21	13.44 - j4.15
880	13.61 - j2.83	12.25 - j3.54
900	12.93 - j2.44	11.19 - j2.90
920	12.27 - j2.01	10.24 - j2.22
940	11.66 - j1.53	9.40 - j1.52
960	11.06 - j1.04	8.65 - j0.81
980	10.52 - j0.54	7.99 - j0.11
1000	9.98 + j0.02	7.38 + j0.62

Obsolete Product(s) - Obsolete Product(s)

4 Typical performance

Figure 3. DC output characterisitics

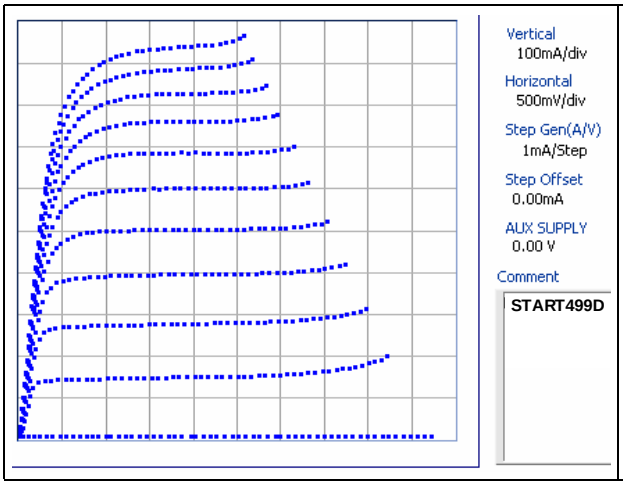


Figure 4. BVEBO

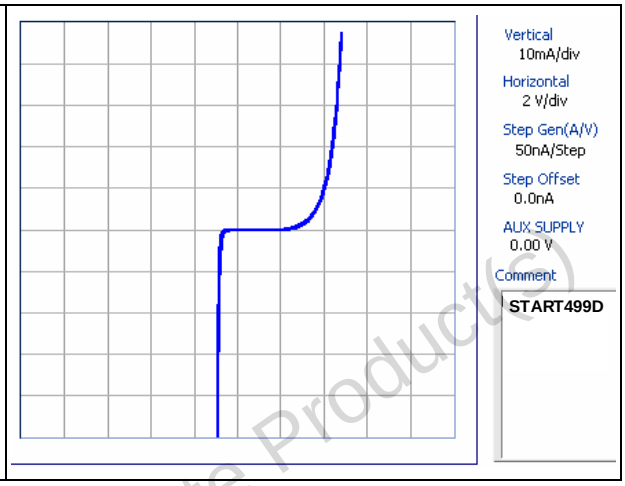
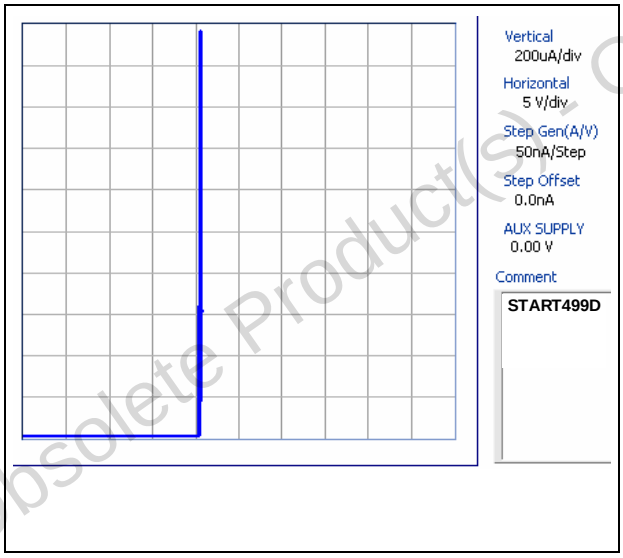


Figure 5. BVCES



Obsolete Product(s) - Obsolete Product(s)

Figure 6. Gain vs frequency

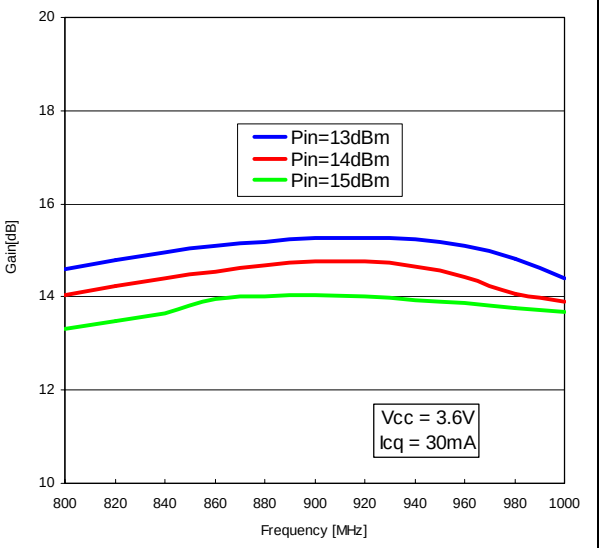


Figure 7. Efficiency vs frequency

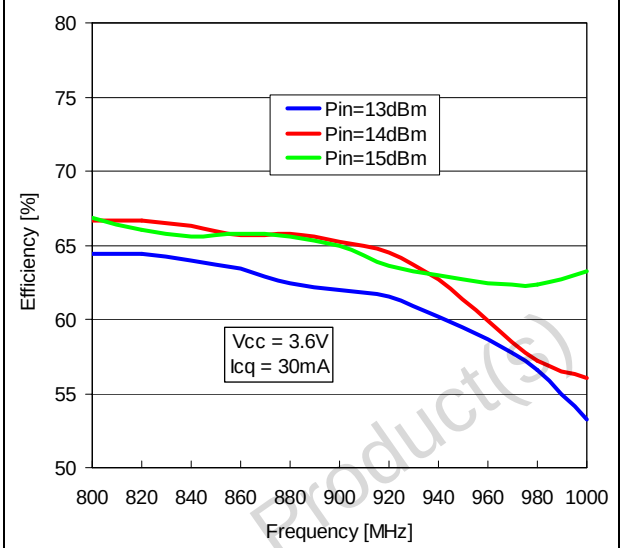


Figure 8. Gain and efficiency vs frequency

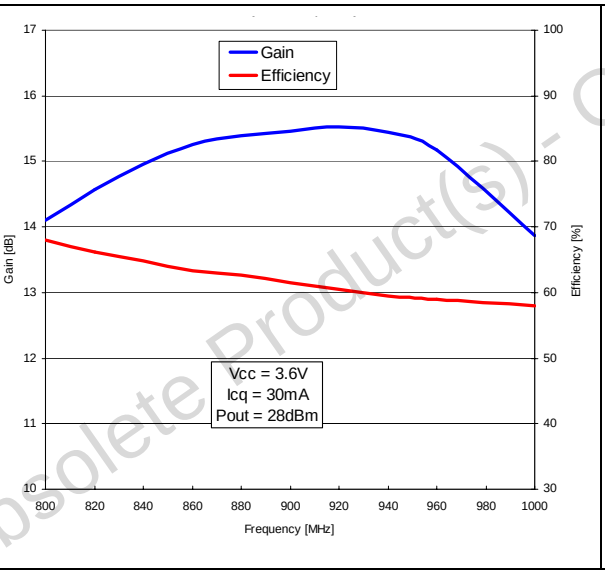
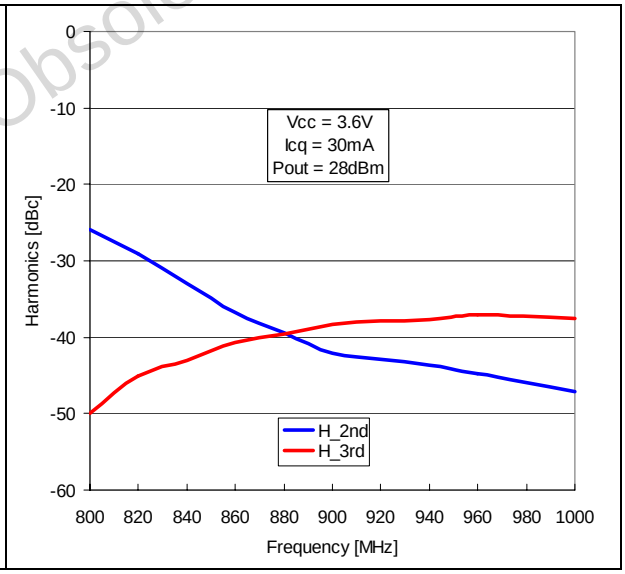


Figure 9. Harmonics vs frequency



Obsolete Product(s) - Obsolete Product(s)

Figure 10. Input return loss vs frequency

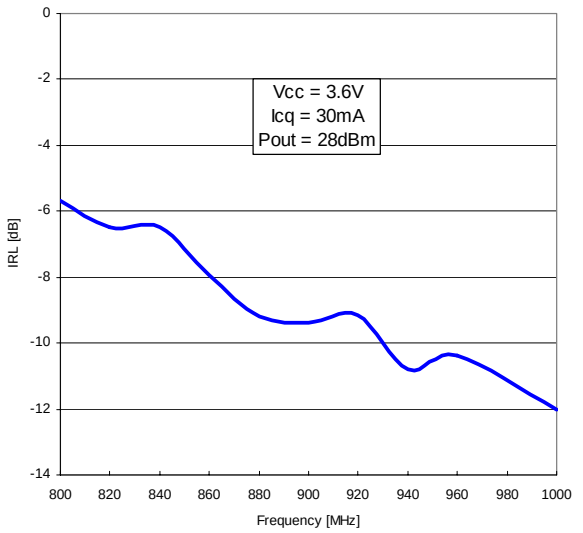


Figure 11. Gain vs output power

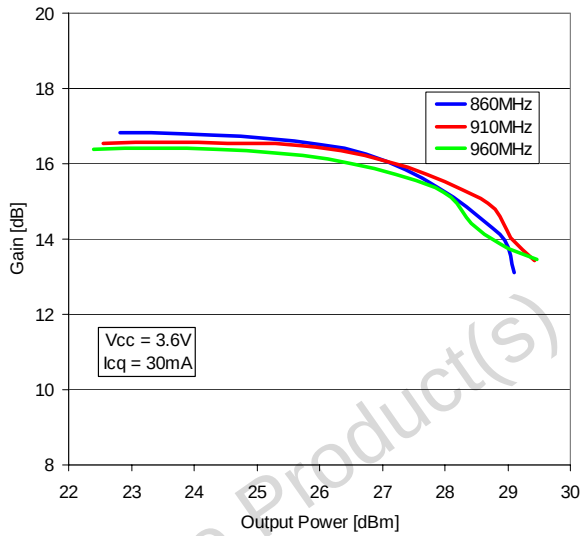


Figure 12. Efficiency vs output power

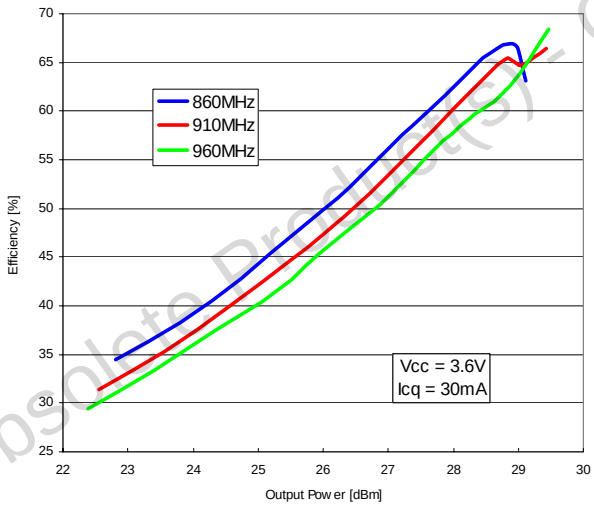
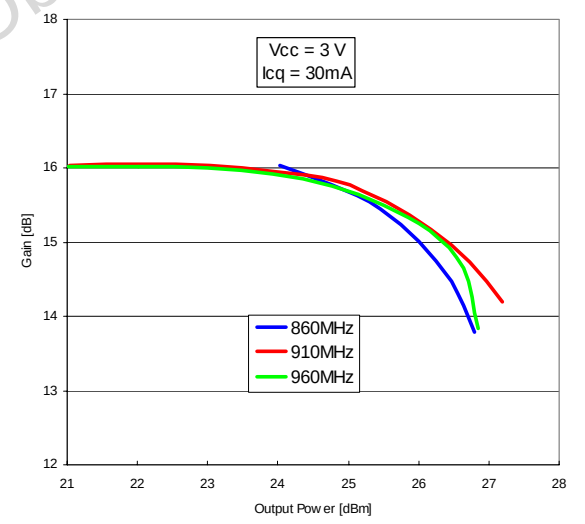


Figure 13. Gain vs output power



Obsolete Product(s) - Obsolete Product(s)

Figure 14. Efficiency vs output power

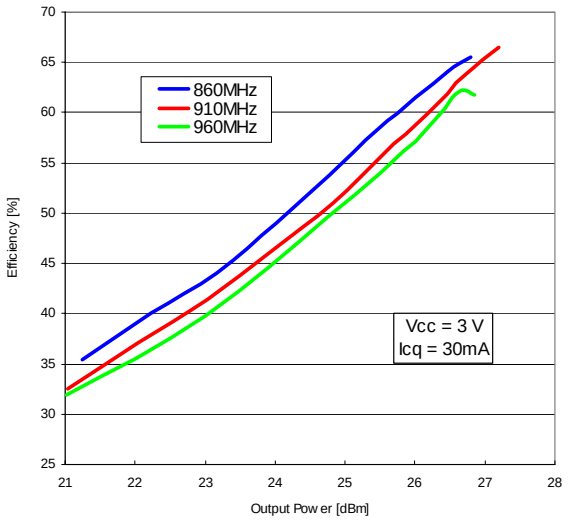


Figure 15. Gain vs output power

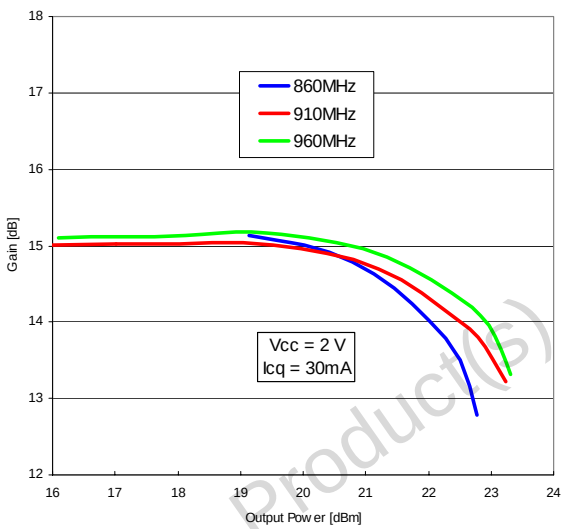
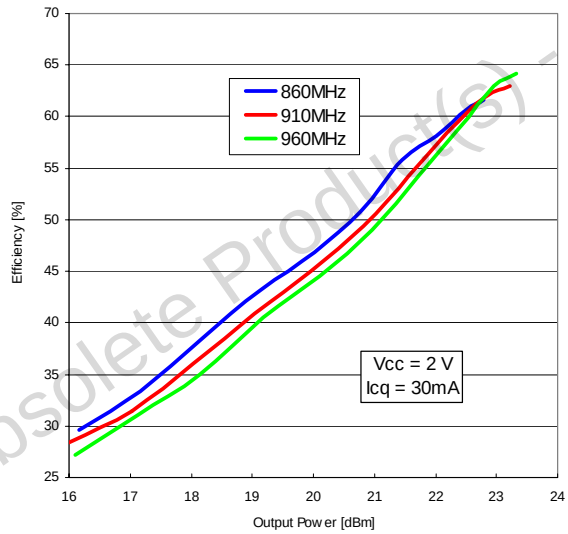


Figure 16. Efficiency vs output power



Obsolete Product(s) - Obsolete Product(s)

5 Test circuit, part list and photo

Figure 17. Test circuit schematic

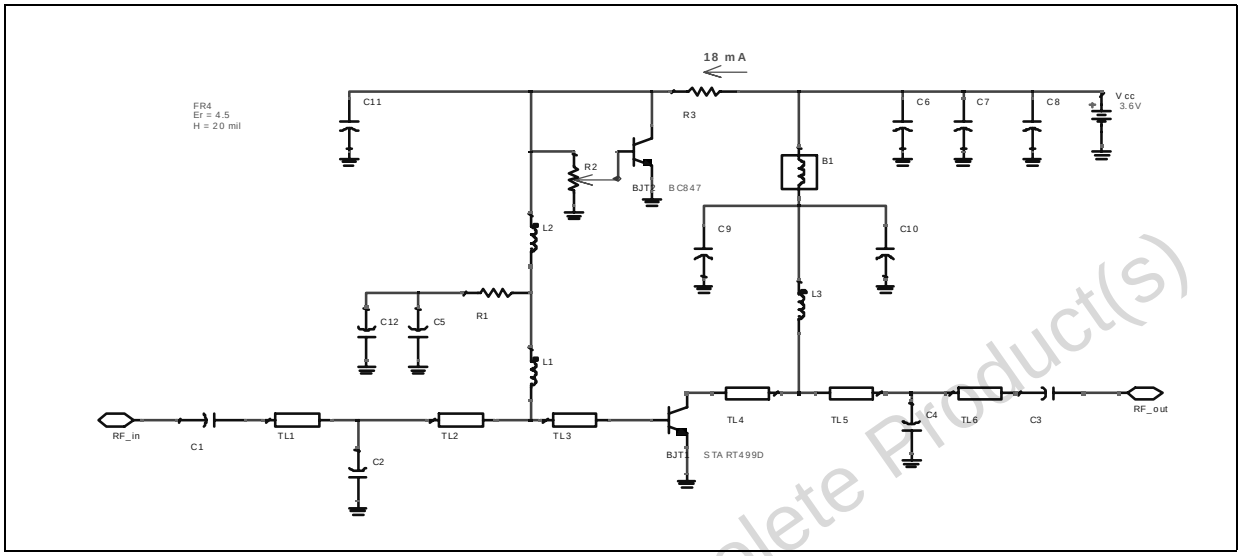


Table 7. Components part list

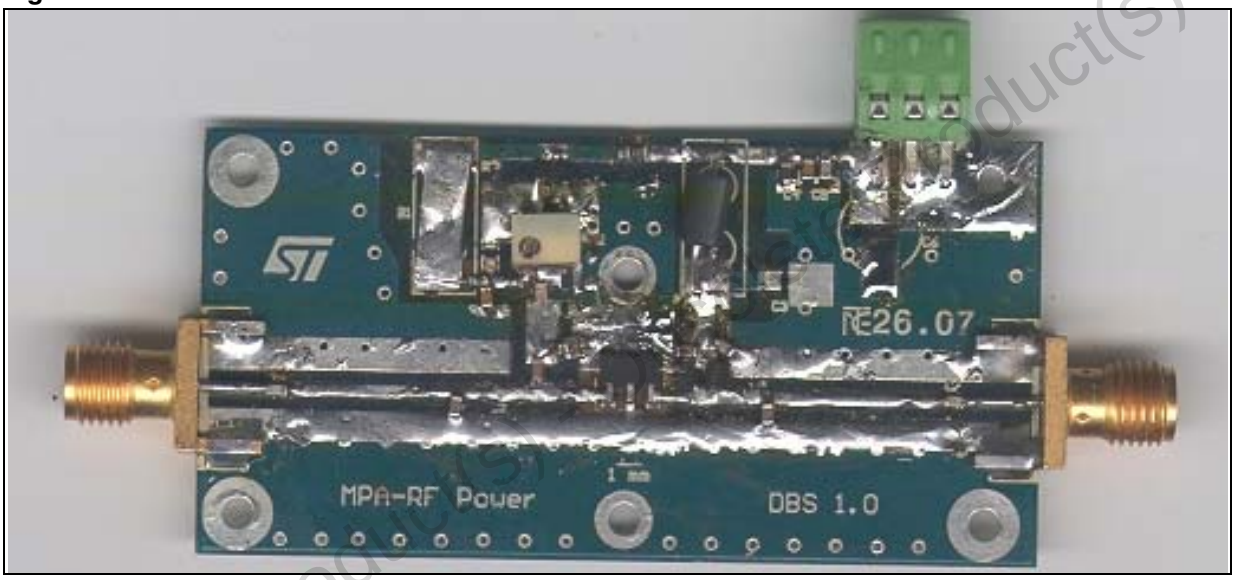
Component ID	Description	Value	Case size	Manufacturer	Part code
C1,C3,C5,C9	Capacitor	100 pF	1608	Murata	GRM1885C1H101JA01
C2	Capacitor	5.6 pF	1608	Murata	GRM1885C1HR50CZ01
C4	Capacitor	6.8 pF	1608	Murata	GRM1885C1H6R8CZ01
C6,C10,C11	Capacitor	1 nF	1608	Murata	GRM1885C1H102JA01
C7	Capacitor	10 nF	1608	Murata	GRM188R71H103KA01
C8	Capacitor	1 uF	1608	Murata	GRM188R71H105KA01
L1	Inductor	11 nH	1608	Coilcraft	0603CS-11NXGB
L2	Inductor	100 nH	1608	Coilcraft	0603CS-R10XGB
L3	Inductor	5.4 nH	2012	Coilcraft	0906-5JLB
B1	Ferrite bead			Panasonic	EXCELDRC35C
R1	Resister	30 ohm	1608		1608 chip resister (0.063 W, ±5 %)
R3	Resister	180 ohm	1608		
R2	Potentiometer	10 KΩ		Bourns electronics	3214W-1-103E
TL1	Transmission line	L=11.9 mm	W=0.9 mm		
TL2	Transmission line	L=5.0 mm	W=0.9 mm		
TL3	Transmission line	L=5.2 mm	W=0.9 mm		

Obsolete Product(s) - Obsolete Product(s)

Table 7. Components part list (continued)

Component ID	Description	Value	Case size	Manufacturer	Part code
TL4	Transmission line	L=3.5 mm	W=0.9 mm		
TL5	Transmission line	L=2.8 mm	W=0.9 mm		
TL6	Transmission line	L=12.2 mm	W=0.9 mm		
BJT2	BJT			STMicroelectronics	BC847
BJT1	BJT			STMicroelectronics	START499D
Board	FR4 Er=4.5 THk=0.020" 1OZ Cu both sides				

Figure 18. Photo



Obsolete Product(s) - Obsolete Product(s)

6 Package mechanical data

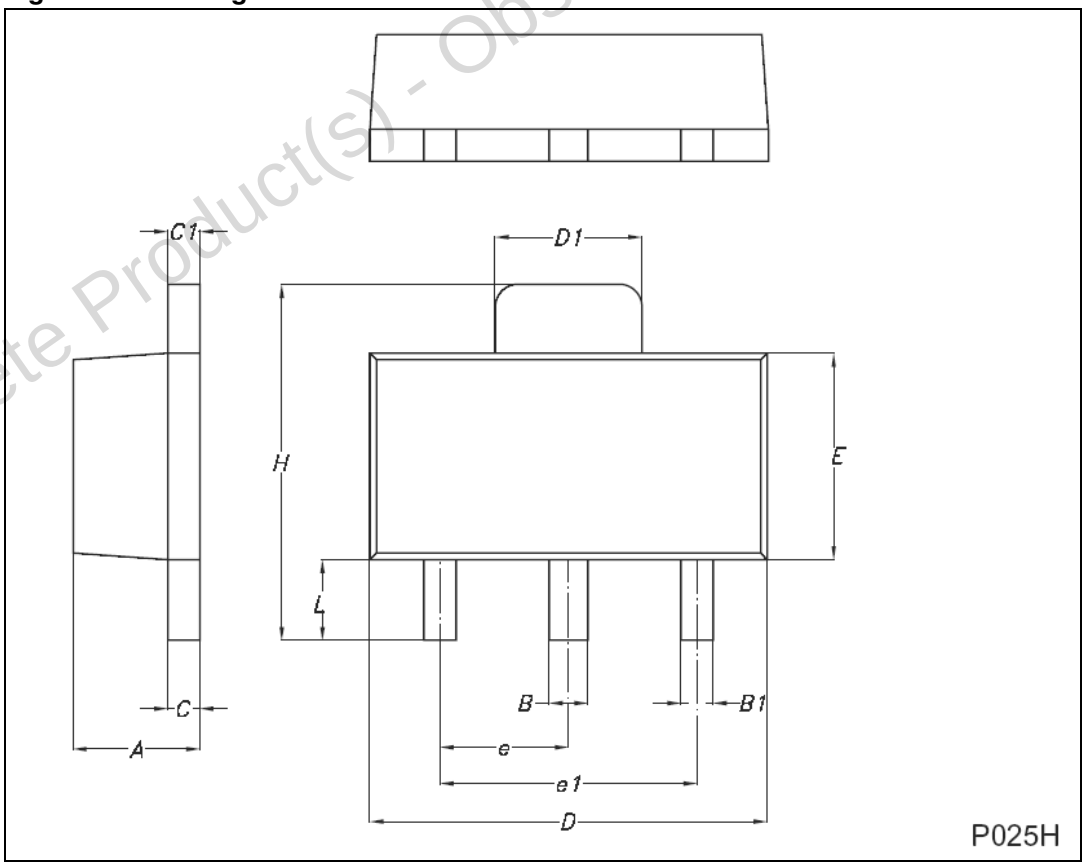
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Obsolete Product(s) - Obsolete Product(s)

Table 8. SOT-89 mechanical data

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	1.4		1.6	55.1		63.0
B	0.44		0.56	17.3		22.0
B1	0.36		0.48	14.2		18.9
C	0.35		0.44	13.8		17.3
C1	0.35		0.44	13.8		17.3
D	4.4		4.6	173.2		181.1
D1	1.62		1.83	63.8		72.0
E	2.40		2.6	94.5		102.4
e	1.42		1.57	55.9		61.8
e1	2.92		3.07	115.0		120.9
H	3.94		4.25	155.1		167.3
L	0.89		1.2	35.0		47.2

Figure 19. Package dimensions



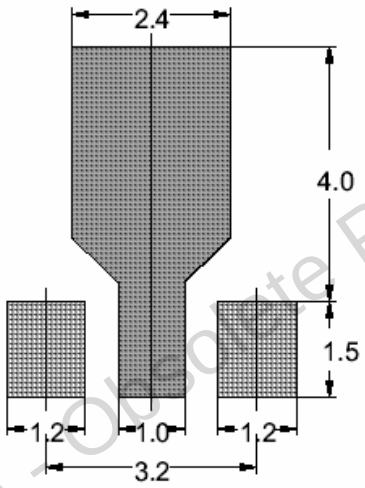
Obsolete Product(s) - Obsolete Product(s)

6.1 Thermal pad and via design

Thernal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device.

The via pattern is based on thru-hole vias with 0.203 mm to 0.330 mm finished hole size on a 0.5 mm to 1.2 mm grid pattern with 0.025 plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

Figure 20. Pad layout details



SOT-89 pattern.
Minimum Pad Size (dimensions in mm)

Obsolete Product(s) - Obsolete Product(s)

6.2 Soldering profile

Figure 21 shows the recommeded solder for devices that have Pb-free terminal plating and where a Pb-free solder is used.

Figure 21. Recommended solder profile

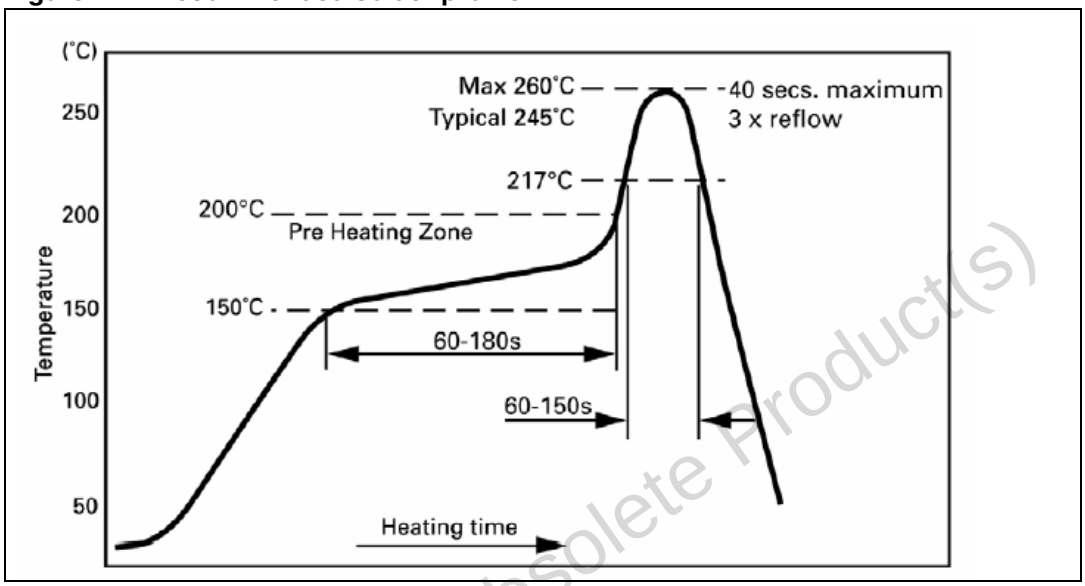
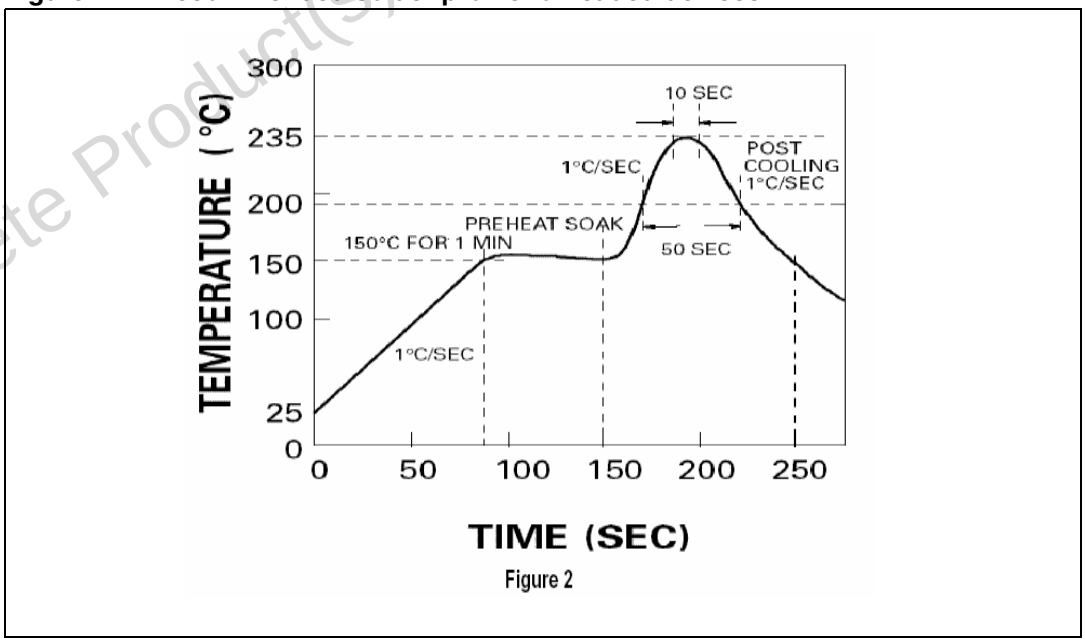


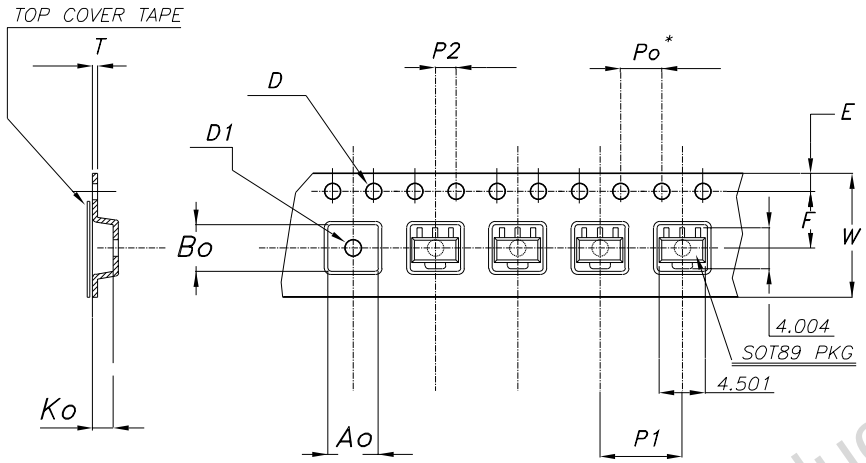
Figure 22 shows the recommeded solder for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 22. Recommended solder profile for leaded devices



Obsolete Product(s) - Obsolete Product(s)

Figure 23. Reel information



Ao	4.91	±0.10
Bo	4.52	±0.10
Ko	1.90	±0.10
F	5.50	±0.10
E	1.75	±0.10
W	12	±0.30
P2	2	±0.10
Po	4	±0.10
P1	8	±0.10
T	0.30	±0.10
D	ø1.55	±0.05
D1	ø1.60	±0.10

NOTES :

– ACCEPTANCE SPEC. Nr. 0031932

* – CUMULATIVE TOLERANCE OF 10 SPROCKET HOLES IS ±0.20

– UNLESS OTHERWISE SPECIFIED TOLERANCE: ±0.10

– MATERIAL CODE : 3CP90069

Obsolete Product(s) - Obsolete Product(s)

7 Revision history

Table 9. Document revision history

Date	Revision	Changes
03-Mar-2008	1	Initial release.
15-Jul-2008	2	Updated *Table 1 on page 1*.
17-Jul-2008	3	Values update on *Table 4 on page 4*.
29-Jun-2010	4	Updated *Table 8 on page 13*.

Obsolete Product(s) - Obsolete Product(s)

Obsolete Product(s) - Obsolete Product(s)

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