TPS75005EVM-023

This user's guide describes the characteristics, operation, and use of the TPS75005EVM-023 evaluation module (EVM). The TPS75005EVM-023 is a reference design for engineering demonstration and evaluation of the TPS75005 dual low-dropout linear regulator (LDO) and triple voltage rail monitor from Texas Instruments. This user's guide includes setup and configuration instructions, a complete schematic diagram, bill of materials (BOM), and printed circuit board (PCB) layouts for the evaluation module. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the TPS75005EVM-023 unless otherwise noted.

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1 Introduction

The TPS75005EVM-023 helps design engineers evaluate the operation and performance of the TPS75005 for possible use in their own circuit applications. The TPS75005 is optimized to be a complete power management solution for Texas Instruments' C2000™ real-time microcontrollers and other DSP/FPGA/ASIC MCUs. The device contains dual, 500-mA LDOs. Each LDO output is monitored by an internal supervisor (SVS) circuit to determine the Power Good (PG) signal. A third supervisor allows the customer to independently monitor an additional external voltage. On this EVM, the third SVS monitor is preset by a resistor divider to monitor an external 2.5-V power rail. The two power outputs are enabled and disabled by a single EN logic input. Sequence and soft-start circuitry provide a means to program the start-up characteristics and to ensure well-behaved output ramp-up.

This document describes the configuration and setup of the TPS75005EVM-023 board.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS75005EVM-023.

2.1 Input / Output Connector Descriptions

J1: EXT SVS

This connector is the input to the voltage monitoring function (VMON) of the TPS75005. When the voltage at this header drops below approximately 2.35 V, the VDET output drops to logic low. The VDET output can be measured at TP1.

J2: VIN

This connector is the input power-supply voltage connector. The positive input lead and ground return lead from the input power supply should be twisted and kept as short as possible to minimize electromagnetic interference (EMI) transmission.

J3: GND

This connector is the return connection for the input power supply. The positive input lead and ground return lead from the input power supply should be twisted and kept as short as possible to minimize EMI.

J4: VOUT2

This connector is the positive output of LDO-2. The LDO-2 output is regulated to 3.3 V.

J5: GND

This connector is the return connection for LDO-2.

J6: VOUT1

This connector is the positive output of LDO-1. The LDO-1 output is regulated to 1.9 V if jumper JP2 is installed, and 1.8 V if jumper JP2 is not installed.

J7: GND

This connector is the return connection for LDO-1.

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2.2 Jumper Description

JP1: EN

This jumper enables or disables the LDO outputs. When the jumper is connected between EN and ON, the power-on sequence is triggered. When it is connected between EN and OFF, the power-down sequence is triggered.

JP2: VSET

This jumper sets the LDO-1 output voltage setting. When the jumper is installed, LDO-1 is set to 1.9 V. When the jumper is not installed, LDO-1 is set to 1.8 V.

JP3: SEQ

This jumper connects the sequence select pin to either logic high or low. When no jumper is installed, the start-up sequence powers up LDO-1 first and LDO-2 second. The shutdown sequence powers down LDO-2 first and then LDO-1. When the jumper is installed, the start-up sequence powers up LDO-2 first and then LDO-1; the shutdown sequence powers down LDO-1 first, followed by LDO-2.

2.3 Test Points

TP1: VDET

This test point is connected to the output of the voltage detector that is monitoring the voltage at the EXT SVS input. When the voltage at EXT SVS drops below approximately 2.35 V, VDET will be logic low. When the voltage at EXT SVS is above approximately 2.4 V, VDET will be logic high. This operates independently of the two LDOs and is not enabled or disabled by EN.

TP2: PG

This test point monitors the voltage at the Power-Good output. When VOUT1 and VOUT2 are both above the respective supervisory threshold voltage for each LDO (V_{SVS1} = 1.88 or 1.78 and V_{SVS2} = 3.26), PG outputs logic high. If either VOUT1 or VOUT2 falls below its supervisory threshold, then PG outputs logic low.

TP3: $\overline{\text{ERR}}$

This test point is connected to the error output. If any error occurs, then $\overline{\text{ERR}}$ drops to logic low. In the absence of errors, $\overline{\text{ERR}}$ stays at logic high. There are three types of errors that trigger $\overline{\text{ERR}}$: thermal shutdown, undervoltage lockout, and current limit.

Thermal Shutdown

Thermal shutdown occurs when the internal junction temperature rises above +160°C. In this case, $\overline{\text{ERR}}$ only returns to logic high when the temperature drops below +140°C.

Undervoltage Lockout (UVLO)

Undervoltage lockout occurs when VIN drops below 3.6 V. While VIN stays below 3.6 V, $\overline{\text{ERR}}$ is at logic low. Once VIN rises above 3.6 V, $\overline{\text{ERR}}$ rises to logic high.

Current Limit

If either LDO output current limits, then an error occurs. The current limit for LDO-1 is between 750 mA to 1150 mA, while the current limit for LDO-2 is between 700 mA and 1000 mA.

NOTE: The name of pin 11 has changed from $\overline{\text{ERR}}$ to TEST on the datasheet.

TP4: VSET

This test point monitors the VSET logic input to the integrated circuit (IC). VSET determines the output voltage of LDO-1. Logic high sets VOUT1 to 1.9 V, and logic low sets VOUT1 to 1.8 V. Installing JP2 increases VSET from logic low to logic high.

TP5: SEQ

This test point is connected to the SEQ input. It is either logic high or low, depending on whether jumper JP3 is installed or not.

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2.4 Other Components

R8

R8 is listed as *not installed* on the schematic and in the bill of materials. It does not need to be installed for the EVM to work properly. Installing a 0-Ω resistor at R8 ties EN to VDET. In this mode, a drop in the EXT SVS voltage, below approximately 2.35 V, disables the LDO-1 and LDO-2 outputs.

WARNING

Uninstall the jumper at JP1 before installing R8. Never have any jumper on JP1 while there is a resistor installed at R8.

C1

A place to install an extra input capacitor is provided at C1. This capacitor is listed as *not installed* on the schematic and in the bill of materials. It does not need to be installed for the EVM to work properly.

C4

C4 programs the delay for the internal SVS-2 of LDO-2.

C5

Programs the soft-start ramp time for LDO-2.

C6

Programs the soft-start ramp time for LDO-1.

C7

C7 programs the delay for the internal SVS-1 of LDO-1.

2.5 Soldering Guidelines

Any solder re-work to modify the EVM for the purpose of repair or other application reasons must be performed using a hot-air system to avoid damaging the IC.

2.6 Equipment Setup

Follow these procedures to properly set up the TPS75005EVM-023 equipment.

- Turn off the input power supply after verifying that its output voltage is set to less than 6.5 V. Connect the positive voltage lead from the input power supply to VIN at the J2 connector of the EVM. Connect the ground lead from the input power supply to GND at the J3 connector of the EVM.
- Turn off the SVS power supply after verifying that its output voltage is set to 2.5 V. Connect the positive voltage lead from the SVS power supply to the EXT SVS input at the J1 connector of the EVM. Connect the ground lead from the SVS power supply to GND at the J3 connector.
- Connect a 0-mA to 500-mA load between the output VOUT1 at connector J6, and GND at connector J7. Connect a 0-mA to 500-mA load between the output VOUT2 at connector J4, and GND at connector J5.

3 Operation

This section provides information about the operation of the TPS75005EVM-023.

3.1 General Operation

- Turn on the input power supply. For initial operation, it is recommended that the input power supply, VIN – J2, be set to 5 V.
- Vary the respective loads and the VIN and EXT SVS voltages as necessary for test purposes.

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4 Test Results

This section provides typical performance waveforms for the TPS75005EVM-023 PCB. These tests were performed with VIN = 5 V.

4.1 Start-Up and Shutdown Sequence

Figure 1 and Figure 2 show the start-up and shutdown sequence, respectively, when JP3 is not installed. If JP3 is installed, then VOUT1 and VOUT2 swap the order in which they turn on and off. For these tests, VIN = 5.0 V, with no load. The start-up ramps of VOUT1 and VOUT2 can be adjusted by modifying C6 and C5, respectively.

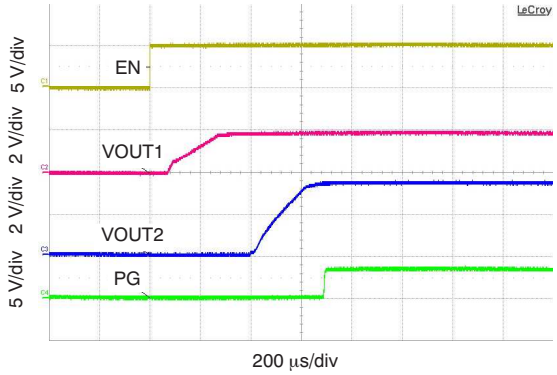

Figure 1. Start-Up Sequence, SEQ Set to Logic Low

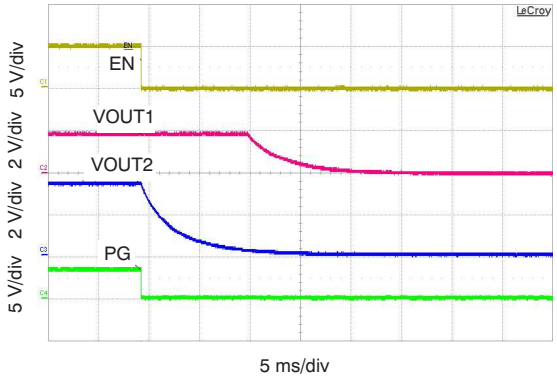

Figure 2. Shutdown Sequence, SEQ Set to Logic Low

4.2 Output Load Transient

Figure 3 and Figure 4 show the load transient responses of LDO-1 and LDO-2, respectively, for a load step from 10 mA to 500 mA. VIN is set at 5.0 V. Figure 3 shows the load transient response at VOUT1 of LDO-1 when VOUT1 is set to 1.8 V. Figure 4 shows the load transient response at VOUT2 of LDO-2.

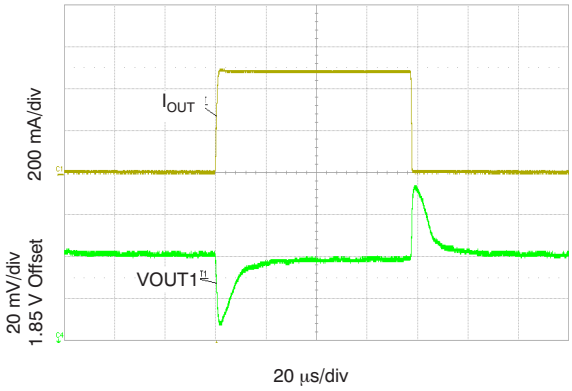

Figure 3. Load Step and Transient Response of LDO-1, VSET Set to Logic Low

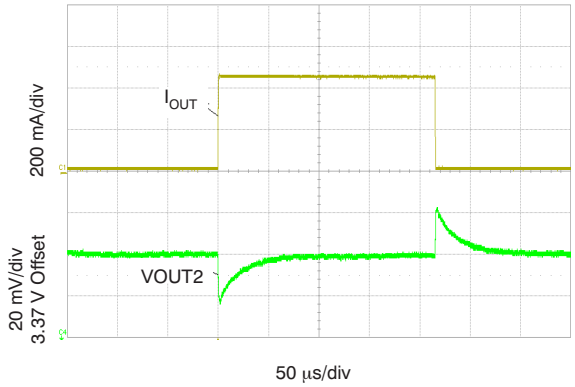

Figure 4. Load Step and Transient Response of LDO-2

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4.3 EXT SVS Voltage Monitor Behavior

Figure 5 shows the VDET output as the EXT SVS input drops below regulation voltage.

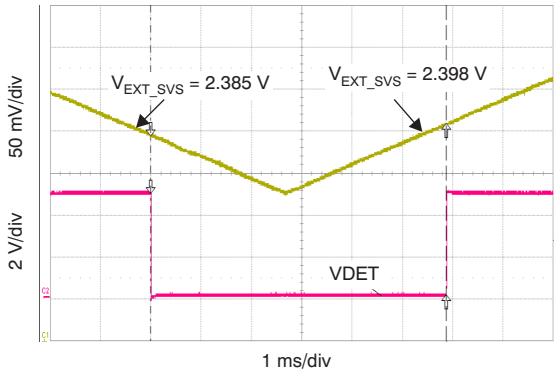

Figure 5. Third Voltage Monitor Behavior (VDET) when EXT SVS Drops Below Regulation

5 Thermal Guidelines and Layout Recommendations

Thermal management is a key component of design of any power converter and is especially important when the power dissipation in the LDO is high. Use the following formula to approximate the maximum power dissipation for a particular ambient temperature:

$$T_J = T_A + P_D \times \theta_{JA}$$

Where T_J is the junction temperature, T_A is the ambient temperature, P_D is the power dissipation in the device (in watts), and θ_{JA} is the thermal resistance from junction to ambient. All temperatures are in degrees Celsius (°C). The absolute maximum silicon junction temperature, T_J, must not be allowed to exceed +150°C. The steady-state maximum of T_J must not exceed +125°C. +125°C is the highest allowable junction temperature at which the TPS75005 can operate for an extended period of time. The layout design must use copper trace and plane areas carefully as thermal sinks (in order to prevent T_J from exceeding the absolute maximum rating under all temperature conditions and voltage conditions across the part).

The designer should carefully consider the thermal design of the PCB for optimal performance over temperature. This EVM employs two copper plane layers as primary spreading layers to sink and spread conducted heat from the TPS75005. Internal layer 1 (shown in Figure 8) is primarily used as a signal/trace layer, but it also contains enough 1-oz copper area to assist with heat dissipation. Internal layer 2 (shown in Figure 9) is an unbroken ground plane (2.3 in by 1.7 in) and thermal spreading layer made of 1-oz copper. The bottom layer (shown in Figure 10) is also a thermal spreading layer, but consists of 2-oz copper.

Table 1 shows the thermal parameters measured in the laboratory for this particular layout. This measurement is made for illustrative purposes only, and should ***not*** be used to replace the more conservative JEDEC-based thermal characteristics found in the TPS75005 product data sheet. The JEDEC model only uses two 1-oz internal spreading planes (3 in by 3 in). Keep in mind that thermal parameters can vary significantly if there is not sufficient copper to act as a heat sink for the part.

Table 1. Approximate Thermal Resistance, θ_{JA}, and Maximum Power Dissipation

Board	Package	θ_{JA}	Max Dissipation without Derating (T_A = +25°C)	Max Dissipation without Derating (T_A = +70°C)
TPS75005EVM-023	RGW	18°C/W	6.944 W	4.444 W

In addition, refer to the Texas Instruments thermal modeling tool, the PCB Thermal Calculator (available at www.ti.com) to calculate the maximum junction temperature for a selectable internal copper spreading area.

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6 Board Layout

This section provides the TPS75005EVM-023 board layout and illustrations.

6.1 Layout

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing TPS75005EVM-023 PCBs.

Figure 6 through Figure 10 show the PCB layouts.

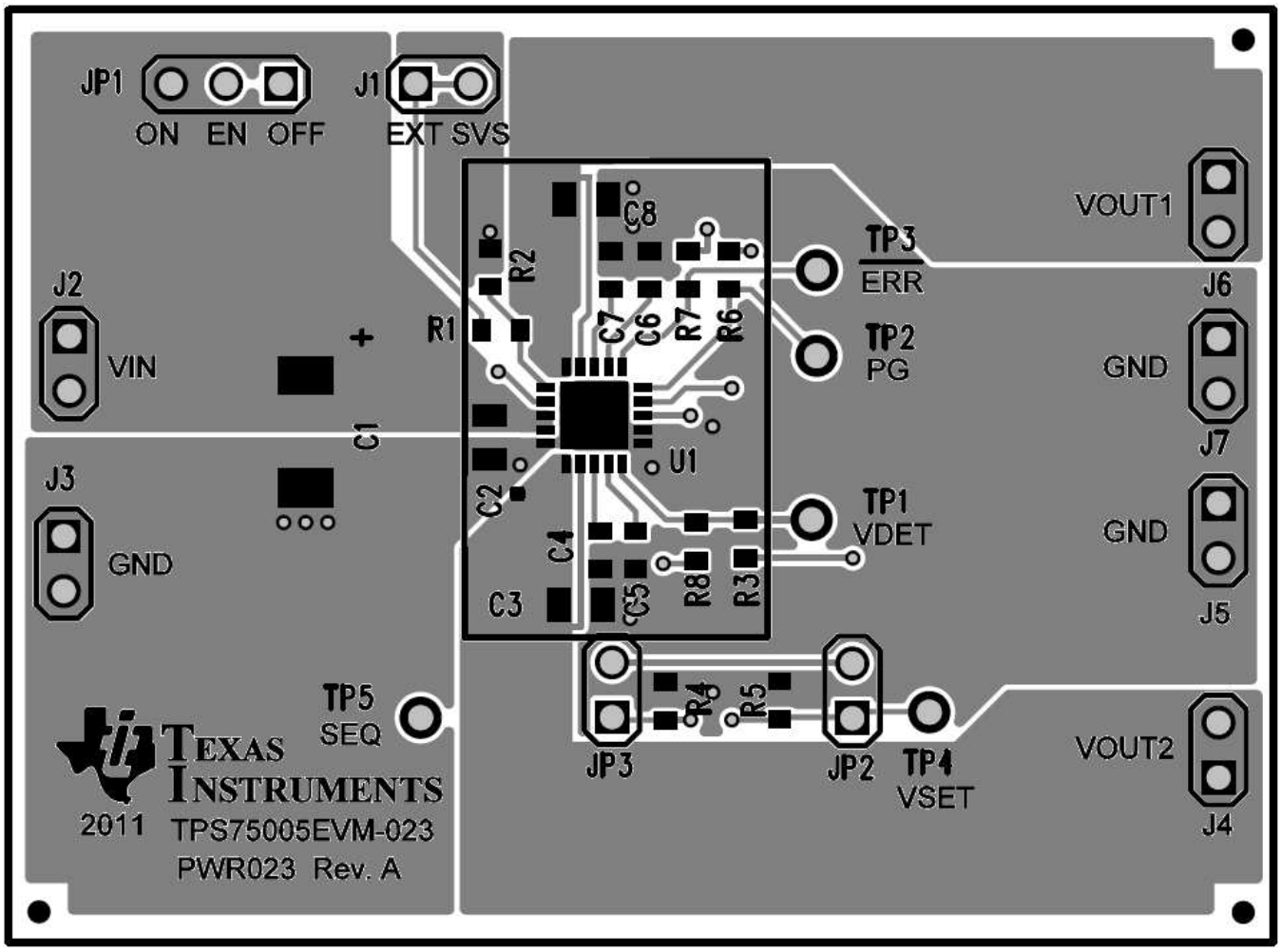

Figure 6. Top Layer with Silk Screen

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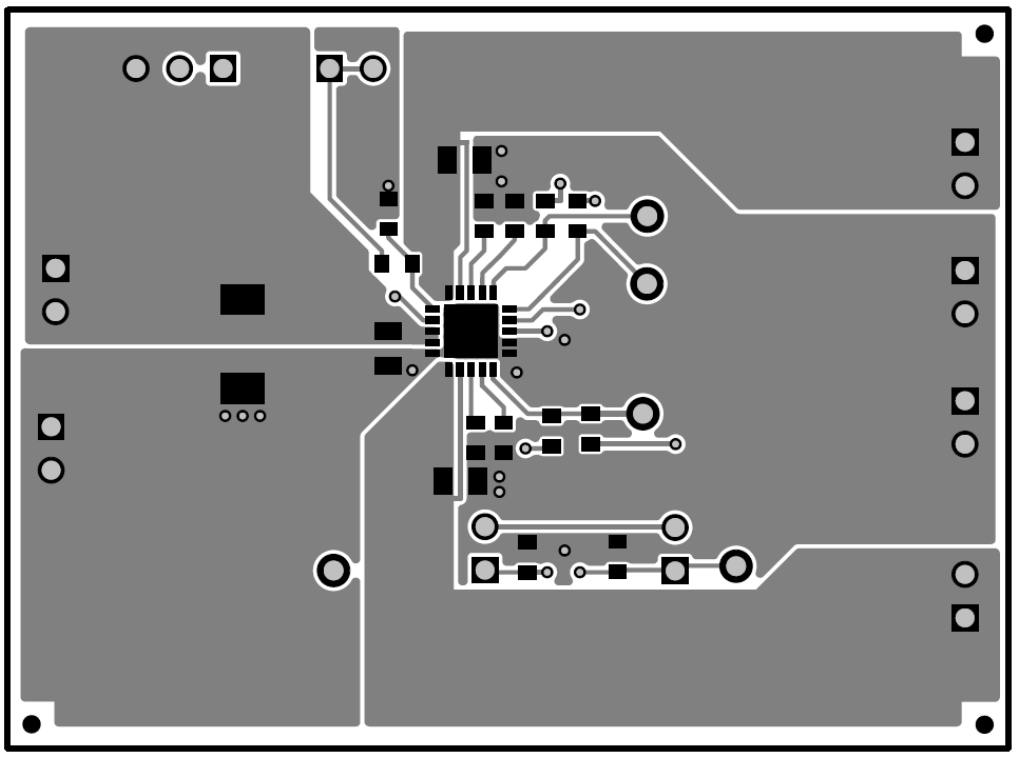

Figure 7. Top Layer

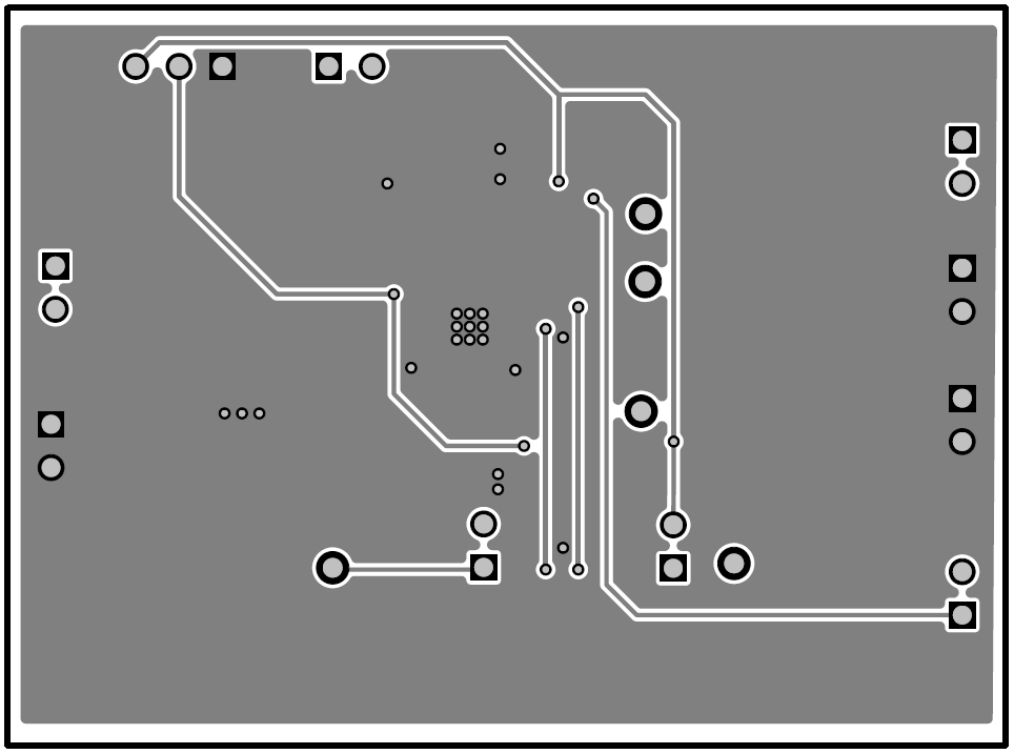

Figure 8. Internal Layer 1

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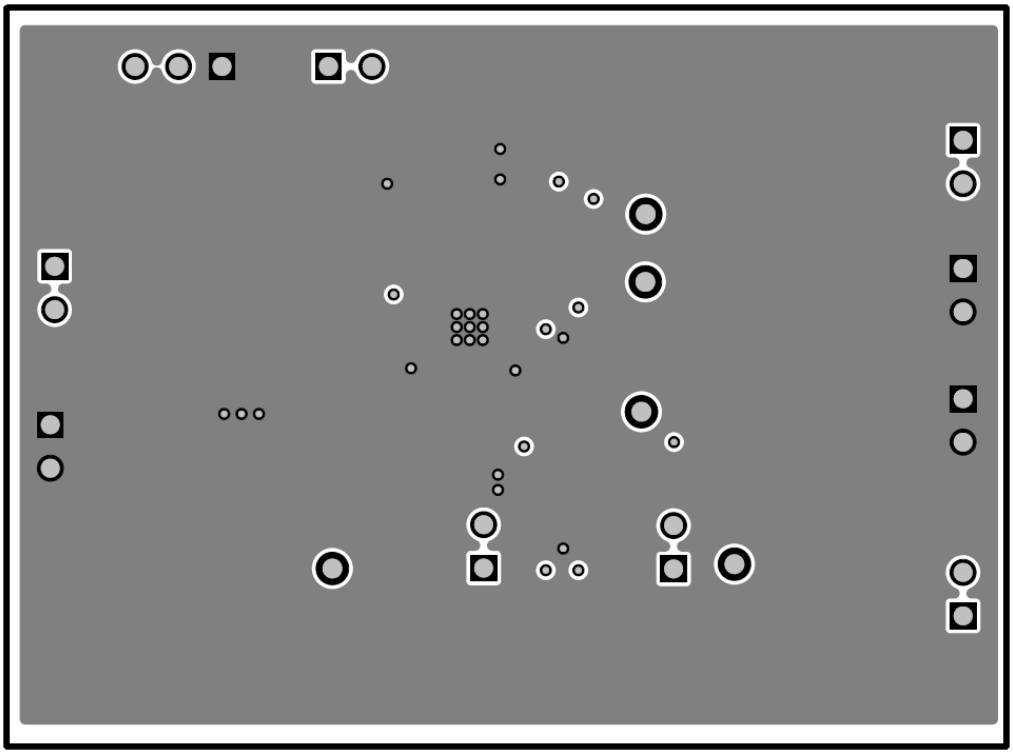

Figure 9. Internal Layer 2

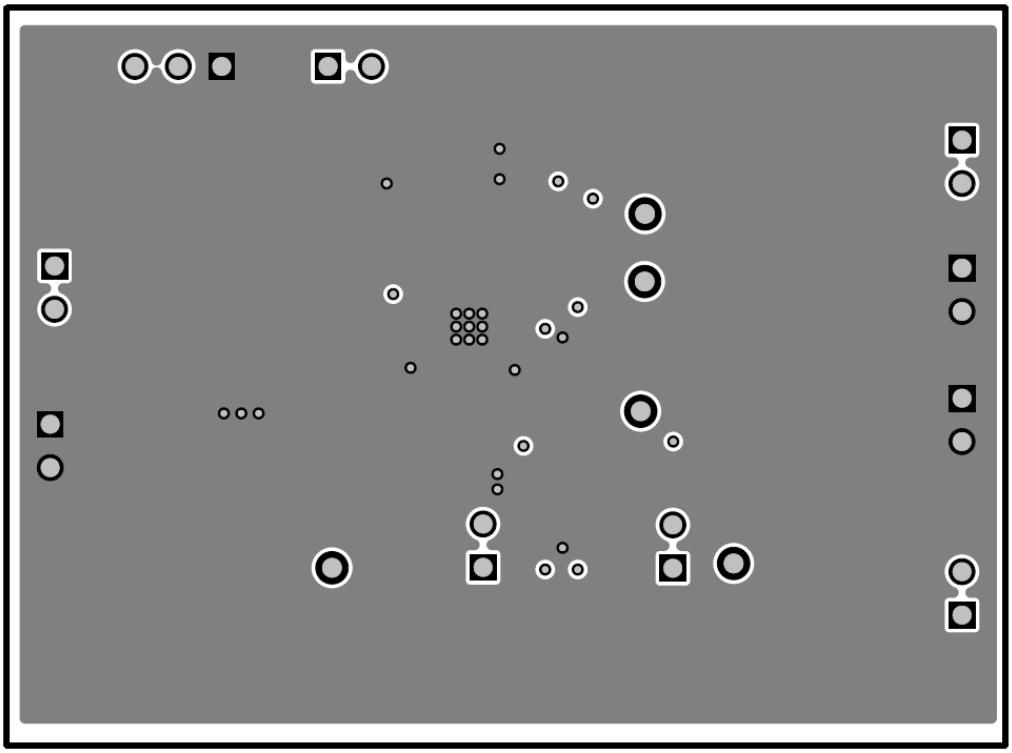

Figure 10. Bottom Layer

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7 Schematic and Bill of Materials

This section provides the TPS75005EVM-023 bill of materials and schematic.

7.1 Schematic

The schematic for this EVM is shown in Figure 11.

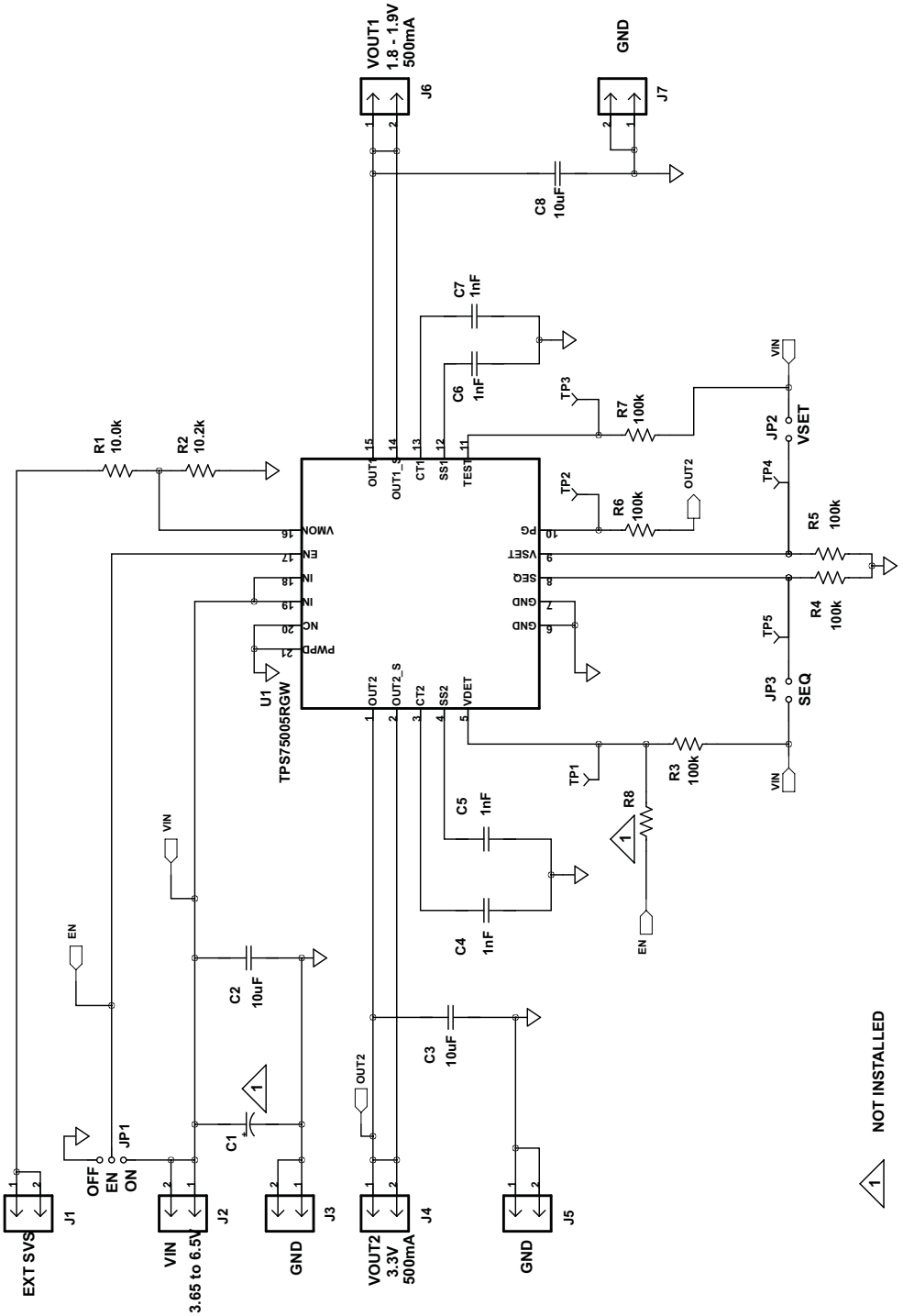

Figure 11. TPS75005EVM-023 Schematic

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7.2 Parts List

Table 2 lists the bill of materials for the TPS75005EVM.

Table 2. TPS75005EVM Bill of Materials[(1)(2)(3)]

Count	RefDes	Value	Description	Size	Part Number	MFR
0	C1	Open	Capacitor, tantalum, 10 V, 20%	6032	Std	Std
3	C2, C3, C8	10 µF	Capacitor, ceramic, 10 V, X5R, 20%	0805	Std	Std
4	C4 to C7	1 nF	Capacitor, ceramic, 10 V, X5R, 10%	0603	Std	Std
7	J1 to J7	PEC02SAAN	Header, male 2-pin, 100-mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
1	JP1	PEC03SAAN	Header, male 3-pin, 100-mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
2	JP2-3	PEC02SAAN	Header, male 2-pin, 100-mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
1	R1	10.0 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R2	10.2 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
5	R3 to R7	100 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
0	R8	Open	Resistor, chip, 1/16W, 1%	0603	Std	Std
5	TP1 to TP5	5000	Test point, red, through-hole color keyed	0.100 x 0.100 inch	5000	Keystone
1	U1	TPS75005RGW	IC, dual 500-mA LDO and Triple voltage rail monitor	QFN-20	TPS75005RGW	TI
3	--		Shunt, 100-mil, black	0.100	929950-00	3M
1	--		PCB, 1.7 in x 2.3 in x 0.062 in		PWR023	Any

(1) These assemblies are ESD sensitive. ESD precautions shall be observed.
(2) These assemblies must be clean and free from flux and all contaminants. Use of *no-clean flux* is not acceptable.
(3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 3.65 V to 6.5 V and the output voltage range of 0 V to 1.9 V for VOUT1 and 0 V to 3.3 V for VOUT2 (fixed outputs).

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +95°C. The EVM is designed to operate properly with certain components above +95°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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