TEXAS INSTRUMENTS

SLVP182

High Accuracy Synchronous Buck DC/DC Converter EVM

User's Guide

February 2001

Power Management Products

SLVU046

Preface

About This Manual

This user's guide describes the SLVP182 synchronous buck converter evaluation module.

How to Use This Manual

- ❑ Chapter 1—Introduction
- ❑ Chapter 2—Design Procedure
- ❑ Chapter 3—Test Results

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation

1) Texas Instruments application report *Designing With The TL5001 PWM Controller* (literature number SLVA034A)

2) Texas Instruments data sheet TL5002 (literature number SLVS304)

3) Texas Instruments data sheet TL5001 (literature number SLVS84E)

4) Abraham I. Pressman, *Switching Power Supply Design*, second edition, McGraw Hill

Contents

1 Introduction 1-1
1.1 Hardware 1-2
1.2 Operating Specifications 1-2
1.3 SLVP182 Schematic 1-3
1.4 SLVP182 Bill of Material 1-4
1.5 EVM Board Layout 1-5

2 Design Procedures 2-1
2.1 Duty Cycle Estimate 2-2
2.2 Output Filter 2-2
2.2.1 Inductor Value 2-2
2.2.2 Capacitor Value 2-2
2.3 Power Switch 2-3
2.4 Output Voltage 2-3
2.5 Controller Functions 2-4
2.5.1 Oscillator Frequency 2-4
2.5.2 Dead Time Control 2-4
2.5.3 Softstart Timing 2-4
2.6 Loop Compensation 2-4

3 Test Results 3-1
3.1 Test Setup 3-2
3.2 Test Results 3-3

Figures

1–1 Typical Synchronous Buck Converter 1-2
1–2 Schematic Diagram 1-3
1–3 Top Silk Screen With Top Copper Layer 1-5
1–4 Bottom Silk Screen With Bottom Copper Layer 1-6
1–5 Top Layer Copper 1-6
1–6 Bottom Layer Copper 1-6
1–7 Layer 2 (Internal) Copper 1-7
1–8 Layer 3 (Internal) Copper 1-7
2–1 Power Stage Gain 2-5
2–2 Power Stage Phase 2-6
2–3 Compensation Circuit 2-6
2–4 Compensation Gain 2-8
2–5 Compensation Phase 2-9
2–6 Overall Loop Gain Response 2-9
2–7 Overall Loop Phase Response 2-10
3–1 Test Setup 3-2
3–2 Efficiency Graph 3-3
3–3 Line Regulation (With JP1 = Short, T_A = 25°C) 3-3
3–4 Line Regulation (With JP1 = Open, T_A = 25°C) 3-4
3–5 Load Regulation (V_I = 5 V, T_A = 25°C) 3-4
3–6 Output Voltage Deviation in Terms of Temperature 3-5
3–7 Output Voltage Deviation in Terms of Temperature 3-5
3–8 Output Voltage Deviation in Terms of Temperature 3-6
3–9 Output Voltage Deviation in Terms of Temperature 3-6
3–10 V_O (Upper Trace) and I_O (2A/div) at Full/No Loads Transient Response 3-7
3–11 Output Voltage (Upper Trace, V_O, and Phase Voltage, V_{phase} 3-7
3–12 EVM Start-Up, Input Voltage (Upper Trace) and Output Voltage 3-8
3–13 The Measured Overall Closed Loop Response (V_I = 5 V, V_O = 18 V, I_O = 7 A) 3-8

Tables

1–1 Operating Specifications 1-2
1–2 SLVP182B Bill of Materials 1-4

Chapter 1

Introduction

The SLVP182 synchronous buck converter evaluation module (SLVP182) provides a reference design for evaluating the performance of a high accuracy power supply using the TL5002 pulse-width-modulation (PWM) controller coupled with a REF-1004 voltage reference. The device contains all of the circuitry necessary to control a switch-mode power supply in a voltage mode configuration. This manual explains how to construct basic power conversion circuits including the design of the control chip functions and the basic loop.

Topic **Page**

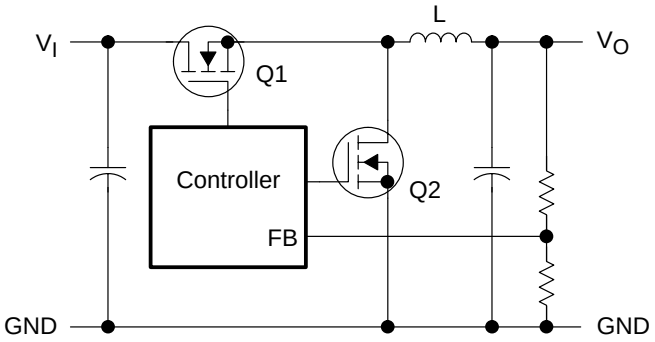
1.1 Hardware 1–2
1.2 Operating Specifications 1–2
1.3 SLVP182 Schematic 1–3
1.4 SLVP182 Bill of Materials 1–4
1.5 EVM Board Layout 1–5

1.1 Hardware

Synchronous buck converters provide smaller size and higher efficiency than a conventional buck converter. The synchronous buck converter reduces power losses associated with a standard buck converter by substituting a power MOSFET for the commutating diode. This reduces the typical 0.5 V to 1V diode voltage drop to 0.3 V or less and increases system efficiency.

Figure 1–1 shows a block diagram of a typical synchronous buck converter. To maintain the desired output voltage, a controller senses the output voltage, compares it to an internal reference voltage and adjusts the width of the power switch (Q1) on time. A commutating switch (Q2) maintains continuous current through the inductor when the power switch is turned off.

Figure 1–1. Typical Synchronous Buck Converter



The SLVP182 synchronous buck converter uses the TI TL5002 PWM controller, REF1004–1.2 voltage reference, and TPS2837 MOSFET driver to give a precision output voltage of 1.8 V ± 1%. The converter operates over an input voltage range of 3.6 V to 12 V with high efficiency. The following section lists the full design specifications.

1.2 Operating Specifications

This section summarizes the performance specifications of the SLVP182 converter. Table 1–1 lists the operating specifications for the SLVP182.

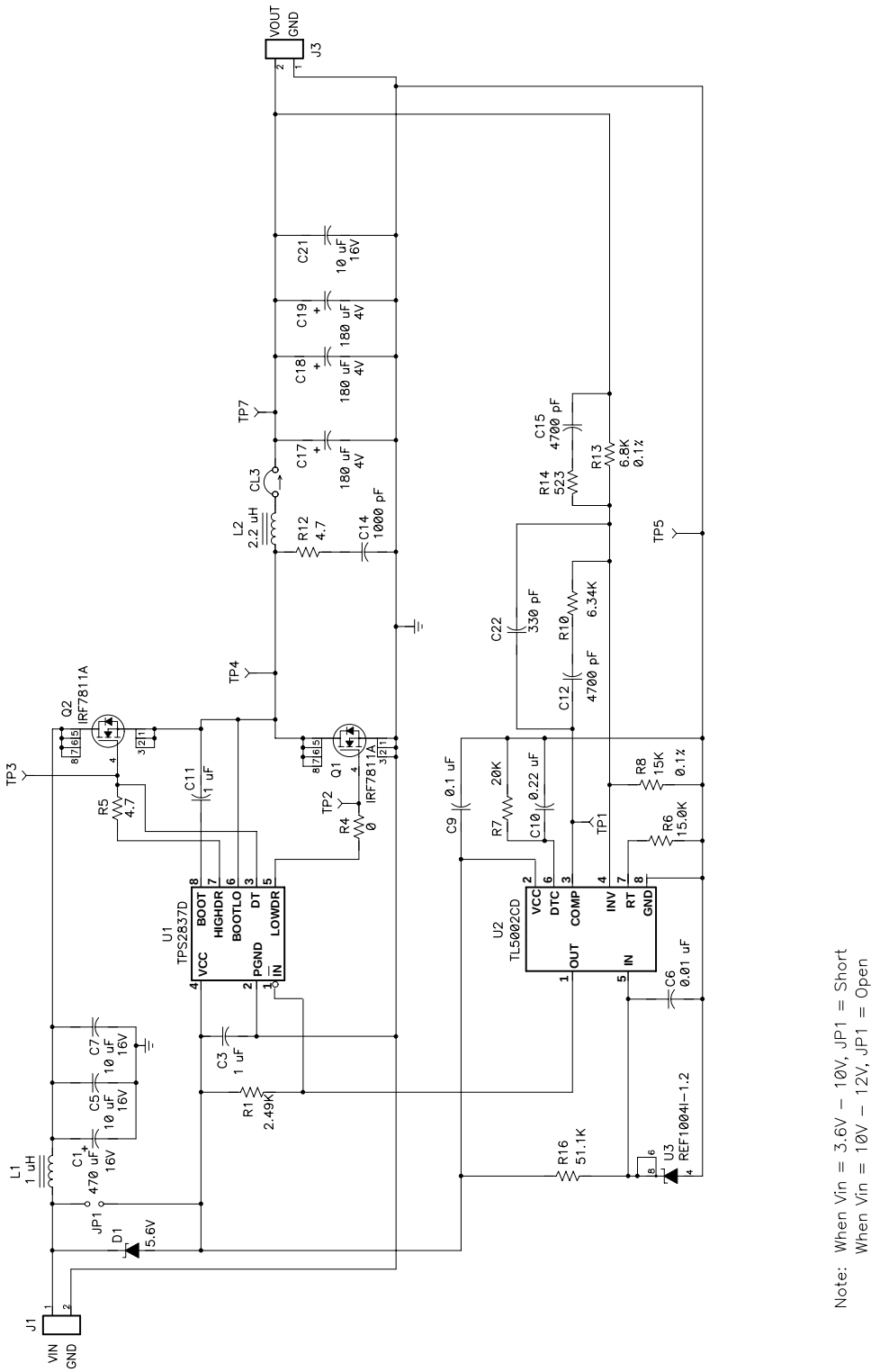
Table 1–1. Operating Specifications

Specification	Min	Typ	Max	Units
Input voltage range	3.6	5	12	V
Output voltage range	1.782	1.8	1.818	V
Output current range			7	A
Output ripple voltage		16†		mV
Operating frequency	380	400	420	kHz
Efficiency			91%‡	
Ambient operating temperature	–20	25	55	°C

† V_I= 5 V, V_O = 1.8 V, I_O = 7 A
‡ V_I= 5 V, V_O = 1.8 V, I_O = 2.5 A

1.3 SLVP182 Schematic

Figure 1–2. Schematic Diagram



1.4 SLVP182 Bill of Material

Table 1–2 lists materials required for the SLVP182.

Table 1–2. SLVP182B Bill of Materials

Count	Ref Des	Part Number	Description	Size	MFR
1	C9	GRM39X7R104K16	Capacitor, ceramic, 0.1 μF, 16 V, X7R, 10%	603	Murata
1	C6	GRM40X7R103K50	Capacitor, ceramic, 0.01 μF, 50 V, X7R, 10%	805	Murata
1	C10	GRM40X7R224K16	Capacitor, ceramic, 0.22 μF, 16 V, X7R, 10%	805	Murata
2	C3, C11	GRM40X7R105K16	Capacitor, ceramic, 1 μF, 16 V, X7R, 10%	805	Murata
1	C22	GRM40X7R331K50	Capacitor, ceramic, 330 pF, 50 V, X7R, 10%	805	Murata
1	C14	GRM40X7R102K25	Capacitor, ceramic, 1000 pF, 25 V, X7R, 10%	805	Murata
2	C12, C15	GRM40X7R472K25	Capacitor, ceramic, 4700 pF, 25 V, X7R, 10%	805	Murata
1	C13	OPEN		805	
3	C5, C7, C21	EMK325BJ106MN	Capacitor, ceramic, 10 μF, 16 V, X5R, ±20%	1210	Taiyo Yuden
3	C2, C4, C8	OPEN		1210	
3	C17,C18, C19	EEF–UE0G181R	Capacitor, aluminum, 180 μF, 4 V, 10% (CD series)	7343	Panasonic
10	C19,C20, C23–C30	OPEN		7343	
1	C1	UUD1C471MNR1GS	Capacitor, aluminum, 470 μF, 16 V, 170 mΩ, 20%	E7	Nichicon
1	CL3	16 AWG Bus	Current Loop, 0.060 holes”		NA
1	D1	1SMB5919BTS	Diode, zener, 5.6 V, 3 W	SMB	On Semi
1	D2	OPEN		SOT23	
1	L1	UP2B–1R0	Inductor, SMT, 1 μH, 9.3–A, 6.5 mΩ,	UP2B	Coiltronics
1	L2	UP4B–2R2	Inductor, SMT, 2.2-μH, 12–A, 4.8 mΩ,	UP4B	Coiltronics
1	JP1	PTC36SAAN	Header, 2 pin, 100 mil spacing, (36–pin strip)		Sullins
1	JP1	929950–00	Shorting jumper unplated		Electronic Specialty Markets/3M
1	R1	Std	Resistor, chip, 2.49 kΩ, 1/16–W, 1%	603	Std
1	R6	Std	Resistor, chip, 15 kΩ, 1/16–W, 1%	603	Std
1	R7	Std	Resistor, chip, 20 kΩ, 1/16–W, 5%	603	Std
1	R16	Std	Resistor, chip, 51.1 kΩ, 1/16–W, 1%	603	Std
2	R2, R3	OPEN		603	
1	R4	Std	Resistor, chip, 0 Ω, 1/10–W, 5%	805	Std
2	R5, R12	Std	Resistor, chip, 4.7 Ω, 1/10–W, 5%	805	Std
1	R10	Std	Resistor, chip, 6.34 kΩ, 1/10–W, 1%	805	Std
1	R13	ERA–6YEB682V	Resistor, chip, 6.8 kΩ, 1/10–W, 0.1%	805	Panasonic
1	R8	ERA–6YEB153V	Resistor, chip, 15 kΩ, 1/10–W, 0.1%	805	Panasonic
1	R14	Std	Resistor, chip, 523 Ω, 1/10–W, 1%	805	Std
2	R9, R11	OPEN		805	

Table 1–2. SLVP182B Bill of Materials (Continued)

Count	Ref Des	Part Number	Description	Size	MFR
1	U3	REF1004I–1.2	IC, voltage reference, 1.2 V, 10 mA	SO8	TI
2	J1, J3	ED1609	Terminal block, 2–pin, 15–A, 5.1 mm		OST
1	J2	OPEN			
1	U2	TL5002CD	IC, low-cost PWM controller with open–collector output	SO8	TI
1	U1	TPS2837D	IC, MOSFET driver, synchronous–buck output	SO8	TI
1	TP5	240–333	Test point, black, 1 mm		Farnell
5	TP1–TP4, TP7	240–345	Test point, red, 1 mm		Farnell
2	TP6, TP8	OPEN			
1	TP9	OPEN			
2	Q1, Q2	IRF7811A	MOSFET, N-ch, 30 V, 11 A, 10 mΩ,	SO8	IR
2	Q3, Q4	OPEN		SO8	
1		92995-00	Shunt		

1.5 EVM Board Layout

Figure 1–3. Top Silk Screen With Top Copper Layer

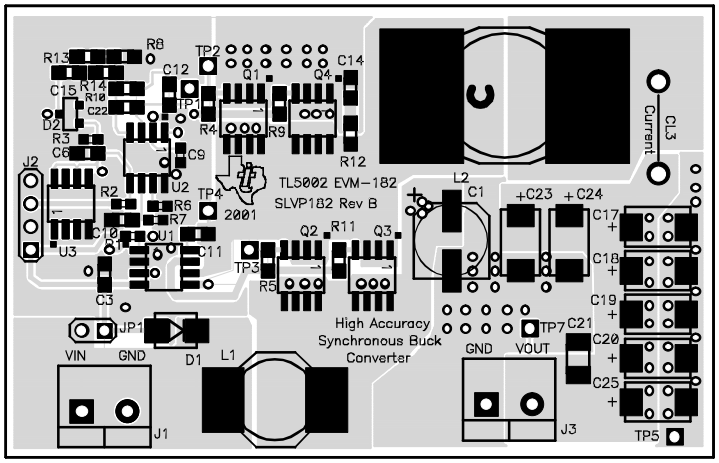


Figure 1–4. Bottom Silk Screen With Bottom Copper Layer

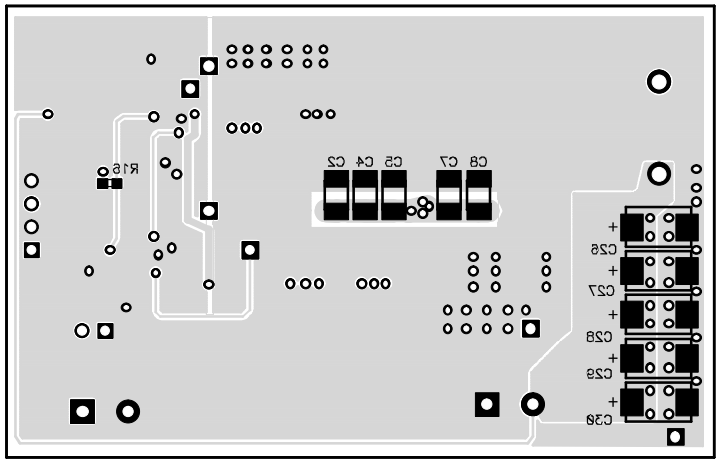


Figure 1–5. Top Layer Copper

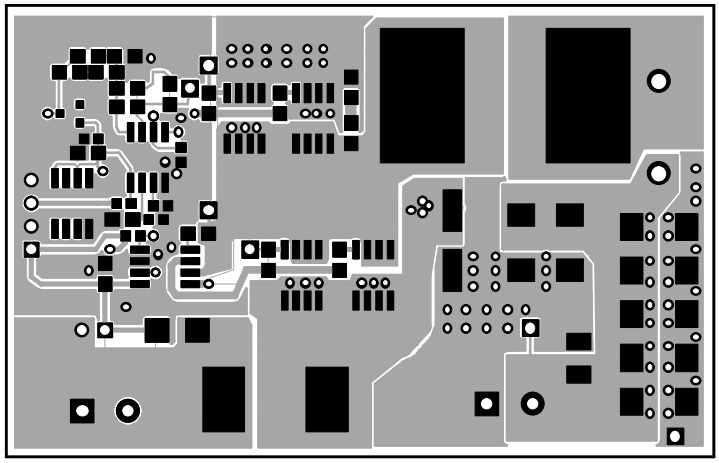


Figure 1–6. Bottom Layer Copper

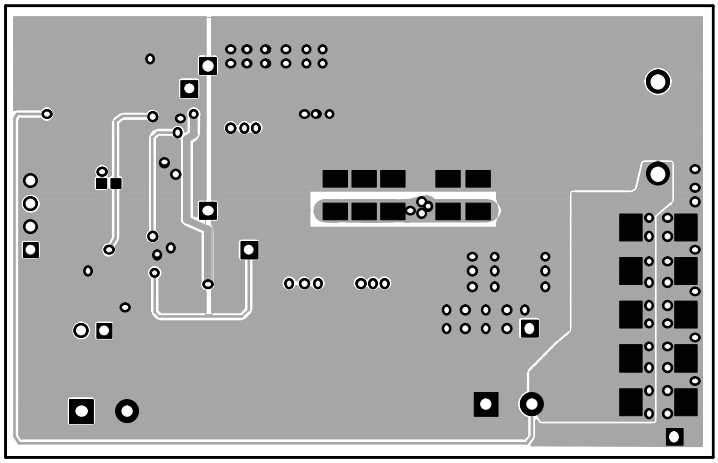


Figure 1–7. Layer 2 (Internal) Copper

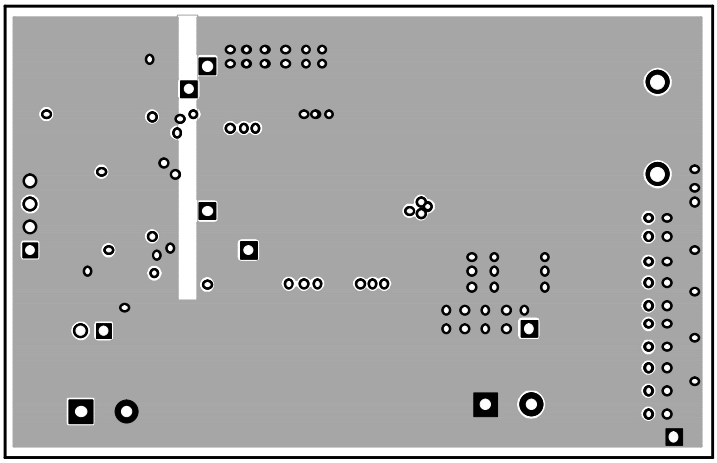
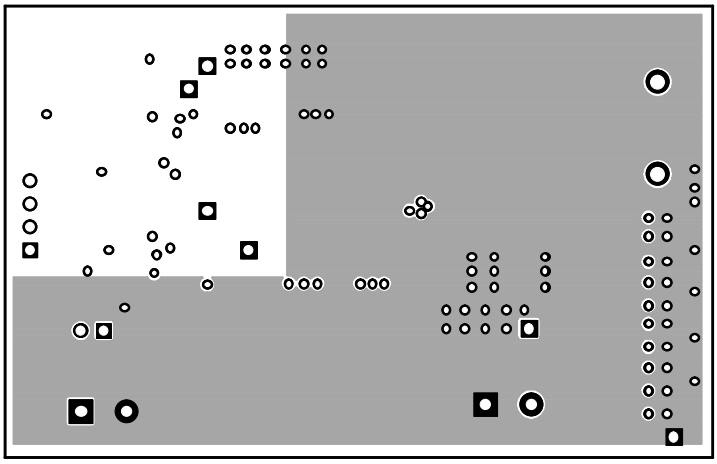


Figure 1–8. Layer 3 (Internal) Copper



Chapter 2

Design Procedures

This chapter shows the procedure used in the design of the SLVP182.

Topic **Page**

2.1	Duty Cycle Estimate	2–2
2.2	Output Filter	2–2
2.3	Power Switch	2–3
2.4	Output Voltage	2–3
2.5	Controller Functions	2–4
2.6	Loop Compensation	2–4

2.1 Duty Cycle Estimate

The duty cycle for a continuous mode stepdown converter is approximately:

$$D = \frac{V_O}{V_I} = \frac{1.8}{5} = 0.36 \quad (2–1)$$

2.2 Output Filter

A synchronous buck converter uses a single-stage LC output filter. Choose an inductor to limit the peak-to-peak ripple current to 15% of the maximum output current:

$$\Delta I_O = 2 \times 0.15 \times I_O = 0.3 \times 7 = 2.1 \text{ A} \quad (2–2)$$

2.2.1 Inductor Value

The inductor value is:

$$L = \frac{\left(V_O + I_{O(max)} \times r_{ds(max)}\right) \times (1 - D)}{f_{(sw)} \times \Delta I_O} = \frac{(1.8 + 7 \times 0.012)0.85}{400000 \times 2.1} \approx 2.2 \ \mu\text{H} \quad (2–3)$$

2.2.2 Capacitor Value

Inductor ripple current flowing through the output capacitors produces an output voltage ripple. Assuming that all inductor ripple current flows through the output capacitors, and the effective series resistance (ESR) is zero, the minimum capacitance needed is:

$$C = \frac{\Delta I_O}{8 \times f_{(sw)} \times \Delta V_O} = \frac{2.1}{8 \times 400000 \times 1.8 \times 0.01} = 36.5 \ \mu\text{F} \quad (2–4)$$

where ΔV_O = 1% of rated output voltage.

Assuming the capacitance is very large, the ESR needed to limit the ripple to 1% of the output voltage is:

$$\text{ESR} < \frac{\Delta V_O}{\Delta I_O} = \frac{0.018}{2.1} = 8.6 \ \text{m}\Omega \quad (2–5)$$

The output filter capacitor should be rated at least ten times the calculated capacitance. This design used three 180-μF capacitors (Panasonic EEF-UE0G181R has a 180 μF with 25 mΩ of ESR at 400 kHz) in parallel with a multilayer ceramic to reduce ESR at high frequency.

2.3 Power Switch

The TL5002 controller can drive two N-channel power MOSFETs in a synchronous rectifier configuration. This design uses the International Rectifier IRF7811A MOSFET, a device chosen for its low $r_{DS(on)}$ of 12 mΩ and drain-to-source breakdown voltage rating of 28 V. Power dissipation for the switching MOSFETs, Q1 and Q2, which includes both conduction and switching losses, is given by:

$$P_{DQ1} = \left(I_O^2 \times r_{ds(on)} \times D\right) + \left(0.5 \times V_I \times I_O \times t_{r+f} \times f_{(sw)}\right) \quad (2–6)$$

$$P_{DQ2} = \left(I_O^2 \times r_{ds(on)} \times (1 - D)\right) + \left(0.5 \times V_I \times I_O \times t_{r+f} \times f_{(sw)}\right) \quad (2–7)$$

An example MOSFET power dissipation calculation for Q1 and Q2 is shown below with the following assumptions;

The total switching time, t_{r+f} = 40 ns

$r_{ds(on)}$ high temperature adjustment factor = 1.35

55°C maximum ambient temperature

V_I = 5 V, V_O = 1.8 V, and I_O = 7 A then;

$$P_{DQ1} = \left(7^2 \times 0.012 \times 1.35 \times 0.36\right) + \left(0.5 \times 5 \times 7 \times 40 \times 10^{-9} \times 400000\right) = 0.57\ W \quad (2–8)$$

$$P_{DQ2} = \left(7^2 \times 0.012 \times 1.35 \times 0.64\right) + \left(0.5 \times 5 \times 7 \times 40 \times 10^{-9} \times 400000\right) = 0.79\ W \quad (2–9)$$

The thermal impedance of these devices is $R_{\theta JA}$ = 50°C/W.

Thus:

$$T_{JQ1} = T_A + \left(R_{\theta JA} \times P_{DQ1}\right) = 55 + (50 \times 0.57) = 84°C \quad (2–10)$$

$$T_{JQ2} = T_A + \left(R_{\theta JA} \times P_{DQ2}\right) = 55 + (90 \times 0.79) = 95°C \quad (2–11)$$

It is good design practice to check power dissipation at the extreme limits of input voltage to find the worst case.

2.4 Output Voltage

The TL5002 controller can have an external reference voltage. The REF1004–1.2, which is a two terminal bandgap reference designed for high accuracy with outstanding temperature characteristics, is used for the external voltage reference (V_{ref}).

This EVM board is designed to maintain the output voltage at 1.8 V ± 1%. The output voltage is obtained with this equation.

$$V_O = \left(1 + \frac{R13}{R8}\right)V_{ref} = \left(1 + \frac{6800}{15000}\right) \times 1.235 = 1.8\ V \quad (2–12)$$

The tolerance of R13 and R8 should be no greater than 0.1%. The compensator components around the error amplifier do not affect the average output voltage.

2.5 Controller Functions

The controller functions, oscillator frequency, softstart, and dead-time-control are discussed in this section.

2.5.1 Oscillator Frequency

The oscillator frequency is set by selecting the resistance value from the graph in Figure 8 of the TL5002 data sheet. For 400 kHz, a value of 15 kΩ is selected for R6.

2.5.2 Dead Time Control

Dead time control provides a maximum on-time for the power switch in each cycle. Set this time by connecting a resistor between DTC and GND. For this design, a maximum duty cycle of 80% is chosen (see TL5002 data sheet). Then, R7 is calculated as:

$$R7 = (R6 + 1.25) \times 10^3 \times \left[D\left(V_{O(100\%)} - V_{O(0\%)}\right) + V_{O(0\%)} \right] \quad (2\text{–}13)$$

$$= (15 + 1.25) \times 10^3 \times [0.8 \times (1.5\text{–}0.4) + 0.4] = 20.8\ \text{k}\Omega \Rightarrow 20\ \text{k}\Omega$$

2.5.3 Softstart Timing

Softstart is added to reduce power-up transients. This is implemented by adding a capacitor across the dead-time resistor (see TL5002 data sheet). In this design, a softstart time of 4.4 ms is used.

$$C10 = \frac{T_r}{R7} = \frac{4.4\ \text{ms}}{20\ \text{k}\Omega} = 0.22\ \mu\text{F} \quad (2\text{–}14)$$

2.6 Loop Compensation

Loop compensation is necessary to stabilize the converter over the full range of load and line conditions. This evaluation converter is designed to maintain greater than 60 degrees of phase margin over all input/output conditions. In addition, sufficient bandwidth must be designed into the circuit to ensure that the converter has a good transient response. Both of these requirements are achieved by adding compensation components around the error amplifier to modify the overall loop response.

The loop compensation design procedure consists of shaping the error amplifier frequency response with external components to stabilize the dc/dc converter feedback control loop without destroying the control loop ability to respond to line or/and load transients. A detailed treatment of dc/dc converter stability analysis and design is well beyond the scope of this report. The following is a simplified approach to designing networks to stabilize continuous mode buck converters.

Ignoring the error amplifier frequency response, the response of the pulse width modulator and power switch operating in continuous mode can be modeled as a simple gain block. The magnitude of the gain is the change in output voltage for a change in the pulse width modulator input voltage (error amplifier COMP voltage). Typically, increasing the COMP voltage from 0.4 V to 1.5 V

increases the duty cycle from 0 to 100% and the output voltage from 0 V to $V_{I,max}$ at the nominal input voltage. The gain A_{PWM} is:

$$A_{(PWM)} = \frac{V_I}{\Delta V_{O(COMP)}} = \frac{5.5}{1.5 - 0.4} = 5 \Rightarrow 14 \text{ dB} \quad (2\text{–}15)$$

Similarly, the gain is 10 dB at 3.6 V and 20 dB at 15 V. Converters with wider input ranges need to check for stability at several line voltages to ensure that gain variation does not cause a stability problem.

The output filter is a LC filter and functions accordingly. The inductor and capacitor produce an underdamped complex–pole pair at the filter resonant frequency and the capacitor ESR (R_{ESR}) puts a zero in the response above the resonant frequency. The double pole is located at:

$$\frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{2.2\ \mu H \times 180\ \mu F \times 3}} = 4.6 \text{ kHz} \quad (2\text{–}16)$$

The zero is located at:

$$\frac{1}{2\pi R_{ESR} C} = \frac{1}{2\pi \times \left(\frac{0.025 \times 1.35}{3}\right) \times 180\ \mu F \times 3} = 26.2 \text{ kHz} \quad (2\text{–}17)$$

It is assumed that ESR high temperature adjustment factor is 1.35.

Figure 2–1 and Figure 2–2 show power stage gain and phase plots.

Figure 2–1. Power Stage Gain

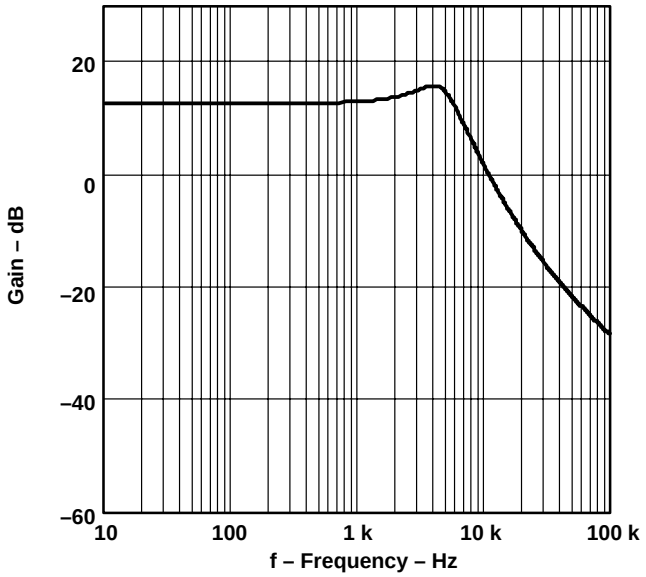
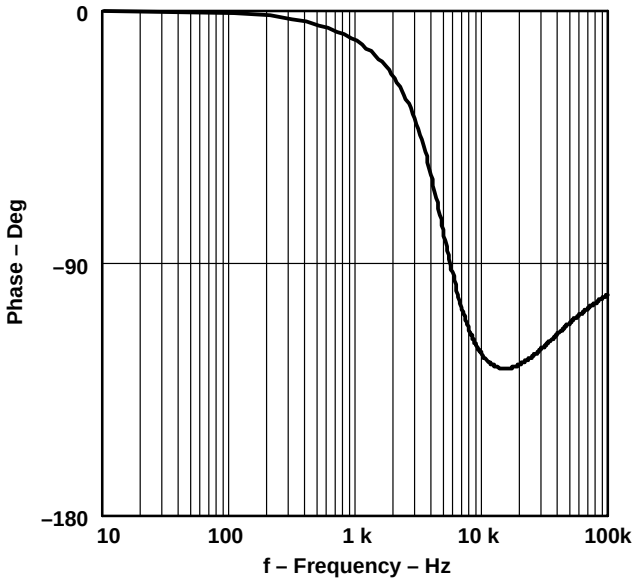
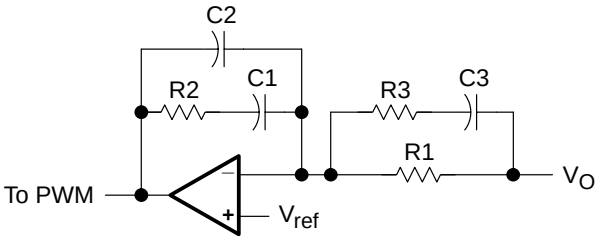


Figure 2–2. Power Stage Phase



Unless the designer is trying to meet an unusual requirement, such as very wide band response, many of the decisions regarding gains, compensation pole and zero locations, and unity-gain bandwidth are largely arbitrary. Generally, the gain at low frequencies is very high to minimize error in the output voltage; compensation zeros are added near the filter poles to correct for the sharp change in phase encountered near the filter resonant frequency; and an open loop unity gain frequency is selected well beyond the filter resonant frequency but no more than 10% of the converter operating frequency. In this instance, a unity gain frequency of approximately 20 kHz is chosen to provide good transient response. Figure 2–3 shows a standard compensation network chosen for this example.

Figure 2–3. Compensation Circuit



The total phase lag through the compensated error amplifier is calculated with this equation:

$$\theta_{ea} = 270° - 2\ \tan^{-1} K + 2\ \tan^{-1}\left(\frac{1}{K}\right) \qquad (2\text{–}18)$$

$$\text{Where : } K = \frac{f_{(bw)}}{f_{(z)}} = \frac{f_{(p)}}{f_{(bw)}}$$

$f_{(bw)}$ = Desired closed loop crossover frequency
$f_{(p)}$ = Error amplifier pole frequency
$f_{(z)}$ = Error amplifier zero frequency

Assuming an ideal amplifier, the transfer function is:

$$A_{(ea)}(s) = \left[\frac{1}{sR1\ (C1 + C2)}\right] \times \frac{[s(R1 + R3)C3 + 1](sR2C1 + 1)}{(sR3C3 + 1)\left[sR2(C2//C1) + 1\right]} \quad (2–19)$$

The location of the double-zero and double-pole frequencies is fixed by the K factor, which yields the desired phase margin. From the transfer function (equation 2–19) and equation 2–18, R and C values that set the zero and pole frequencies at the desired frequencies are determined.

To obtain the desired phase margin (60 degree) at cross over frequency (BW=20 kHz), the total phase lag (total phase lag = power stage phase + error amp phase) at crossover frequency should be equal to the desired phase margin. As shown in Figure 2–2 (power stage phase), the power stage phase lag at 20 kHz is recorded as about 150°. Thus, K factor is obtained using equation 2–18 (K=3.7).

Then, two zeros and poles are calculated as:

$$f_{(z1)} = f_{(z2)} = \frac{f_{(bw)}}{K} = \frac{20000}{3.7} = 5.4\ \text{kHz} \quad (2–20)$$

$$f_{(p1)} = f_{(p2)} = K \times f_{(bw)} = 74\ \text{kHz} \quad (2–21)$$

Now, the components around the error amplifier can be calculated using the following equations:

A first zero of

$$f_{(z1)} = \frac{1}{2\pi R2C1} \quad (2–22)$$

A second zero of

$$f_{(z2)} = \frac{1}{2\pi(R1 + R3)C3} \quad (2–23)$$

A first pole of

$$f_{(p1)} = \frac{1}{2\pi R3C3} \quad (2–24)$$

A second pole of

$$f_{(p2)} = \frac{C1 + C2}{2\pi R2(C1C2)} \quad (2–25)$$

When the higher value of R1 is chosen, the compensation capacitor values become smaller so that the compensation component values may become less than a parasitic capacitance. Thus, R1 is chosen as follows:

$$R1 = 6.8\ k\Omega \quad (2–26)$$

Then calculate using equations (2–22) to (2–25):

$$C3 = \frac{\frac{1}{f(z2)} - \frac{1}{f(p1)}}{2\pi R1} = 4014\ \text{pF} \quad (2–27)$$

$$R3 = \frac{1}{2\pi C3\ f_{(p1)}} = 535\ \Omega \quad (2–28)$$

The first zero (at 5.4 kHz) occurs when R2=X_{c1} and the error amplifier gain at that frequency is approximately R2/R1. Thus, from Figure 2–1 (power stage gain), the error amplifier gain at 5.4 kHz should be –0.864 dB. The gain of –0.864 dB translates to a voltage of 0.905 V. Therefore, R2 is obtained as follows:

$$R2 = 0.905 \times R1 = 6.156\ k\Omega \quad (2–29)$$

$$C2 = \frac{1}{2\pi R2\ f_{(p2)}} = 349\ pF \quad (2–30)$$

$$C1 = \frac{1}{2\pi R2\ f_{(z1)}} = 4783\ pF \quad (2–31)$$

Figure 2–4 and Figure 2–5 show the bode plot for the compensation network. Figure 2–6 and Figure 2–7 show the overall loop response.

Figure 2–4. Compensation Gain

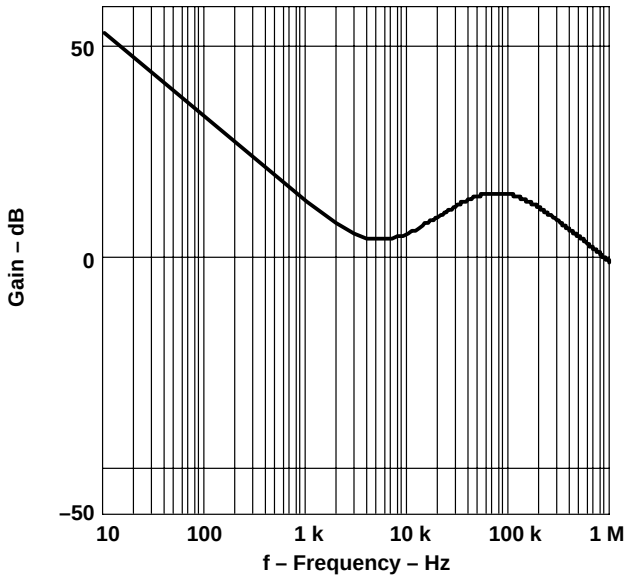


Figure 2–5. Compensation Phase

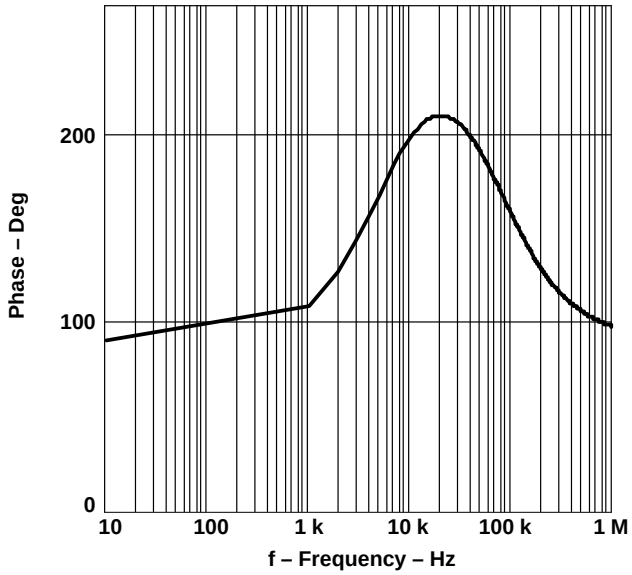


Figure 2–6. Overall Loop Gain Response

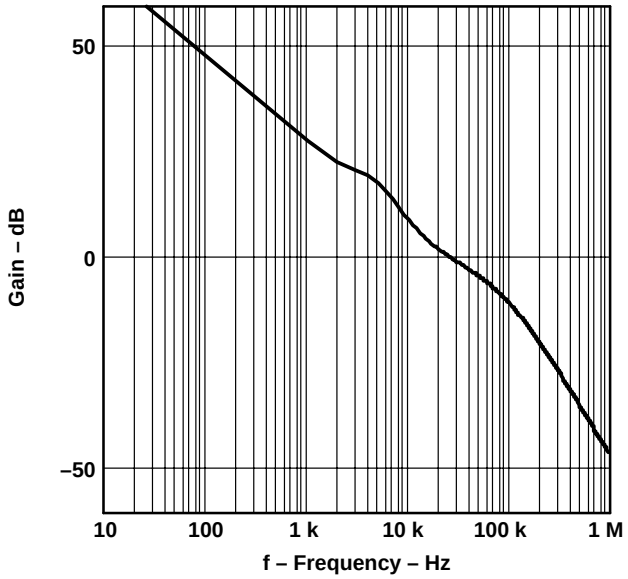
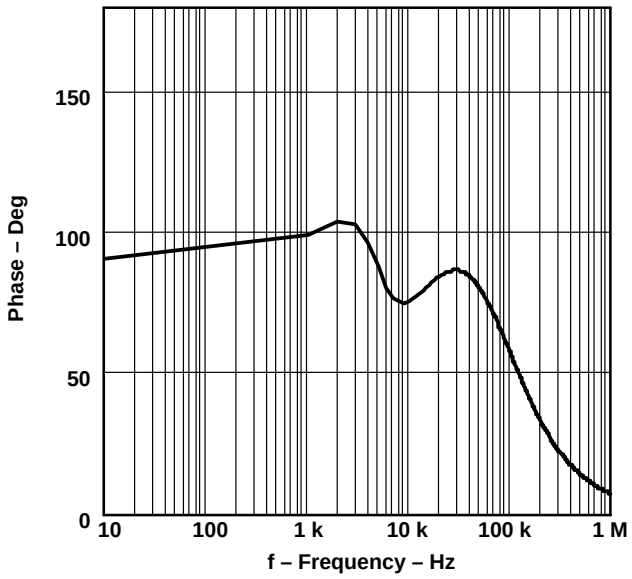


Figure 2–7. Overall Loop Phase Response



Note from the overall response shown in Figure 2–6 and Figure 2–7 that the phase margin is 60 degree and the bandwidth is 20 kHz under nominal operating conditions.

Chapter 3

Test Results

A power supply that has a power capability of 15 V/13 A is required for this test.

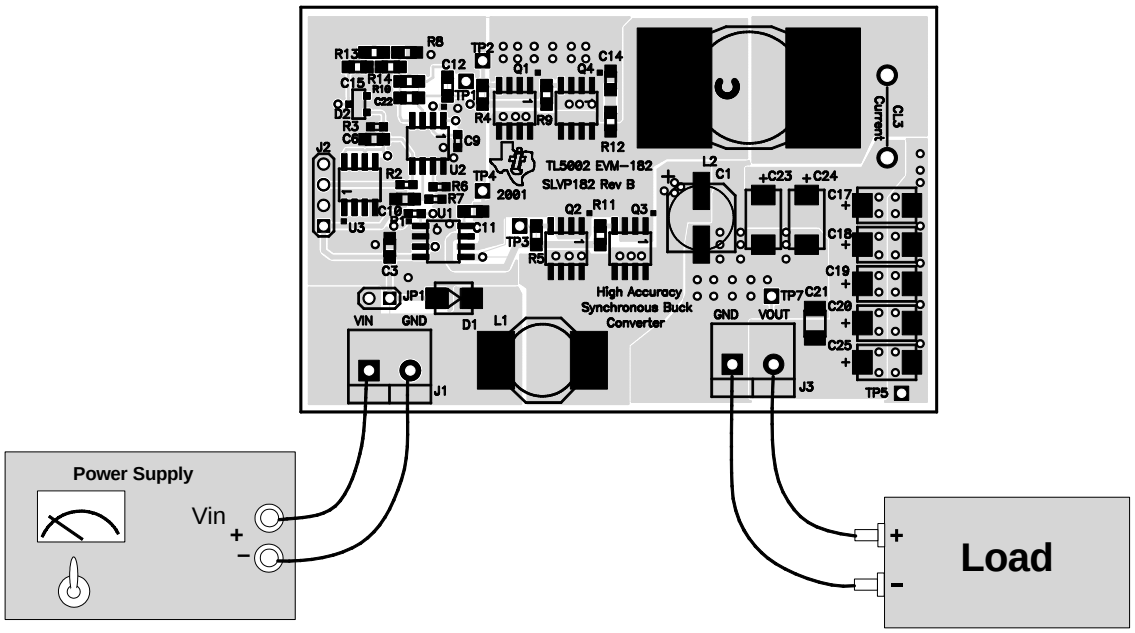
Topic **Page**

3.1 Test Setup 3–2
3.2 Test Result 3–3

3.1 Test Setup

Figure 3–1 shows the input/output connections to the SLVP182.

Figure 3–1. Test Setup



3.2 Test Results

Figures 3–2 through Figure 3–13 show the test results for the SLVP182.

Figure 3–2. Efficiency Graph

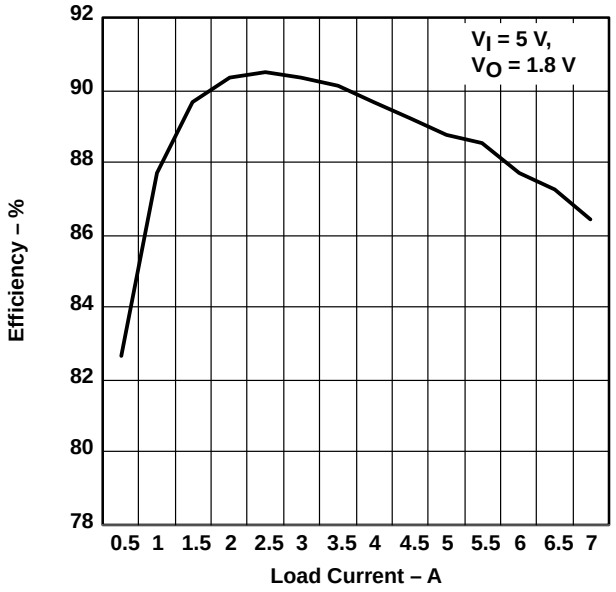


Figure 3–3. Line Regulation (With JP1 = Short, T_A = 25°C)

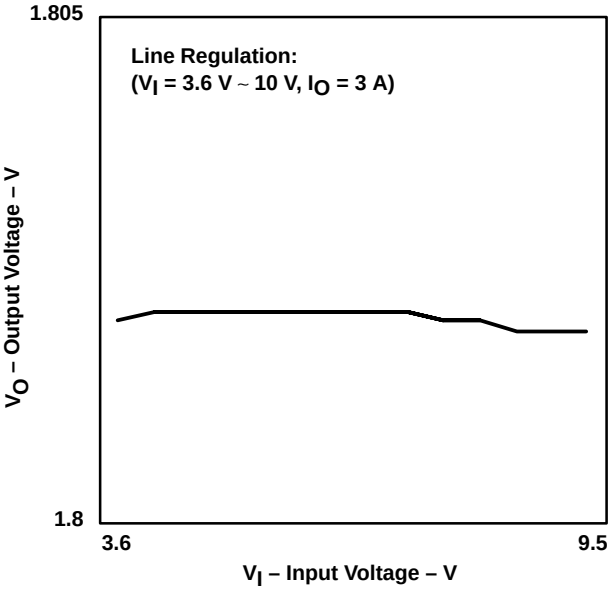


Figure 3–4. Line Regulation (With JP1 = Open, T_A = 25°C)

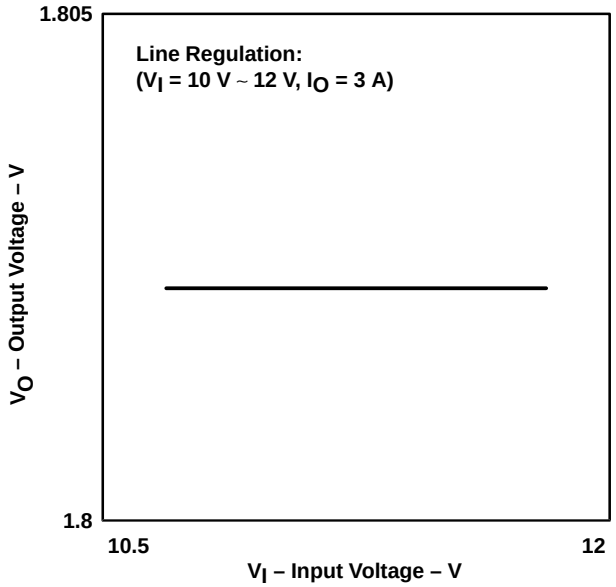


Figure 3–5. Load Regulation (V_I = 5 V, T_A = 25°C)

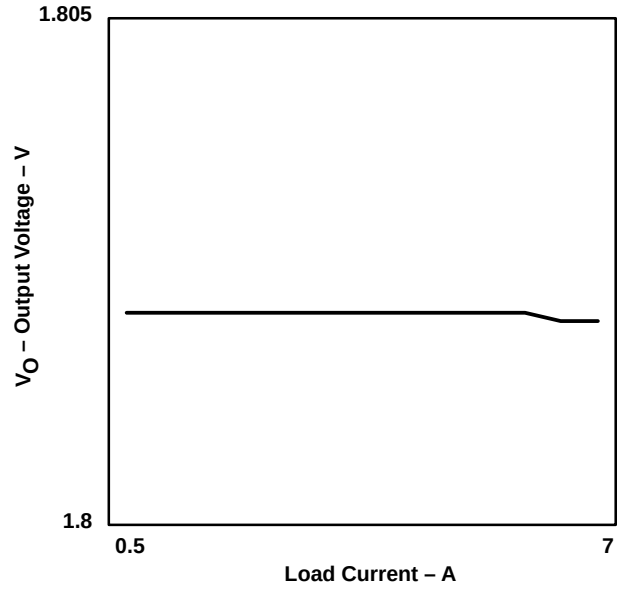


Figure 3–6. Output Voltage Deviation in Terms of Temperature

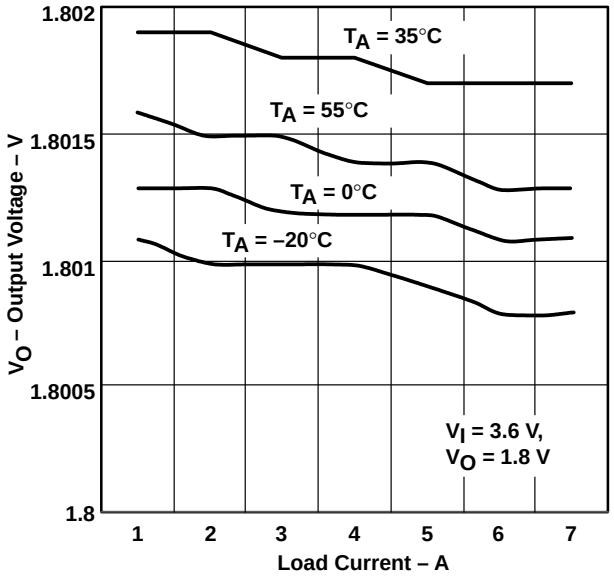


Figure 3–7. Output Voltage Deviation in Terms of Temperature

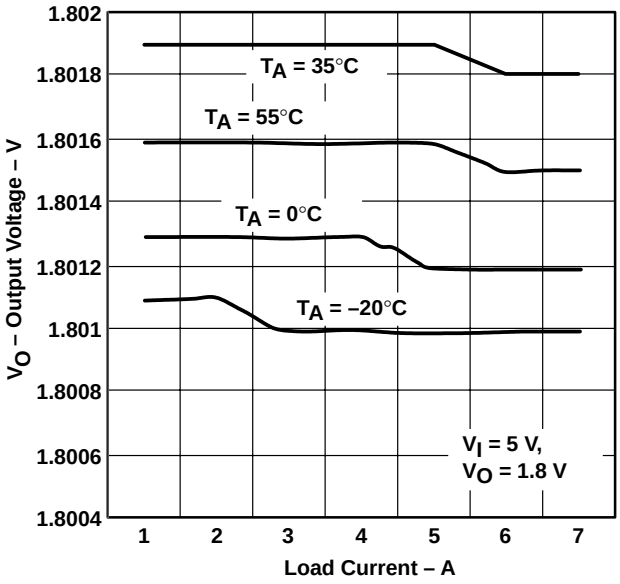


Figure 3–8. Output Voltage Deviation in Terms of Temperature

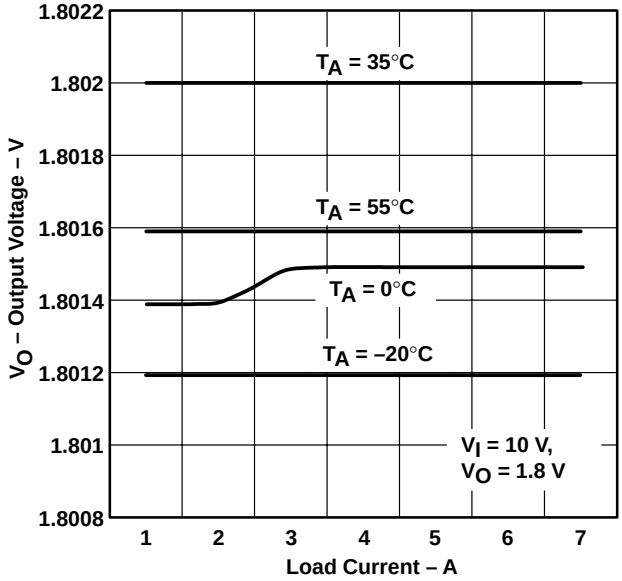


Figure 3–9. Output Voltage Deviation in Terms of Temperature

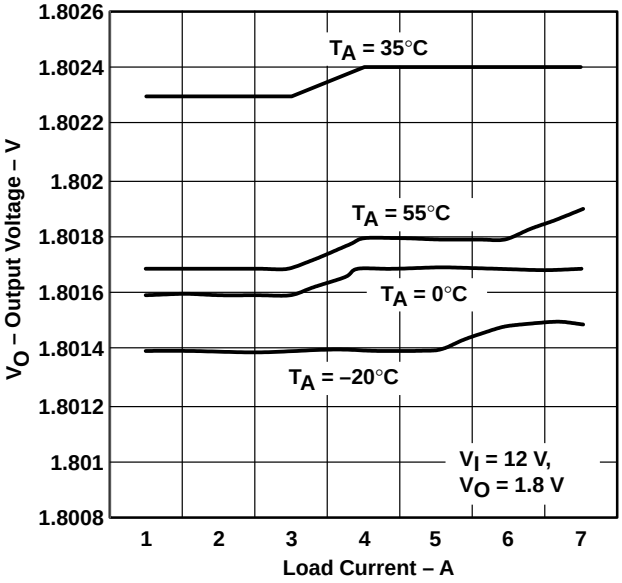


Figure 3–10. V_O (Upper Trace) and I_o (2A/div) at Full/No Loads Transient Response

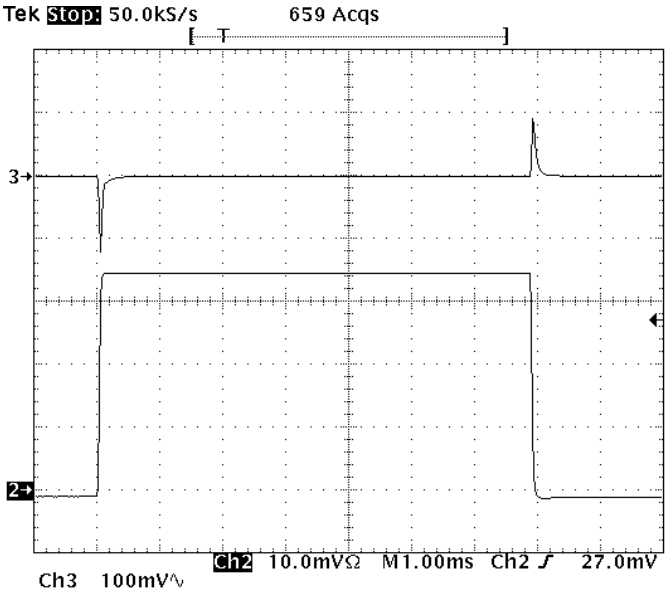


Figure 3–11. Output Voltage (Upper Trace, V_O, and Phase Voltage, V_{phase}

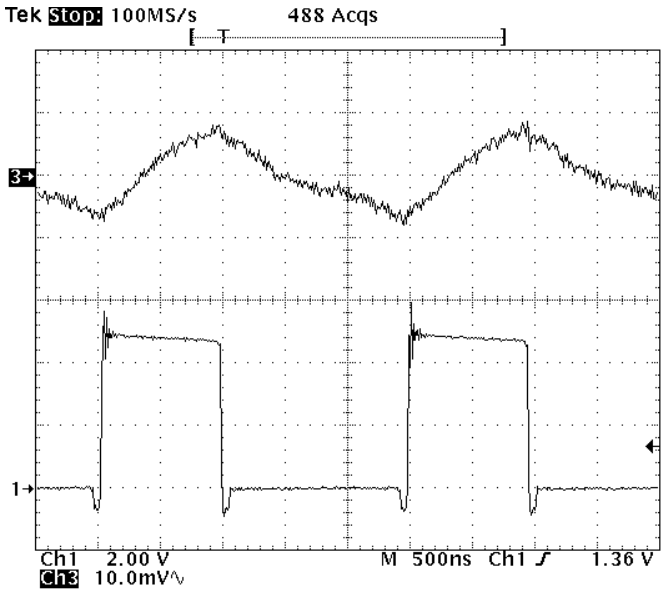


Figure 3–12. EVM Start-Up, Input Voltage (Upper Trace) and Output Voltage

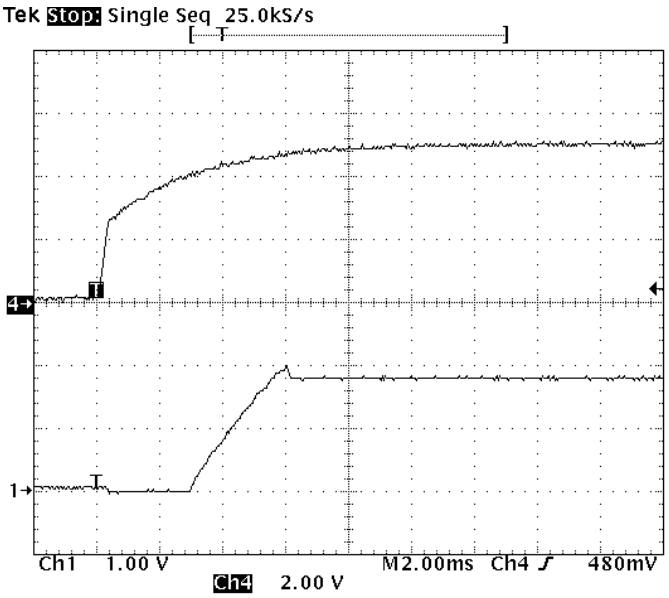
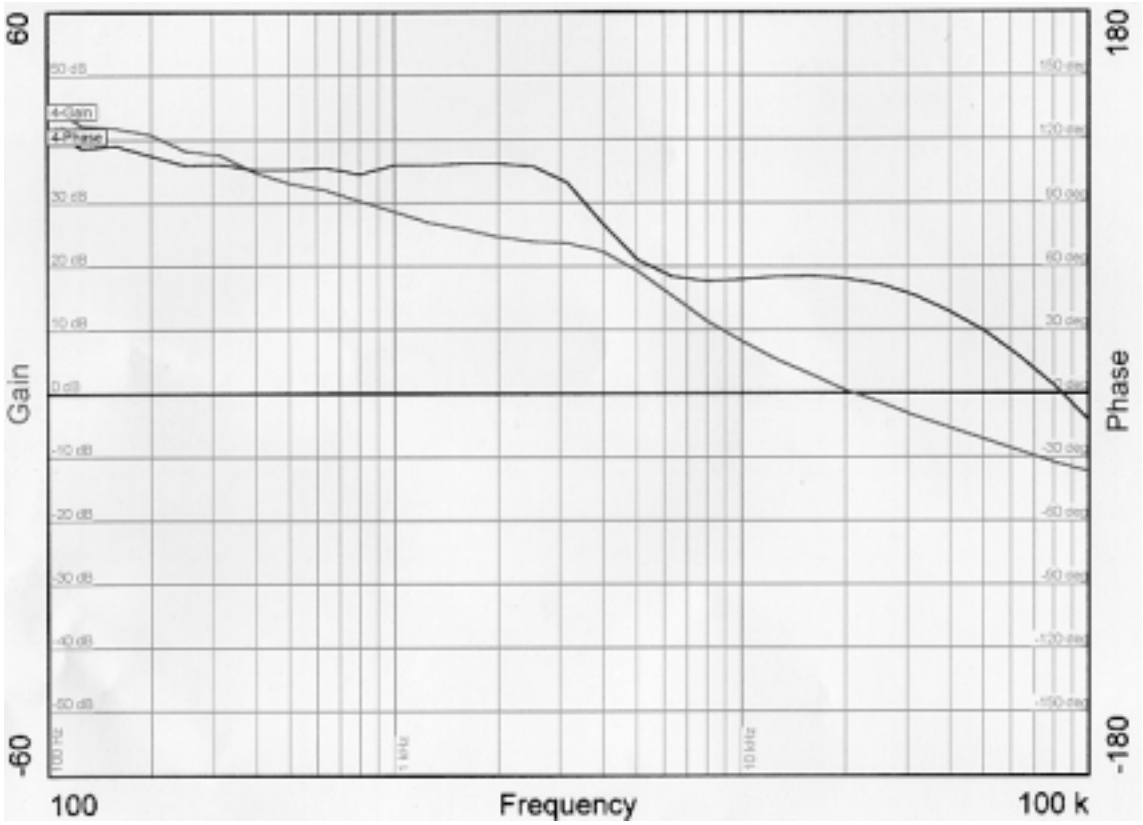


Figure 3–13. The Measured Overall Closed Loop Response (V_I = 5 V, V_O = 1.8 V, I_O = 7 A)



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265