Ultracompact, 3 A Thermoelectric Cooler (TEC) Controller

Data Sheet

ADN8835

FEATURES

- High efficiency single inductor architecture
- Integrated low R_{DSON} MOSFETs for the TEC controller
- TEC voltage and current operation monitoring
- No external sense resistor required
- Independent TEC heating and cooling current-limit settings
- Programmable maximum TEC voltage
- 2.0 MHz (typical) PWM driver switching frequency
- External synchronization
- Two integrated, zero-drift, rail-to-rail chopper amplifiers
- Compatible with NTC or RTD thermal sensors
- 2.50 V reference output with 1% accuracy
- Temperature lock indicator
- Available in a 36-lead, 6 mm × 6 mm LFCSP

APPLICATIONS

- TEC temperature control
- Optical modules
- Optical fiber amplifiers
- Optical networking systems
- Instruments requiring TEC temperature control

FUNCTIONAL BLOCK DIAGRAM

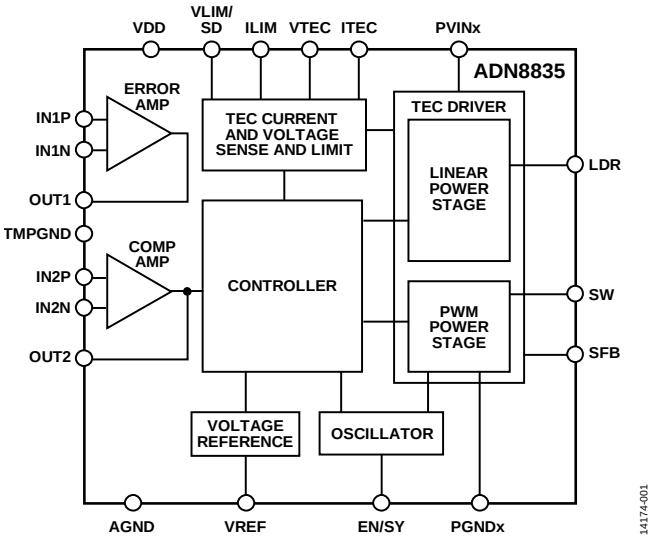


Figure 1.

GENERAL DESCRIPTION

The ADN8835[1] is a monolithic TEC controller with an integrated TEC controller. It has a linear power stage, a pulse-width modulation (PWM) power stage, and two zero-drift, rail-to-rail chopper amplifiers. The linear controller works with the PWM driver to control the internal power MOSFETs in an H bridge configuration. By measuring the thermal sensor feedback voltage and using the integrated operational amplifiers as a proportional integral differential (PID) compensator to condition the signal, the ADN8835 drives current through a TEC to settle the temperature of a laser diode or a passive component attached to the TEC module to the programmed target temperature.

The ADN8835 supports negative temperature coefficient (NTC) thermistors as well as positive temperature coefficient (PTC) resistive temperature detectors (RTDs). The target temperature is set as an analog voltage input either from a digital-to-analog converter (DAC) or from an external resistor divider.

The temperature control loop of the ADN8835 is stabilized by PID compensation utilizing the built in, zero-drift chopper amplifiers. The internal 2.50 V reference voltage provides a 1% accurate output that biases a thermistor temperature sensing bridge as well as a voltage divider network to program the maximum TEC current and voltage limits for both the heating and cooling modes. With the zero-drift chopper amplifiers, excellent long-term temperature stability is maintained via an autonomous analog temperature control loop.

Table 1. TEC Family Models

Device No.	MOSFET	Thermal Loop	Package
ADN8831	Discrete	Digital/analog	LFCSP (CP-32-7)
ADN8833	Integrated	Digital	WLCSP (CB-25-7), LFCSP (CP-24-15)
ADN8834	Integrated	Digital/analog	WLCSP (CB-25-7), LFCSP (CP-24-15)
ADN8835	Integrated	Digital/analog	LFCSP (CP-36-5)

[1] Product is covered by U.S. Patent No. 6,486,643.

Rev. B Document Feedback

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
Functional Block Diagram ... 1
General Description ... 1
Revision History ... 2
Detailed Functional Block Diagram ... 3
Specifications ... 4
Absolute Maximum Ratings ... 7
  Thermal Resistance ... 7
  Maximum Power Dissipation ... 7
  ESD Caution ... 7
Pin Configuration and Function Descriptions ... 8
Typical Performance Characteristics ... 9
Theory of Operation ... 13
  Analog PID Control ... 14
  Digital PID Control ... 14
  Powering the Controller ... 14
  Enable and Shutdown ... 15
  Oscillator Clock Frequency ... 15
  Temperature Lock Indicator ... 15
  Soft Start on Power-Up ... 15
  TEC Voltage/Current Monitor ... 16
  Maximum TEC Voltage Limit ... 16
  Maximum TEC Current Limit ... 16
Applications Information ... 18
  Signal Flow ... 18
  Thermistor Setup ... 18
  Thermistor Amplifier (Chopper 1) ... 19
  PID Compensation Amplifier (Chopper 2) ... 19
  MOSFET Driver Amplifiers ... 20
  PWM Output Filter Requirements ... 20
  Input Capacitor Selection ... 21
  Power Dissipation ... 21
  Thermal Consideration ... 22
PCB Layout Guidelines ... 23
  Block Diagrams and Signal Flow ... 23
  Guidelines for Reducing Noise and Minimizing Power Loss 23
  Example PCB Layout Using Two Layers ... 24
Outline Dimensions ... 27
  Ordering Guide ... 27

REVISION HISTORY

9/2018—Rev. A to Rev. B

Added Patent Information ... 1
Changes to Specifications, Table 2, Voltage Measurement Accuracy Parameter ... 6

5/2017—Rev. 0 to Rev. A

Changes to PID Compensation Amplifier (Chopper 2) Section ... 18
Changes to Ordering Guide ... 26

12/2016—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAM

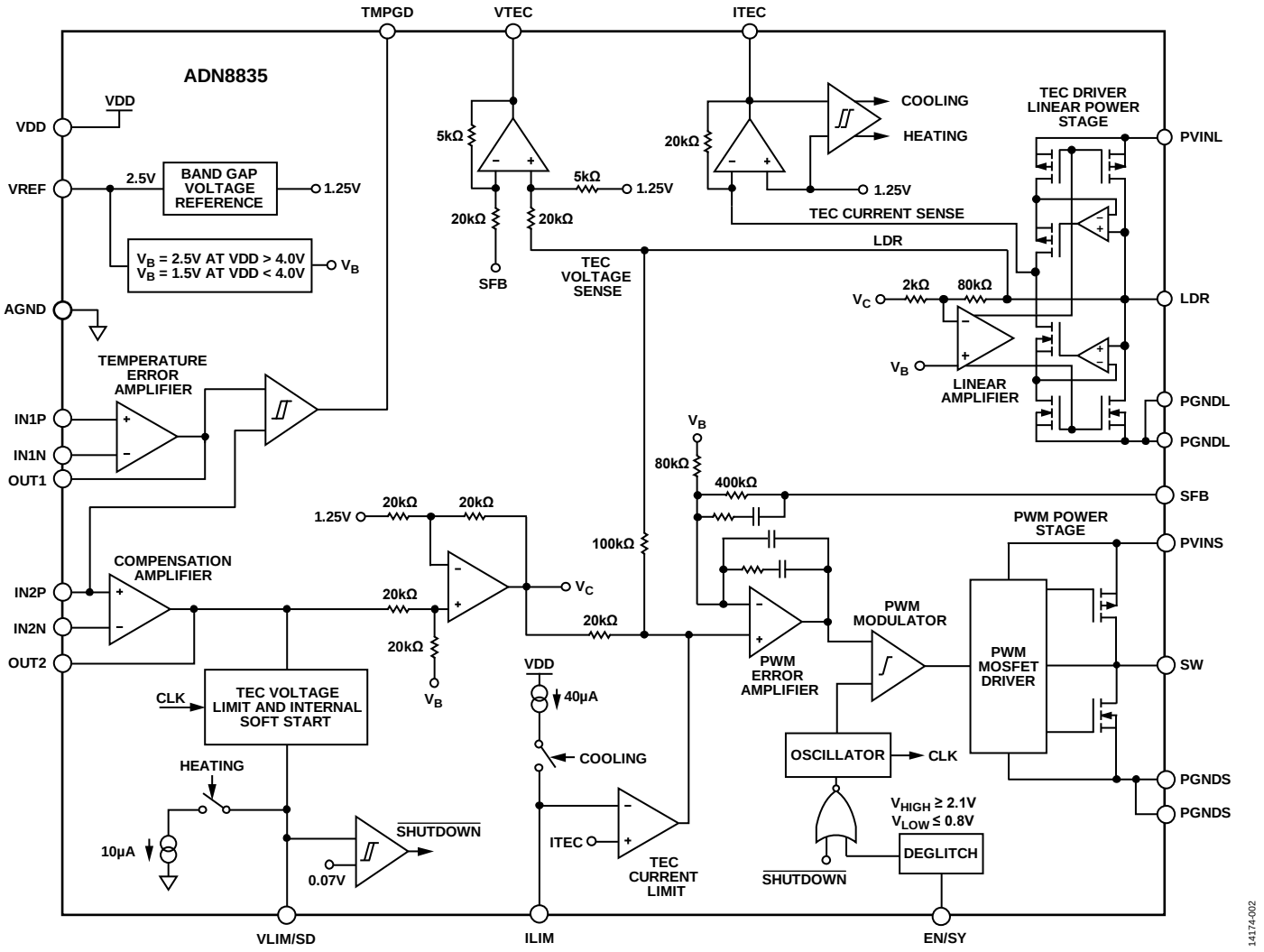


Figure 2. Detailed Functional Block Diagram of the ADN8835

SPECIFICATIONS

V_{IN} = 2.7 V to 5.5 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Driver Supply Voltage	V_{PVIN}		2.7		5.5	V
Controller Supply Voltage	V_{VDD}		2.7		5.5	V
Supply Current	I_{VDD}	PWM not switching		3.3	5	mA
Shutdown Current	I_{SD}	EN/SY = AGND or VLIM/SD = AGND		350	700	µA
Undervoltage Lockout (UVLO)	V_{UVLO}	V_{VDD} rising	2.45	2.55	2.65	V
UVLO Hysteresis	$UVLO_{HYST}$		80	90	100	mV
REFERENCE VOLTAGE	V_{VREF}	I_{VREF} = 0 mA to 10 mA	2.475	2.50	2.525	V
LINEAR OUTPUT						
Output Voltage	V_{LDR}	I_{LDR} = 0 A				
Low				0		V
High				V_{PVIN}		V
Maximum Source Current	I_{LDR_SOURCE}		3.5			A
Maximum Sink Current	I_{LDR_SINK}				3.5	A
On Resistance		I_{LDR} = 1.5 A				
P-MOSFET	$R_{DS_PL(ON)}$	V_{PVIN} = 5.0 V		50	70	mΩ
		V_{PVIN} = 3.3 V		55	85	mΩ
N-MOSFET	$R_{DS_NL(ON)}$	V_{PVIN} = 5.0 V		45	80	mΩ
		V_{PVIN} = 3.3 V		50	90	mΩ
Leakage Current						
P-MOSFET	$I_{LDR_P_LKG}$			0.1	10	µA
N-MOSFET	$I_{LDR_N_LKG}$			0.1	10	µA
Linear Amplifier Gain	A_{LDR}			40		V/V
LDR Short-Circuit Threshold	$I_{LDR_SH_GNDL}$	LDR short to PGNDL, enter hiccup		4		A
	$I_{LDR_SH_PVIN(L)}$	LDR short to PVIN, enter hiccup		−4		A
Hiccup Cycle	t_{HICCUP}			15		ms
PWM OUTPUT						
Output Voltage	V_{SFB}	I_{SFB} = 0 A				V
Low				0.06 × V_{PVIN}		V
High				0.93 × V_{PVIN}		V
Maximum Source Current	I_{SW_SOURCE}		3.5			A
Maximum Sink Current	I_{SW_SINK}				3.5	A
On Resistance		I_{SW} = 1.5 A				
P-MOSFET	$R_{DS_PS(ON)}$	V_{PVIN} = 5.0 V		60	85	mΩ
		V_{PVIN} = 3.3 V		70	100	mΩ
N-MOSFET	$R_{DS_NS(ON)}$	V_{PVIN} = 5.0 V		45	85	mΩ
		V_{PVIN} = 3.3 V		55	95	mΩ
Leakage Current						
P-MOSFET	$I_{SW_P_LKG}$			0.1	10	µA
N-MOSFET	$I_{SW_N_LKG}$			0.1	10	µA
SW Node Rise Time[1]	t_{SW_R}	C_{SW} = 1 nF		1		ns
PWM Duty Cycle[2]	D_{SW}		6		93	%
SFB Input Bias Current	I_{SFB}			1	2	µA
PWM OSCILLATOR						
Internal Oscillator Frequency	f_{OSC}	EN/SY high	1.85	2.0	2.15	MHz

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
EN/SY Input Voltage						
Low	V_{EN/SY_ILOW}				0.8	V
High	V_{EN/SY_IHIGH}		2.1			V
External Synchronization Frequency	f_{SYNC}		1.85		3.25	MHz
Synchronization Pulse Duty Cycle	D_{SYNC}		10		90	%
EN/SY Rising to PWM Rising Delay	t_{SYNC_PWM}			50		ns
EN/SY to PWM Lock Time	t_{SY_LOCK}	Number of sync cycles			11	Cycles
EN/SY Input Current	$I_{EN/SY}$			0.3	0.5	µA
Pull-Down Current				0.3	0.5	µA
ERROR/COMPENSATION AMPLIFIERS						
Input Offset Voltage	V_{OS1}	V_{CM1} = 1.5 V, $V_{OS1} = V_{IN1P} - V_{IN1N}$		10	100	µV
	V_{OS2}	V_{CM2} = 1.5 V, $V_{OS2} = V_{IN2P} - V_{IN2N}$		10	100	µV
Input Voltage Range	V_{CM1}, V_{CM2}		0		V_{VDD}	V
Common-Mode Rejection Ratio (CMRR)	$CMRR_1$, $CMRR_2$	V_{CM1}, V_{CM2} = 0.2 V to V_{VDD} − 0.2 V		120		dB
Output Voltage						
High	V_{OH1}, V_{OH2}		V_{VDD} − 0.04			V
Low	V_{OL1}, V_{OL2}				10	mV
Power Supply Rejection Ratio (PSRR)	$PSRR_1$, $PSRR_2$			120		dB
Output Current	I_{OUT1}, I_{OUT2}	Sourcing and sinking	5			mA
Gain Bandwidth Product[1]	GBW_1, GBW_2	V_{OUT1}, V_{OUT2} = 0.5 V to V_{VDD} − 1 V		2		MHz
TEC CURRENT LIMIT						
ILIM Input Voltage Range						
Cooling	V_{ILIMC}		1.3		V_{VREF} − 0.2	V
Heating	V_{ILIMH}		0.2		1.2	V
Current-Limit Threshold						
Cooling	V_{ILIMC_TH}	V_{ITEC} = 0.5 V	1.98	2.0	2.02	V
Heating	V_{ILIMH_TH}	V_{ITEC} = 2 V	0.48	0.5	0.52	V
ILIM Input Current						
Heating	I_{ILIMH}		−0.2		+0.2	µA
Cooling	I_{ILIMC}	Sourcing current	37.5	40	42.5	µA
Cooling to Heating Current Detection Threshold	$I_{COOL_HEAT_TH}$			40		mA
TEC VOLTAGE LIMIT						
Voltage Limit Gain	A_{VLIM}	$(V_{DRL} - V_{SFB})/V_{VLIM}$		2		V/V
VLIM/SD Input Voltage Range[1]	V_{VLIMC}, V_{VLIMH}		0.2		$V_{VDD}/2$	V
VLIM/SD Input Current						
Cooling	I_{ILIMC}	$V_{OUT2} < V_{VREF}/2$	−0.2		+0.2	µA
Heating	I_{ILIMH}	$V_{OUT2} > V_{VREF}/2$, sinking current	8	10	12	µA
TEC CURRENT MEASUREMENT						
Current Sense Gain	R_{CS}			0.285		V/A
Current Measurement Accuracy	I_{LDR_ERROR}	1 A ≤ I_{LDR} ≤ 3 A	15		15	%
ITEC Voltage Accuracy	$V_{ITEC_AT_1_A}$	Cooling, $V_{VREF}/2 + I_{LDR} \times R_{CS}$	1.493	1.535	1.577	V
ITEC Voltage Output Range	V_{ITEC}	I_{TEC} = 0 A	0		V_{VREF} − 0.05	V
ITEC Bias Voltage	V_{ITEC_B}	I_{LDR} = 0 A	1.210	1.250	1.285	V
Maximum ITEC Output Current	I_{ITEC}		−2		+2	mA
TEC VOLTAGE MEASUREMENT						
Voltage Sense Gain	A_{VTEC}		0.24	0.25	0.26	V/V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Voltage Measurement Accuracy	$V_{VTEC_AT_1_V}$	$V_{LDR} - V_{SFB} = 1$ V, $V_{VREF}/2 + A_{VTEC} \times (V_{LDR} - V_{SFB})$	1.475	1.50	1.525	V
VTEC Output Voltage Range	V_{VTEC}		0.005		2.625	V
VTEC Bias Voltage	V_{VTEC_B}	$V_{LDR} = V_{SFB}$	1.225	1.250	1.285	V
Maximum VTEC Output Current	R_{VTEC}		−2		+2	mA
TEMPERATURE GOOD						
TMPGD Output Voltage		No load				
Low	V_{TMPGD_LO}				0.4	V
High	V_{TMPGD_HO}		2.0			V
TMPGD Output Impedance						
Low	R_{TMPGD_LOW}			25		Ω
High	R_{TMPGD_LOW}			50		Ω
Threshold		IN2N tied to OUT2, V_{IN2P} = 1.5 V				
High	V_{OUT1_THH}			1.54	1.56	V
Low	V_{OUT1_THL}		1.40	1.46		V
INTERNAL SOFT START						
Soft Start Time	t_{SS}			150		ms
VLIM/SD SHUTDOWN						
Low Voltage Threshold	V_{VLIM/SD_THL}				0.07	V
THERMAL SHUTDOWN						
Threshold	T_{SHDN_TH}			170		°C
Hysteresis	T_{SHDN_HYS}			17		°C

[1] This specification is guaranteed by design.
[2] This specification is guaranteed by characterization.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
PVINL to PGNDL	−0.3 V to +6 V
PVINS to PGNDS	−0.3 V to +6 V
LDR to PGNDL	−0.3 V to V_{PVINL}
SW to PGNDS	−0.3 V to +6 V
SFB to AGND	−0.3 V to V_{VDD}
AGND to PGNDL	−0.3 V to +0.3 V
AGND to PGNDS	−0.3 V to +0.3 V
VLIM/SD to AGND	−0.3 V to V_{VDD}
ILIM to AGND	−0.3 V to V_{VDD}
VREF to AGND	−0.3 V to +3 V
VDD to AGND	−0.3 V to +6 V
IN1P to AGND	−0.3 V to V_{VDD}
IN1N to AGND	−0.3 V to V_{VDD}
OUT1 to AGND	−0.3 V to +6 V
IN2P to AGND	−0.3 V to V_{VDD}
IN2N to AGND	−0.3 V to V_{VDD}
OUT2 to AGND	−0.3 V to +6 V
EN/SY to AGND	−0.3 V to V_{VDD}
ITEC to AGND	−0.3 V to +6 V
VTEC to AGND	−0.3 V to +6 V
Maximum Current	
VREF to AGND	20 mA
OUT1 to AGND	50 mA
OUT2 to AGND	50 mA
ITEC to AGND	50 mA
VTEC to AGND	50 mA
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages, and is based on a 4-layer standard JEDEC board.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JT}	Ψ_{JB}	Unit
36-Lead LFCSP	33	1.2	12.3	°C/W

MAXIMUM POWER DISSIPATION

The maximum power that the ADN8835 can dissipate is limited by the associated rise in junction temperature. The maximum safe junction temperature for a plastic encapsulated device is determined by the glass transition temperature of the plastic, approximately 125°C. Exceeding this limit may cause a shift in parametric performance or device failure.

The driver stage of the ADN8835 is designed for maximum load current capability. To ensure proper operation, it is necessary to observe the corresponding maximum power derating curves.

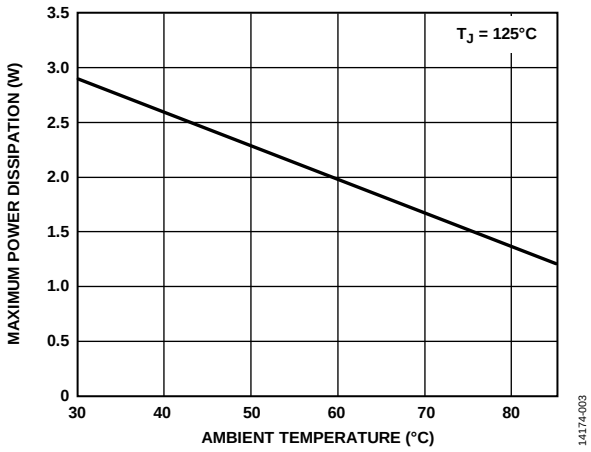


Figure 3. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

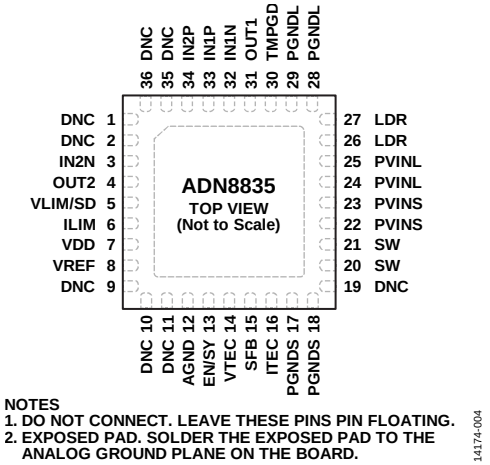


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	EPAD	Exposed Pad. Solder the exposed pad to the analog ground plane on the board.
1, 2, 9, 10, 11, 19, 35, 36	DNC	Do Not Connect. Leave these pins floating.
3	IN2N	Inverting Input of the Compensation Amplifier.
4	OUT2	Output of the Compensation Amplifier.
5	VLIM/SD	Voltage Limit/Shutdown. This pin sets the cooling and heating TEC voltage limits. When this pin is pulled low, the device shuts down.
6	ILIM	Current Limit. This pin sets the TEC cooling and heating current limits.
7	VDD	Power for the Controller Circuits.
8	VREF	2.5 V Reference Output.
12	AGND	Signal Ground.
13	EN/SY	Enable/Synchronization. Set this pin high to enable the device. An external synchronization clock input can be applied to this pin.
14	VTEC	TEC Voltage Output.
15	SFB	Feedback of the PWM TEC Controller Output.
16	ITEC	TEC Current Output.
17, 18	PGNDS	Power Ground of the PWM TEC Controller.
20, 21	SW	Switch Node Output of the PWM TEC Controller.
22, 23	PVINS	Power Input for the PWM TEC Driver.
24, 25	PVINL	Power Input for the Linear TEC Driver.
26, 27	LDR	Output of the Linear TEC Controller.
28, 29	PGNDL	Power Ground of the Linear TEC Controller.
30	TMPGD	Temperature Good Output.
31	OUT1	Output of the Error Amplifier.
32	IN1N	Inverting Input of the Error Amplifier.
33	IN1P	Noninverting Input of the Error Amplifier.
34	IN2P	Noninverting Input of the Compensation Amplifier.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

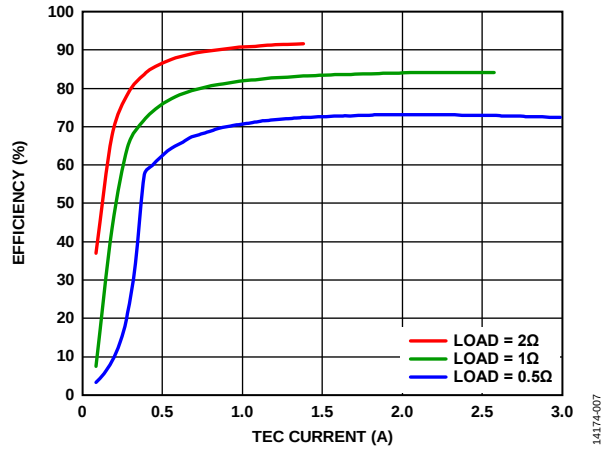


Figure 5. Efficiency vs. TEC Current at V_{IN} = 3.3 V at Various Loads in Cooling Mode

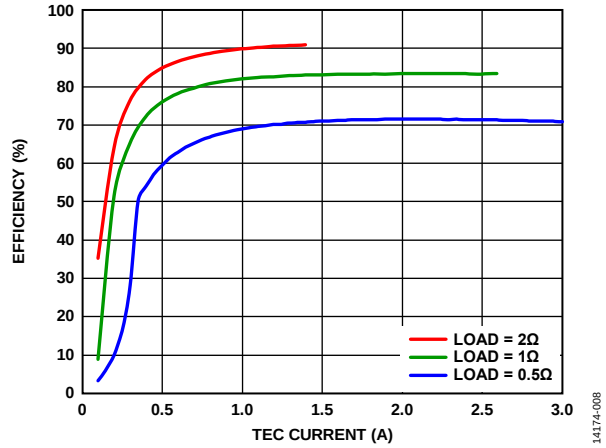


Figure 6. Efficiency vs. TEC Current at V_{IN} = 3.3 V at Various Loads in Heating Mode

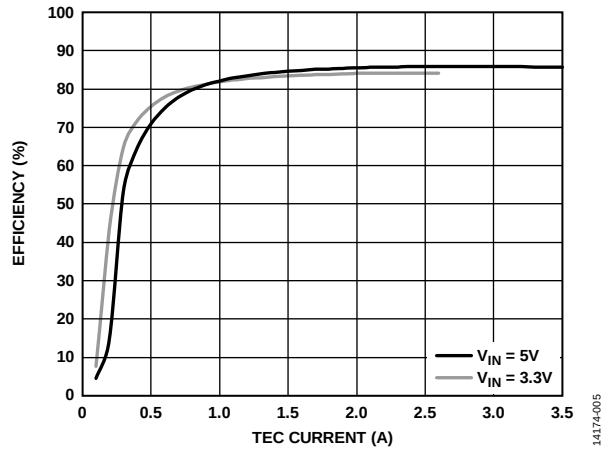


Figure 7. Efficiency vs. TEC Current at V_{IN} = 3.3 V and 5 V in Cooling Mode with 1 Ω Load

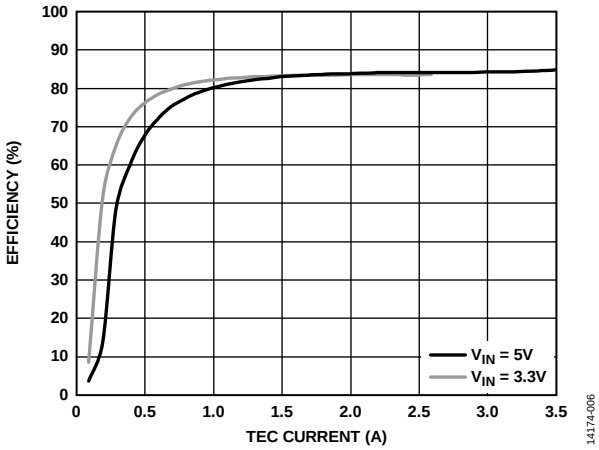


Figure 8. Efficiency vs. TEC Current at V_{IN} = 3.3 V and 5 V in Heating Mode with 1 Ω Load

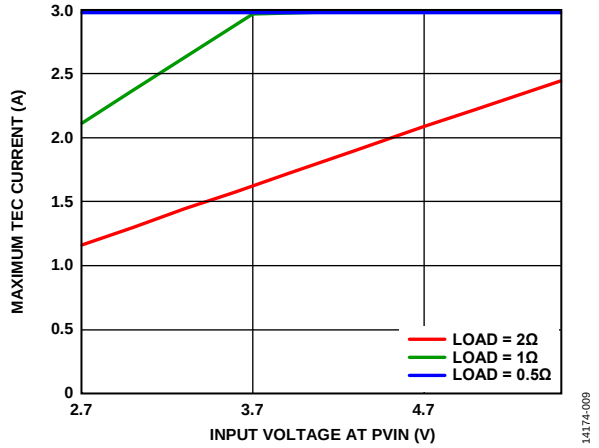


Figure 9. Maximum TEC Current vs. Input Voltage at PVIN at Various Loads, Without Voltage and Current Limit

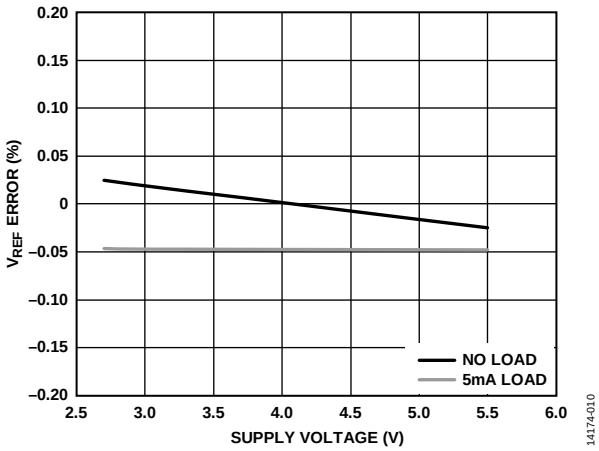


Figure 10. V_{REF} Line Regulation

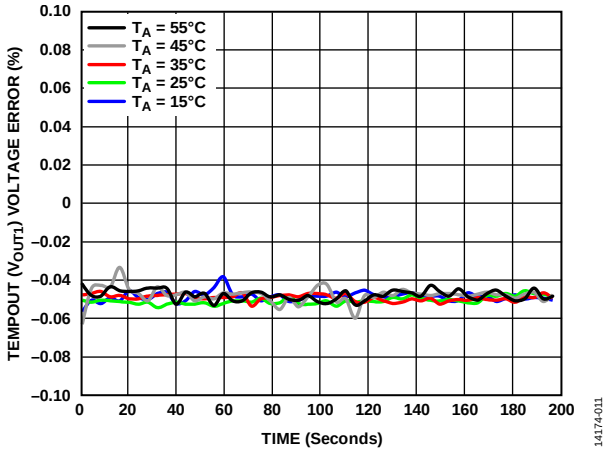


Figure 11. Thermal Stability (TEMPOUT) Voltage Error at Various Ambient Temperatures, V_{IN} = 3.3 V, $V_{TEMPSET}$ = 1 V

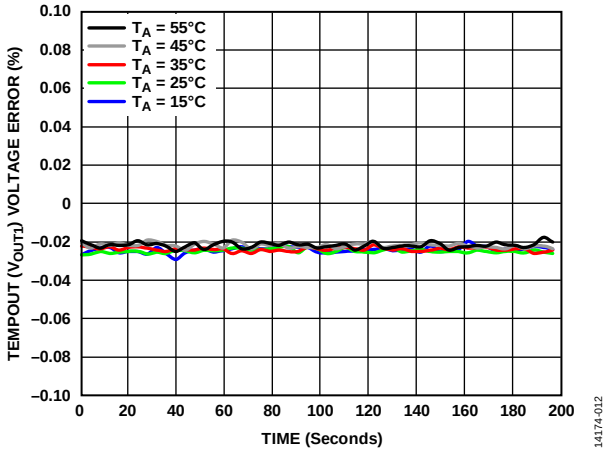


Figure 12. Thermal Stability (TEMPOUT) Voltage Error at Various Ambient Temperatures, V_{IN} = 3.3 V, $V_{TEMPSET}$ = 1.5 V

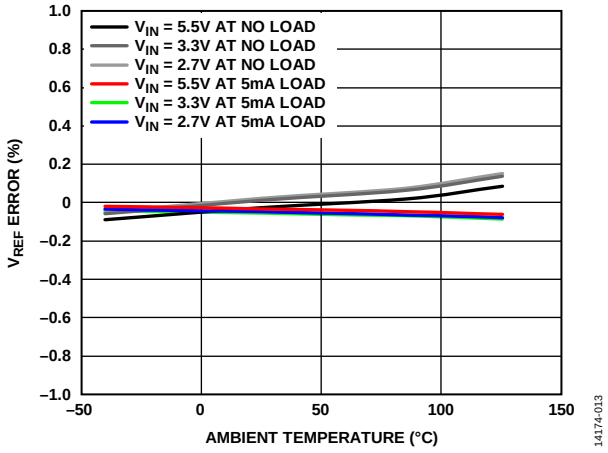


Figure 13. V_{REF} Error vs. Ambient Temperature

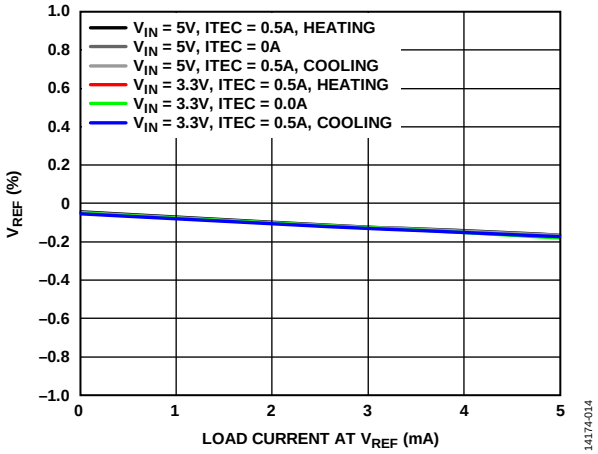


Figure 14. V_{REF} Load Regulation

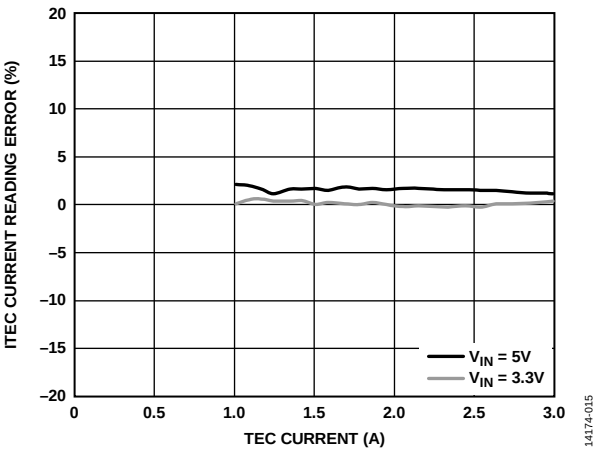


Figure 15. ITEC Current Reading Error vs. TEC Current in Cooling Mode

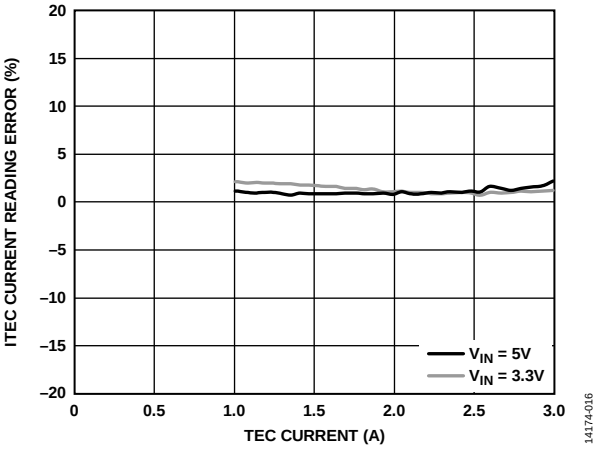


Figure 16. ITEC Current Reading Error vs. TEC Current in Heating Mode

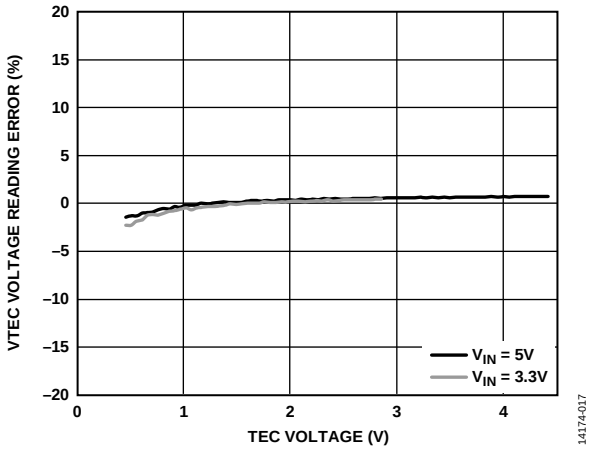


Figure 17. VTEC Voltage Reading Error vs. TEC Voltage in Cooling Mode

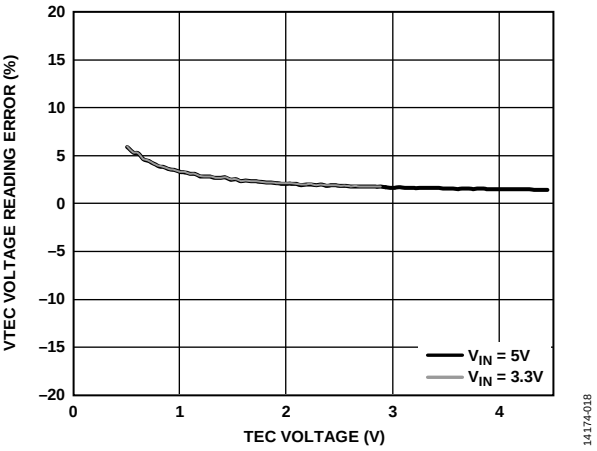


Figure 18. VTEC Voltage Reading Error vs. TEC Voltage in Heating Mode

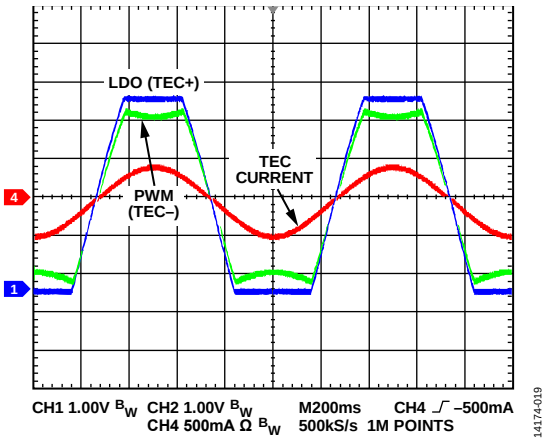


Figure 19. Cooling to Heating Transition

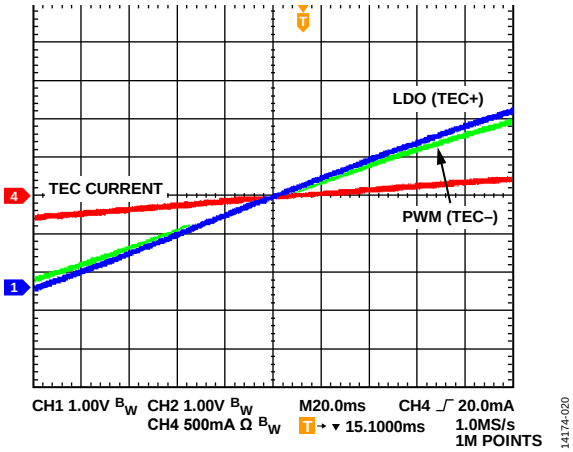


Figure 20. Zero-Crossing TEC Current Zoom In from Heating to Cooling

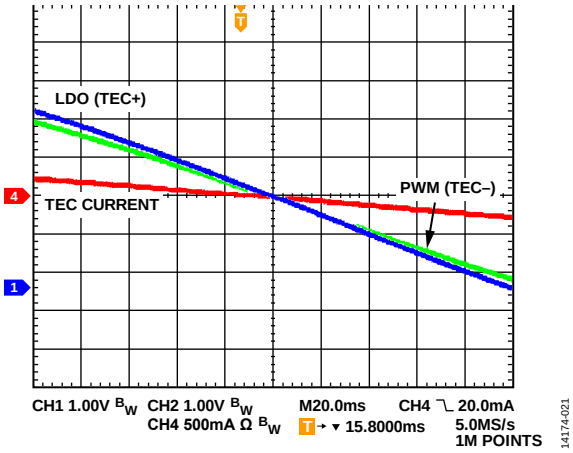


Figure 21. Zero-Crossing TEC Current Zoom In from Cooling to Heating

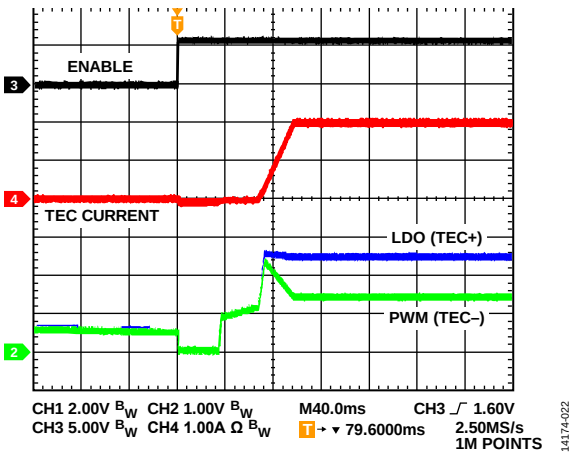


Figure 22. Typical Enable Waveforms in Cooling Mode, V_{IN} = 5 V, Load = 1 Ω, TEC Current = 2 A

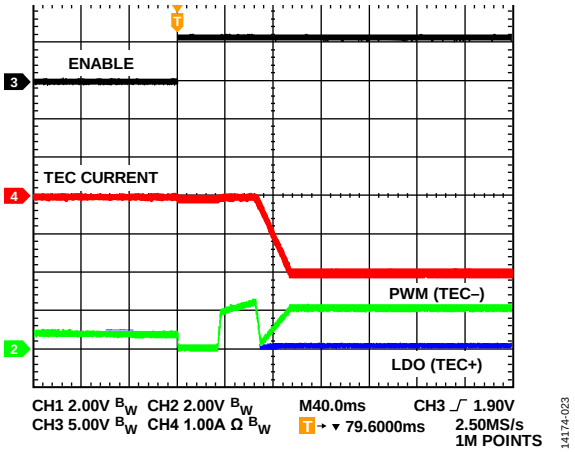


Figure 23. Typical Enable Waveforms in Heating Mode, V_{IN} = 5 V, Load = 1 Ω, TEC Current = 2 A

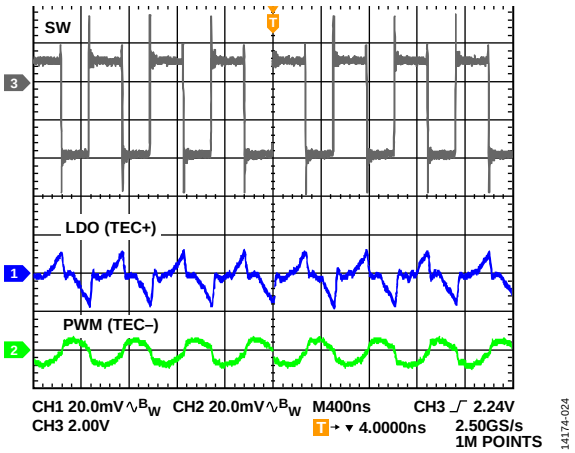


Figure 24. Typical Switch and Voltage Ripple Waveforms in Cooling Mode V_{IN} = 5 V, Load = 1 Ω, TEC Current = 2 A

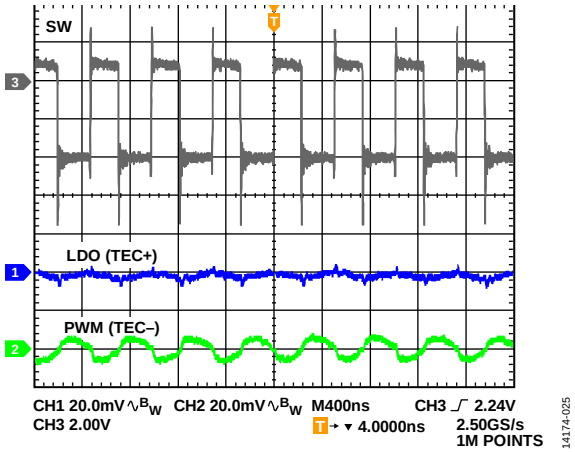


Figure 25. Typical Switch and Voltage Ripple Waveforms in Heating Mode, V_{IN} = 5 V, Load = 1 Ω, TEC Current = 2 A

THEORY OF OPERATION

The ADN8835 is a single-chip TEC controller that sets and stabilizes a TEC temperature. A voltage applied to the input of the ADN8835 corresponds to the temperature setpoint of the target object attached to the TEC. The ADN8835 controls an internal FET H bridge whereby the direction of the current fed through the TEC can be either positive (for cooling mode) to pump heat away from the object attached to the TEC, or negative (for heating mode) to pump heat into the object attached to the TEC.

Temperature is measured with a thermal sensor attached to the target object, and the sensed temperature (voltage) is fed back to the ADN8835 to complete a closed thermal control loop of the TEC. For the best overall stability, couple the thermal sensor close to the TEC. In most laser diode modules, a TEC and a NTC thermistor are already mounted in the same package to regulate the laser diode temperature.

The TEC is differentially driven in an H bridge configuration.

The ADN8835 drives its internal MOSFET transistors to provide the TEC current. To provide good power efficiency and zero-crossing quality, only one side of the H bridge uses a PWM driver. Only one inductor and one capacitor are required to filter out the switching frequency. The other side of the H bridge uses a linear output without requiring any additional circuitry. This proprietary configuration allows the ADN8835 to provide efficiency of >90%. For most applications, a 1 µH inductor, a 10 µF capacitor, and a switching frequency of 2.0 MHz maintain less than 1% of the worst-case output voltage ripple across a TEC.

The maximum voltage across the TEC and the current flowing through the TEC are set by using the VLIM/SD and ILIM pins. The maximum cooling and heating currents can be set independently to allow asymmetric heating and cooling limits. For additional details, see the Maximum TEC Voltage Limit section and the Maximum TEC Current Limit section.

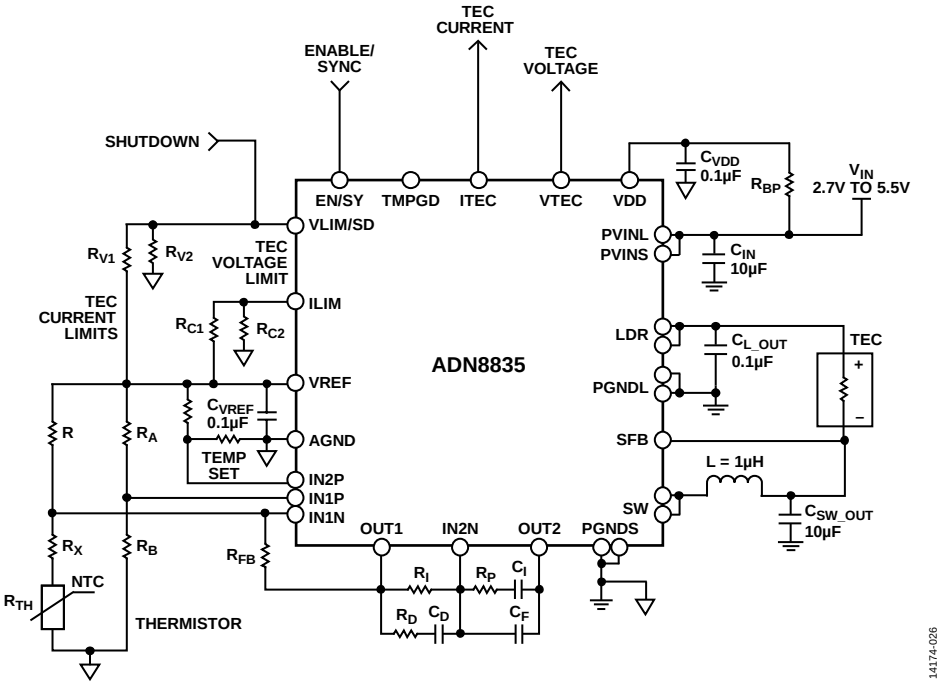


Figure 26. Typical Application Circuit with Analog PID Compensation in a Temperature Control Loop

ANALOG PID CONTROL

The ADN8835 integrates two self correcting, auto-zeroing amplifiers (Chopper 1 and Chopper 2). The Chopper 1 amplifier takes a thermal sensor input and converts or regulates the input to a linear voltage output. The OUT1 voltage is proportional to the object temperature. The OUT1 voltage is fed into the compensation amplifier (Chopper 2) and is compared with a temperature setpoint voltage, which creates an error voltage that is proportional to the difference. For autonomous analog temperature control, Chopper 2 can implement a PID network as shown in Figure 26 to set the overall stability and response of the thermal loop. Adjusting the PID network optimizes the step response of the TEC control loop. A compromised settling time and the maximum current ringing become available when this adjustment is done. To adjust the compensation network, see the PID Compensation Amplifier (Chopper 2) section.

DIGITAL PID CONTROL

The ADN8835 can also be configured for use in a software controlled PID loop. In this scenario, the Chopper 1 amplifier can either be left unused or configured as a thermistor input amplifier connected to an external temperature measurement analog-to-digital converter (ADC). For more information, see the Thermistor Amplifier (Chopper 1) section. If Chopper 1 is left unused, tie IN1N and IN1P to AGND.

The Chopper 2 amplifier is used as a buffer for the external DAC, which controls the temperature setpoint. Connect the DAC to IN2P and short the IN2N and OUT2 pins together. See Figure 27 for an overview of how to configure the ADN8835 external circuitry for digital PID control.

POWERING THE CONTROLLER

The ADN8835 operates at an input voltage range of 2.7 V to 5.5 V that is applied to the PVINS pins and PVINL pins. The VDD pin is the input power for the driver and internal reference. The PVINS and the PVINL input power pins are for the PWM driver and the linear driver, respectively. Apply the same input voltage to all power input pins. In some circumstances, an RC low-pass filter can be added between the PVINS/PVINL and the VDD pins to prevent high frequency noise from entering VDD, as shown in Figure 27. The capacitor and resistor values are typically 10 Ω and 0.1 µF, respectively.

When configuring the power supply to the ADN8835, keep in mind that at high current loads, the input voltage may drop substantially due to a voltage drop on the wires between the front-end power supply and the PVINS and the PVINL pins. Leave a proper voltage margin when designing the front-end power supply to maintain the performance. Minimize the trace length from the power supply to the PVINS and the PVINL pins to help mitigate the voltage drop.

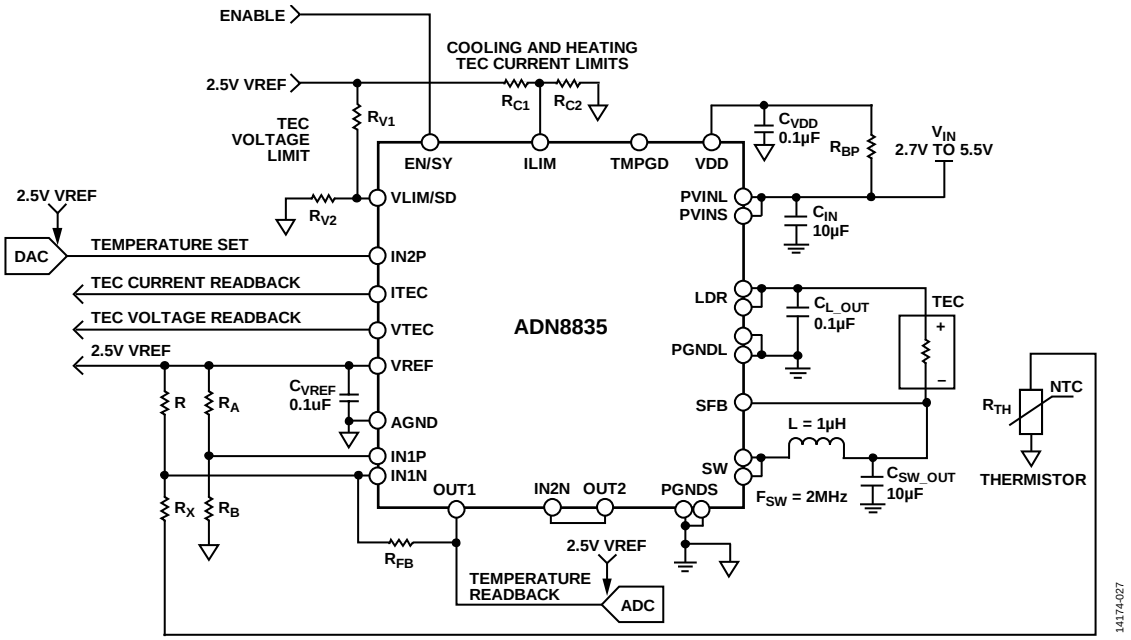


Figure 27. TEC Controller in a Digital Temperature Control Loop

ENABLE AND SHUTDOWN

To enable the ADN8835, apply a logic high voltage to the EN/SY pin while the voltage at the VLIM/SD pin is above the maximum shutdown threshold of 0.07 V. If either the EN/SY pin voltage is set to logic low or the VLIM/SD voltage is below 0.07 V, the controller goes into an ultralow current state. The current drawn in shutdown mode is 350 µA typically. Most of the current is consumed by the VREF circuit block, which is always on even when the device is disabled or shut down. The device can also be enabled when an external synchronization clock signal is applied to the EN/SY pin, and the voltage at VLIM/SD input is above 0.07 V. Table 6 shows the combinations of the two input signals that are required to enable the ADN8835.

Table 6. Enable Pin Combinations

EN/SY Input	VLIM/SD Input	Controller
>2.1 V	>0.07 V	Enabled
Switching Between High (>2.1 V) and Low (<0.8 V)	>0.07 V	Enabled
<0.8 V	No effect[1]	Shutdown
Floating	No effect[1]	Shutdown
No effect[1]	≤0.07 V	Shutdown

[1] No effect means this signal has no effect in shutting down or in enabling the device.

OSCILLATOR CLOCK FREQUENCY

The ADN8835 has an internal oscillator that generates a 2.0 MHz switching frequency for the PWM output stage. This oscillator is active when the enabled voltage at the EN/SY pin is set to a logic level higher than 2.1 V and the VLIM/SD pin voltage is greater than the shutdown threshold of 0.07 V.

External Clock Operation

The PWM switching frequency of the ADN8835 can be synchronized to an external clock from 1.85 MHz to 3.25 MHz, applied to the EN/SY input pin, as shown on Figure 28.

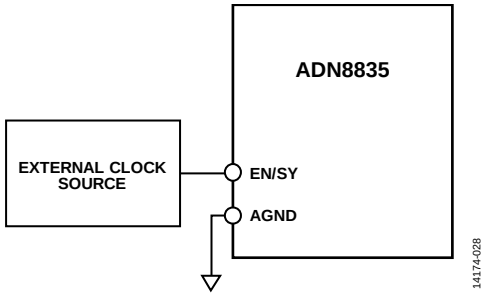


Figure 28. Synchronize to an External Clock

Connecting Multiple ADN8835 Devices

Multiple ADN8835 devices can be driven from a single master clock signal by connecting the external clock source to the EN/SY pin of each slave device. The input ripple can be greatly reduced by operating the ADN8835 devices 180° out of phase from each other and placing an inverter at one of the EN/SY pins, as shown in Figure 29.

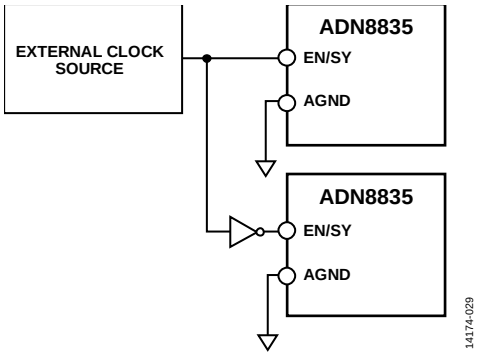


Figure 29. Multiple ADN8835 Devices Driven from a Master Clock

TEMPERATURE LOCK INDICATOR

The TMPGD pin outputs logic high when the temperature error amplifier output voltage, V_{OUT1}, reaches the IN2P temperature setpoint (TEMPSET) voltage. The TMPGD pin has a detection range between 1.46 V and 1.54 V of V_{OUT1} and hysteresis. The TMPGD function allows direct interfacing either to the microcontrollers or to the supervisory circuitry.

SOFT START ON POWER-UP

The ADN8835 has an internal soft start circuit that generates a ramp with a typical 150 ms profile to minimize inrush current during power-up. The settling time and the final voltage across the TEC depends on the TEC voltage required by the control voltage of voltage loop. The higher the TEC voltage is, the longer it requires to increase.

When the ADN8835 is first powered up, the linear side discharges the output of any prebias voltage. As soon as the prebias is eliminated, the soft start cycle begins. During the soft start cycle, both the PWM and linear outputs track the internal soft start ramp until they reach midscale, where the control voltage, V_C, is equal to the bias voltage, V_B. From the midscale voltage, the PWM and linear outputs are then controlled by V_C and diverge from each other until the required differential voltage is developed across the TEC or the differential voltage reaches the voltage limit. The voltage developed across the TEC depends on the control point at that moment in time. Figure 30 shows an example of the soft start profile in cooling mode. Note that, as both the LDR and SFB voltages increase with the soft start ramp and approach V_B, the ramp slows to avoid possible current overshoot at the point where the TEC voltage starts to increase.

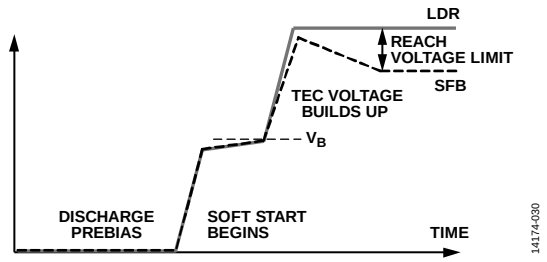


Figure 30. Soft Start Profile in Cooling Mode

TEC VOLTAGE/CURRENT MONITOR

The TEC real-time voltage and current are detectable at VTEC and ITEC, respectively.

Voltage Monitor

VTEC is an analog voltage output pin with a voltage proportional to the actual voltage across the TEC. A center VTEC voltage of 1.25 V corresponds to 0 V across the TEC. Convert the voltage at VTEC and the voltage across the TEC using the following equation:

$$V_{VTEC} = 1.25\ V + 0.25 \times (V_{LDR} - V_{SFB})$$

Current Monitor

ITEC is an analog voltage output pin with a voltage proportional to the actual current through the TEC. A center ITEC voltage of 1.25 V corresponds to 0 A through the TEC. Convert the voltage at ITEC and the current through the TEC using the following equations:

$$V_{ITEC_COOLING} = 1.25\ V + I_{LDR} \times R_{CS}$$

where the current sense gain (R_{CS}) is 0.285 V/A.

$$V_{ITEC_HEATING} = 1.25\ V - I_{LDR} \times R_{CS}$$

MAXIMUM TEC VOLTAGE LIMIT

The maximum TEC voltage is set by applying a voltage divider at the VLIM/SD pin to protect the TEC. The voltage limiter operates bidirectionally and allows the cooling limit to be different from the heating limit.

Using a Resistor Divider to Set the TEC Voltage Limit

Separate voltage limits are set using a resistor divider. The internal current sink circuitry connected to VLIM/SD draws a current when the ADN8835 drives the TEC in a heating direction, which lowers the voltage at VLIM/SD. The current sink is not active when the TEC is driven in a cooling direction; therefore, the TEC heating voltage limit is always lower than the cooling voltage limit.

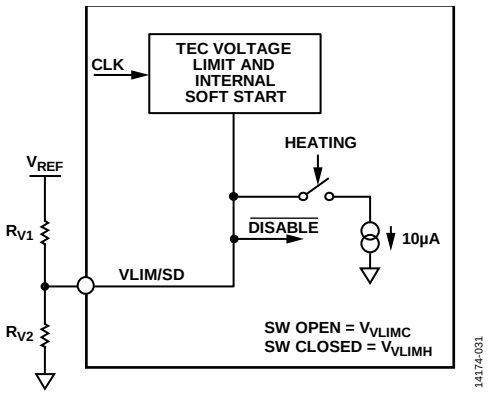


Figure 31. Using a Resistor Divider to Set the TEC Voltage Limit

Calculate the cooling and heating limits using the following equations:

$$V_{VLIMC} = V_{REF} \times R_{V2}/(R_{V1} + R_{V2})$$

where V_{REF} = 2.5 V.

$$V_{VLIMH} = V_{VLIMC} - I_{LIMH} \times R_{V1}||R_{V2}$$

where I_{LIMH} = 10 µA.

$$V_{TEC_MAX_COOLING} = V_{VLIMC} \times A_{VLIM}$$

where A_{VLIM} = 2 V/V.

$$V_{TEC_MAX_HEATING} = V_{VLIMH} \times A_{VLIM}$$

MAXIMUM TEC CURRENT LIMIT

To protect the TEC, separate maximum TEC current limits in cooling and heating directions are set by applying a voltage combination at the ILIM pin.

Using a Resistor Divider to Set the TEC Current Limit

The internal current sink circuitry connected to ILIM draws a 40 µA current when the ADN8835 drives the TEC in a cooling direction, which allows a high cooling current. Use the following equations to calculate the maximum TEC currents:

$$V_{ILIMH} = V_{REF} \times R_{C2}/(R_{C1} + R_{C2})$$

where V_{REF} = 2.5 V.

$$V_{ILIMC} = V_{ILIMH} + I_{LIMC} \times R_{C1}||R_{C2}$$

where I_{LIMC} = 40 µA.

$$I_{TEC_MAX_COOLING} = \frac{V_{ILIMC} - 1.25\ V}{R_{CS}}$$

where R_{CS} = 0.285 V/A.

$$I_{TEC_MAX_HEATING} = \frac{1.25\ V - V_{ILIMH}}{R_{CS}}$$

V_{ILIMH} must not exceed 1.2 V and V_{ILIMC} must be more than 1.3 V to leave proper margins between the heating and the cooling modes.

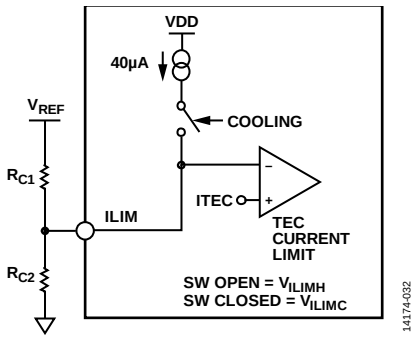


Figure 32. Using a Resistor Divider to Set the TEC Current Limit

APPLICATIONS INFORMATION

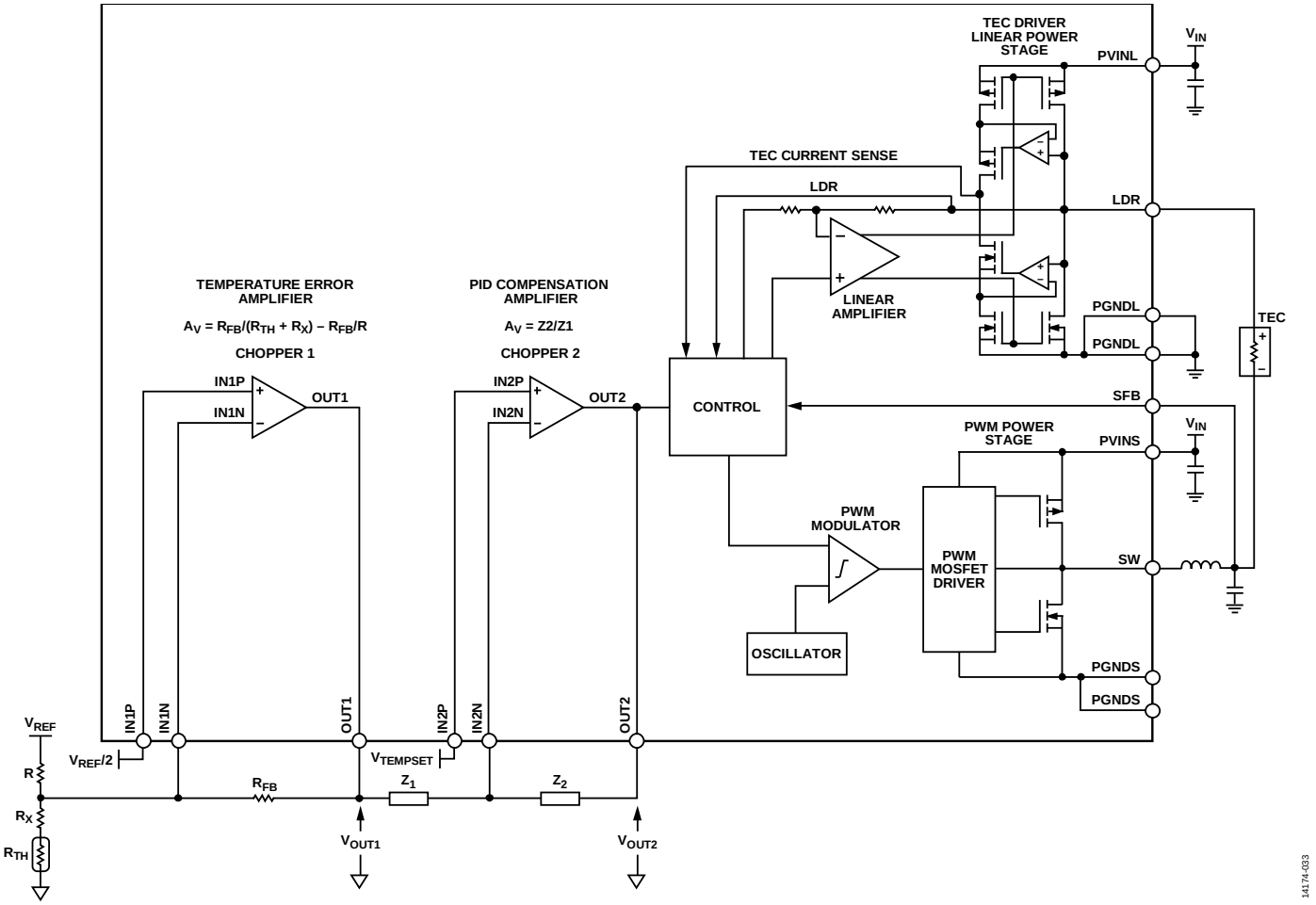


Figure 33. Signal Flow Block Diagram

SIGNAL FLOW

The ADN8835 integrates two auto-zero amplifiers, defined as the Chopper 1 amplifier and the Chopper 2 amplifier. Both of the amplifiers can be used as standalone amplifiers; therefore, the implementation of temperature control can vary. Figure 33 shows the signal flow through the ADN8835, and a typical implementation of the temperature control loop using the Chopper 1 amplifier and the Chopper 2 amplifier.

In Figure 33, the Chopper 1 and Chopper 2 amplifiers are configured as the thermistor input amplifier and the PID compensation amplifier, respectively. The thermistor input amplifier amplifies the thermistor voltage, and then outputs to the PID compensation amplifier. The PID compensation amplifier then compensates a loop response over the frequency domain.

The output from the compensation loop at OUT2 is fed to the linear MOSFET gate driver. The voltage at LDR is fed with OUT2 into the PWM MOSFET gate driver. Including the internal transistors, the gain of the differential output section is fixed at 5. For details on the output drivers, see the MOSFET Driver Amplifier section.

THERMISTOR SETUP

The thermistor has a nonlinear relationship to temperature; near optimal linearity over a specified temperature range can be achieved with the proper value of a compensation resistor, R_X, placed in series with the thermistor.

First, the resistance of the thermistor must be known, where

- $R_{LOW} = R_{TH}$ at T_{LOW}
- $R_{MID} = R_{TH}$ at T_{MID}
- $R_{HIGH} = R_{TH}$ at T_{HIGH}

T_{LOW} and T_{HIGH} are the endpoints of the temperature range and T_{MID} is the average. In some cases, with only the β constant available, calculate R_{TH} using the following equation:

$$R_{TH} = R_R \exp\left(\beta\left(\frac{1}{T} - \frac{1}{T_R}\right)\right)$$

where:
R_{TH} is a resistance at T (K).
R_R is a resistance at T_R (K).

Calculate R_X using the following equation:

$$R_X = \left(\frac{R_{LOW}R_{MID} + R_{MID}R_{HIGH} - 2R_{LOW}R_{HIGH}}{R_{LOW} + R_{HIGH} - 2R_{MID}} \right)$$

THERMISTOR AMPLIFIER (CHOPPER 1)

The Chopper 1 amplifier can be used as a thermistor input amplifier. In Figure 33, the output voltage is a function of the thermistor temperature. The voltage at OUT1 is expressed as:

$$V_{OUT1} = \left(\frac{R_{FB}}{R_{TH} + R_X} - \frac{R_{FB}}{R} + 1 \right) \times \frac{V_{REF}}{2}$$

where:
R_{FB} is the feedback resistor.
R_{TH} is a thermistor.
R_X is a compensation resistor.

Calculate R using the following equation:

$$R = R_X + R_{TH_AT_25°C}$$

V_{OUT1} is centered around $V_{VREF}/2$ at 25°C. An average temperature to voltage coefficient is −25 mV/°C at a range of 5°C to 45°C.

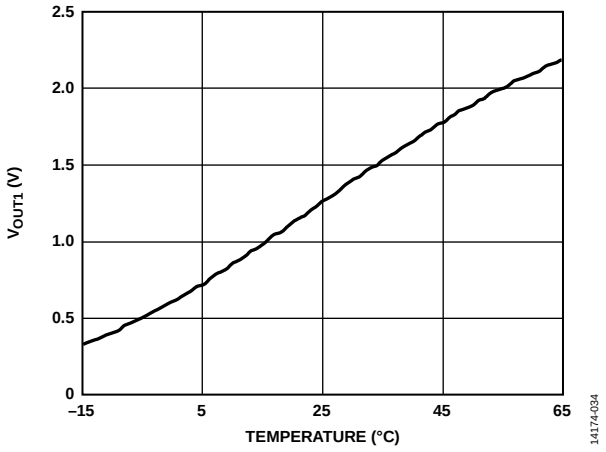


Figure 34. V_{OUT1} vs. Temperature

PID COMPENSATION AMPLIFIER (CHOPPER 2)

Use the Chopper 2 amplifier as the PID compensation amplifier. The voltage at OUT1 feeds into the PID compensation amplifier. The frequency response of the PID compensation amplifier is dictated by the compensation network. Apply the temperature set voltage at IN2P. In Figure 39, the voltage at OUT2 is calculated using the following equation:

$$V_{OUT2} = V_{TEMPSET} - \frac{Z2}{Z1}\left(V_{OUT1} - V_{TEMPSET}\right)$$

where:
$V_{TEMPSET}$ is the temperature setpoint voltage to the IN2P pin.
Z1 is the combination of R_I, R_D, and C_D (see Figure 35).
Z2 is the combination of R_P, C_I, and C_F (see Figure 35).

The user sets the exact compensation network. This network varies from a simple integrator to proportional integral (PI), PID, or any other type of network. The user also determines the type of compensation and component values because they are dependent on the thermal response of the object and the TEC. One method to empirically determine these values is to input a step function to IN2P (thus changing the target temperature), and adjust the compensation network to minimize the settling time of the TEC temperature.

A typical compensation network for temperature control of a laser module is a PID loop consisting of a very low frequency pole and two separate zeros at higher frequencies. Figure 35 shows a simple network for implementing PID compensation. To reduce the noise sensitivity of the control loop, an additional pole is added at a higher frequency than that of the zeros. The bode plot of the magnitude is shown in Figure 36. Use the following equation to calculate the unity-gain crossover frequency of the feedforward amplifier:

$$f_{0dB} = \frac{1}{2\pi R_I C_I} \times \left(\frac{R_{FB}}{R_{TH} + R_X} - \frac{R_{FB}}{R} \right) \times TECGAIN$$

where TECGAIN is the symbolic gain of the TEC module.

TECGAIN is critical to the mathematical design of the PID loop. However, the thermal time constant of the TEC module is usually unspecified, making it difficult to characterize TECGAIN as well as the feedback transfer function. In this case, the PID loop can be determined empirically by tuning the components step by step. There are many documents written on loop stabilization, and it is beyond the scope of this data sheet to discuss all methods and trade-offs for optimizing compensation networks.

V_{OUT1} is a convenient measure to gauge the thermal instability of the system, which is also known as TEMPOUT. If the thermal loop is in steady state, the TEMPOUT voltage equals the TEMPSET voltage, meaning that the temperature of the controlled object equals the target temperature.

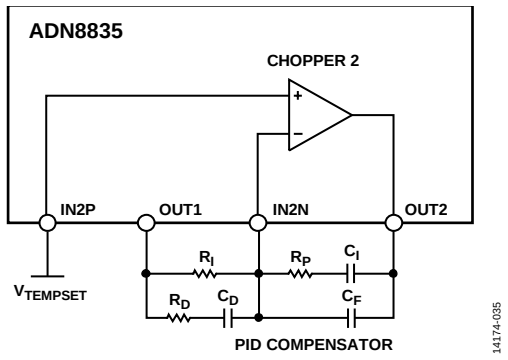


Figure 35. Implementing a PID Compensation Loop

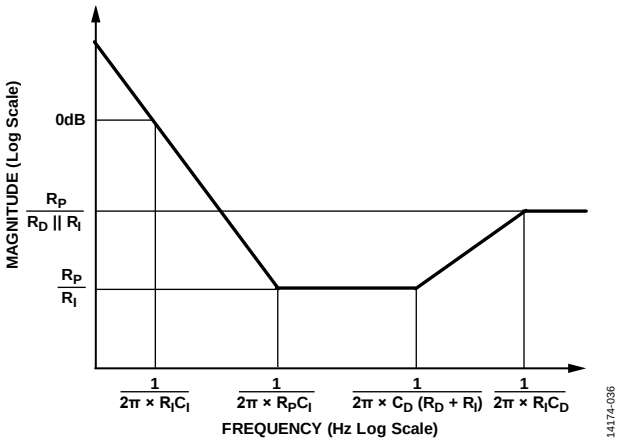


Figure 36. Bode Plot for PID Compensation

MOSFET DRIVER AMPLIFIERS

The ADN8835 has two separate MOSFET drivers: a switched output or PWM amplifier, and a high gain linear amplifier. Each amplifier has a pair of outputs that drive the gates of the internal MOSFETs, which, in turn, drive the TEC as shown in Figure 33. A voltage across the TEC is monitored via the SFB and LDR pins. Although both MOSFET drivers achieve the same result, to provide constant voltage and high current, their operation is different. The exact equations for the two outputs are

$$V_{LDR} = V_B - 80(V_{OUT2} - 1.25\ V)$$

$$V_{SFB} = V_{LDR} + 5(V_{OUT2} - 1.25\ V)$$

where:
V_{OUT2} is the voltage at OUT2.
V_B is determined by V_{VDD} as

V_B = 1.5 V for V_{VDD} < 4.0 V

V_B = 2.5 V for V_{VDD} > 4.0 V

The compensation network that receives the temperature set voltage and the thermistor voltage fed by the input amplifier determines the voltage at OUT2. V_{LDR} and V_{SFB} have a low limit of 0 V and an upper limit of V_{VDD}. Figure 37, Figure 38, and Figure 39 show the graphs of these equations.

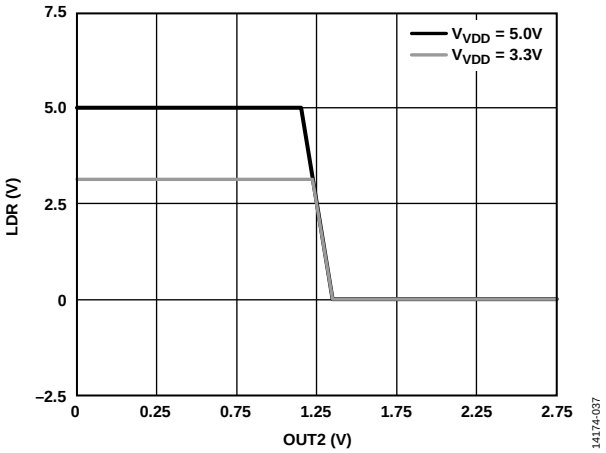


Figure 37. LDR Voltage vs. OUT2 Voltage

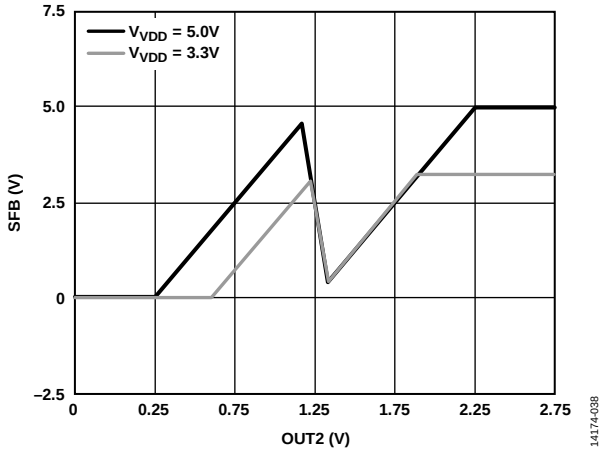


Figure 38. SFB Voltage vs. OUT2 Voltage

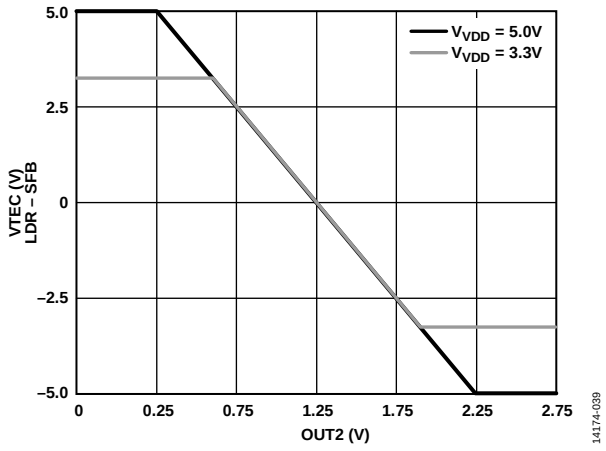


Figure 39. TEC Voltage (LDR – SFB) vs. OUT2 Voltage

PWM OUTPUT FILTER REQUIREMENTS

A Type III compensator internally compensates the PWM amplifier. Because the poles and zeros of the compensator are designed and fixed by assuming the resonance frequency of the output LC tank is 50 kHz, the selection of the inductor and the capacitor must follow this guideline to ensure system stability.

Inductor Selection

The inductor selection determines the inductor current ripple and loop dynamic response. Larger inductance results in smaller current ripple and slower transient response because smaller inductance results in the opposite performance. To optimize the performance, the trade-off must be made between transient response speed, efficiency, and component size. Calculate the inductor value with the following equation:

$$L = \frac{V_{SW_OUT} \times (V_{IN} - V_{SW_OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

where:
V_{SW_OUT} is the PWM amplifier output.
f_{SW} is the switching frequency (2 MHz by default).
ΔI_L is the inductor current ripple.

A 1 µH inductor is typically recommended to allow reasonable output capacitor selection while maintaining a low inductor current ripple. If lower inductance is required, a minimum inductor value of 0.68 µH is suggested to ensure that the current ripple is set to a value between 30% and 40% of the maximum load current.

Except for the inductor value, the equivalent dc resistance (DCR) inherent in the metal conductor is also a critical factor for inductor selection. The DCR accounts for most of the power loss on the inductor by DCR × I_{OUT}^2. Using an inductor with high DCR degrades the overall efficiency significantly. In addition, there is a conduct voltage drop across the inductor because of the DCR. When the PWM amplifier is sinking current in cooling mode, this voltage drives the minimum voltage of the amplifier higher than 0.06 × V_{PVIN} by at least tenth of millivolts. Similarly, the maximum PWM amplifier output voltage is lower than 0.93 × V_{PVIN}.

This voltage drop is proportional to the value of the DCR, and reduces the output voltage range at the TEC.

When selecting an inductor, ensure that the saturation current rating is higher than the maximum current peak to prevent saturation. In general, ceramic multilayer inductors are suitable for low current applications due to small size and low DCR. When the noise level is critical, use a shielded ferrite inductor to reduce the electromagnetic interference (EMI).

Table 7. Recommended Inductors

Vendor	Value	Device No.	Footprint (mm)
Coilcraft	1.0 µH ± 20%	XFL4020-102MEB	4.3 × 4.3
Murata	1.0 µH ± 20%	DFE252012P-1R0M	2.5 × 2.0

Capacitor Selection

The output capacitor selection determines the output voltage ripple, transient response, as well as the loop dynamic response of the PWM amplifier output. Use the following equation to select the capacitor:

$$C = \frac{V_{SW_OUT} \times (V_{IN} - V_{SW_OUT})}{V_{IN} \times 8 \times L \times (f_{SW})^2 \times \Delta V_{OUT}}$$

Note that the voltage caused by the product of current ripple, ΔI_L, and the capacitor equivalent series resistance (ESR) also add up to the total output voltage ripple. Selecting a capacitor with low ESR can increase overall regulation and efficiency performance.

Table 8. Recommended Output Capacitors

Vendor	Value	Device No.	Footprint (mm)
Murata	10 µF ± 10%, 10 V	ZRB18AD71A106KE01L	1.6 × 0.8
Murata	10 µF ± 20%, 10 V	GRM188D71A106MA73	1.6 × 0.8
Taiyo Yuden	10 µF ± 20%, 10 V	LMK107BC6106MA-T	1.6 × 0.8

INPUT CAPACITOR SELECTION

On the PVIN pin, the amplifiers require an input capacitor to decouple the noise and to provide the transient current to maintain a stable input and output voltage. A 10 µF ceramic capacitor rated at 10 V is the minimum recommended value. Increasing the capacitance reduces the switching ripple that couples into the power supply but increases the capacitor size. Because the current at the input terminal of the PWM amplifier is discontinuous, a capacitor with low effective series inductance (ESL) is preferred to reduce voltage spikes.

In most applications, a decoupling capacitor is used in parallel with the input capacitor. The decoupling capacitor is usually a 100 nF ceramic capacitor with very low ESR and ESL, which provides better noise rejection at high frequency bands.

POWER DISSIPATION

This section provides guidelines to calculate the power dissipation of the ADN8835. Approximate the total power dissipation in the device by

$$P_{LOSS} = P_{PWM} + P_{LINEAR}$$

where:
P_{PWM} is the power dissipation in the PWM regulator.
P_{LOSS} is the total power dissipation in the ADN8835.
P_{LINEAR} is the power dissipation in the linear regulator.

PWM Regulator Power Dissipation

The PWM power stage is configured as a buck regulator and its dominant power dissipation (P_{PWM}) includes power switch

conduction losses (P_{COND}), switching losses (P_{SW}), and transition losses (P_{TRAN}). Other sources of power dissipation are usually less significant at the high output currents of the application thermal limit and can be neglected in approximation.

Use the following equation to estimate the power dissipation of the buck regulator:

$$P_{LOSS} = P_{COND} + P_{SW} + P_{TRAN}$$

Conduction Loss (P_{COND})

The conduction loss consists of two parts: inductor conduction loss (P_{COND_L}) and power switch conduction loss (P_{COND_S}).

$$P_{COND} = P_{COND_L} + P_{COND_S}$$

Inductor conduction loss is proportional to the DCR of the output inductor, L. Using an inductor with low DCR enhances the overall efficiency performance. Estimate inductor conduction loss by

$$P_{COND_L} = DCR \times I_{OUT}^2$$

Power switch conduction losses are caused by the flow of the output current through both the high-side and low-side power switches, each of which has its own internal on resistance (R_{DSON}).

Use the following equation to estimate the amount of power switch conduction loss:

$$P_{COND_S} = (R_{DSON_HS} \times D + R_{DSON_LS} \times (1 - D)) \times I_{OUT}^2$$

where:
R_{DSON_HS} is the on resistance of the high-side MOSFET.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).
R_{DSON_LS} is the on resistance of the low-side MOSFET.

Switching Losses (P_{SW})

Switching losses are associated with the current drawn by the controller to turn the power devices on and off at the switching frequency. Each time a power device gate is turned on or off, the controller transfers a charge from the input supply to the gate, and then from the gate to ground. Use the following equation to estimate the switching loss:

$$P_{SW} = (C_{GATE_HS} + C_{GATE_LS}) \times V_{IN}^2 \times f_{SW}$$

where:
C_{GATE_HS} is the gate capacitance of the high-side MOSFET.
C_{GATE_LS} is the gate capacitance of the low-side MOSFET.
f_{SW} is the switching frequency.

For the ADN8835, the total of $C_{GATE_HS} + C_{GATE_LS}$ is approximately 1 nF.

Transition Losses (P_{TRAN})

Transition losses occur because the high-side MOSFET cannot turn on or off instantaneously. During a switch node transition, the MOSFET provides all the inductor current. The source to drain voltage of the MOSFET is half the input voltage, resulting in power loss. Transition losses increase with both load and input voltage and occur twice for each switching cycle.

Use the following equation to estimate the transition loss:

$$P_{TRAN} = 0.5 \times V_{PVIN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}$$

where:
V_{PVIN} is the voltage at PVIN.
I_{OUT} is the output current of the PWM regulator.
t_R is the rise time of the switch node.
t_F is the fall time of the switch node.

Linear Regulator Power Dissipation

In the ADN8835, the output voltage of linear regulator is typically tied either to ground or V_{IN}. The main power dissipation in this case comes from the conduction loss of the FETs and thus is quite low. When the load is light and the linear regulator must operate in a linear region, the power dissipation can be calculated using the following equation:

$$P_{LINEAR} = ((V_{IN} - V_{OUT}) \times I_{OUT}) + (V_{IN} \times I_{GND})$$

where:
V_{IN} and V_{OUT} are the input and output voltages of the linear regulator.
I_{OUT} is the load current of the linear regulator.
I_{GND} is the ground current of the linear regulator.

Power dissipation due to the ground current is generally small and can be ignored for the purposes of this calculation.

THERMAL CONSIDERATION

To ensure that the ADN8835 operates below the maximum junction temperature even at high load, careful attention must be paid to provide a lower θ_{JA} value of the device. Typical techniques for enhancing heat dissipation include using larger copper layer and vias on the printed circuit board (PCB) and adding a heat sink.

The ADN8835 LFCSP package has a large exposed pad (EPAD) at the bottom that must be soldered to the analog ground plane on the board. The majority of the heat of the device dissipates through the EPAD. Therefore, the copper layer connected to the EPAD as well as the vias on it must be optimized to conduct the heat effectively. It is recommended to use at least a 6 × 6 via array and distribute them evenly on the EPAD. Generally, it is more effective to increase the number of vias than to increase the diameter of the via within a limited area.

PCB LAYOUT GUIDELINES

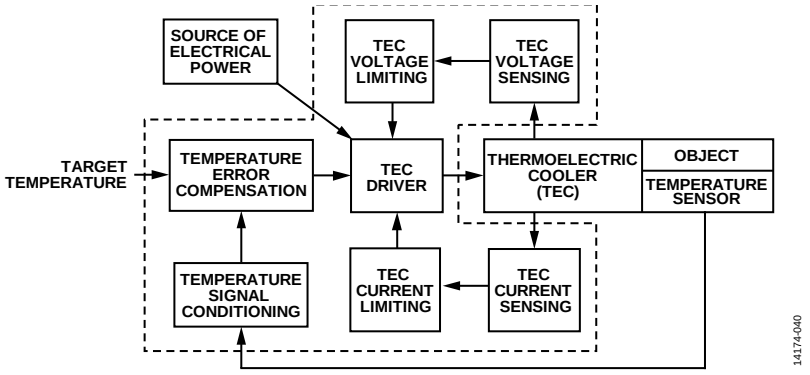


Figure 40. System Block Diagram

BLOCK DIAGRAMS AND SIGNAL FLOW

The ADN8835 integrates analog signal conditioning blocks, a load protection block, and a TEC controller power stage, all in a single IC. To achieve the best possible circuit performance, attention must be paid to keep the noise of the power stage from contaminating the sensitive analog conditioning and protection circuits. In addition, the layout of the power stage must be performed such that the IR losses are minimized to obtain the best possible electrical efficiency.

The system block diagram of the ADN8835 is shown in Figure 40.

GUIDELINES FOR REDUCING NOISE AND MINIMIZING POWER LOSS

Each PCB layout is unique because of the physical constraints defined by the mechanical aspects of a given design. In addition, several other circuits work in conjunction with the TEC controller; these circuits have their own layout requirements. Therefore, there are always compromises that must be made for a given system. However, to minimize noise and keep power losses to a minimum during the PCB layout process, observe the following guidelines.

General PCB Layout Guidelines

Switching noise can interfere with other signals in the system; therefore, the switching signal traces must be placed away from the power stage to minimize the effect. If possible, place the ground plate between the small signal layer and power stage layer as a shield.

Supply voltage drop on traces is also an important consideration because it determines the voltage headroom of the TEC controller at high currents. For example, if the supply voltage from the front-end system is 3.3 V, and the voltage drop on the traces is 0.5 V, PVIN sees only 2.8 V, which limits the maximum voltage of the linear regulator as well as the maximum voltage across the TEC. To mitigate the voltage waste on traces and impedance interconnection, place the ADN8835 and the input decoupling components close to the supply voltage terminal. This placement not only improves the system efficiency but also provides better regulation performance at the output.

To prevent the noise signal from circulating through the ground plates, reference all of the sensitive analog signals to AGND and connect AGND to PGNDS using only a single-point connection. This connection ensures that the switching currents of the power stage do not flow into the sensitive AGND node.

PWM Power Stage Layout Guidelines

The PWM power stage consists of a MOSFET pair that forms a switch mode output that switches current from PVINS to the load via an LC filter. The ripple voltage on the PVINS pin is caused by the discontinuous current switched by the PWM side MOSFETs. This rapid switching causes voltage ripple to form at the PVINS input, which must be filtered using a bypass capacitor. Place a 10 µF capacitor as close as possible to the PVINS pin to connect PVINS to PGNDS. Because the 10 µF capacitor is sometimes bulky and has higher ESR and ESL, a 100 nF decoupling capacitor is usually used in parallel with it, placed between PVINS and PGNDS.

Because the decoupling is part of the pulsating current loop, which carries high di/dt signals, the traces must be short and wide to minimize the parasitic inductance. As a result, this capacitor is usually placed on the same side of the board as the ADN8835 to ensure short connections. If the layout requires that a 10 µF capacitor be on the opposite side of the PCB, use multiple vias to reduce via impedance.

The layout around the SW node is also critical because it switches between PVINS and ground rapidly, which makes this node a strong EMI source. Keep the copper area that connects the SW node to the inductor small to minimize parasitic capacitance between the SW node and other signal traces. The small copper area helps minimize noise on the SW node due to excessive charge injection. However, in high current applications, the copper area can be increased reasonably to provide a heat sink and to sustain high current flow.

Connect the ground side of the capacitor in the LC filter as close as possible to PGNDS to minimize the ESL in the return path.

Linear Power Stage Layout Guidelines

The linear power stage consists of a MOSFET pair that forms a linear amplifier, which operates in linear mode for very low output currents, and changes to fully enhanced mode for greater output currents.

Because the linear power stage does not switch currents rapidly like the PWM power stage, it does not generate noise currents. However, the linear power stage still requires a minimum amount of bypass capacitance to decouple its input.

Place a 100 nF capacitor that connects from PVINL to PGNDL as close as possible to the PVINL pin.

Placing the Thermistor Amplifier and PID Components

The thermistor conditioning and PID compensation amplifiers work with very small signals and have gain; therefore, attention must be paid when placing the external components with these circuits.

Place the thermistor conditioning and PID circuit components close to each other near the inputs of Chopper 1 and Chopper 2. Avoid crossing paths between the amplifier circuits and the power stages to prevent noise pickup on the sensitive nodes. Always reference the thermistor to AGND to have the cleanest connection to the amplifier input and to avoid any noise or offset buildup.

EXAMPLE PCB LAYOUT USING TWO LAYERS

Figure 41, Figure 42, and Figure 43 show an example ADN8835 PCB layout that uses two layers. This layout example achieves a small solution size of approximately 20 mm^2 with all of the conditioning circuitry and PID included. Using more layers and blinds via allows the solution size to be reduced even further because more of the discrete components can relocate to the bottom side of the PCB.

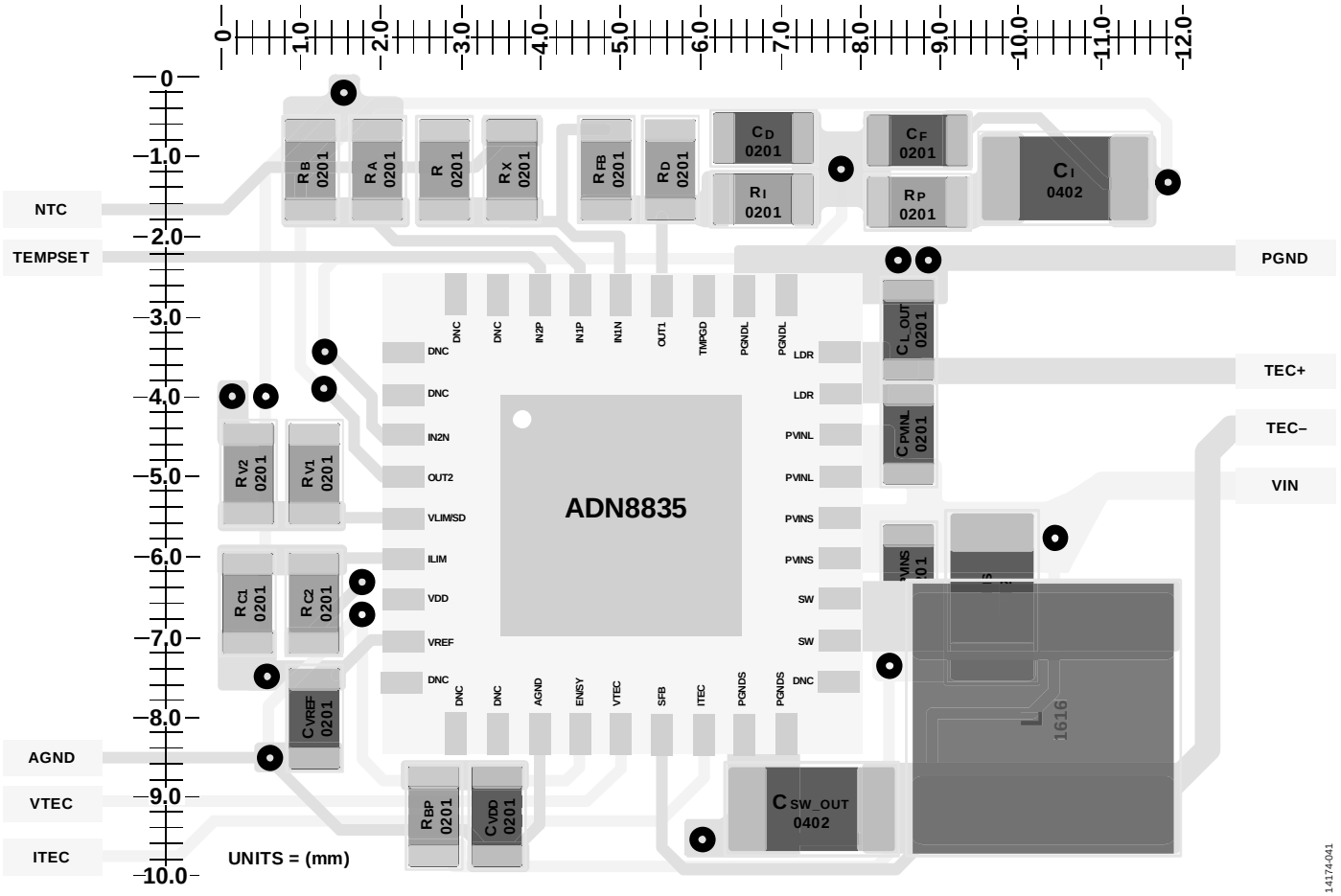


Figure 41. Example PCB Layout Using Two Layers (Top and Bottom Layers)

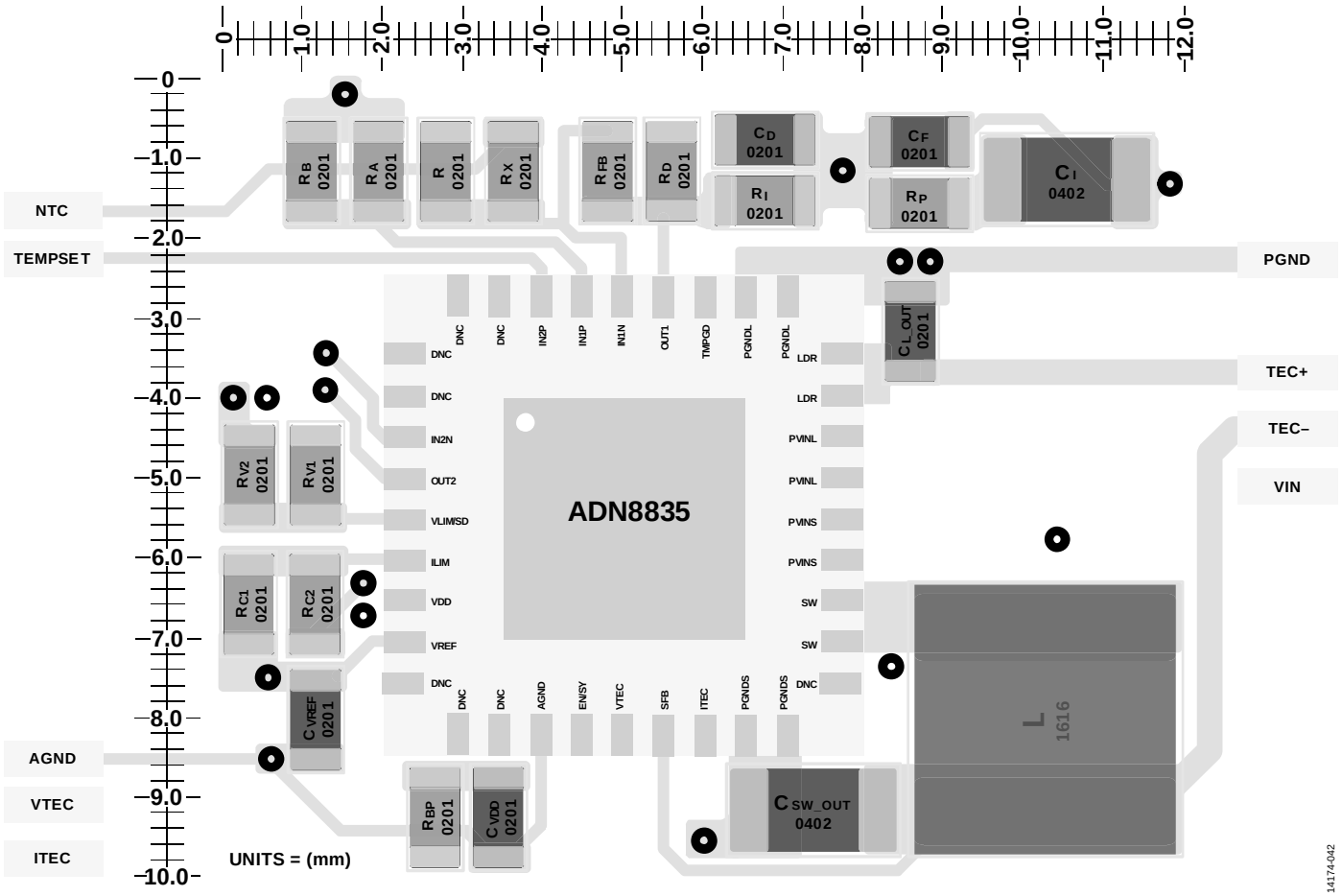


Figure 42. Example PCB Layout Using Two Layers (Top Layer Only)

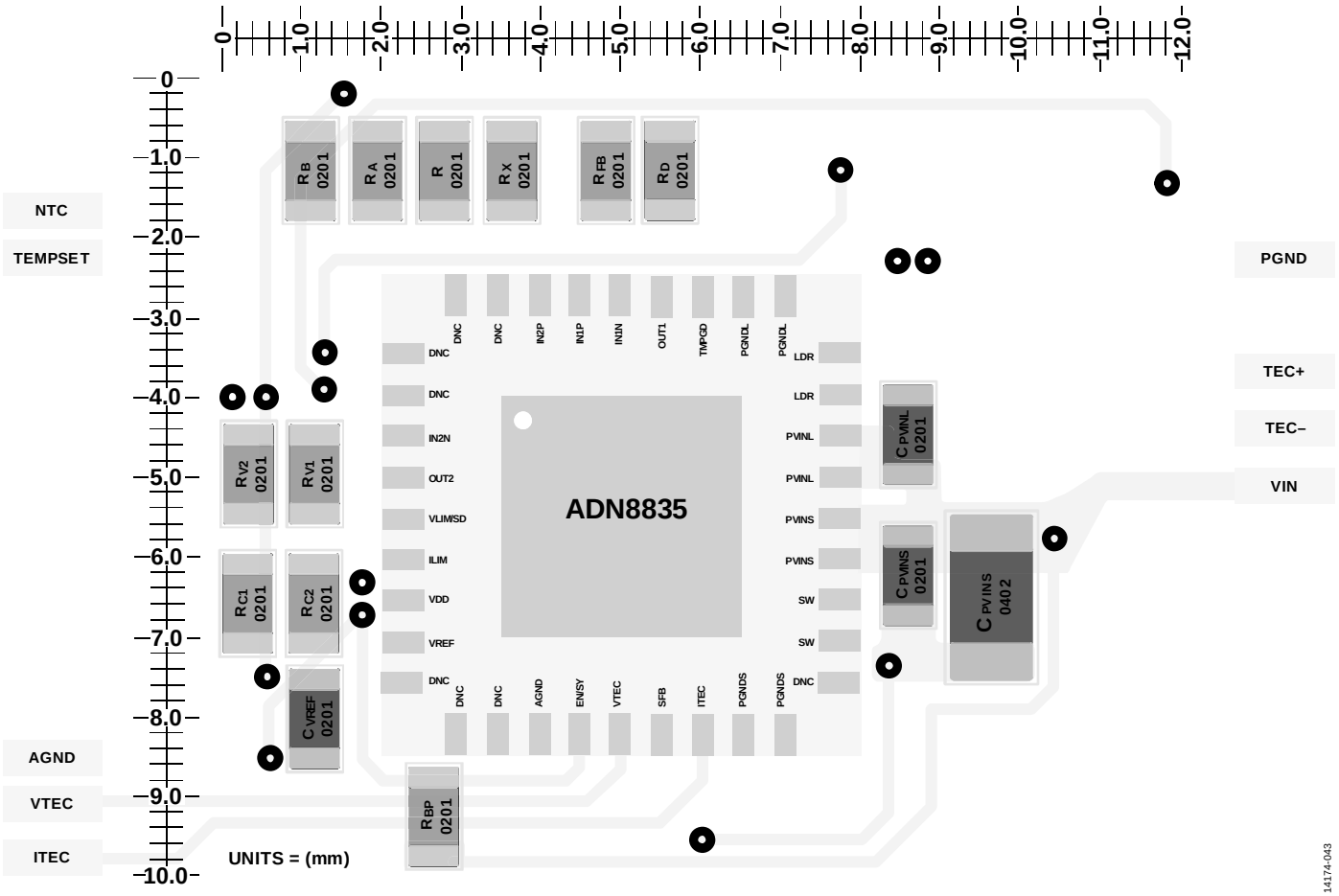
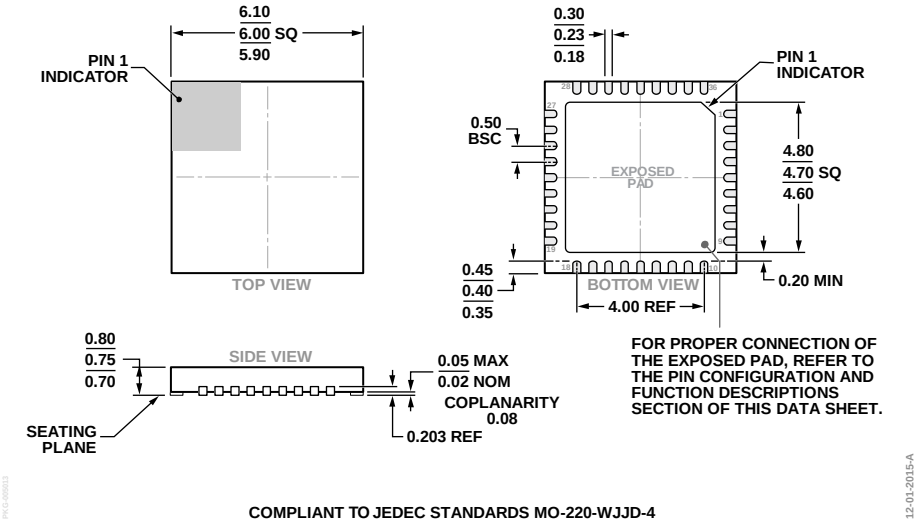


Figure 43. Example PCB Layout Using Two Layers (Bottom Layer Only)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD-4

Figure 44. 36-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.75 mm Package Height
(CP-36-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range[2]	Package Description	Package Option
ADN8835ACPZ-R7	−40°C to +125°C	36-Lead Lead Frame Chip Scale Package [LFCSP]	CP-36-5
ADN8835CP-EVALZ		36-Lead LFCSP Evaluation Board: 3 A (Source/Sink) TEC Current Limit, 5 V TEC Voltage Limit	
ADN8834MB-EVALZ[3]		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] Operating junction temperature range. The ambient operating temperature range is −40°C to +85°C.
[3] The ADN8834MB-EVALZ evaluation board can be used with the ADN8835CP-EVALZ to evaluate the ADN8835 product.

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