The Future of Analog IC Technology

# MP2159A

## 1 A, 6 V, 1.5 MHz, Low $I_Q$, COT Synchronous Step-Down Converter in 8-pin TSOT23

## DESCRIPTION

The MP2159A is a monolithic step-down, switch-mode converter with built-in power MOSFETs. It achieves a 1 A continuous output current from a 2.5 V to 6 V input voltage range with excellent load and line regulation. The output voltage can be regulated as low as 0.6 V.

The constant-on-time (COT) control scheme provides fast transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The MP2159A is available in a small TSOT23-8 package and requires a minimum number of readily available, standard, external components.

The MP2159A is ideal for a wide range of applications including high-performance DSPs, FPGAs, PDAs, and portable instruments.

## FEATURES

- Very Low $I_Q$: 17 µA
- Default 1.5 MHz Switching Frequency
- 1.5% $V_{FB}$ Accuracy
- EN and Power Good for Power Sequencing
- Wide 2.5 V to 6 V Operating Input Range
- Output Adjustable from 0.6 V
- Up to 1 A Output Current
- 100% Duty Cycle in Dropout
- 120 mΩ and 90 mΩ Internal Power MOSFET Switches
- Cycle-by-Cycle Over-Current Protection
- Short-Circuit Protection with Hiccup Mode
- Stable with Low ESR Output Ceramic Capacitors
- Available in a TSOT23-8 Package

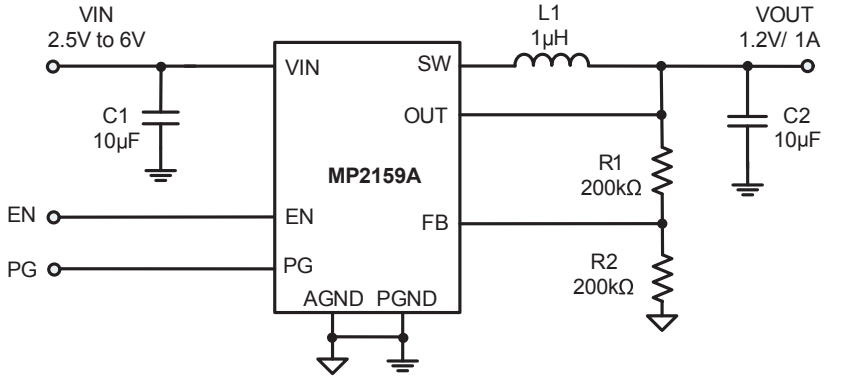
## APPLICATIONS

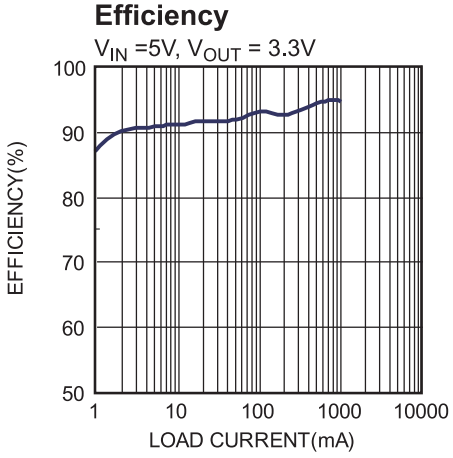
- Wireless/Networking Cards
- Portable Instruments
- Battery Powered Devices
- Low Voltage I/O System Power

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## TYPICAL APPLICATION





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## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MP2159AGJ | TSOT23-8 | *See Below* |

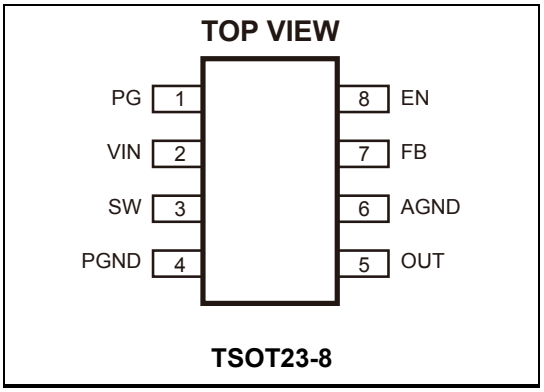
* For Tape & Reel, add suffix –Z (eg. MP2159AGJ–Z)

## TOP MARKING




AMR: Product code of MP2159AGJ
Y: Year code

## PACKAGE REFERENCE





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## ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage ($V_{IN}$) ..... 6.5 V
$V_{SW}$ ..... -0.3 V (-1.5 V for < 20n s & -4 V for < 8 ns) to 6.5 V (10 V for <10 ns)
All other pins ..... -0.3 V to 6.5 V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation ($T_A$ = +25°C) **(2)** ..... 1.25 W
Storage temperature ..... -65°C to +150°C

## *Recommended Operating Conditions* (3)

Supply voltage ($V_{IN}$) ..... 2.5 V to 6 V
Operating junction temp. ($T_J$) ..... -40°C to +125°C

## *Thermal Resistance* (4) $\theta_{JA}$ $\theta_{JC}$

| | | |
|---|---|---|
| TSOT23-8 | 100 | 55 °C/W |

**NOTES:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.


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## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 5 V, $T_A$ = +25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Feedback voltage | $V_{FB}$ | 2.5 V ≤ $V_{IN}$ ≤ 6 V, $T_A$=25°C | -1.5 | 0.600 | +1.5 | V/% |
| | | $T_A$ = -40°C to +85°C(6) | -2.5 | | +2.5 | V/% |
| Feedback current | $I_{FB}$ | $V_{FB}$ = 0.6 V | | 10 | 50 | nA |
| PFET switch on resistance | $R_{DSON_P}$ | | | 120 | | mΩ |
| NFET switch on resistance | $R_{DSON_N}$ | | | 90 | | mΩ |
| Switch leakage | | $V_{EN}$ = 0 V, $V_{IN}$ = 6 V<br>$V_{SW}$ = 0 V and 6 V | | 0 | 1 | µA |
| PFET current limit | | | 2 | | | A |
| On time | $T_{ON}$ | $V_{IN}$ = 5 V, $V_{OUT}$ = 1.2 V | | 166 | | ns |
| | | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.2 V | | 220 | | |
| Switching frequency | $F_s$ | $V_{OUT}$ = 1.2 V | -20% | 1500 | +20% | kHz/% |
| | | $T_A$ = -40°C to +85°C(6) | -25% | 1500 | +25% | kHz/% |
| Minimum off time(6) | $T_{MIN-OFF}$ | | | 60 | | ns |
| Soft-start time | $T_{SS-ON}$ | $V_{OUT}$ from 10% to 90% | 0.6 | 1.15 | 1.7 | ms |
| Power good upper trip threshold | $PG_H$ | FB voltage respect to the regulation | | +10 | | % |
| Power good lower trip threshold | $PG_L$ | | | -10 | | % |
| Power good delay | $PG_D$ | | | 50 | | µs |
| Power good sink current capability | $V_{PG-L}$ | Sink 1 mA | | | 0.4 | V |
| Power good logic high voltage | $V_{PG-H}$ | $V_{IN}$ = 5 V, $V_{FB}$ = 0.6 V | 4.9 | | | V |
| Power good internal pull-up resistor | $R_{PG}$ | | | 550 | | kΩ |
| Under-voltage lockout threshold—rising | | | 2.15 | 2.3 | 2.45 | V |
| Under-voltage lockout threshold—hysteresis | | | | 260 | | mV |
| EN input logic low voltage | | | | | 0.4 | V |
| EN input logic high voltage | | | 1.2 | | | V |
| EN input current | | $V_{EN}$ = 2 V | | 1.5 | | µA |
| | | $V_{EN}$ = 0 V | | 0 | | µA |
| Supply current (shutdown) | | $V_{EN}$ = 0 V, $V_{IN}$ = 3 V | | 20 | 100 | nA |
| Supply current (quiescent) | | $V_{EN}$ = 2 V, $V_{FB}$ = 0.63 V, $V_{IN}$ = 5 V | | 17 | 20 | µA |
| Thermal shutdown(5) | | | | 150 | | °C |
| Thermal hysteresis(5) | | | | 30 | | °C |

**NOTES:**

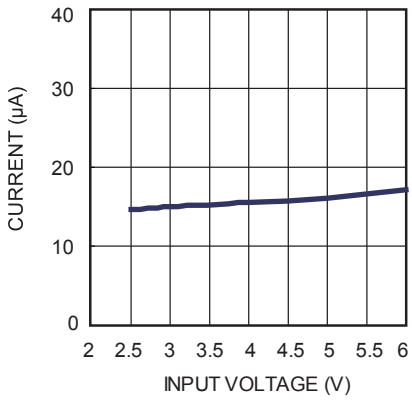
5) Guaranteed by design.
6) Guaranteed by characterization test.


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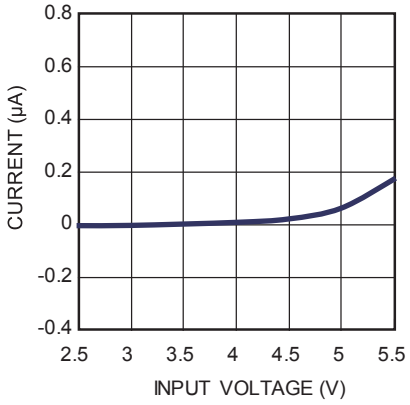
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 5 V, $V_{OUT}$ = 1.2 V, L = 1.0 µH, $T_A$ = +25ºC, unless otherwise noted.**

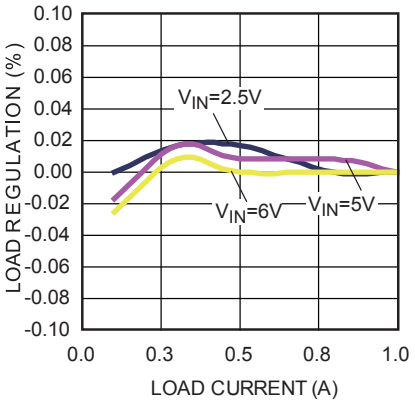
### Quiescent Current vs. Input Voltage



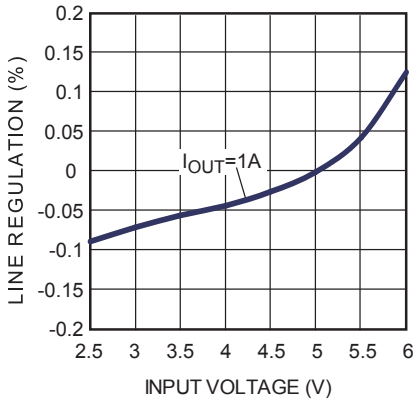

### Shutdown Current vs. Input Voltage




### Load Regulation

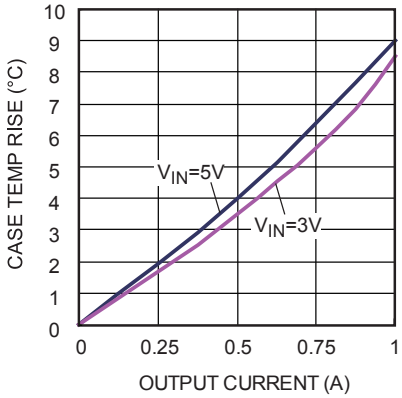



### Line Regulation



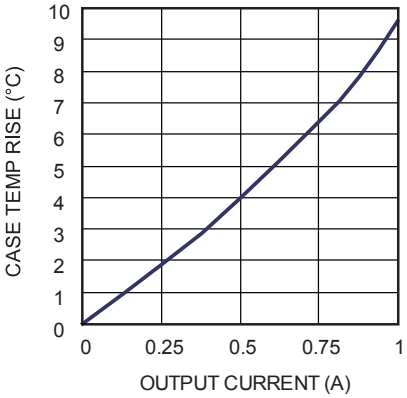

### Case Temperature Rise

$V_{IN}$=3/5V, $V_{OUT}$=1.2V

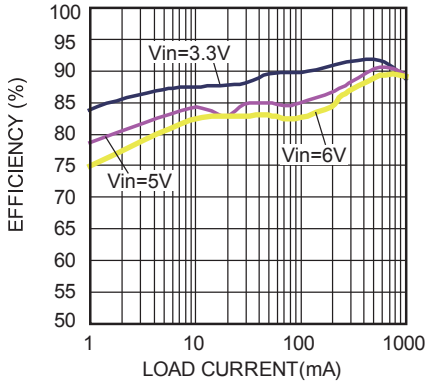



### Case Temperature Rise

$V_{IN}$=5V, $V_{OUT}$=3.3V

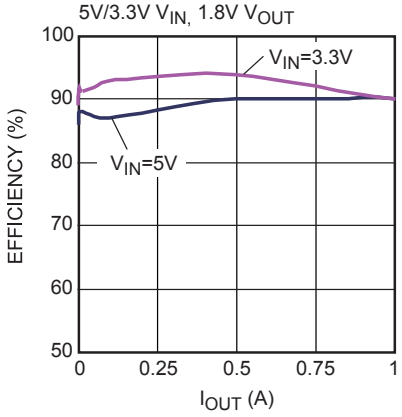



### Efficiency



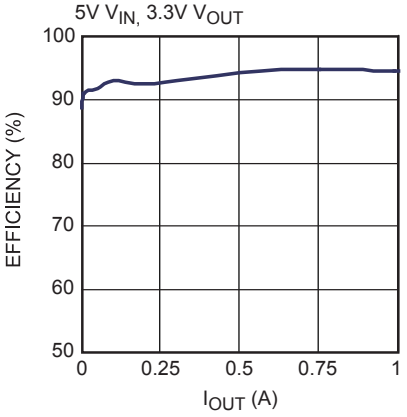

### Efficiency

5V/3.3V $V_{IN}$, 1.8V $V_{OUT}$




### Efficiency

5V $V_{IN}$, 3.3V $V_{OUT}$



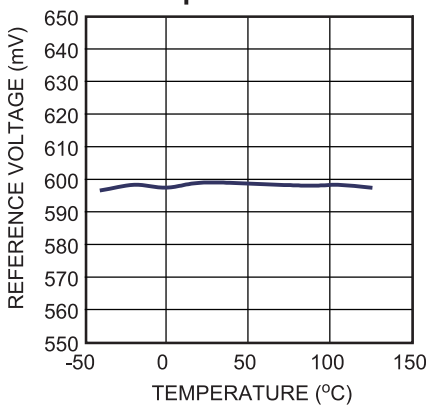


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## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5 V, $V_{OUT}$ = 1.2 V, L = 1.0 µH, $T_A$ = +25ºC, unless otherwise noted.**

**Reference Voltage vs. Temperature**



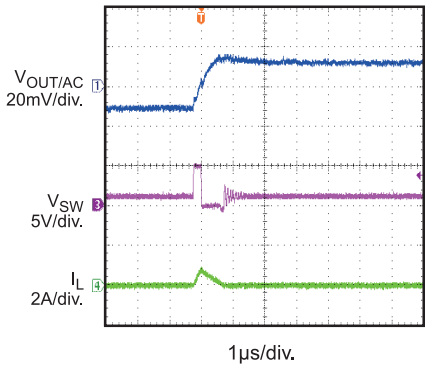


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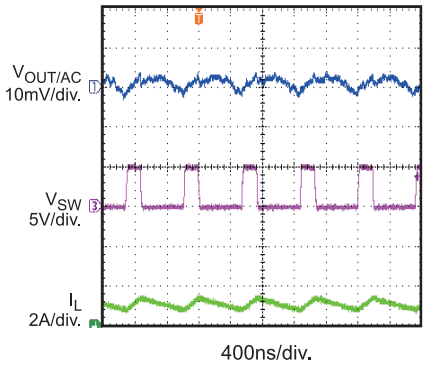
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5 V, $V_{OUT}$ = 1.2 V, L = 1.0 µH, $T_A$ = +25ºC, unless otherwise noted.**

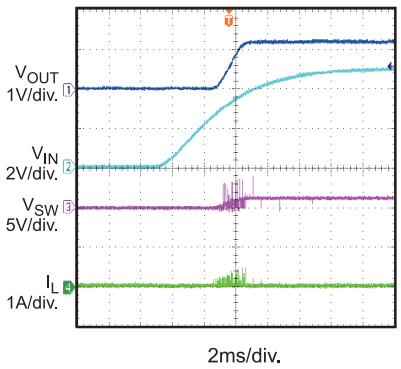
### Output Ripple
$I_{OUT}$=0A



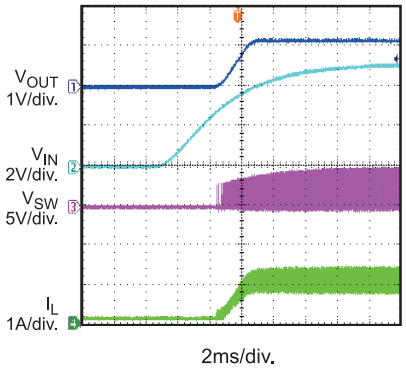

### Output Ripple
$I_{OUT}$=1A



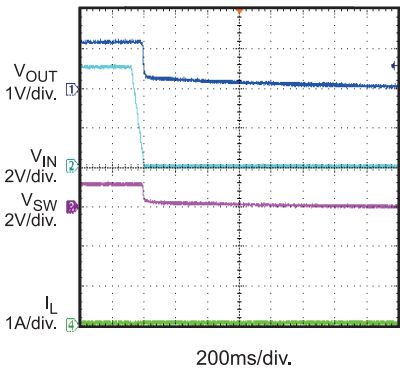

### VIN Power-Up without Load



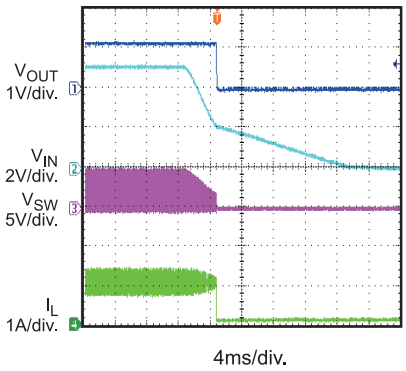

### VIN Power-Up with 1A Load



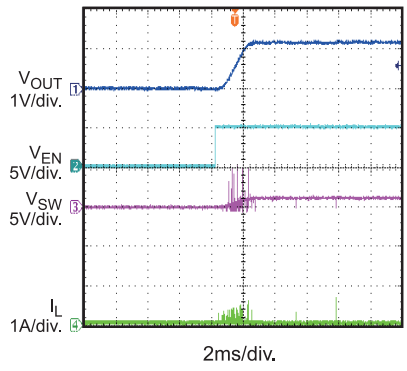

### VIN Shutdown without Load



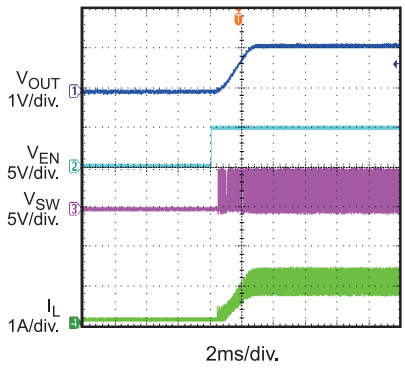

### VIN Shutdown with 1A Load



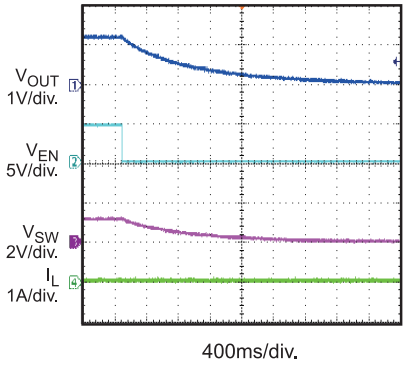

### EN Start-Up without Load




### EN Start-Up with 1A Load




### EN Shutdown without Load



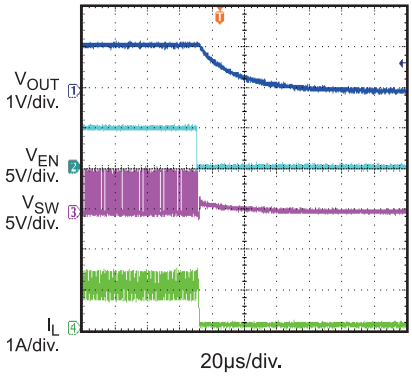


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## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5 V, $V_{OUT}$ = 1.2 V, L = 1.0 µH, $T_A$ = +25ºC, unless otherwise noted**

**EN Shutdown with 1A Load**





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## PIN FUNCTIONS

| TSOT23-8 Pin # | Name | Description |
|---|---|---|
| 1 | PG | **Power good indicator.** The output of PG is an open drain with an internal pull-up resistor to VIN. PG is pulled up to VIN when the FB voltage is within ±10% of the regulation level. If FB voltage is out of this regulation range, it is low. |
| 2 | VIN | **Supply voltage.** The MP2159A operates from a +2.5 V to +6 V unregulated input. C1 is required to prevent large voltage spikes from appearing at the input. |
| 3 | SW | **Switch output.** |
| 4 | PGND | **Power ground.** |
| 5 | OUT | **Input sense pin for output voltage.** |
| 6 | AGND | **Analog ground for internal control circuit.** |
| 7 | FB | **Feedback.** An external resistor divider from the output to AGND (tapped to FB) sets the output voltage. |
| 8 | EN | **On/off control.** |


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## FUNCTIONAL BLOCK DIAGRAM

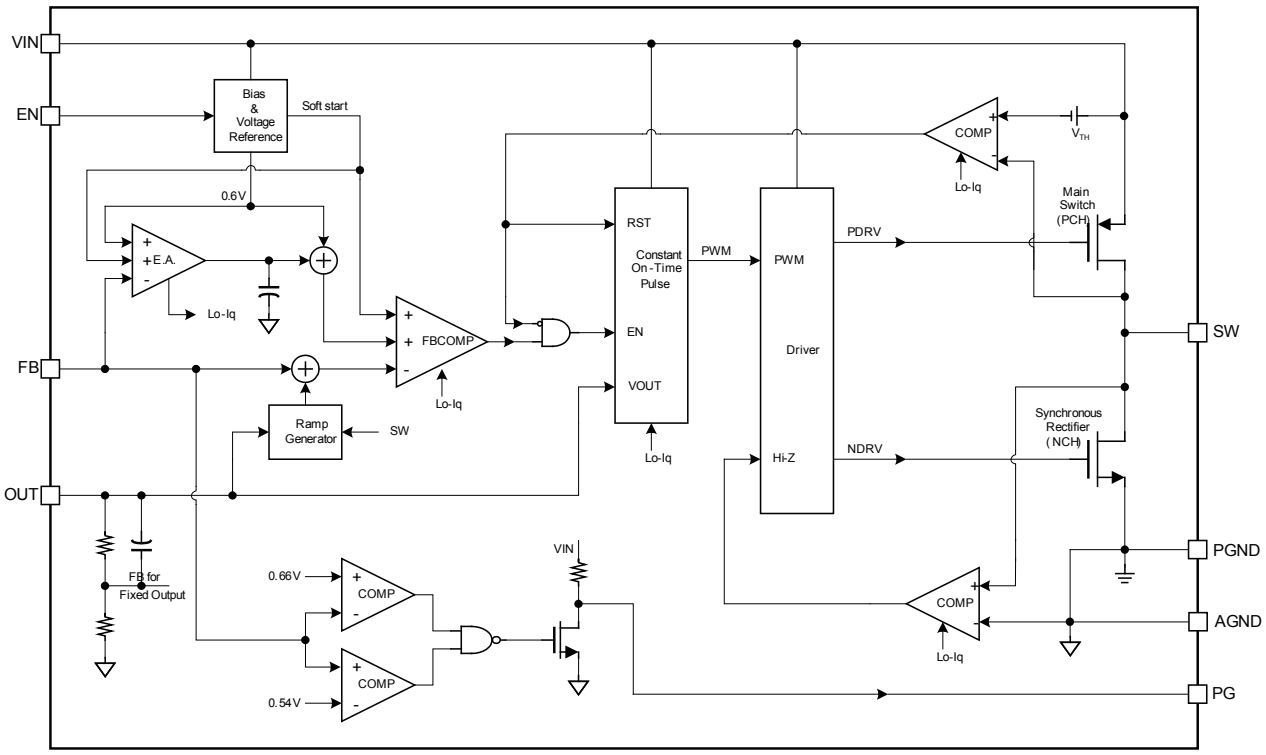



**Figure 1—Functional block diagram**


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## OPERATION

The MP2159A uses constant-on-time (COT) control with input voltage feed forward to stabilize the switching frequency over a full input range. At light load, the MP2159A employs a proprietary control of the low-side switch and the inductor current to eliminate ringing on the switching node and improve efficiency.

### Constant-On-Time (COT) Control

Compare to fixed frequency PWM control, constant-on-time control offers the advantage of a simpler control loop and faster transient response. By using input voltage feed forward, MP2159A maintains a nearly constant switching frequency across the input and output voltage range. The on time of the switching pulse can be estimated using Equation (1):

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.667\mu s \quad (1)$$

To prevent inductor current runaway during load transient, the MP2159A fixes the minimum off time at 60 ns. However, this minimum-off time limit will not affect operation of the MP2159A in steady-state operation.

### Light-Load Operation

In a light-load condition, the MP2159A uses a proprietary control scheme to save power and improve efficiency. It turns off the low-side switch when the inductor current begins to reverse. Then it works in discontinuous conduction mode (DCM) operation.

There is a zero current cross circuit to detect if the inductor current starts to reverse. Considering the internal circuit propagation time, the typical delay is 50 ns. This means the inductor current will still fall after the ZCD is triggered in this delay. If the inductor current falling slew rate is fast (Vo voltage is high or close to Vin), the low-side MOSFET (LS-FET) is turned off, and the inductor current may be negative. This phenomena prevents the MP2159A from entering DCM operation even if there is no load. If DCM is required, the off time of the LS-FET in CCM should be longer than 100 ns (2 times the propagation delay). For example, if Vin is 3.6 V and Vo is 3.3 V, the off time in CCM is 55 ns. It is difficult to enter DCM at light load. Using a smaller inductor improves this problem, making it easier to enter DCM.

### Enable (EN)

When the input voltage is greater than the under-voltage lockout threshold (2.3 V, typically), the MP2159A is enabled by pulling EN higher than 1.2 V. Floating EN or pulling EN down to ground disables the MP2159A. There is an internal 1 MΩ resistor from EN to ground.

### Soft Start (SS)

MP2159A has built-in soft start that ramps up the output voltage in a controlled slew rate, avoiding overshoot at start-up. The soft-start time period is about 1.15 ms, typically.

### Power GOOD Indicator (PG)

MP2159A has an open drain with a 550 kΩ pull-up resistor pin that functions as a power good indicator (PG). When FB is within +/-10% of the regulation voltage (i.e., 0.6 V), PG is pulled up to VIN by the internal resistor. If the FB voltage is out of the +/-10% window, PG is pulled down to ground by an internal MOSFET. The MOSFET has a maximum $R_{dson}$ of less than 400 Ω.

### Current Limit

MP2159A has a minimum 2 A current limit for the high-side switch. When the high-side switch hits the current limit, the MP2159A remains at the hiccup threshold until the current decreases. This prevents the inductor current from continuing to build up, which will result in damage to the components.

### Short Circuit and Recovery

The MP2159A enters short-circuit protection mode when the current limit is reached, and it tries to recover from the short circuit with hiccup mode. During a short-circuit protection, the MP2159A disables the output power stage, discharges the soft-start capacitor, and then automatically tries to soft-start again. If the short-circuit condition still holds after the soft-start ends, the MP2159A repeats this operation cycle until the short circuit disappears, and the output rises back to regulation level.


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# APPLICATION INFORMATION

## COMPONENT SELECTION

### Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application on page 1). The value of the feedback resistor (R1) cannot be too large or too small, considering the trade-off between a dynamic circuit and stability in the circuit. Choose R1 around 120 kΩ to 200 kΩ. R2 is then given using Equation (2):

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1} \quad (2)$$

The feedback circuit is highly recommended (see Figure 2).

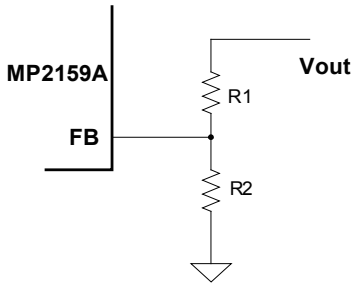



**Figure 2—Feedback network**

Table 1 lists the recommended resistor values for common output voltages.

**Table 1—Resistor selection for common output voltages**

| $V_{OUT}$ (V) | R1 (kΩ) | R2 (kΩ) |
|---|---|---|
| 1.0 | 200(1%) | 300(1%) |
| 1.2 | 200(1%) | 200(1%) |
| 1.8 | 200(1%) | 100(1%) |
| 2.5 | 200(1%) | 63.2(1%) |
| 3.3 | 200(1%) | 44.2(1%) |

### Selecting the Inductor

A 0.68 µH to 2.2 µH inductor is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15 mΩ. For most designs, the inductance value can be derived from Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where $\Delta I_L$ is the inductor ripple current.

Choose the inductor current to be approximately 30 percent of the maximum load current. The maximum inductor peak current can be calculated using Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

### Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10 µF capacitor is sufficient. For a higher output voltage, a 22 µF capacitor may be needed for a more stable system.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated using Equation (5) and Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (e.g., 0.1 µF) should be placed as close to the IC as possible. When using ceramic capacitors, make sure they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated using Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$


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### Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated using Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

(8)

Where $L_1$ is the inductor value and $R_{ESR}$ is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated using Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

(10)

The characteristics of the output capacitor affect the stability of the regulation system.

### PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the high-frequency switching converter, a poor layout design can result in poor line or load regulation and stability issues. For best results, refer to Figure 3 and follow the guidelines below:

1. Place the high current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close as possible to VIN and GND.
3. Place the external feedback resistors next to FB.
4. Keep the switching node (SW) short and away from the feedback network.

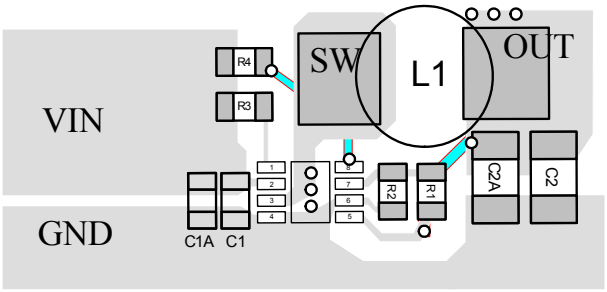



**Figure 3—Recommended PCB layout**

### Design Example

Table 2 shows a design example following the application guidelines for the given specifications:

**Table 2—Design example**

| | |
|---|---|
| **$V_{IN}$** | 5 V |
| **$V_{OUT}$** | 1.2 V |
| **$f_{SW}$** | 1500 kHz |

The detailed application schematic is shown in Figure 4. The typical performance and circuit waveforms have been shown in the “Typical Performance Characteristics” section. For more device applications, please refer to the related evaluation board datasheets.


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## TYPICAL APPLICATION CIRCUITS

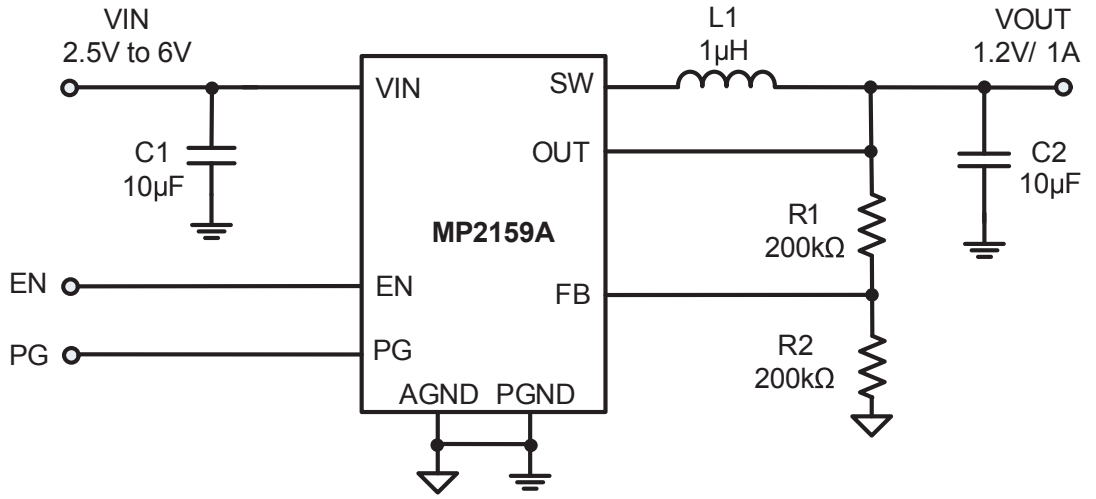



**Figure 4—Typical application circuit**

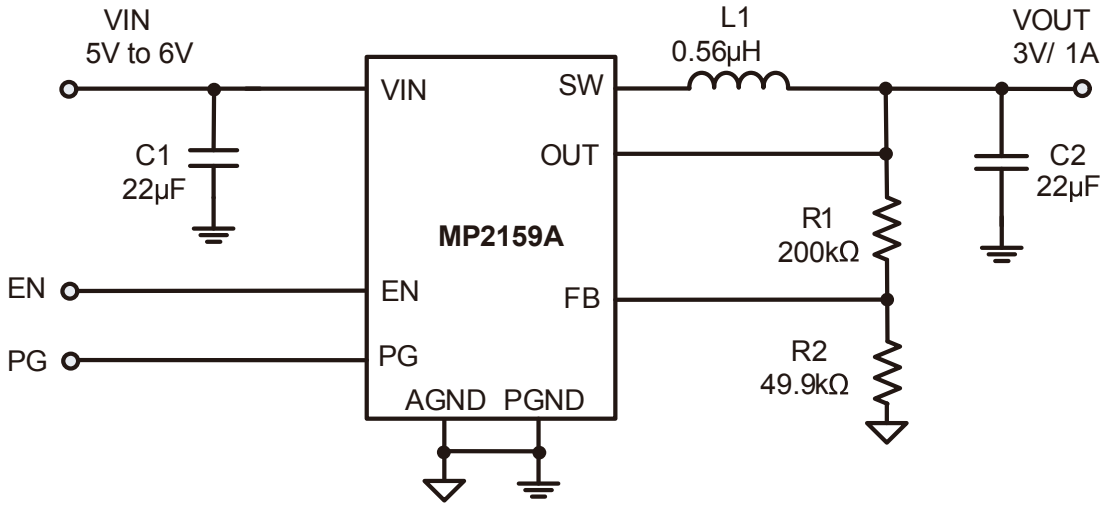
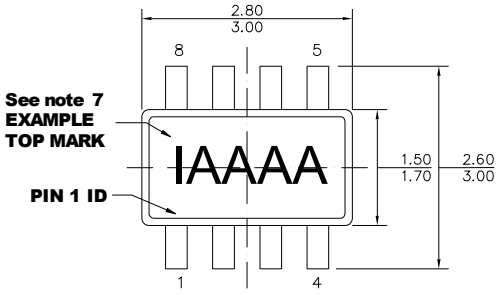



**Figure 5—Typical application circuit for higher efficiency at light load**

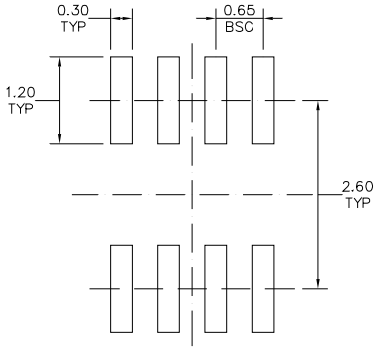

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## PACKAGE INFORMATION

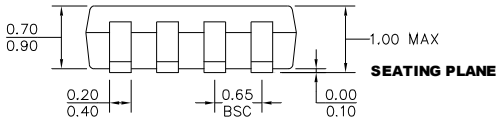
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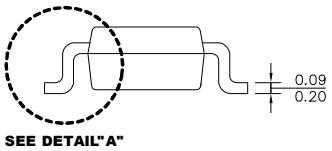

**TOP VIEW**



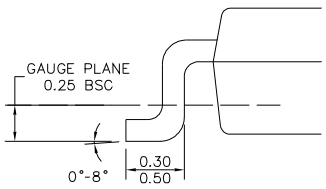

**RECOMMENDED LAND PATTERN**




**FRONT VIEW**




**SIDE VIEW**




**DETAIL "A"**

**NOTE:**

**1) ALL DIMENSIONS ARE IN MILLIMETERS**
**2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR**
**3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION**
**4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX**
**5) JEDEC REFERENCE IS MO-193, VARIATION BA**
**6) DRAWING IS NOT TO SCALE**
**7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)**

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