Dual, Serial Input 14-Bit Multiplying Digital-to-Analog Converter

FEATURES

- **Relative Accuracy: 1 LSB Max**
- **Differential Nonlinearity: 1 LSB Max**
- **2-mA Full-Scale Current ±20%, with V_{REF} = ±10 V**
- **0.5 μs Settling Time**
- **Midscale or Zero-Scale Reset**
- **Separate 4Q Multiplying Reference Inputs**
- **Reference Bandwidth: 10 MHz**
- **Reference Dynamics: –105 dB THD**
- **SPI™-Compatible 3-Wire Interface: 50 MHz**
- **Double Buffered Registers to Enable Simultaneous Multichannel Update**
- **Internal Power-On Reset**
- **Industry-Standard Pin Configuration**

APPLICATIONS

- **Automatic Test Equipment**
- **Instrumentation**
- **Digitally Controlled Calibration**

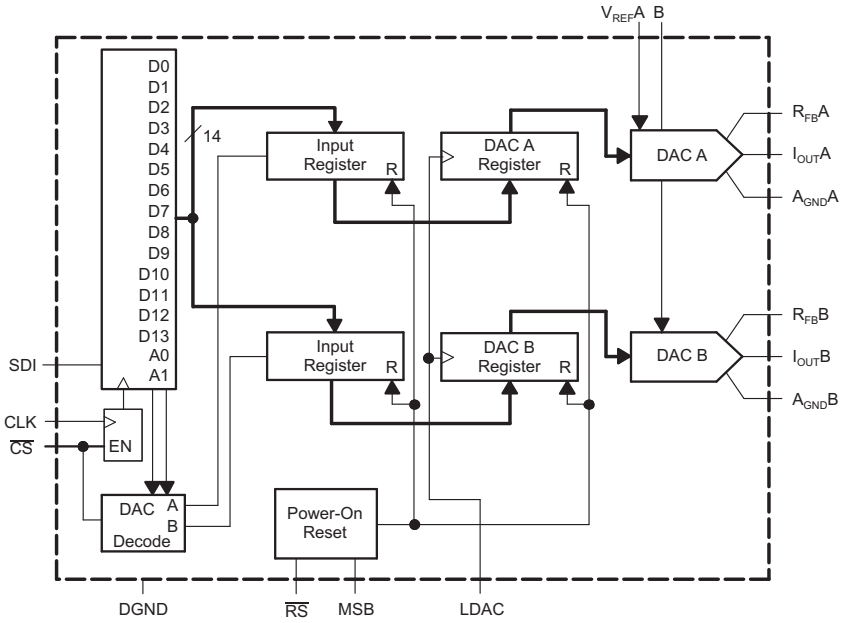
DESCRIPTION

The DAC8802 is a dual, 14-bit, current-output digital-to-analog converter (DAC) designed to operate from a single 2.7 V to 5.5 V supply.

The applied external reference input voltage V_{REF} determines the full-scale output current. An internal feedback resistor (R_{FB}) provides temperature tracking for the full-scale output when combined with an external I-to-V precision amplifier.

A doubled-buffered, serial data interface offers high-speed, 3-wire, SPI and microcontroller compatible inputs using serial data in (SDI), clock (CLK), and a chip-select ($\overline{CS}$). A common level-sensitive load DAC strobe ($\overline{LDAC}$) input allows simultaneous update of all DAC outputs from previously loaded input registers. Additionally, an internal power-on reset forces the output voltage to zero at system turn-on. An MSB pin allows system reset assertion ($\overline{RS}$) to force all registers to zero code when MSB = 0, or to half-scale code when MSB = 1.

The DAC8802 is available in an TSSOP-16 package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE-LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8802	±1	±1	–40°C to 85°C	TSSOP-16	PW	DAC8802IPW	Tubes, 90
						DAC8802IPWR	Tape and Reel, 2500

(1) For the most current specifications and package information, see the Package Option Addendum located at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		DAC8802	UNIT
V_{DD} to GND		–0.3 to 7	V
$V_{REF}X$, $R_{FB}X$ to GND		–18 to 18	V
Digital logic inputs to GND		– 0.3 to + V_{DD} + 0.3	V
$V(I_{OUT})$ to GND		– 0.3 to V_{DD} + 0.3	V
$A_{GND}X$ to DGND		–0.3 to +0.3	V
Input current to any pin except supplies		±50	mA
Package power dissipation		$(T_J max – T_A)/\theta_{JA}$	W
Thermal resistance, θ_{JA}		100	°C/W
Maximum junction temperature ($T_J$max)		150	°C
Operating temperature range		– 40 to 85	°C
Storage temperature range		– 65 to 150	°C
ESD	HBM	4	kV
	CDM	1	kV

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS(1)

V_{DD} = 2.7 V to 5.5 V, $I_{OUT}X$ = Virtual GND, $A_{GND}X$ = 0 V, $V_{REF}A$, B = 10 V, T_A = full operating temperature range, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(2)						
Resolution					14	Bits
Relative accuracy	INL				±1	LSB
Differential nonlinearity	DNL				±1	LSB
Output leakage current	$I_{OUT}X$	Data = 0000h, T_A = 25°C			10	nA
		Data = 0000h, T_A = T_A max			20	nA
Full-scale gain error	G_{FSE}	Data = 3FFFh		±0.75	±4	mV
Full-scale tempco(3)	TCV_{FS}			1		ppm/°C
Feedback resistor	$R_{FB}X$	V_{DD} = 5 V		5		kΩ
REFERENCE INPUT(3)						
$V_{REF}X$ Range	$V_{REF}X$		–15		15	V
Input resistance	$R_{REF}X$		4	5	6	kΩ
Input resistance match	$R_{REF}X$	Channel-to-channel		1		%
Input capacitance	$C_{REF}X$			5		pF
ANALOG OUTPUT(3)						
Output current	$I_{OUT}X$	Data = 3FFFh	1.6		2.5	mA
Output capacitance	$C_{OUT}X$	Code-dependent		50		pF
LOGIC INPUTS(3)						
Input low voltage	V_{IL}	V_{DD} = 2.7 V			0.6	V
		V_{DD} = 5 V			0.8	V
Input high voltage	V_{IH}	V_{DD} = 2.7 V	2.1			V
		V_{DD} = 5 V	2.4			V
Input leakage current	I_{IL}				1	µA
Input capacitance	C_{IL}				10	pF
INTERFACE TIMING (4)						
Clock width high	t_{CH}		10			ns
Clock width low	t_{CL}		10			ns
$\overline{CS}$ to Clock setup	t_{CSS}		0			ns
Clock to $\overline{CS}$ hold	t_{CSH}		10			ns
Clock to SDO prop delay	t_{PD}		2		20	ns
Load DAC pulsewidth	$t_{\overline{LDAC}}$		20			ns
Data setup	t_{DS}		10			ns
Data hold	t_{DH}		10			ns
Load setup	t_{LDS}		5			ns
Load hold	t_{LDH}		25			ns

(1) Specifications subject to change without notice.
(2) All static performance tests (except I_{OUT}) are performed in a closed-loop system using an external precision OPA277 I-to-V converter amplifier. The DAC8802 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at +25°C.
(3) These parameters are specified by design and not subject to production testing.
(4) All input control signals are specified with t_R = t_F = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 2.7 V to 5.5 V, $I_{OUT}X$ = Virtual GND, $A_{GND}X$ = 0 V, $V_{REF}A$, B = 10 V, T_A = full operating temperature range, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CHARACTERISTICS						
Power supply range	$V_{DD\ RANGE}$		2.7		5.5	V
Positive supply current	I_{DD}	Logic inputs = 0 V, V_{DD} = 4.5 V to 5.5 V		2	5	µA
		Logic inputs = 0 V, V_{DD} = 2.7 V to 3.6 V		1	2.5	µA
Power dissipation	P_{DISS}	Logic inputs = 0 V			0.0275	mW
Power supply sensitivity	P_{SS}	ΔV_{DD} = ±5%			0.006	%
AC CHARACTERISTICS(5)(6)						
Output voltage settling time	t_s	To ±0.1% of full-scale, Data = 0000h to 3FFFh to 0000h		0.3		µs
		To ±0.006% of full-scale, Data = 0000h to 3FFFh to 0000h		0.5		µs
Reference multiplying BW	BW –3 dB	$V_{REF}X$ = 100 mV_{RMS}, Data = 3FFFh, C_{FB} = 3 pF		10		MHz
DAC glitch impulse	Q	$V_{REF}X$ = 10 V, Data = 1FFFh to 2000h to 1FFFh		5		nV/s
Feedthrough error	$V_{OUT}X/V_{REF}X$	Data = 0000h, $V_{REF}X$ = 100 mV_{RMS}, f = 100 kHz		–70		dB
Crosstalk error	$V_{OUT}A/V_{REF}B$	Data = 0000h, $V_{REF}B$ = 100 mV_{RMS}, Adjacent channel, f = 100 kHz		–100		dB
Digital feedthrough	Q	$\overline{CS}$ = 1 and f_{CLK} = 1 MHz		1		nV/s
Total harmonic distortion	THD	V_{REF} = 5 V_{PP}, Data = 3FFFh, f = 1 kHz		–105		dB
Output spot noise voltage	e_n	f = 1 kHz, BW = 1 Hz		12		nV/√Hz

(5) These parameters are specified by design and not subject to production testing.
(6) All ac characteristic tests are performed in a closed-loop system using an THS4011 I-to-V converter amplifier.

PARAMETER MEASUREMENT INFORMATION

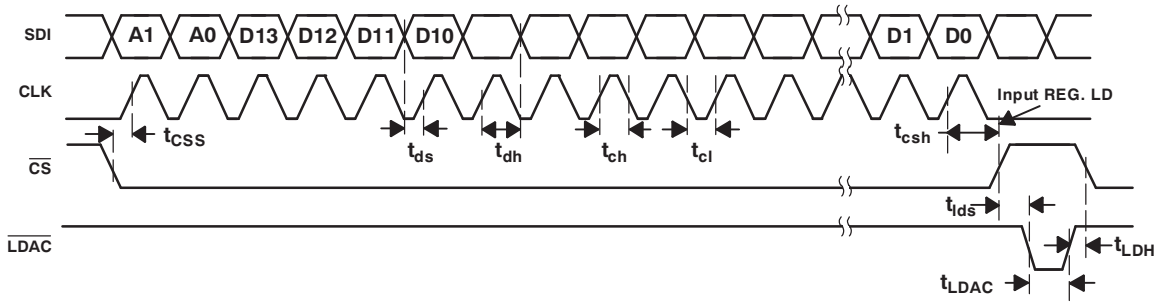
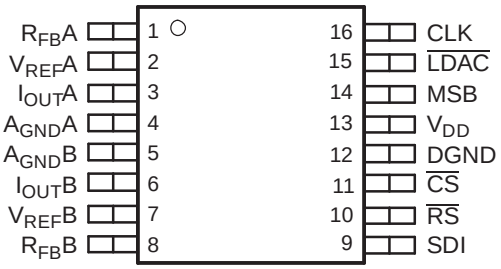


Figure 1. DAC8802 Timing Diagram

PIN CONFIGURATIONS

DAC8802
(TOP VIEW)



PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	$R_{FB}A$	Establish voltage output for DAC A by connecting to external amplifier output.
2	$V_{REF}A$	DAC A Reference voltage input terminal. Establishes DAC A full-scale output voltage. Can be tied to V_{DD} pin.
3	$I_{OUT}A$	DAC A Current output.
4	$A_{GND}A$	DAC A Analog ground.
5	$A_{GND}B$	DAC B Analog ground.
6	$I_{OUT}B$	DAC B Current output.
7	$V_{REF}B$	DAC B Reference voltage input terminal. Establishes DAC B full-scale output voltage. Can be tied to V_{DD} pin.
8	$R_{FB}B$	Establish voltage output for DAC B by connecting to external amplifier output.
9	SDI	Serial data input; data loads directly into the shift register.
10	$\overline{RS}$	Reset pin; active low input. Input registers and DAC registers are set to all 0s or midscale. Register data = 0x0000 when MSB = 0. Register data = 0x2000 when MSB = 1 for DAC8802.
11	$\overline{CS}$	Chip-select; active low input. Disables shift register loading when high. Transfers serial register data to input register when $\overline{CS}$ goes high. Does not affect $\overline{LDAC}$ operation.
12	DGND	Digital ground.
13	V_{DD}	Positive power-supply input. Specified range of operation is 2.7 V to 5.5 V.
14	MSB	MSB bit sets output to either 0 or midscale during a RESET pulse ($\overline{RS}$) or at system power-on. Output equals zero scale when MSB = 0 and midscale when MSB = 1. MSB pin can be permanently tied to ground or V_{DD}.
15	$\overline{LDAC}$	Load DAC register strobe; level sensitive active low. Transfers all input register data to the DAC registers. Asynchronous active low input. See Table 2 for operation.
16	CLK	Clock input. Positive edge clocks data into shift register.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V

At T_A = 25°C, $+V_{DD}$ = 5 V, unless otherwise noted.

Channel A

LINEARITY ERROR vs DIGITAL INPUT CODE

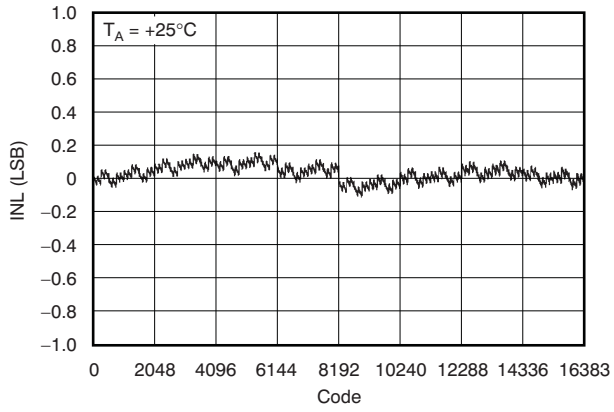


Figure 2.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

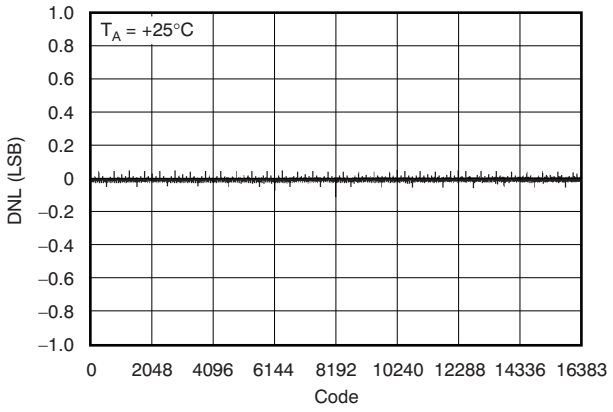


Figure 3.

LINEARITY ERROR vs DIGITAL INPUT CODE

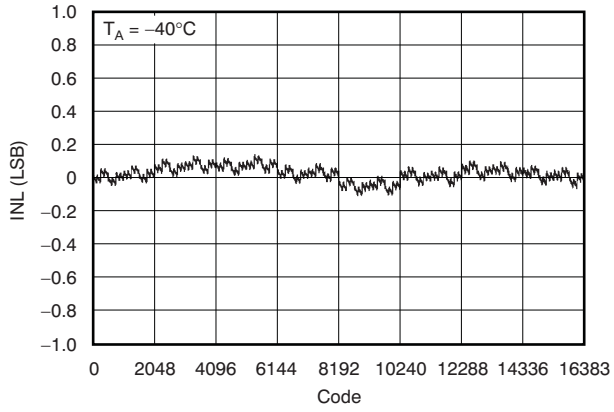


Figure 4.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

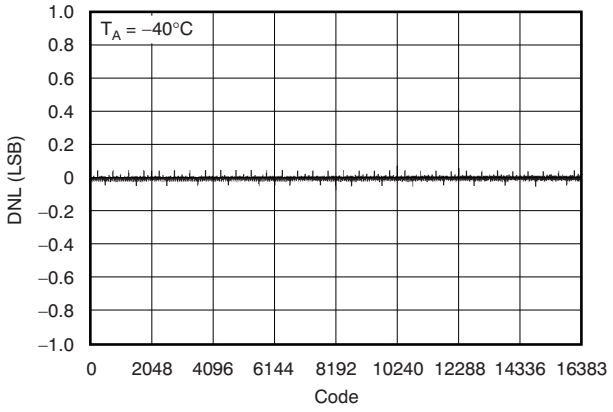


Figure 5.

LINEARITY ERROR vs DIGITAL INPUT CODE

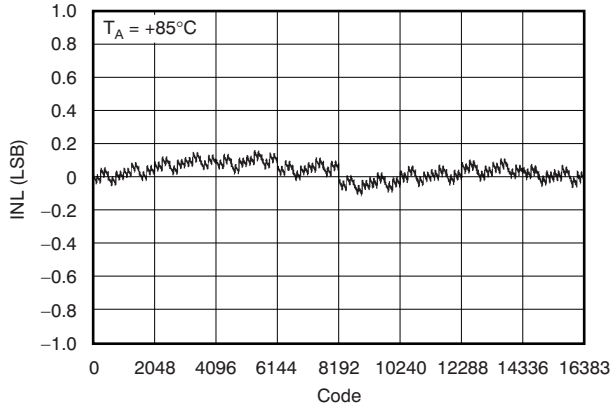


Figure 6.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

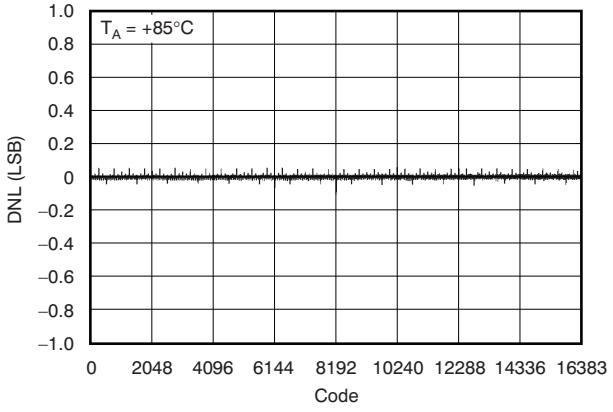


Figure 7.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V (continued)

At T_A = 25°C, $+V_{DD}$ = 5 V, unless otherwise noted.

Channel B

LINEARITY ERROR vs DIGITAL INPUT CODE

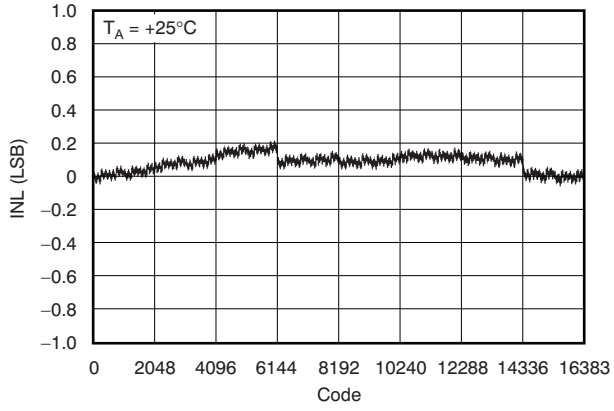


Figure 8.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

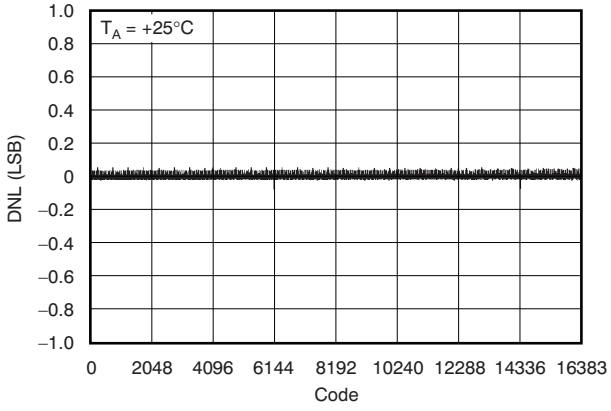


Figure 9.

LINEARITY ERROR vs DIGITAL INPUT CODE

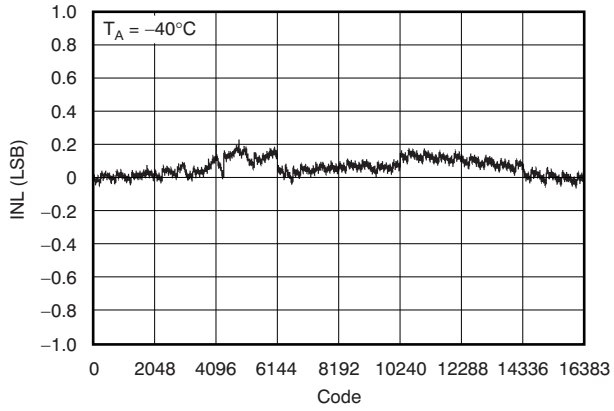


Figure 10.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

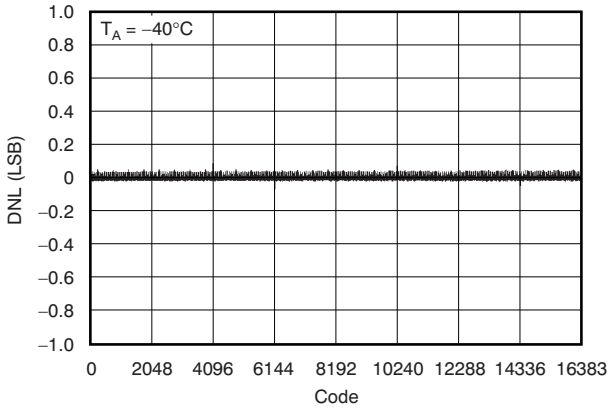


Figure 11.

LINEARITY ERROR vs DIGITAL INPUT CODE

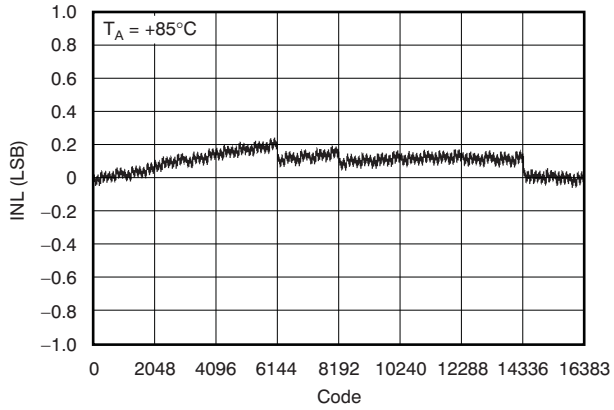


Figure 12.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

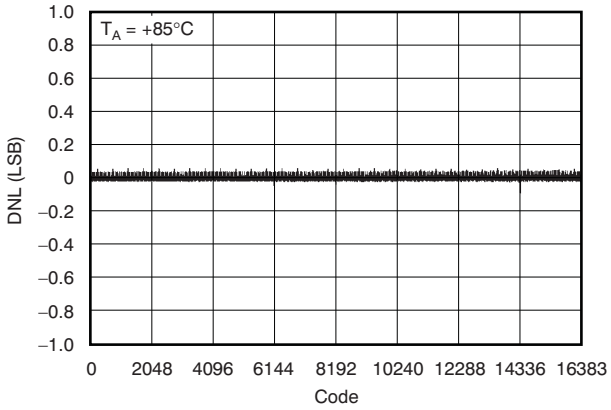


Figure 13.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V (continued)

At T_A = 25°C, $+V_{DD}$ = 5 V, unless otherwise noted.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

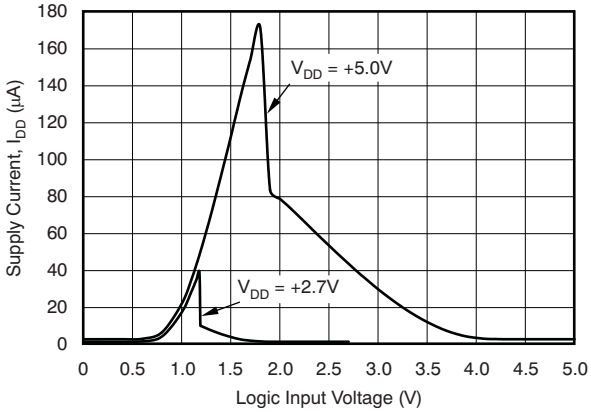


Figure 14.

REFERENCE MULTIPLYING BANDWIDTH

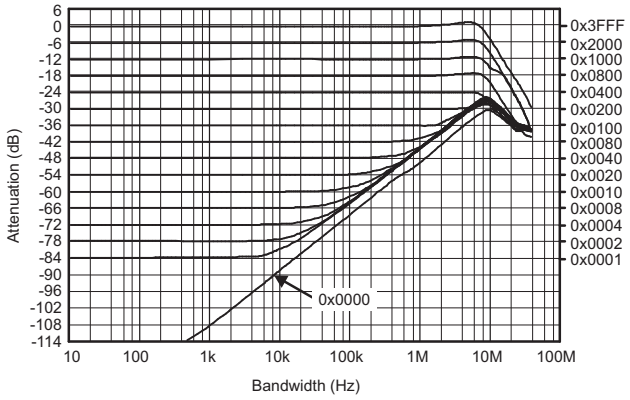


Figure 15.

DAC GLITCH

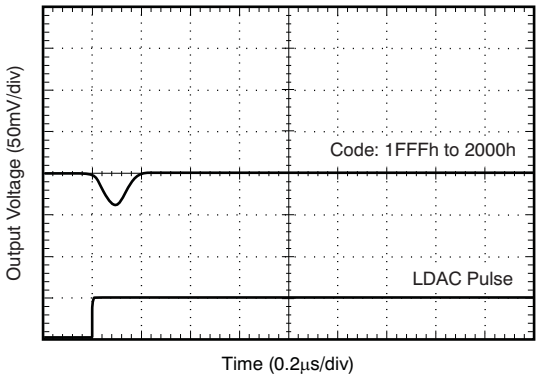


Figure 16.

DAC SETTLING TIME

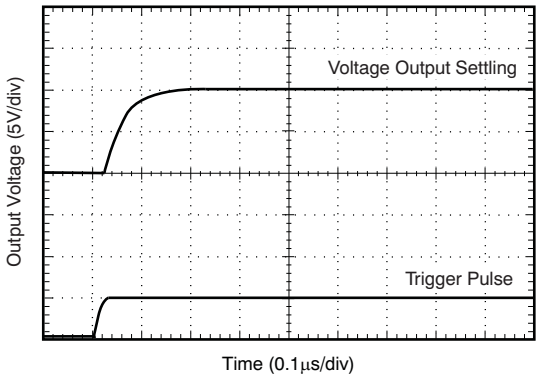


Figure 17.

TYPICAL CHARACTERISTICS: V_{DD} = 2.7 V

At T_A = 25°C, $+V_{DD}$ = 2.7 V, unless otherwise noted.

Channel A

LINEARITY ERROR
vs DIGITAL INPUT CODE

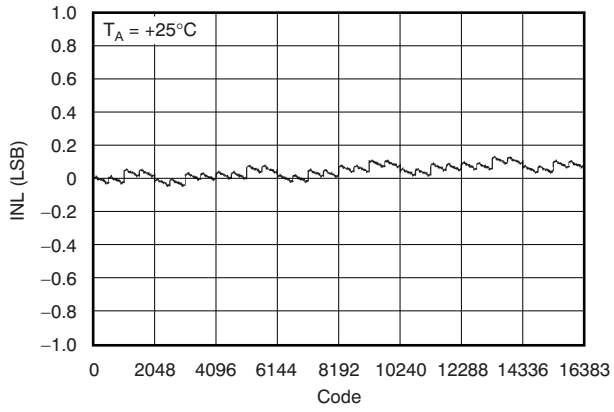


Figure 18.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

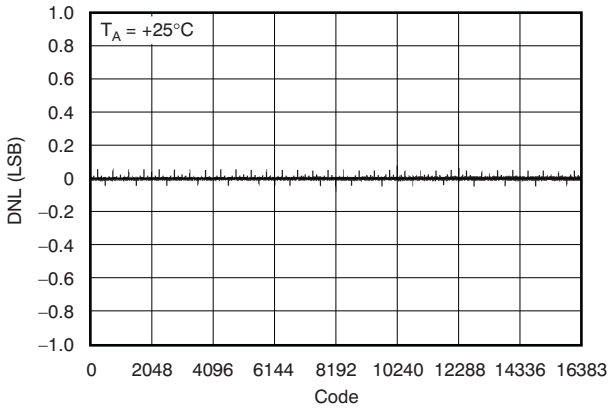


Figure 19.

LINEARITY ERROR
vs DIGITAL INPUT CODE

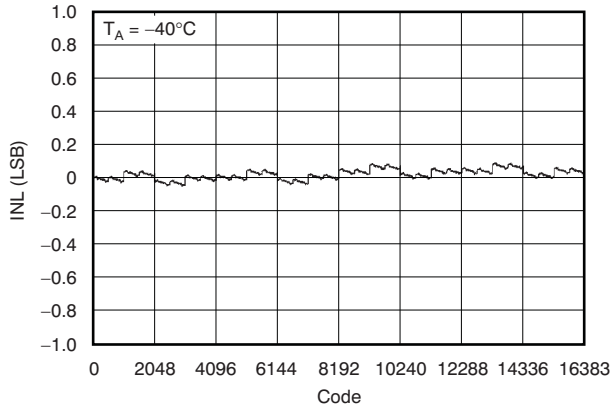


Figure 20.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

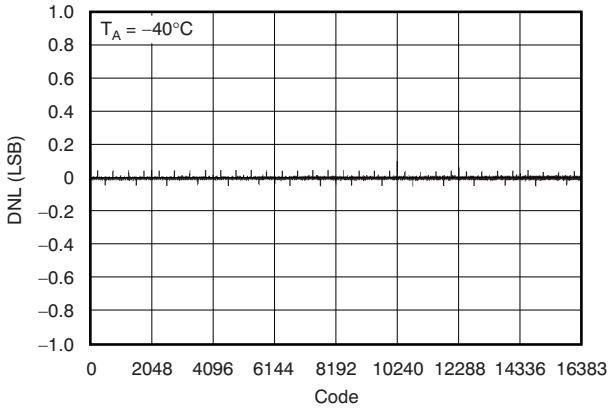


Figure 21.

LINEARITY ERROR
vs DIGITAL INPUT CODE

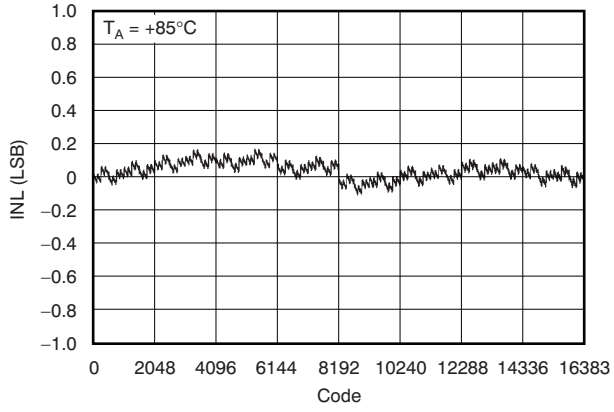


Figure 22.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

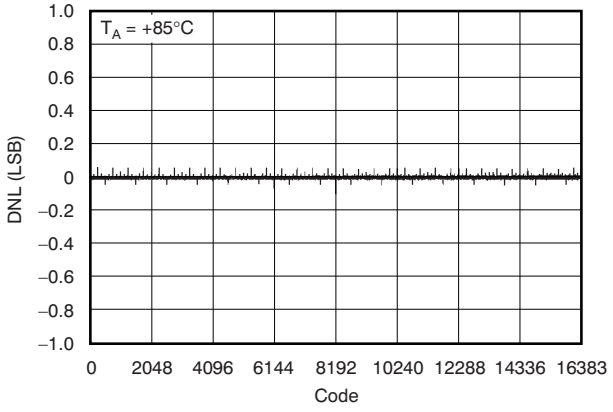


Figure 23.

TYPICAL CHARACTERISTICS: V_{DD} = 2.7 V (continued)

At T_A = 25°C, $+V_{DD}$ = 2.7 V, unless otherwise noted.

Channel B

LINEARITY ERROR vs DIGITAL INPUT CODE

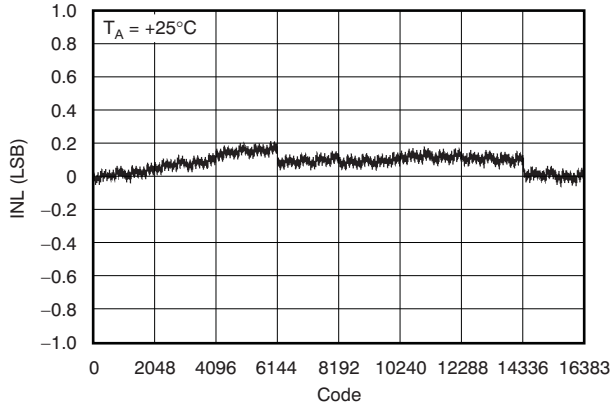


Figure 24.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

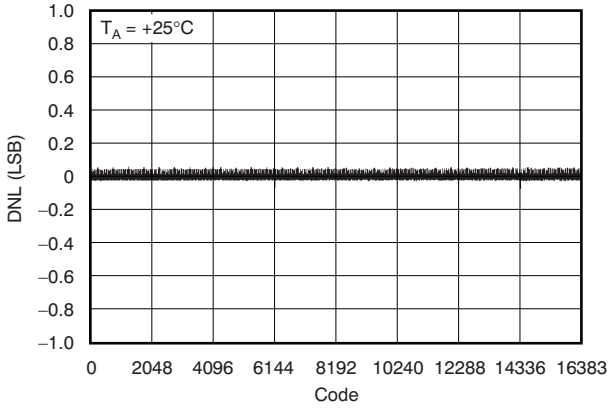


Figure 25.

LINEARITY ERROR vs DIGITAL INPUT CODE

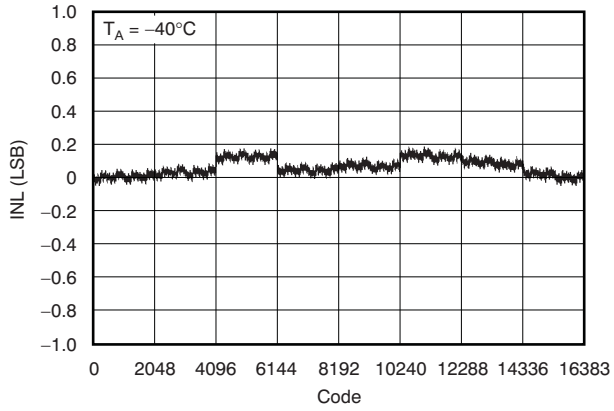


Figure 26.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

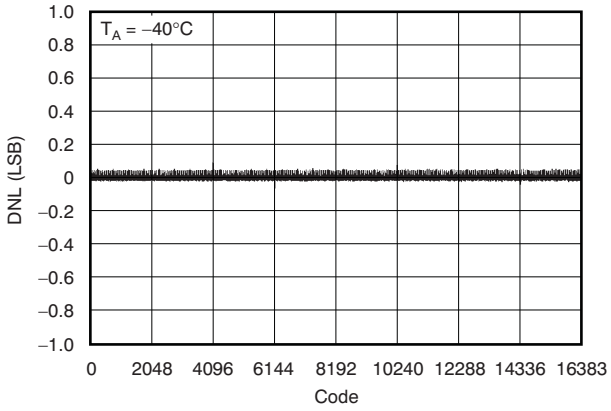


Figure 27.

LINEARITY ERROR vs DIGITAL INPUT CODE

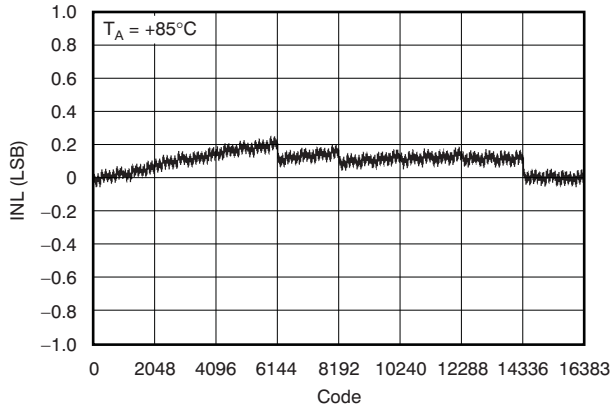


Figure 28.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

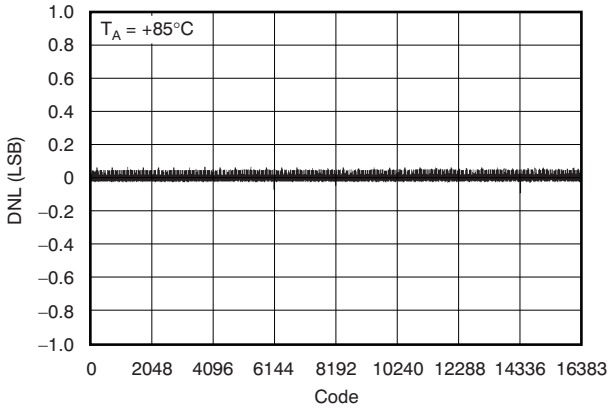


Figure 29.

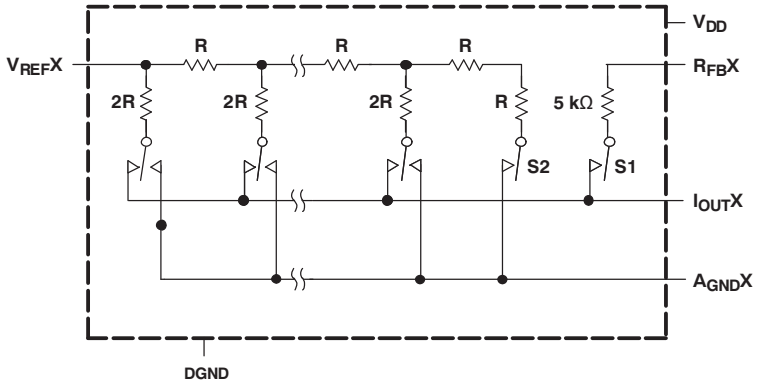
THEORY OF OPERATION

CIRCUIT OPERATION

The DAC8802 contains two 14-bit, current-output, digital-to-analog converters (DACs). Each DAC has its own independent multiplying reference input. The DAC8802 uses a 3-wire, SPI-compatible serial data interface, with a configurable asynchronous $\overline{RS}$ pin for half-scale (MSB = 1) or zero-scale (MSB = 0) preset. In addition, an $\overline{LDAC}$ strobe enables two-channel simultaneous updates for hardware-synchronized output voltage changes.

Digital-to-Analog Converters

The DAC8802 contains two current-steering R-2R ladder DACs. Figure 30 shows a typical equivalent DAC. Each DAC contains a matching feedback resistor for use with an external I-to-V converter amplifier. The $R_{FB}X$ pin is connected to the output of the external amplifier. The $I_{OUT}X$ terminal is connected to the inverting input of the external amplifier. The $A_{GND}X$ pin should be Kelvin-connected to the load point in the circuit requiring the full 14-bit accuracy.



Digital interface connections are omitted for clarity.
Switches S1 and S2 are closed; V_{DD} must be powered.

Figure 30. Typical Equivalent DAC Channel

The DAC is designed to operate with both negative or positive reference voltages. The V_{DD} power pin is only used by the logic to drive the DAC switches on and off. Note that a matching switch is used in series with the internal 5 kΩ feedback resistor. If users are attempting to measure the value of R_{FB}, power must be applied to V_{DD} in order to achieve continuity. The DAC output voltage is determined by V_{REF} and the digital data (D) according to Equation 1:

$$V_{OUT} = -V_{REF} \times \frac{D}{16384} \quad (1)$$

Note that the output polarity is opposite of the V_{REF} polarity for dc reference voltages.

The DAC is also designed to accommodate ac reference input signals. The DAC8802 accommodates input reference voltages in the range of -15 V to 15 V. The reference voltage inputs exhibit a constant nominal input resistance of 5 kΩ, ±20%. On the other hand, DAC outputs I_{OUT}A and B are code-dependent and produce various output resistances and capacitances.

The choice of external amplifier should take into account the variation in impedance generated by the DAC8802 on the amplifiers' inverting input node. The feedback resistance, in parallel with the DAC ladder resistance, dominates output voltage noise. For multiplying mode applications, an external feedback compensation capacitor, C_{FB} (4 pF to 20 pF typical), may be needed to provide a critically damped output response for step changes in reference input voltages.

Figure 15 shows the gain vs frequency performance at various attenuation settings using a 3 pF external feedback capacitor connected across the $I_{OUT}X$ and $R_{FB}X$ terminals. In order to maintain good analog performance, power supply bypassing of 0.01 µF, in parallel with 1 µF, is recommended. Under these conditions, a clean power supply with low ripple voltage capability should be used. Switching power supplies is usually not suitable for this application due to the higher ripple voltage and P_{SS} frequency-dependent characteristics. It is best to derive the DAC8802 5-V supply from the system analog supply voltages (do not use the digital 5-V supply); see Figure 31.

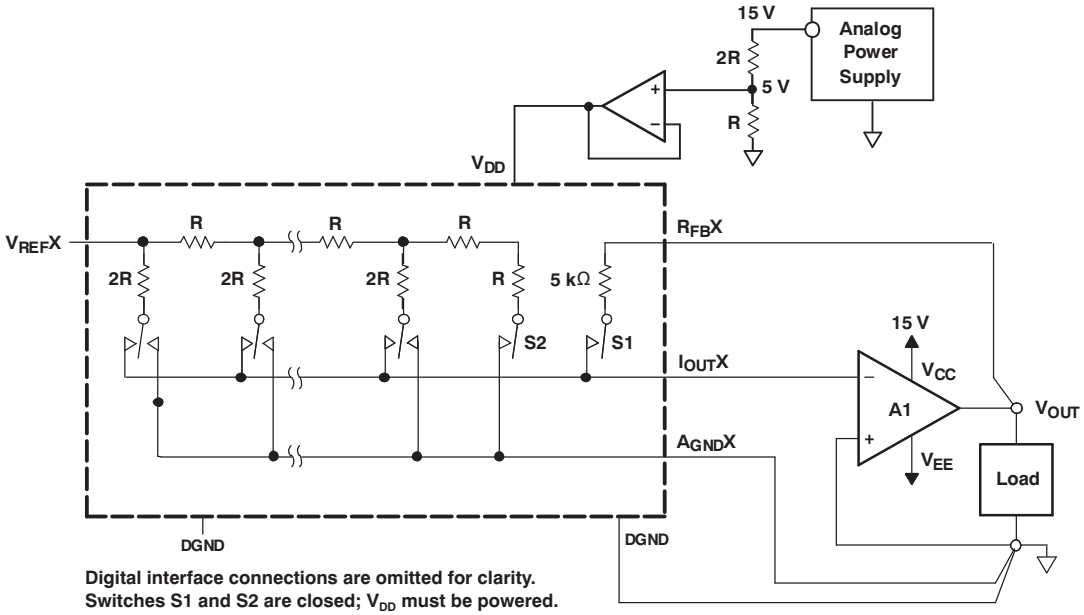


Figure 31. Recommended Kelvin-Sensed Hookup

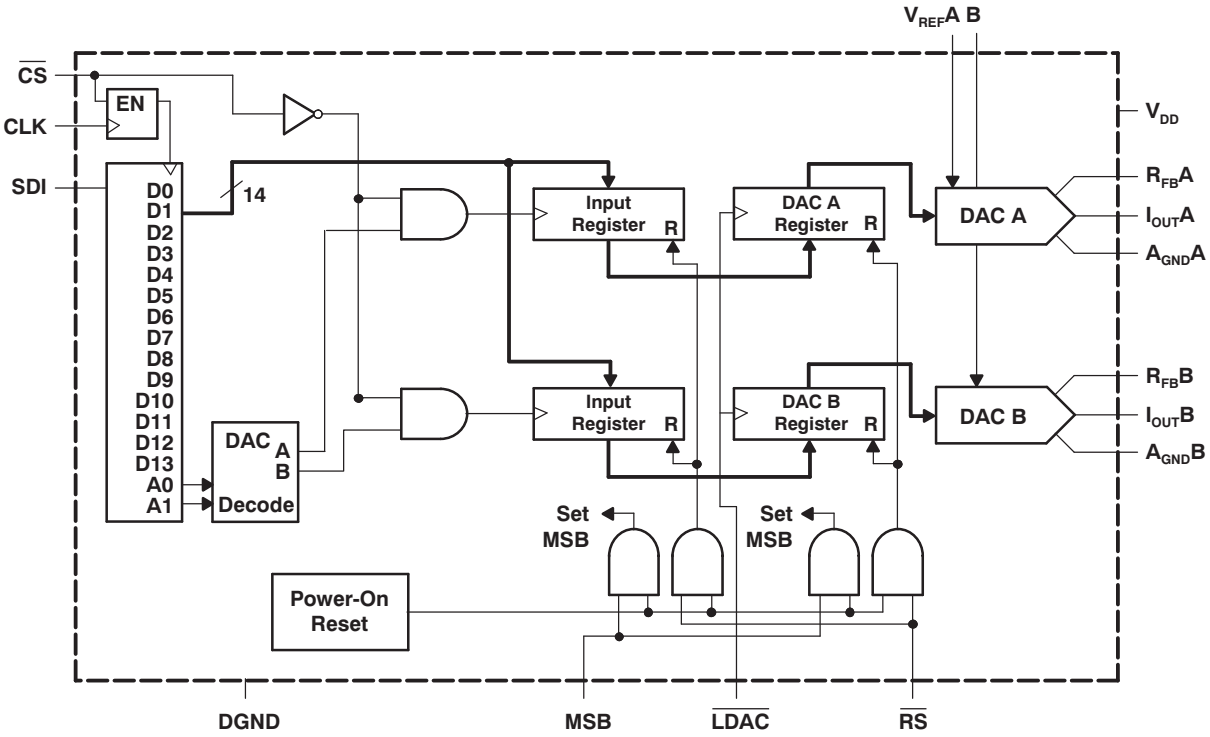


Figure 32. System Level Digital Interfacing

SERIAL DATA INTERFACE

The DAC8802 uses a 3-wire ($\overline{CS}$, SDI, CLK) SPI-compatible serial data interface. Serial data of the DAC8802 is clocked into the serial input register in an 16-bit data-word format. MSB bits are loaded first. Table 1 defines the 16 data-word bits for the DAC8802.

Data is placed on the SDI pin, and clocked into the register on the positive clock edge of CLK subject to the data setup and data hold time requirements specified in the *Interface Timing* specifications of the Electrical Characteristics. Data can only be clocked in while the $\overline{CS}$ chip select pin is active low. For the DAC8802, only the last 16 bits clocked into the serial register are interrogated when the $\overline{CS}$ pin returns to the logic high state.

Since most microcontrollers output serial data in 8-bit bytes, two right-justified data bytes can be written to the DAC8802. Keeping the $\overline{CS}$ line low between the first and second byte transfer will result in a successful serial register update.

Once the data is properly aligned in the shift register, the positive edge of the $\overline{CS}$ initiates the transfer of new data to the target DAC register, determined by the decoding of address bits A1and A0. For the DAC8802, Table 1, Table 2, Table 3, and Figure 1 define the characteristics of the software serial interface.

Table 1. Serial Input Register Data Format, Data Loaded MSB First(1)

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
Data	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

(1) Only the last 16 bits of data clocked into the serial register (address + data) are inspected when the $\overline{CS}$ line positive edge returns to logic high. At this point an internally-generated load strobe transfers the serial register data contents (bits D13-D0) to the decoded DAC-input-register address determined by bits A1 and A0. Any extra bits clocked into the DAC8802 shift register are ignored; only the last 16 bits clocked in are used. If double-buffered data is not needed, the $\overline{LDAC}$ pin can be tied logic low to disable the DAC registers.

Table 2. Control Logic Truth Table(1)

$\overline{CS}$	CLK	$\overline{LDAC}$	$\overline{RS}$	MSB	SERIAL SHIFT REGISTER	INPUT REGISTER	DAC REGISTER
H	X	H	H	X	No effect	Latched	Latched
L	L	H	H	X	No effect	Latched	Latched
L	↑+	H	H	X	Shift register data advanced one bit	Latched	Latched
L	H	H	H	X	No effect	Latched	Latched
↑+	L	H	H	X	No effect	Selected DAC updated with current SR contents	Latched
H	X	L	H	X	No effect	Latched	Transparent
H	X	H	H	X	No effect	Latched	Latched
H	X	↑+	H	X	No effect	Latched	Latched
H	X	H	L	0	No effect	Latched data = 0000h	Latched data = 0000h
H	X	H	L	H	No effect	Latched data = 2000h	Latched data = 2000h

(1) ↑**+** = Positive logic transition; **X** = Do not care

Table 3. Address Decode

A1	A0	DAC DECODE
0	0	None
0	1	DAC A
1	0	DAC B
1	1	DAC A and DAC B

Figure 33 shows the equivalent logic interface for the key digital control pins for the DAC8802.

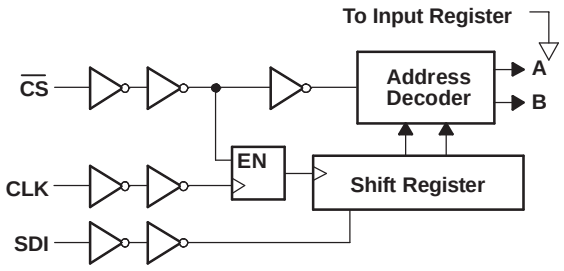


Figure 33. DAC8802 Equivalent Logic Interface

Two additional pins $\overline{RS}$ and MSB provide hardware control over the preset function and DAC register loading. If these functions are not needed, the $\overline{RS}$ pin can be tied to logic high. The asynchronous input $\overline{RS}$ pin forces all input and DAC registers to either the zero-code state (MSB = 0), or the half-scale state (MSB = 1).

POWER ON RESET

When the V_{DD} power supply is turned on, an internal reset strobe forces all the Input and DAC registers to the zero-code state or half-scale, depending on the MSB pin voltage. The V_{DD} power supply should have a smooth positive ramp without drooping, in order to have consistent results, especially in the region of V_{DD} = 1.5 V to 2.3 V. The DAC register data stays at the zero or half-scale setting until a valid serial register data load takes place.

ESD Protection Circuits

All logic-input pins contain back-biased ESD protection zener diodes connected to ground (DGND) and V_{DD}, as shown in Figure 34.

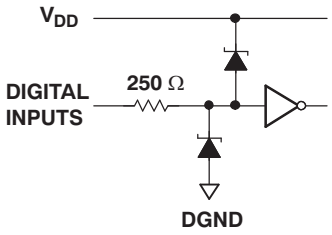


Figure 34. Equivalent ESD Protection Circuits

PCB LAYOUT

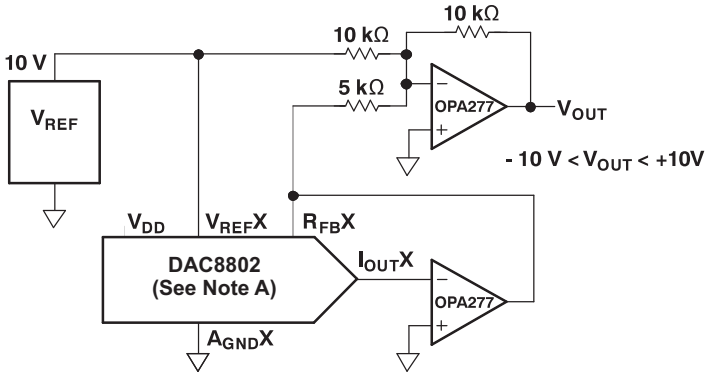
The DAC8802 is a high-accuracy DAC that can have its performance compromised by grounding and printed circuit board (PCB) lead trace resistance. The 14-bit DAC8802 with a 10-V full-scale range has an LSB value of 610 µV. The ladder and associated reference and analog ground currents for a given channel can be as high as 2 mA. With this 2 mA current level, a series wiring and connector resistance of only 305 mΩ will cause 1 LSB of voltage drop. The preferred PCB layout for the DAC8802 is to have all $A_{GND}X$ pins connected directly to an analog ground plane at the unit. The noninverting input of each channel I/V converter should also either connect directly to the analog ground plane or have an individual sense trace back to the $A_{GND}X$ pin connection. The feedback resistor trace to the I/V converter should also be kept short and low resistance to prevent IR drops from contributing to gain error. This attention to wiring ensures the optimal performance of the DAC8802.

APPLICATION INFORMATION

The DAC8802, a 2-quadrant multiplying DAC, can be used to generate a unipolar output. The polarity of the full-scale output I_{OUT} is the inverse of the input reference voltage at V_{REF}.

Some applications require full 4-quadrant multiplying capabilities or bipolar output swing, as shown in Figure 35. An additional external op amp (A2) is added as a summing amp. In this circuit, the first and second amps (A1 and A2) provide a gain of 2X that widens the output span to 20 V. A 4-quadrant multiplying circuit is implemented by using a 10-V offset of the reference voltage to bias A2. According to the following circuit transfer equation (Equation 2), input data (D) from code 0 to full scale produces output voltages of V_{OUT} = –10 V to V_{OUT} = 10 V.

$$V_{OUT} = \left(\frac{D}{8192} - 1\right) \times V_{REF} \quad (2)$$



A. This figure represents one channel only. X is channel A or B (i.e. V_{REF} x = V_{REF}A or V_{REF}B)

Figure 35. Four-Quadrant Multiplying Application Circuit

Cross-Reference

The DAC8802 has an industry-standard pinout. Table 4 provides the cross-reference information.

Table 4. Cross-Reference

PRODUCT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS-REFERENCE PART NUMBER
DAC8802IPW	±1	±1	-40°C to 85°C	16-Lead Thin Shrink Small-Outline Package	TSSOP-16	AD5555CRU

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8802IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8802	Samples
DAC8802IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8802	Samples
DAC8802IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8802	Samples
DAC8802IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8802	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

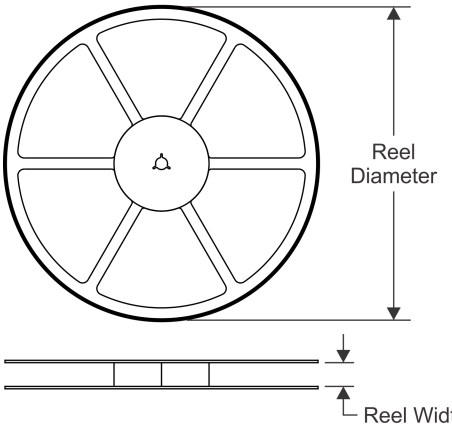
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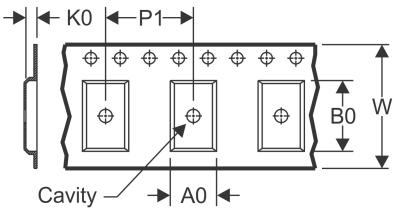
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

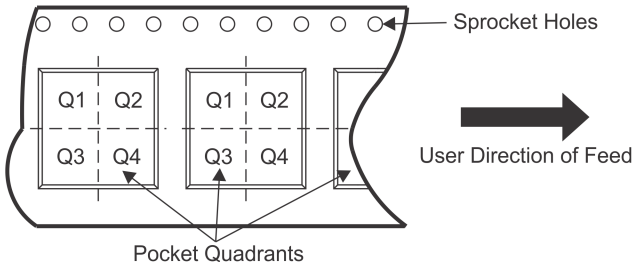


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

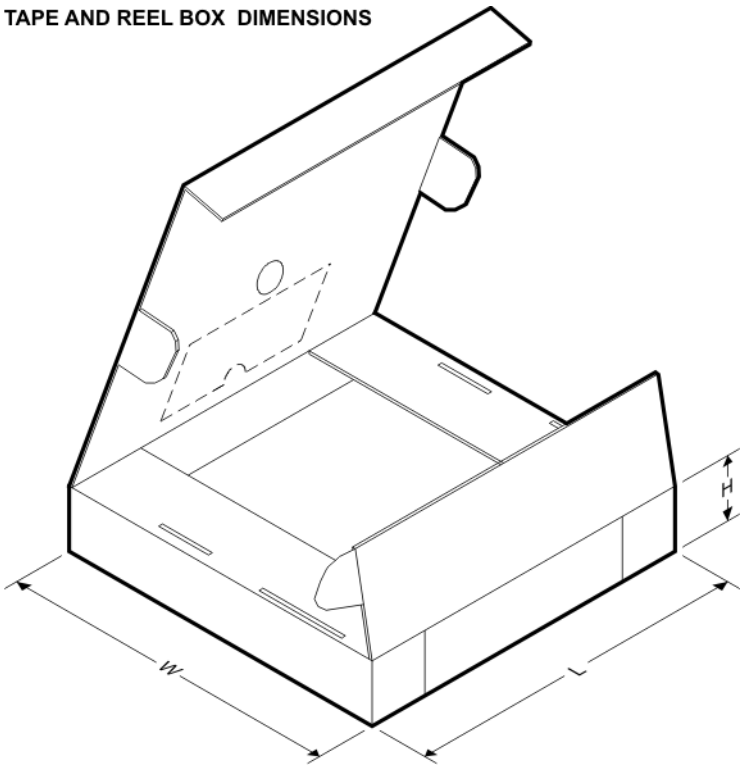
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8802IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

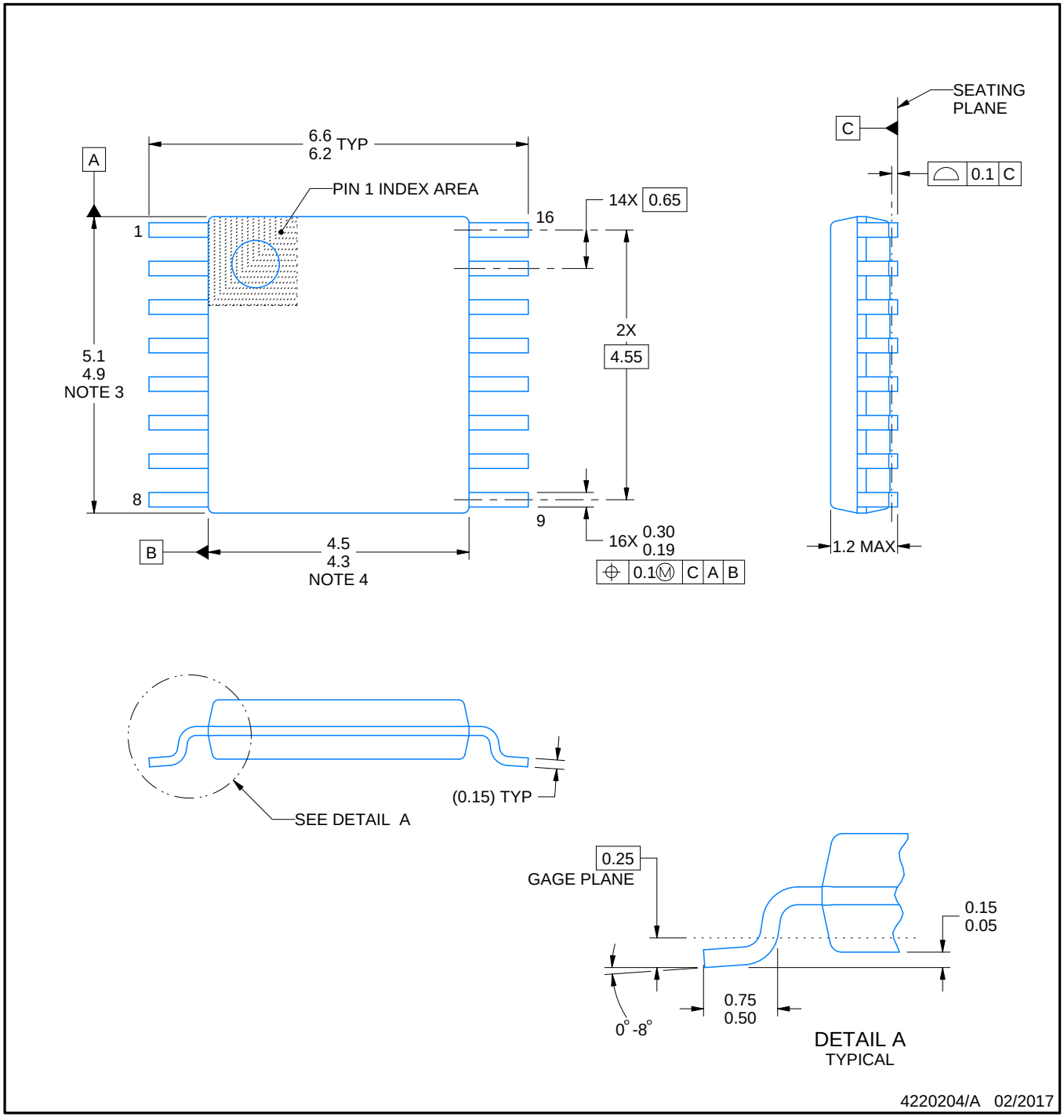
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8802IPWR	TSSOP	PW	16	2000	350.0	350.0	43.0

PACKAGE OUTLINE

PW0016A

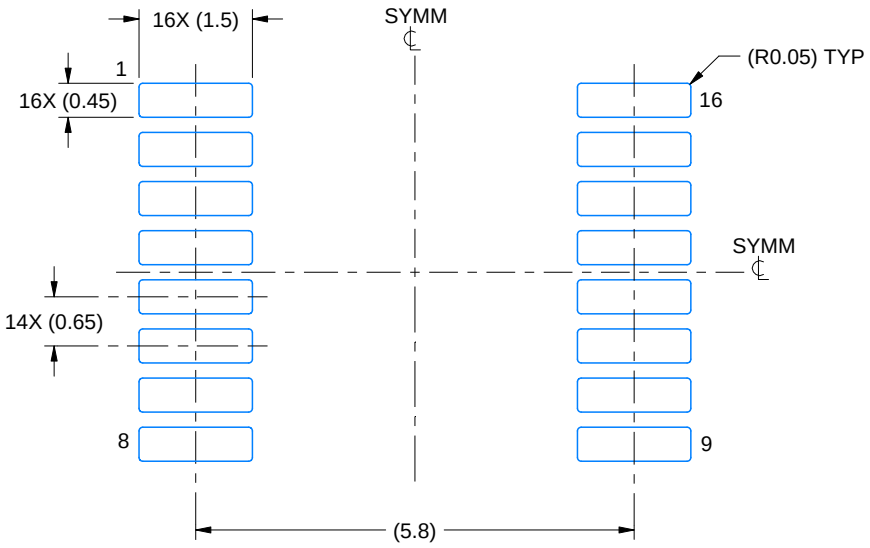
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

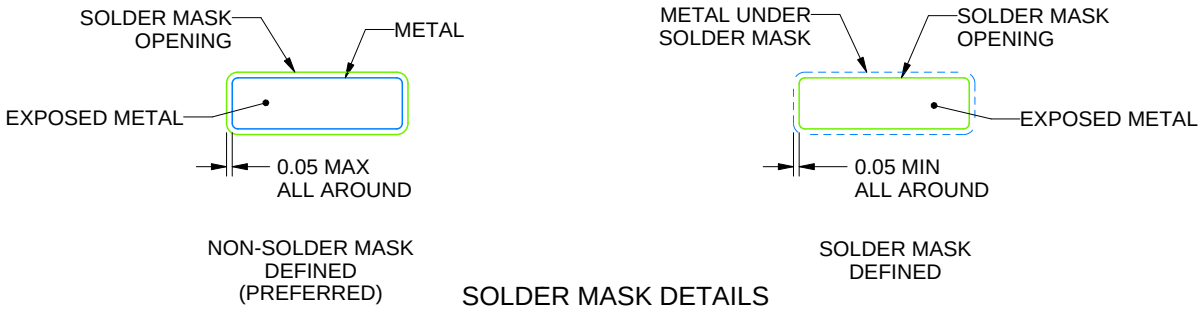


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

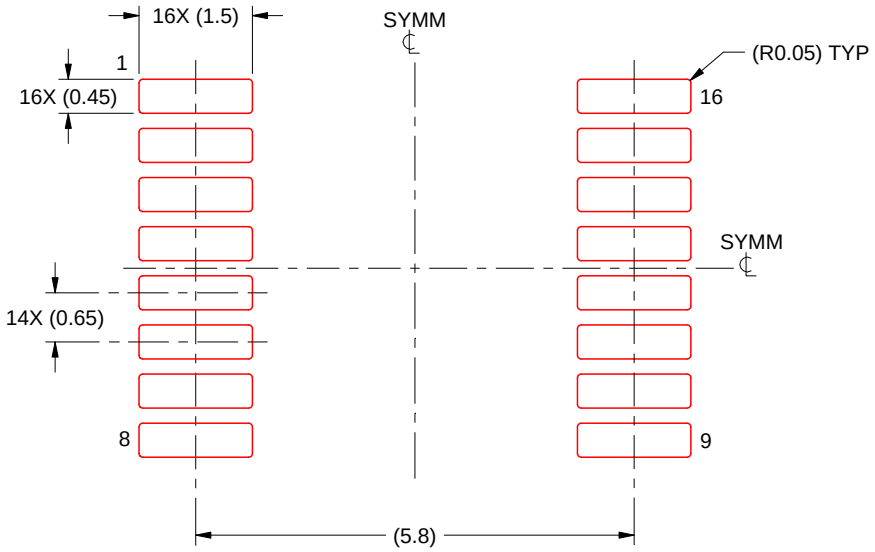


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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