FDWS9520L-F085

Power MOSFET, Dual P-Channel

−40 V, −20 A, 12.5 mΩ

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low QG and Capacitance to Minimize Driver Losses
- Wettable Flanks for Enhanced Optical Inspection
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−40	V
Gate−to−Source Voltage			V_{GS}	±16	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25°C	I_D	−60.8	A
		T_C = 100°C		−43.0	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	75	W
		T_C = 100°C		37.5	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_C = 25°C	I_D	−12.2	A
		T_C = 100°C		−8.6	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)		T_C = 25°C	P_D	3.0	W
		T_C = 100°C		1.5	
Pulsed Drain Current	T_C = 25°C, t_p = 10 μs		I_{DM}	−281	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	−20	A
Single Pulse Drain−to−Source Avalanche Energy (IL(pk) = −19)			E_{AS}	90	mJ
Lead Temperature for Soldering Purposes (1/83 from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

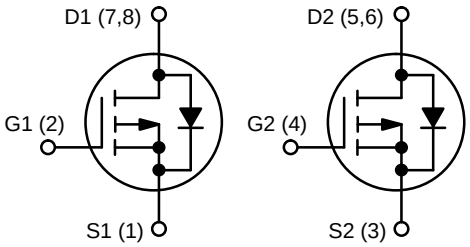
Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State	$R_{\theta JC}$	2	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	50	°C/W

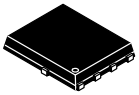
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

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$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
−40 V	12.5 mΩ @ −10 V	−20 A
	19.5 mΩ @ −4.5 V	





PQFN8 5x6, 1.27P
CASE 483BL

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 3 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Off Characteristics							
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}$/ T_J				21		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −40 V	T_J = 25°C			−1	μA
			T_J = 175°C			−1	mA
Zero Gate Voltage Drain Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±16 V				±100	nA
On Characteristics (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−1	−1.8	−3	V
Threshold Temperature Coefficient	$V_{GS(TH)}$/T_J				−5.5		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −10 V	I_D = −20 A		10.4	12.5	mΩ
		V_{GS} = −4.5 V	I_D = −10 A		14.6	19.5	
Charges, Capacitances & Gate Resistance							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = −20 V			2370		pF
Output Capacitance	C_{oss}				940		pF
Reverse Transfer Capacitance	C_{rss}				40		pF
Gate Resistance	R_g	V_{GS} = 0.5 V, f = 1 MHz			17		Ω
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −10 V, V_{DS} = −32 V; I_D = −20 A			33		nC
		V_{GS} = −4.5V, V_{DS} = −32 V; I_D = −20 A			13		
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to −1 V			2		
Gate to Source Gate Charge	Q_{gs}	V_{DD} = −20 V, I_D = −20 A			7		
Gate to Drain “Miller” Charge	Q_{gd}				4		
Plateau Voltage	V_{GP}				−4		V
Switching Characteristics							
Turn−On Delay Time	$t_{d(ON)}$	V_{DD} = −20 V, I_D = −20 A, V_{GS} = −10 V, R_{GEN} = 6 Ω			8		ns
Turn−On Rise Time	t_r				21		ns
Turn−Off Delay Time	$t_{d(OFF)}$				120		ns
Turn−Off Fall Time	t_f				34		ns
Drain−Source Diode Characteristics							
Source to Drain Diode Voltage	V_{SD}	I_{SD} = −20 A, V_{GS} = 0 V			−0.9	−1.25	V
		I_{SD} = −10 A, V_{GS} = 0 V			−0.83	−1.2	V
Reverse Recovery Time	T_{RR}	V_{GS} = 0 V, dI_{SD}/dt = 100 A/us, I_S = −20 A			46		ns
Charge Time	t_a				22		
Discharge Time	t_b				24		
Reverse Recovery Charge	Q_{RR}				37		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
5. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Device Marking	Package	Shipping†
FDWS9520L−F085	FDWS9520L	PQFN8 5x6, 12.7P (Pb−Free, Halogen Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

TYPICAL CHARACTERISTICS

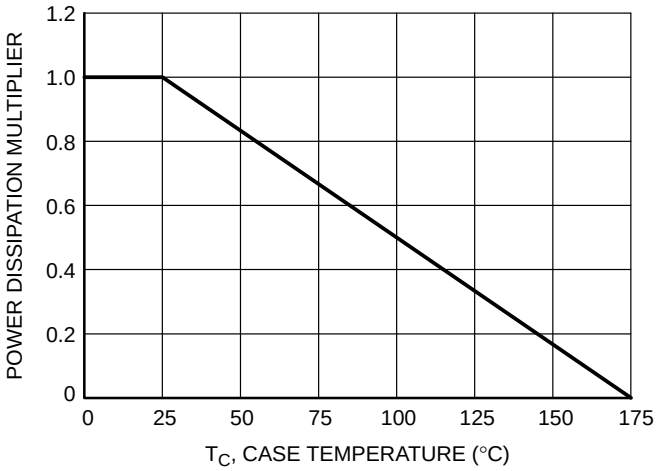


Figure 1. Normalized Power Dissipation vs. Case Temperature

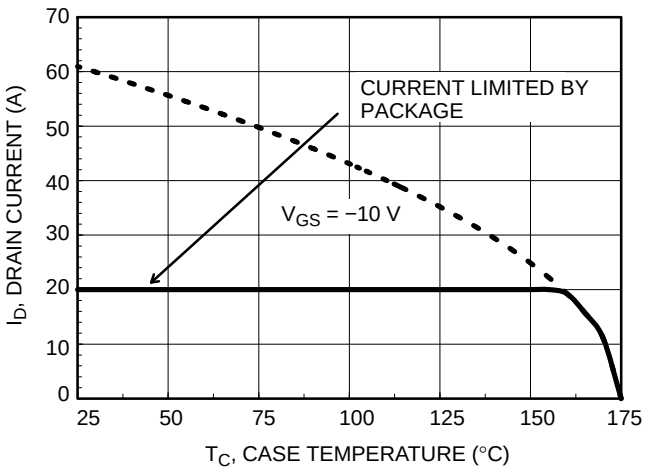


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

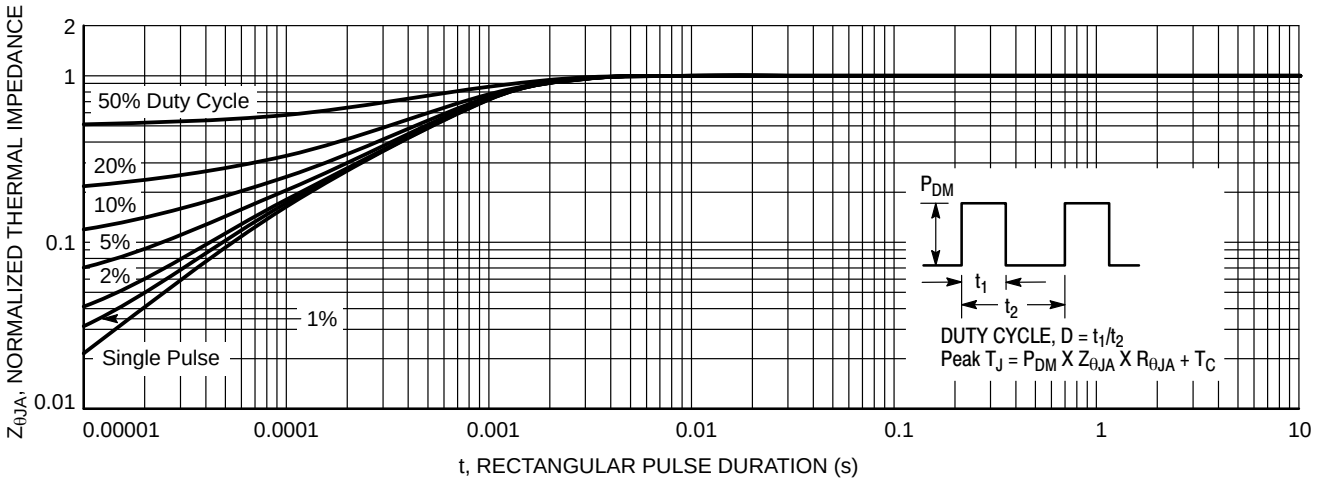


Figure 3. Normalized Maximum Transient Thermal Impedance

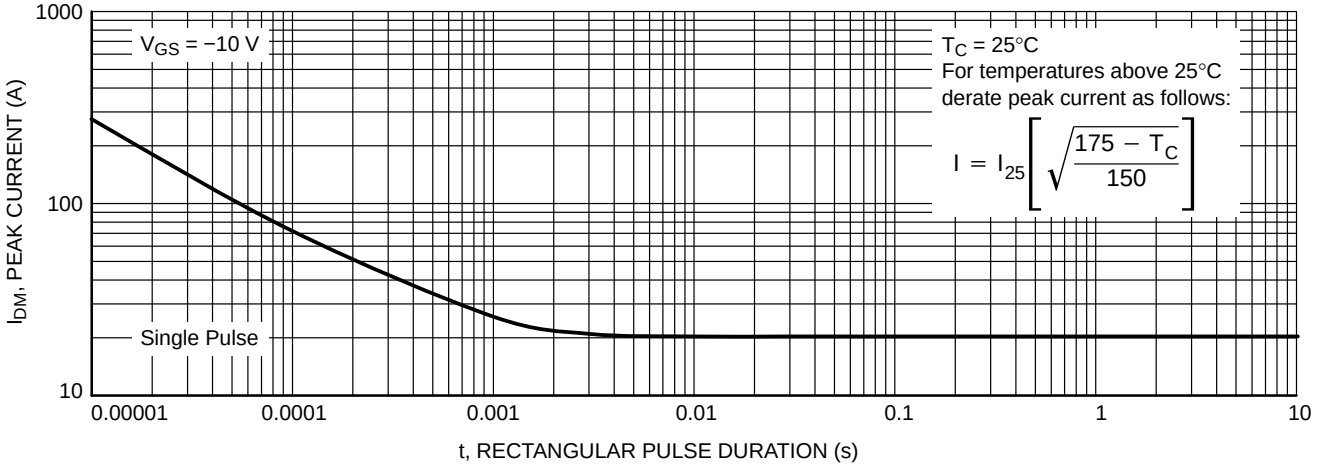


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

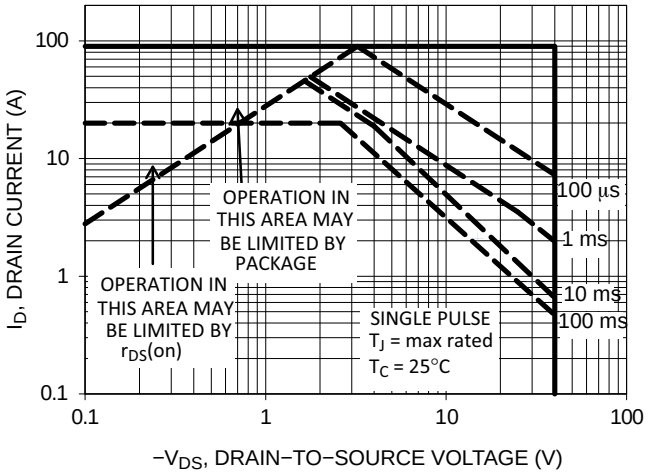
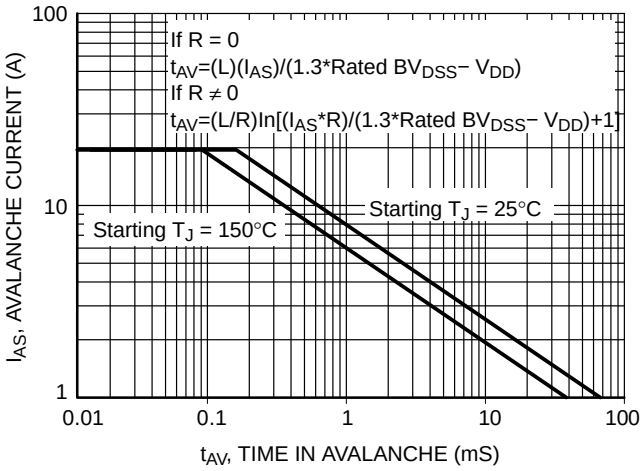


Figure 5. Forward Bias Safe Operating Area



Note: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

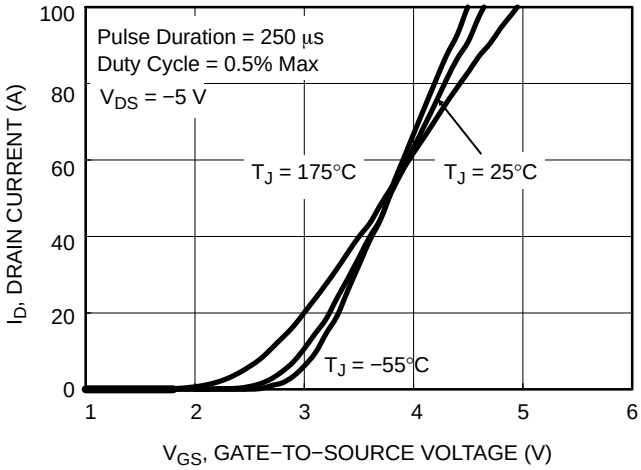


Figure 7. Transfer Characteristics

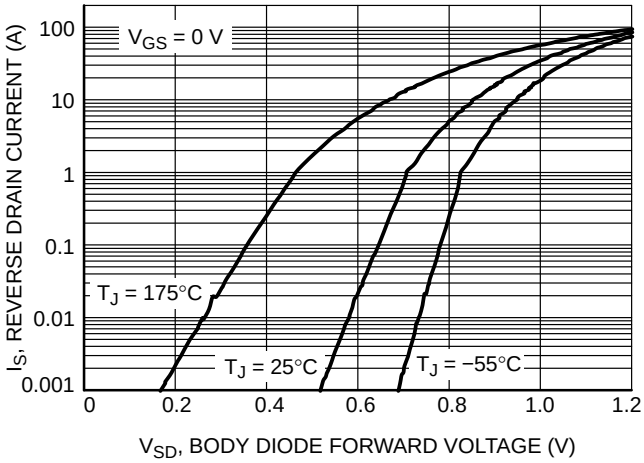


Figure 8. Forward Diode Characteristics

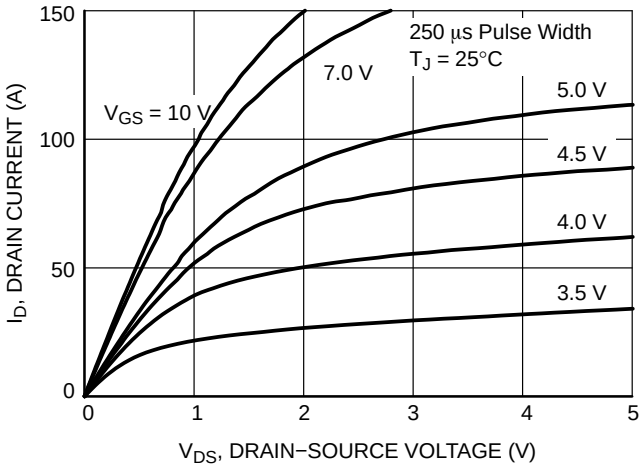


Figure 9. Saturation Characteristics

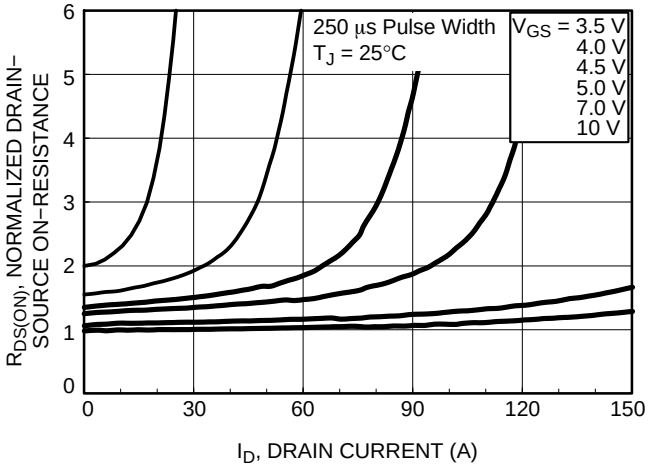


Figure 10. Normalized $R_{DS(ON)}$ vs. Drain Current

TYPICAL CHARACTERISTICS

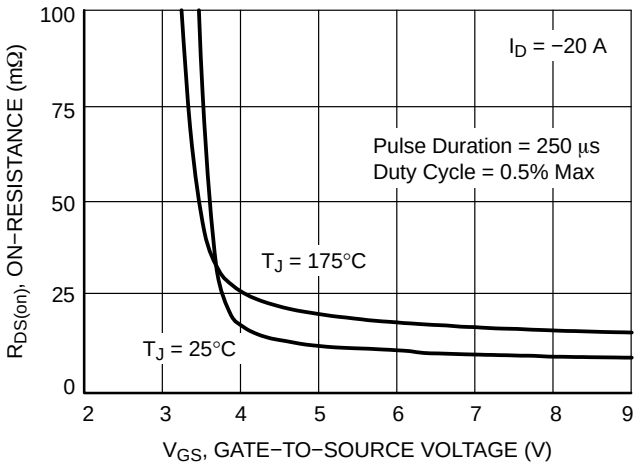


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

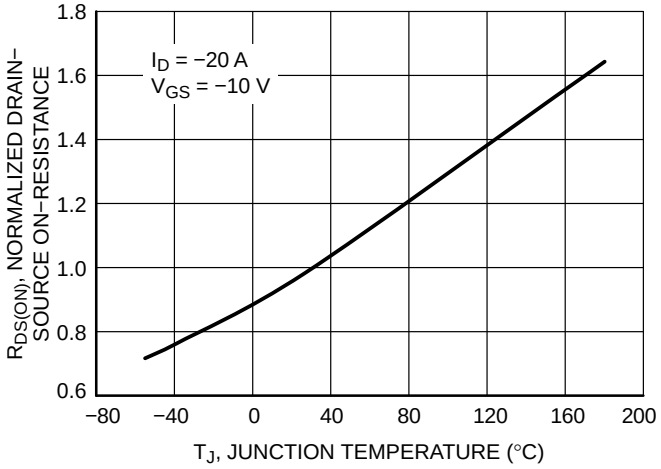


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

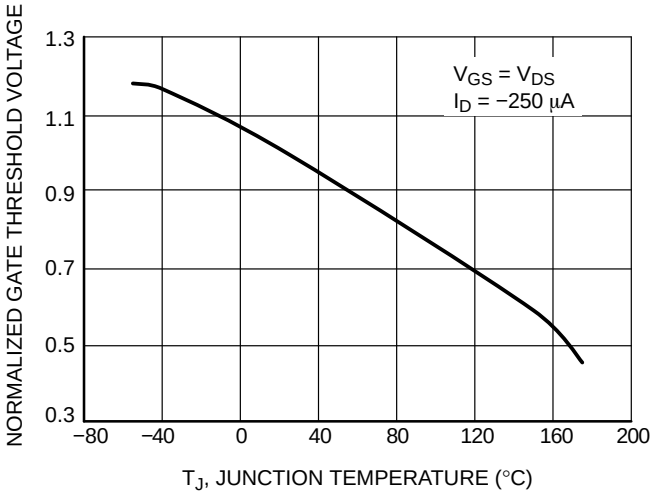


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

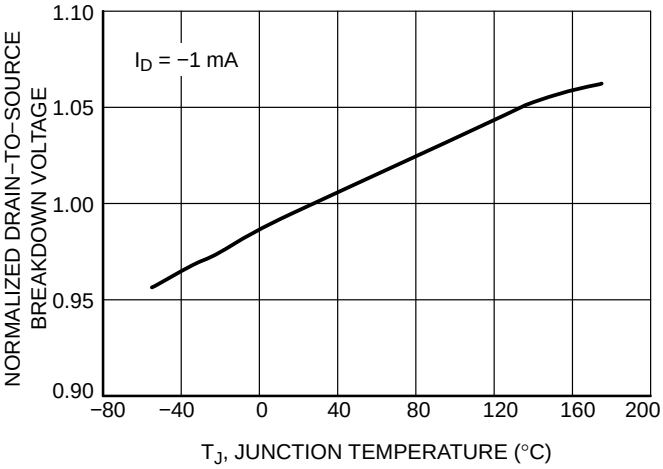


Figure 14. Normalized Drain−to−Source Breakdown Voltage vs. Junction Temperature

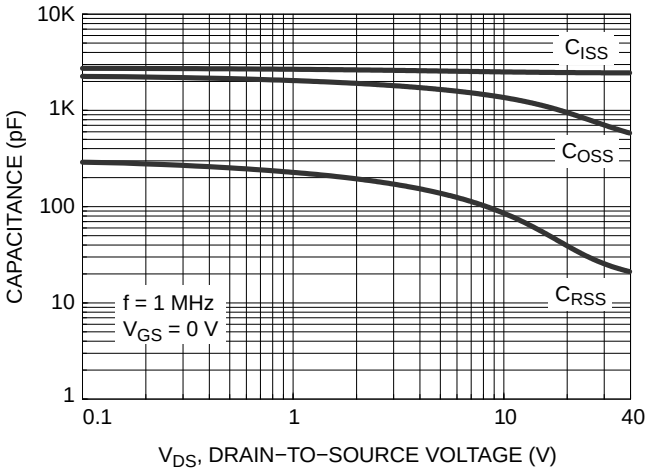


Figure 15. Capacitance vs. Drain−to−Source Voltage

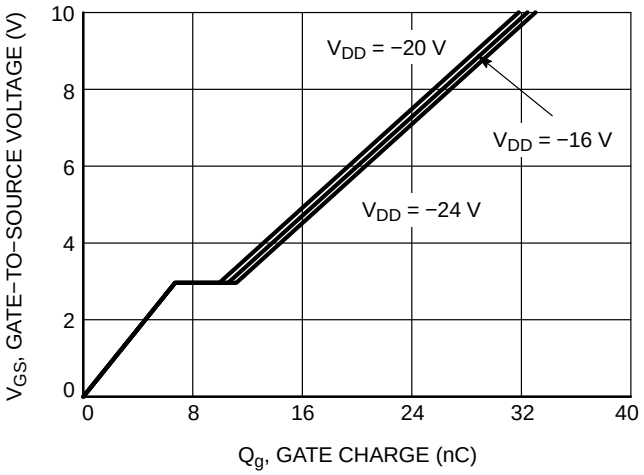
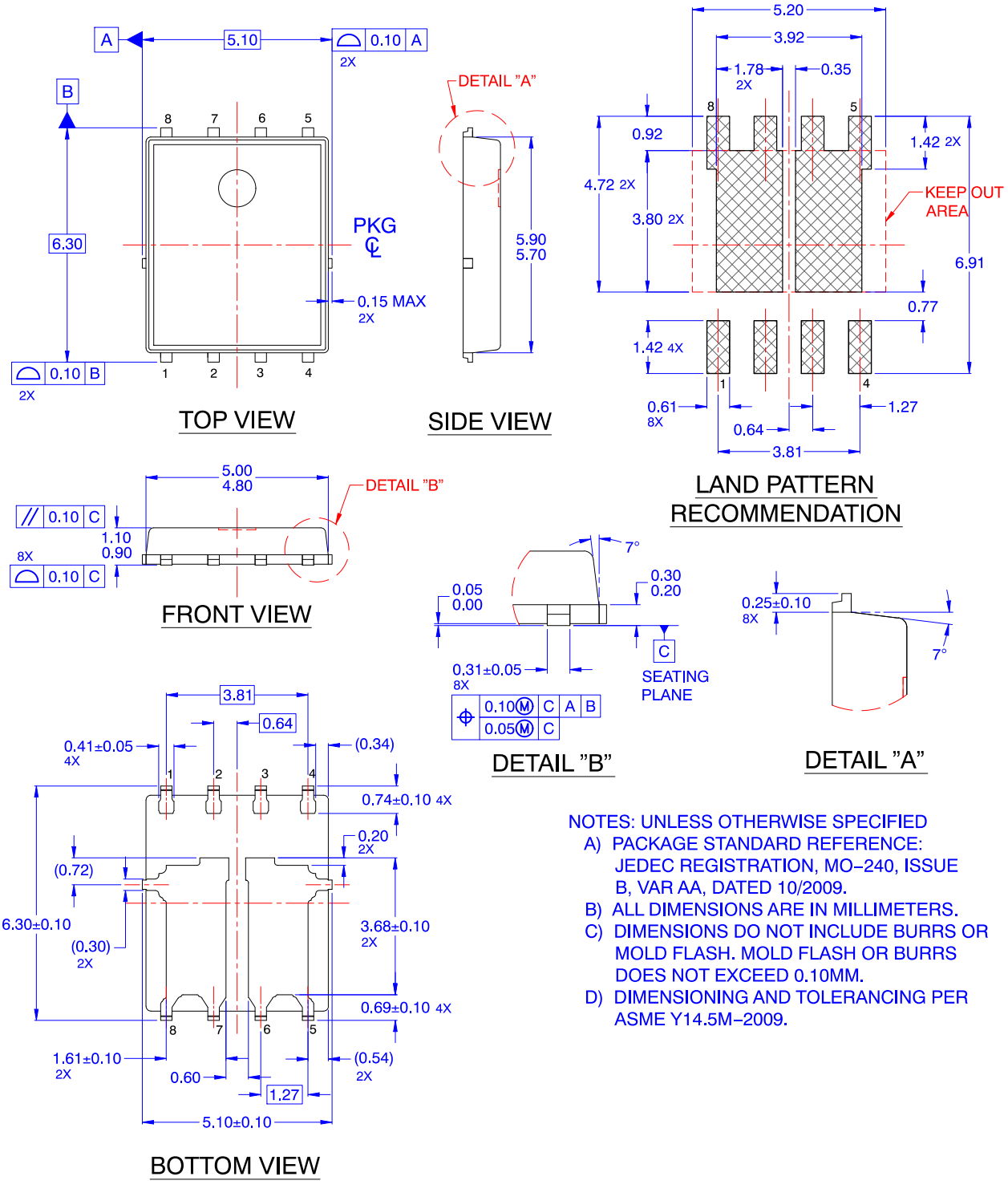


Figure 16. Gate Charge vs. Gate−to−Source Voltage

PACKAGE DIMENSIONS

PQFN8 5X6, 1.27P
CASE 483BL
ISSUE O



NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC REGISTRATION, MO−240, ISSUE B, VAR AA, DATED 10/2009.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−2009.

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