SN74HCS74 Schmitt-Trigger Input Dual D-Type Positive-Edge-Triggered Flip-Flops With Clear and Preset

1 Features

- Wide operating voltage range: 2 V to 6 V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
  - Typical I_{CC} of 100 nA
  - Typical input leakage current of ±100 nA
- ±7.8-mA output drive at 5 V
- Extended ambient temperature range: –40°C to +125°C, T_A

2 Applications

- Convert a momentary switch to a toggle switch
- Hold a signal during controller reset
- Input slow edge-rate signals
- Operate in noisy environments
- Divide a clock signal by two

3 Description

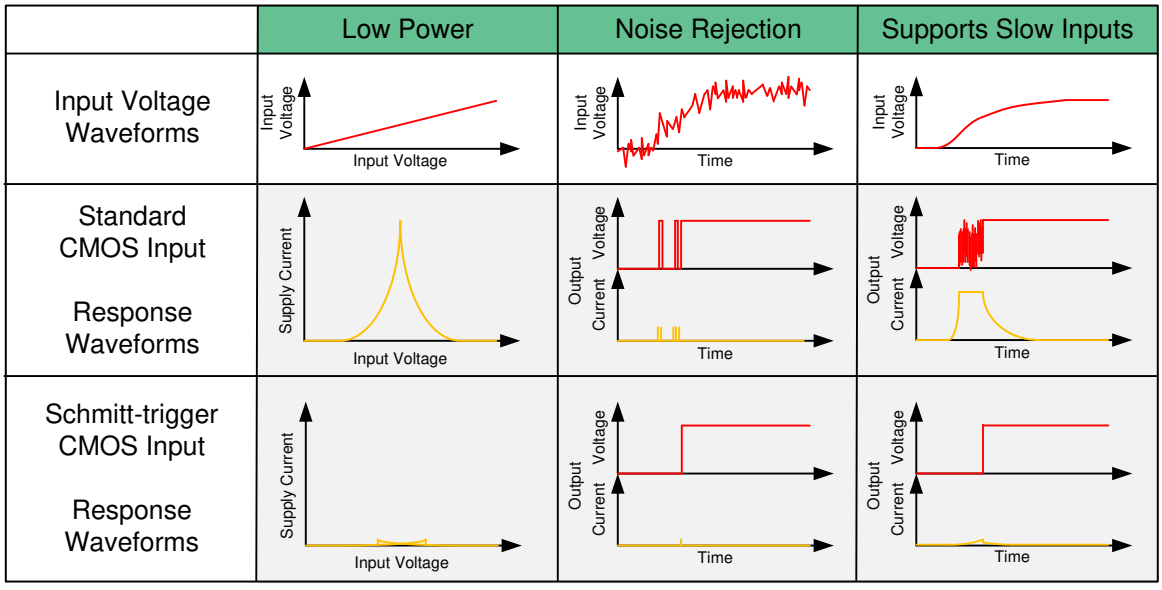
The device contains two independent D-type positive-edge-triggered flip-flops. All inputs include Schmitt triggers, allowing for slow or noisy input signals. A low level at the preset ($\overline{PRE}$) input sets the output high. A low level at the clear ($\overline{CLR}$) input resets the output low. Preset and clear functions are asynchronous and not dependent on the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs (Q, $\overline{Q}$) on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the input clock (CLK) signal. Following the hold-time interval, data at the data (D) input can be changed without affecting the levels at the outputs (Q, $\overline{Q}$).

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HCS74DR	SOIC (14)	8.70 mm x 3.90 mm
SN74HCS74PWR	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Benefits of Schmitt-trigger Inputs



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

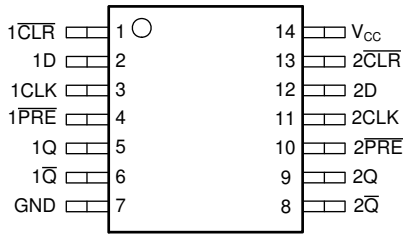
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2019) to Revision A	Page
• Added D package information to Device Information	1
• Added D package information to *Pin Configuration and Functions*	3
• Added D package column to *Thermal Information* table	4

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5 Pin Configuration and Functions

D and PW Package
14-Pin SOIC and TSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1$\overline{CLR}$	1	Input	Clear for channel 1, active low
1D	2	Input	Data for channel 1
1CLK	3	Input	Clock for channel 1, rising edge triggered
1$\overline{PRE}$	4	Input	Preset for channel 1, active low
1Q	5	Output	Output for channel 1
1$\overline{Q}$	6	Output	Inverted output for channel 1
GND	7	—	Ground
2$\overline{Q}$	8	Output	Inverted output for channel 2
2Q	9	Output	Output for channel 2
2$\overline{PRE}$	10	Input	Preset for channel 2, active low
2CLK	11	Input	Clock for channel 2, rising edge triggered
2D	12	Input	Data for channel 2
2$\overline{CLR}$	13	Input	Clear for channel 2, active low
V_{CC}	14	—	Positive supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output clamp current(2)	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature(3)			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Guaranteed by design.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC		SN74HCS74		UNIT
		PW (TSSOP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.7	133.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.4	89.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	89.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.2	45.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.1	89.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

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6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
V_{T-}	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9		2.2	
				6 V	1.2		3.0	
ΔV_T	Hysteresis (V_{T+} - V_{T-})(1)			2 V	0.2		1.0	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = -20 µA	2 V to 6 V	V_{CC} – 0.1	V_{CC} – 0.002		V
			I_{OH} = -6 mA	4.5 V	4.0	4.3		
			I_{OH} = -7.8 mA	6 V	5.4	5.75		
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V to 6 V		0.002	0.1	V
			I_{OL} = 6 mA	4.5 V		0.18	0.30	
			I_{OL} = 7.8 mA	6 V		0.22	0.33	
I_I	Input leakage current	V_I = V_{CC} or 0		6 V		±100	±1000	nA
I_{CC}	Supply current	V_I = V_{CC} or 0, I_O = 0		6 V		0.1	2	µA
C_i	Input capacitance			2 V to 6 V			5	pF
C_{pd}	Power dissipation capacitance per gate	No load		2 V to 6 V		10		pF

(1) Guaranteed by design.

6.6 Switching Characteristics

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See Parameter Measurement Information.

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
f_{max}	Max switching frequency			2 V	18	31		MHz
				4.5 V	45	95		
				6 V	65	105		
t_{pd}	Propagation delay	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		19	42	ns
				4.5 V		8	19	
				6 V		7	15	
		CLK	Q or $\overline{Q}$	2 V		19	42	ns
				4.5 V		8	19	
				6 V		7	15	
t_t	Transition-time		Q or $\overline{Q}$	2 V		9	16	ns
				4.5 V		5	9	
				6 V		4	8	

6.7 Timing Characteristics

C_L = 50 pF; over operating free-air temperature range (unless otherwise noted). See Parameter Measurement Information.

PARAMETER			V_{CC}	MIN	MAX	UNIT
f_{clock}	Clock frequency		2 V		18	MHz
			4.5 V		45	
			6 V		65	

Timing Characteristics (continued)

C_L = 50 pF; over operating free-air temperature range (unless otherwise noted). See Parameter Measurement Information.

PARAMETER			V_{CC}	MIN	MAX	UNIT
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2 V	11		ns
			4.5 V	11		
			6 V	11		
		CLK high or low	2 V	14		ns
			4.5 V	12		
			6 V	11		
t_{su}	Setup time before CLK high	Data	2 V	24		ns
			4.5 V	9		
			6 V	6		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2 V	7		ns
			4.5 V	5		
			6 V	5		
t_h	Hold time	Data after CLK↑	2 V	0		ns
			4.5 V	0		
			6 V	0		

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6.8 Typical Characteristics

T_A = 25°C

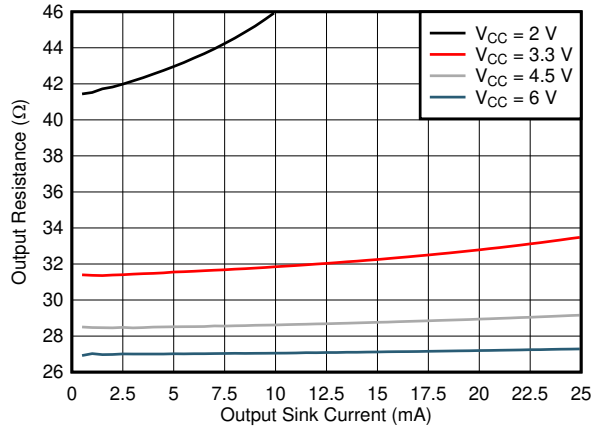


Figure 1. Output driver resistance in LOW state.

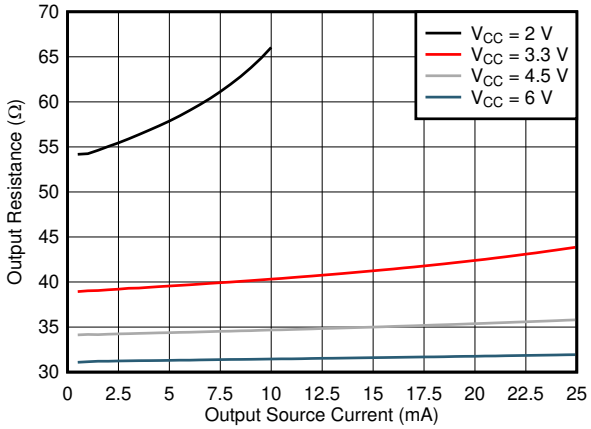


Figure 2. Output driver resistance in HIGH state.

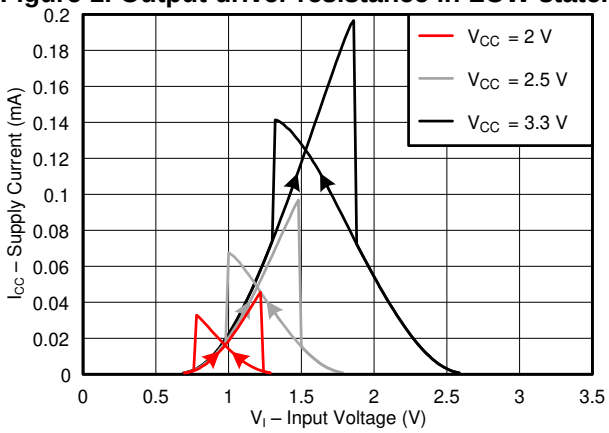


Figure 3. Supply current across input voltage, 2-, 2.5-, and 3.3-V supply

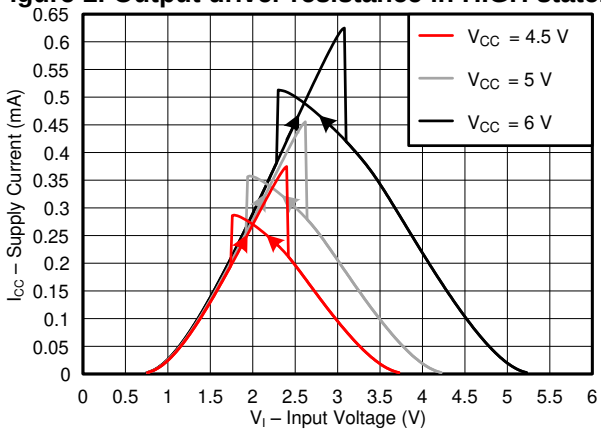


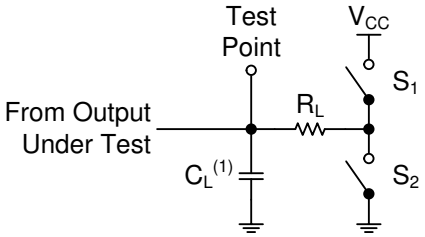
Figure 4. Supply current across input voltage, 4.5-, 5-, and 6-V supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 2.5 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



C_L includes probe and test-fixture capacitance.

Figure 5. Load Circuit

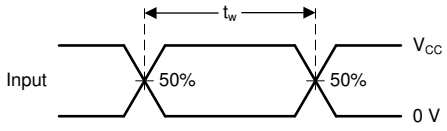


Figure 6. Voltage Waveforms, Pulse Duration

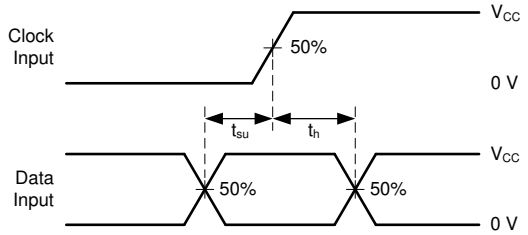
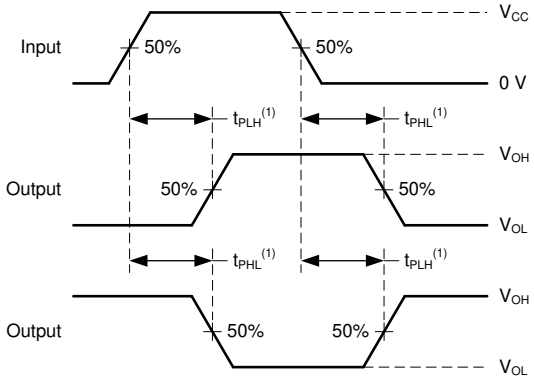


Figure 7. Voltage Waveforms, Setup and Hold Times



Voltage Waveforms, Propagation Delay specifications t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 8.

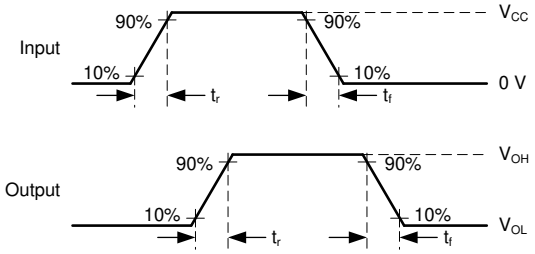


Figure 9. Voltage Waveforms, Input and Output Transition Times

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8 Detailed Description

8.1 Overview

Figure 10 describes the SN74HCS74. As the SN74HCS74 is a dual D-Type positive-edge-triggered flip-flop with clear and preset, the diagram below describes one of the two device flip-flops.

8.2 Functional Block Diagram

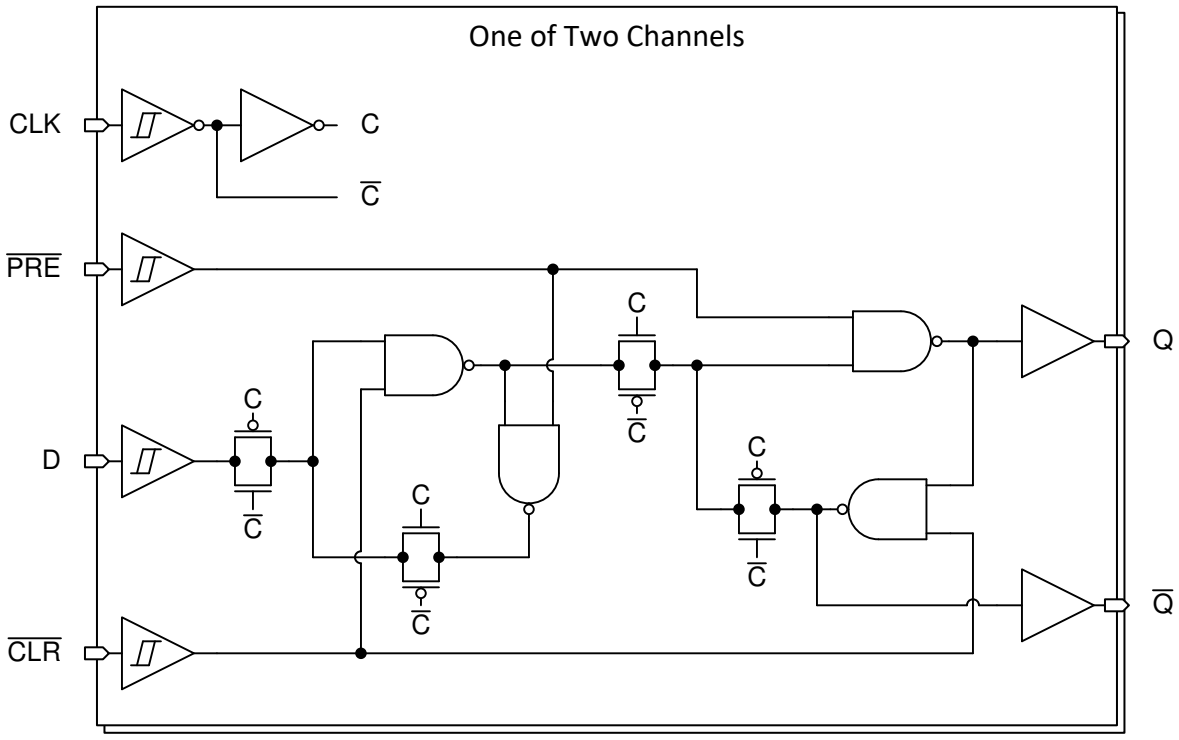


Figure 10. Logic Diagram (Positive Logic) for one channel of SN74HCS74

8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* must be followed at all times.

8.3.2 CMOS Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics*, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

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Feature Description (continued)

8.3.3 Positive and Negative Clamping Diodes

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Figure 11.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

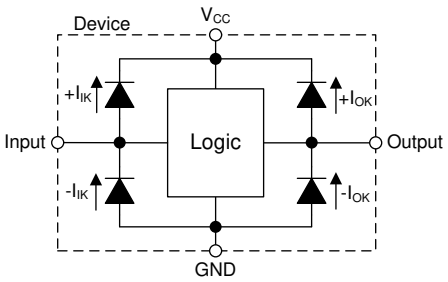


Figure 11. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74HCS74.

Table 1. Function Table

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H(1)	H(1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

(1) This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Toggle switches are typically large, mechanically complex and relatively expensive. It is desirable to use a momentary switch instead because they are small, mechanically simple and low cost. Some systems require a toggle switch's functionality but are space or cost constrained and must use a momentary switch instead. The SN74HCS74 has integrated Schmitt-trigger inputs that eliminate the need for a second IC for signal conditioning, reducing the required board space. This makes the SN74HCS74 an ideal device for converting a momentary switch into a toggle switch.

If the data input (D) of the SN74HCS74 is tied to the inverted output ($\overline{Q}$), then each clock pulse will cause the value at the output (Q) to toggle. The momentary switch can be debounced and directly connected to the clock input (CLK) to toggle the output.

9.2 Typical Application

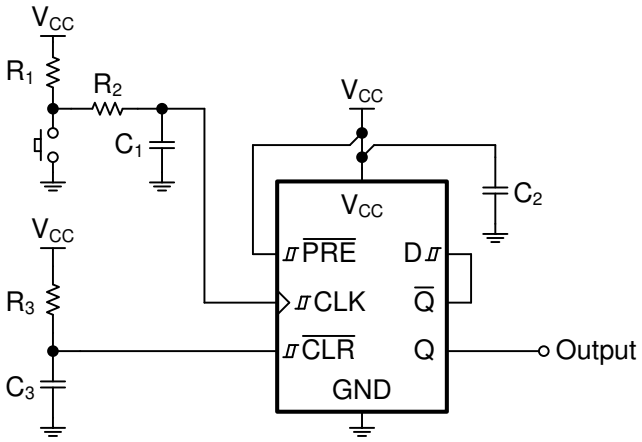


Figure 12. Device Power Button Circuit

9.2.1 Design Requirements

The supply voltage of the D-Type flip-flop must be chosen to meet the supply voltage specification from the *Recommended Operating Conditions*. The same supply must be used for the pushbutton and power on reset circuit allowing for the high and low level input voltage conditions, V_{T+} and V_{T-}, to meet the requirements in *Electrical Characteristics*.

When the flip-flop is first powered on, it will start in an unknown state if both the ($\overline{PRE}$) and ($\overline{CLR}$) pins are directly tied high. However, if either the ($\overline{PRE}$) or ($\overline{CLR}$) pin is held low, then the flip-flop will be in a known state.

With the SN74HCS74, a power on reset circuit only requires a resistor (R) and capacitor (C) to create a delay. The R and C values create a delay that is approximately 2.2×RC. An additional Schmitt-trigger input device would be required to allow this slow rise if the flip-flop did not have Schmitt-trigger inputs. In this application, it is desired to have the output (Q) in the LOW state at startup, so R_3 and C_3 are connected directly to the $\overline{CLR}$ pin, as shown in Figure 12.

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Typical Application (continued)

9.2.1.1 Designing with Momentary Switches

Push buttons are the most common type of momentary switch. This application uses a normally open push-button switch. The mechanical linkages inside a switch can bounce, causing multiple outputs for each button press. It is important to eliminate these multiple outputs when working with a device fast enough to trigger from each bounce, such as the SN74HCS74.

To eliminate this bouncing, a debounce circuit can be used. The debounce circuit is a delay circuit, consisting of a resistor and a capacitor, that smooths out the bouncing enough to produce a single transition. Similar to the power on reset circuit, the resistor and capacitor values create a delay that is approximately 2.2 times the RC time constant. ($t_{delay} \approx 2.2RC$). To prevent a false trigger during power on, the debounce delay needs to be much smaller than the power on reset circuit's delay ($R_3 \times C_3 >> R_2 \times C_1$).

The D-Type flip-flop reads in the input (D) when there is a positive edge on the clock. The circuitry described above is called a 'trigger on release' system, producing a positive clock edge only when the button is released. The 'trigger on press' circuit can be achieved by simply swapping the R_1 and button positions in the schematic.

9.2.1.2 Output Considerations

In general, the load needs to be considered in the design to determine if the device will have the capability to drive it. For this application, we assume that the button output is transmitting over a relatively short trace (under 10 cm) to a CMOS input on a microcontroller.

Primary load factors to consider:

- Load Capacitance: approximately 15 pF
  - See the *Switching Characteristics* section for the capacitive loads tested with this device.
  - Increasing capacitance will proportionally increase output transition times.
  - Decreasing capacitance will proportionally decrease output transition times, and can produce ringing due to very fast transition rates. A 25-Ω resistor can be added in series with the output if ringing needs to be dampened.
- Load Current: expected maximum of 10 µA
  - Leakage current into connected devices.
  - Parasitic current from other components.
  - Resistive load current.
- Output Voltage: see *Electrical Characteristics* for output voltage ratings at a given current.
  - Output HIGH (V_{OH}) and output LOW (V_{OL}) voltage levels affect the input voltage, V_{IH} and V_{IL}, respectively, to subsequent devices.

9.2.1.3 Input Considerations

The SN74HCS74 has Schmitt-trigger inputs. Schmitt-trigger inputs have no limitation on transition rate, however the input voltage must be larger than $V_{T+(max)}$ to be guaranteed to be read as a logic high, and below $V_{T-(min)}$ to be guaranteed to be read as a logic low, as defined in the *Electrical Characteristics*. Do not exceed the values specified in the *Absolute Maximum Ratings* or the device could be damaged.

9.2.1.4 Timing Considerations

The SN74HCS74 is a clocked device. As such, it requires special timing considerations to ensure normal operation.

Primary timing factors to consider:

- Maximum clock frequency: the maximum operating clock frequency defined in *Timing Characteristics* is the maximum frequency at which the device is guaranteed to function. This value refers specifically to the triggering waveform, measuring from one trigger level to the next.
- Pulse duration: ensure that the triggering event duration is larger than the minimum pulse duration, as defined in the *Timing Characteristics*.
- Setup time: ensure that the data has changed at least one setup time prior to the triggering event, as defined in the *Timing Characteristics*.
- Hold time: ensure that the data remains in the desired state at least one hold time after the triggering event,

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Typical Application (continued)

as defined in the *Timing Characteristics*.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - Input signals to Schmitt-trigger inputs, like those found on the HCS family of devices, can support unlimited edge rates.
   - Input thresholds are listed in the *Electrical Characteristics*.
   - Inputs include positive clamp diodes. Input voltages can exceed the device's supply so long as the clamp current ratings are observed from the *Absolute Maximum Ratings*. Do not exceed the absolute maximum voltage rating of the device or it could be damaged.
2. Recommended Output Conditions:
   - Load currents should not exceed the value listed in the *Absolute Maximum Ratings*.
   - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.
3. Recommended Circuit Design Procedure:
   - For proper startup, the debounce circuit should have a much smaller delay than the power on reset circuit, $10R_2C_1 < R_3C_3$.
   - To perform a trigger on press instead of trigger on release, the button can be connected from V_{cc} to the input and R_1 can be connected from the input to the GND.

9.2.3 Application Curve

Figure 13 illustrates an example of a single button press bouncing and causing the output to toggle multiple times. This will cause issues in the desired application. Figure 14 illustrates 4 button presses with an added debounce circuit, fixing the unwanted toggling and allowing for proper toggle switch operation.

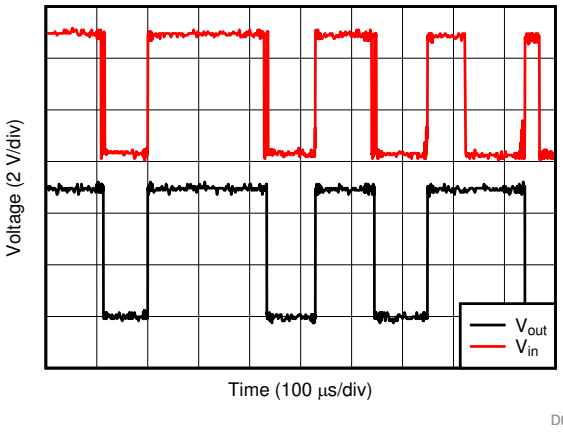


Figure 13. Circuit response without RC debounce
V_{in} := CLK input, V_{out} := Q output

Typical Application (continued)

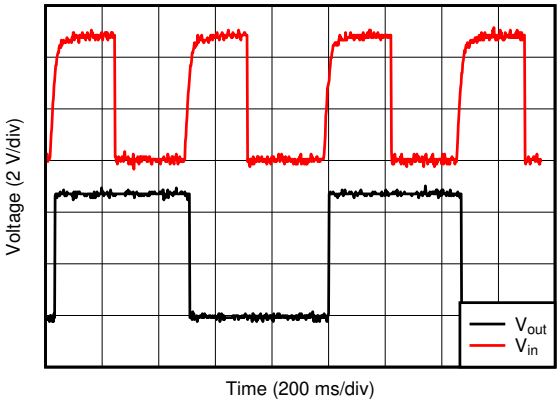


Figure 14. Circuit response with RC debounce
V_{in} := CLK input, V_{out} := Q output

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* table. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. For this device, a 0.1-µF capacitor is recommended. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminals as possible for best results.

11 Layout

11.1 Layout Guidelines

In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4 channels are used. Such input pins should not be left completely unconnected because the unknown voltages result in undefined operational states.

Specified in Figure 15 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is recommended to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This pin keeps the input section of the I/Os from being disabled and floated.

11.2 Layout Example

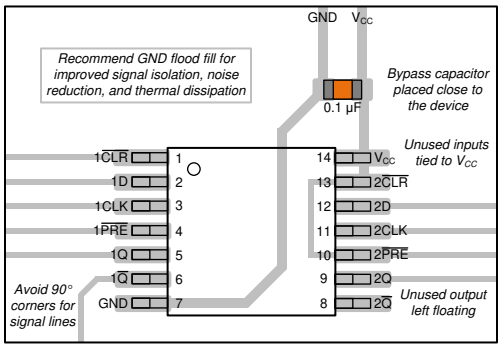


Figure 15. Layout Example

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Documentation Support

12.1.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report
- Texas Instruments, *Reduce Noise and Save Power with the New HCS Logic Family* application report
- Texas Instruments, *Understanding Schmitt Triggers* application report

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Trademarks

E2E is a trademark of Texas Instruments.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCS74DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HCS74	Samples
SN74HCS74PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HCS74	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74HCS74 :

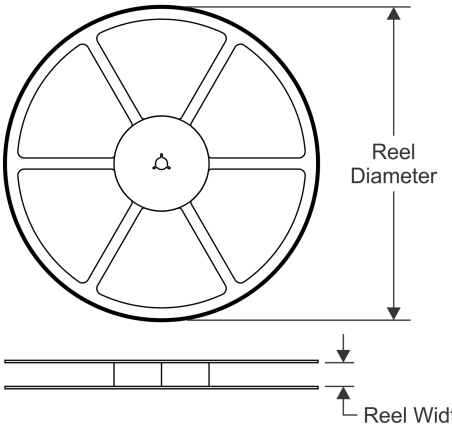
- Automotive: SN74HCS74-Q1

NOTE: Qualified Version Definitions:

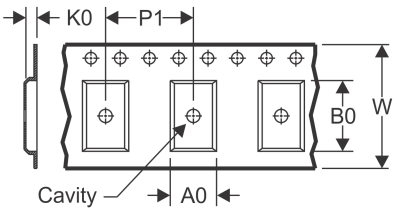
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

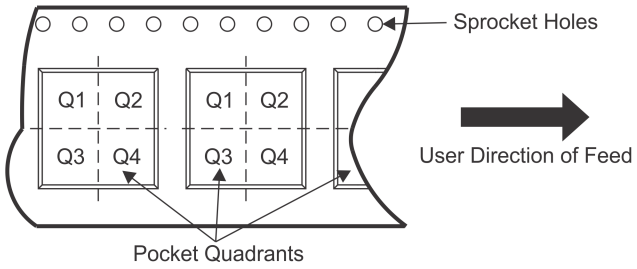


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

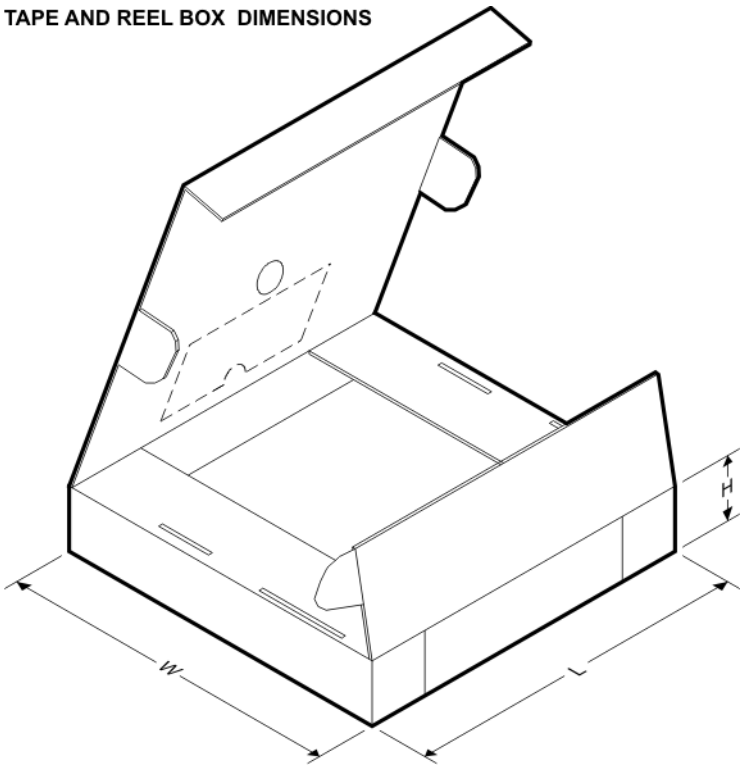
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCS74DR	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74HCS74PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCS74PWR	TSSOP	PW	14	2000	330.0	16.4	6.8	5.4	1.6	8.0	16.0	Q1

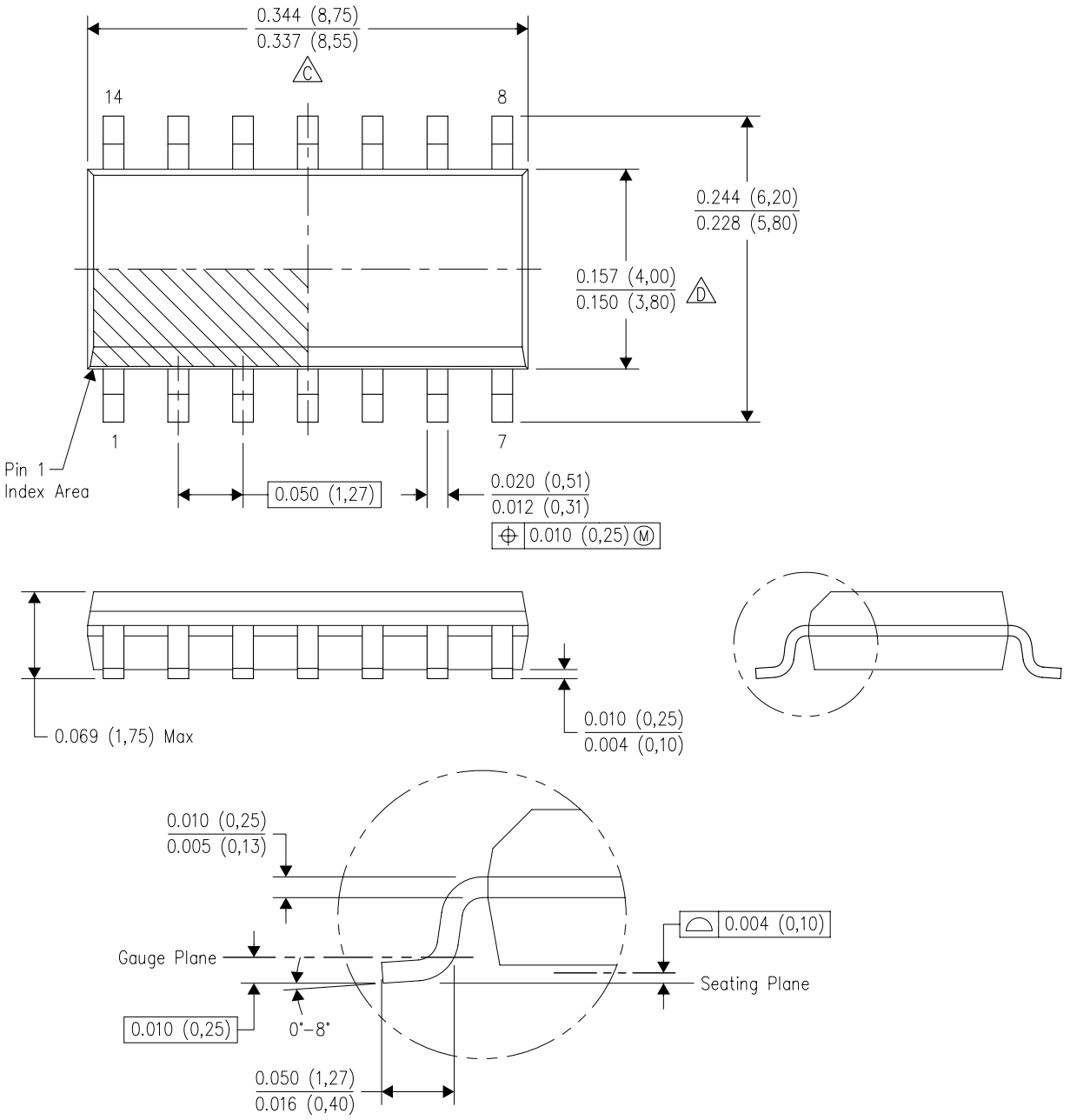
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS74DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74HCS74DR	SOIC	D	14	2500	366.0	364.0	50.0
SN74HCS74PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HCS74PWR	TSSOP	PW	14	2000	366.0	364.0	50.0

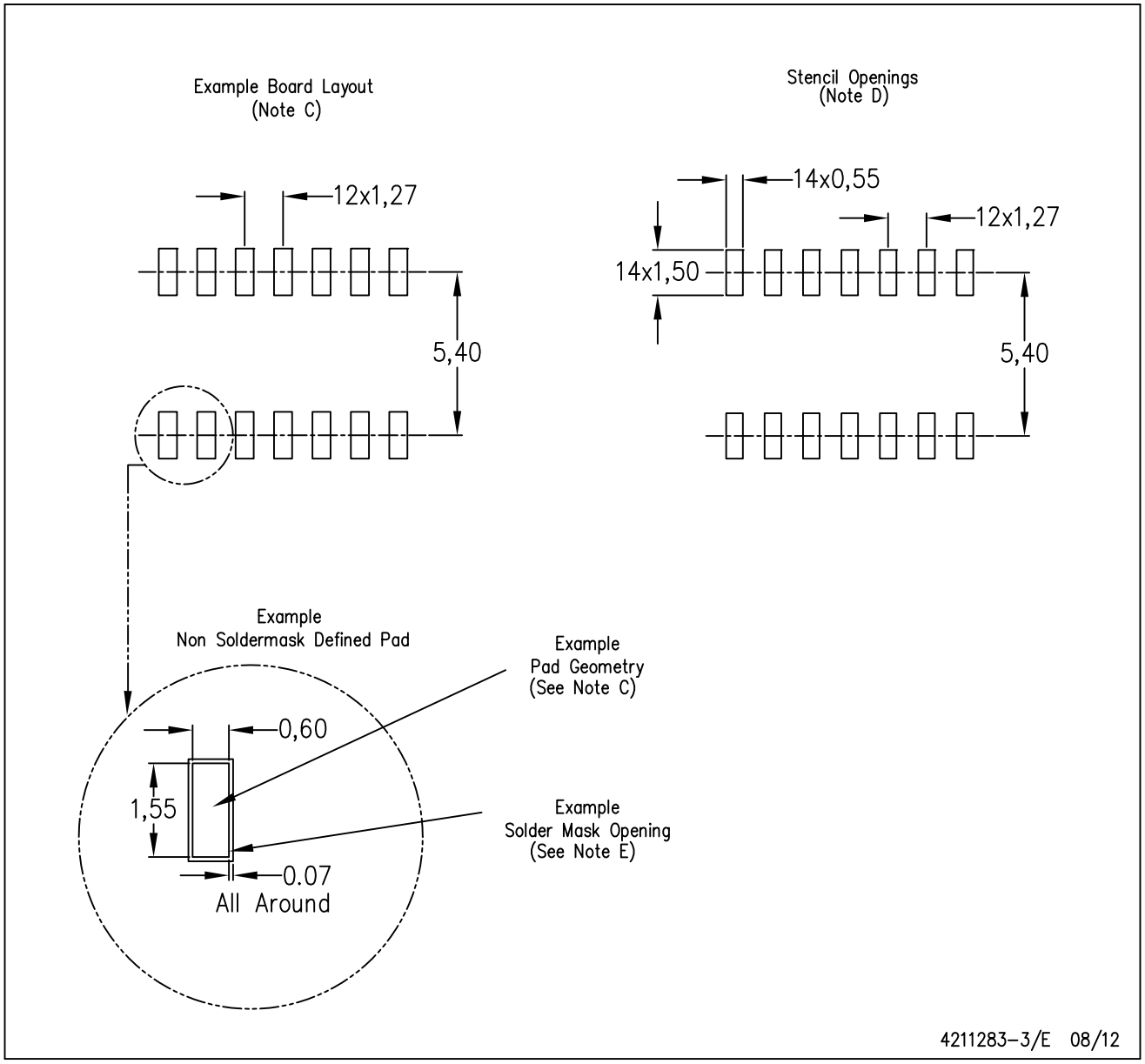
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

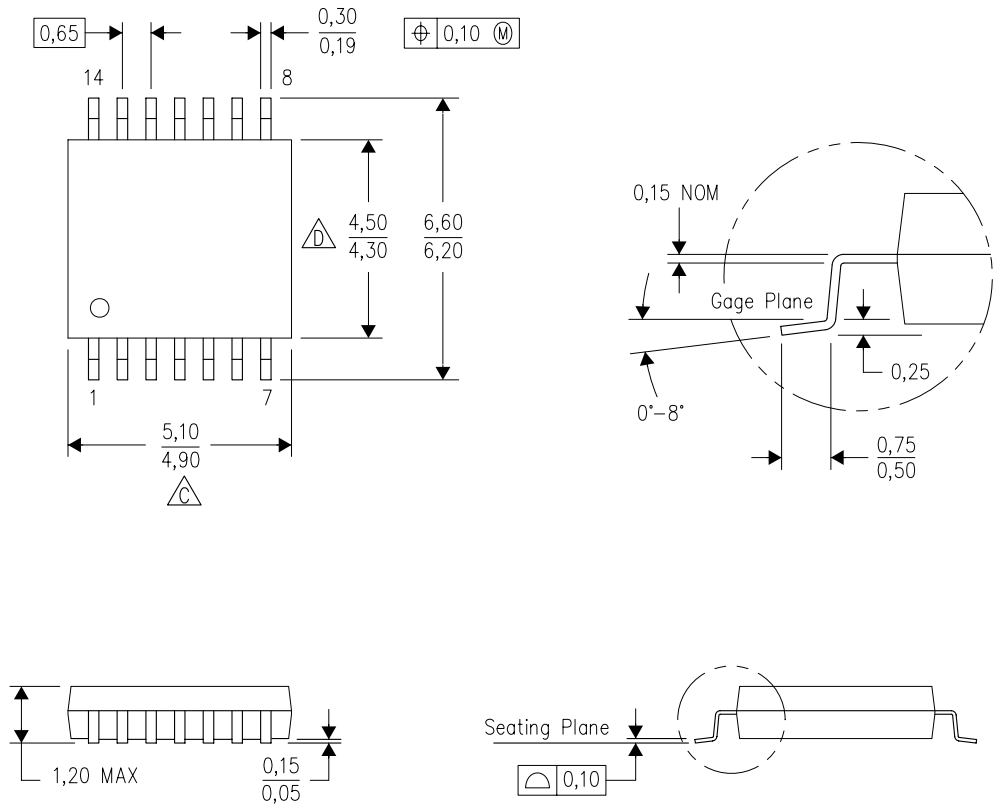
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

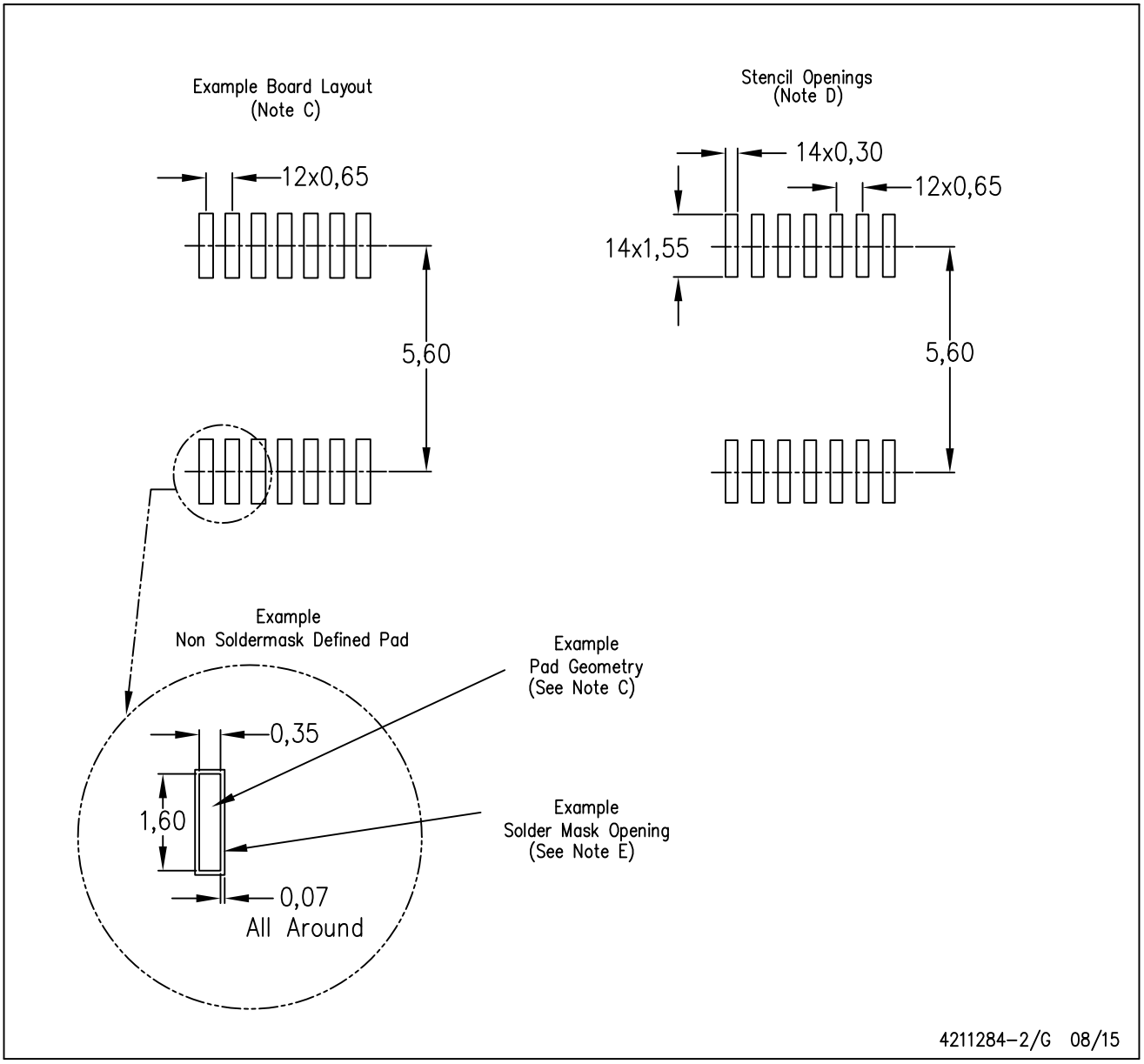
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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