Low-Current, SPI-Compatible Real-Time Clock

General Description

The DS1347 SPI-compatible real-time clock (RTC) contains a real-time clock/calendar and 31 x 8 bits of static random-access memory (SRAM). The real-time clock/calendar provides seconds, minutes, hours, day, date, month, year, and century information. A time/date programmable polled ALARM is included in the device. The end-of-the-month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24hr or 12hr format with an AM/PM indicator. The device operates with a supply voltage of +2V to +5.5V, are available in the ultra-small 8-pin TDFN package, and work over the -40°C to +85°C industrial temperature range.

Applications

Point-of-Sale Equipment

Intelligent Instruments

Fax Machines

Battery-Powered Products

Portable Instruments

Ordering Information

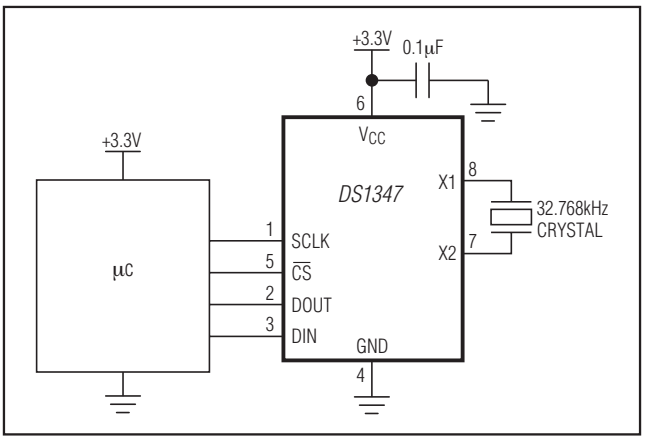
PART	TEMP RANGE	OSC C_L (pF)	PIN-PACKAGE
DS1347T+	-40°C to +85°C	12.5	8 TDFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Benefits and Features

- Completely Manages All Timekeeping Functions
  - RTC Counts Seconds, Minutes, Hours, Day of Week, Date of Month, Month, Year, and Century
  - Leap-Year Compensation
  - 31 x 8-Bit SRAM for Scratchpad Data Storage
  - Programmable Time/Date Polled ALARM Function
  - Uses Standard 32.768kHz Watch Crystal
- Low-Power Operation Extends Battery Life
  - Low Timekeeping Current (400nA at 2V)
  - +2V to +5.5V Wide Operating Voltage Range
- Standard Serial Port Interfaces with Most Microcontrollers
  - SPI (Mode 1 or 3) Interface: 4MHz at 5V, 1MHz at 2V
  - Single-Byte or Multiple-Byte (Burst Mode) Data Transfer for Read or Write of Clock Registers or SRAM
- 3mm x 3mm x 0.8mm, 8-Pin TDFN Package Minimizes Required Space
  - No External Crystal Bias Resistors or Capacitors Required

Typical Operating Circuit



maxim integrated™

Absolute Maximum Ratings

V_{CC} to GND .....-0.3V to +6V
All Other Pins to GND .....-0.3V to (V_{CC} + 0.3V)
Current into Any Pin.....±20mA
Rate of Rise, V_{CC} 100V/µs
Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 24.4mW/°C above +70°C).....1.375mW
Junction Temperature .....+150°C
Storage Temperature Range..... -55°C to +125°C
ESD Protection (All Pins, Human Body Model).....±2000V
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{CC} = +2.0V to +5.5V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		2		5.5	V
Active Supply Current (Note 2)	I_{CC}	V_{CC} = +2V			0.1	mA
		V_{CC} = +5V			0.25	
Timekeeping Supply Current (Note 3)	I_{TK}	V_{CC} = +2V		0.35	0.7	µA
		V_{CC} = +3.6V		0.35	0.7	
		V_{CC} = +5V		0.4	0.8	
SPI DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$)						
Input High Voltage	V_{IH}	V_{CC} = +2V	1.4			V
		V_{CC} = +5V	2.2			
Input Low Voltage	V_{IL}	V_{CC} = +2V			0.6	V
		V_{CC} = +5V			0.8	
Input Leakage Current	I_{IL}	V_{IN} = 0 to V_{CC}	-0.1		+0.1	µA
Input Capacitance	C_{IN}	(Note 4)		10		pF
SPI DIGITAL OUTPUT (DOUT)						
Output Leakage Current	I_O	$\overline{CS}$ = V_{IH}	-0.1		+0.1	µA
Output Capacitance	C_{OUT}	(Note 4)		15		pF
Output Low Voltage	V_{OL}	V_{CC} = +2V, I_{SINK} = 1.5mA			0.4	V
		V_{CC} = +5V, I_{SINK} = 4mA			0.4	
Output High Voltage	V_{OH}	V_{CC} = +2V, I_{SOURCE} = -0.4mA	1.8			V
		V_{CC} = +5V, I_{SOURCE} = -1mA	4.5			

AC Electrical Characteristics

(V_{CC} = +2.0V to +5.5V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Figure 5, Notes 1, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI SERIAL TIMING						
Input Rise Time	t_{rIN}	DIN, SCLK, $\overline{CS}$		5		ns
Input Fall Time	t_{fIN}	DIN, SCLK, $\overline{CS}$		5		ns
Output Rise Time	t_{rOUT}	DOUT, C_{LOAD} = 100pF		10		ns
Output Fall Time	t_{fOUT}	DOUT, C_{LOAD} = 100pF		10		ns
SCLK Period	t_{CP}	V_{CC} = +2V	1000			ns
		V_{CC} = +5V	238			
SCLK High Time	t_{CH}		100			ns
SCLK Low Time	t_{CL}		100			ns
SCLK Fall to DOUT Valid	t_{DO}	V_{CC} = +2V, C_{LOAD} = 100pF			300	ns
		V_{CC} = +5V, C_{LOAD} = 100pF			100	
DIN to SCLK Setup Time	t_{DS}		100			ns
DIN to SCLK Hold Time	t_{DH}		20			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}	V_{CC} = +2V	200			ns
		V_{CC} = +5V	50			
$\overline{CS}$ High Pulse Width	t_{CSW}		200			ns
$\overline{CS}$ High to DOUT High Impedance	t_{CSZ}				100	ns
$\overline{CS}$ to SCLK Setup Time	t_{CSS}		100			ns

Note 1: All parameters are 100% tested at T_A = +25°C. Limits over temperature are guaranteed by design and characterization and not production tested.
Note 2: I_{CC} is specified with DOUT open, $\overline{CS}$ = DIN = GND, SCLK = 4MHz at V_{CC} = +5V; SCLK = 1MHz at V_{CC} = +2.0V.
Note 3: Timekeeping current is specified with $\overline{CS}$ = V_{CC}, SCLK = DIN = GND, DOSF = 0, EGFIL = 1.
Note 4: Guaranteed by design and not 100% production tested.
Note 5: All values referred to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

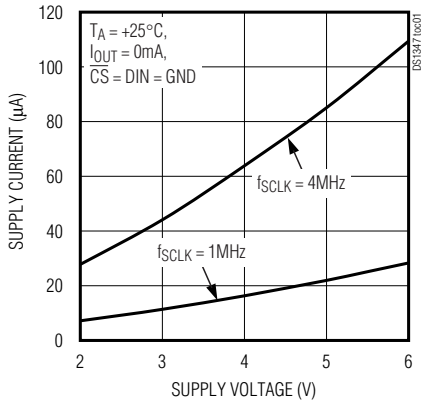
Crystal Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O			32.768		kHz
Series Resistance	ESR				100	kΩ
Load Capacitance	C_L			12.5		pF

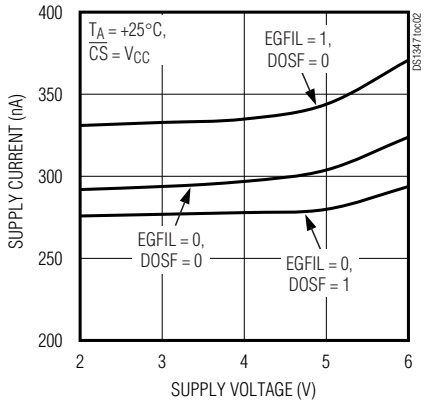
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

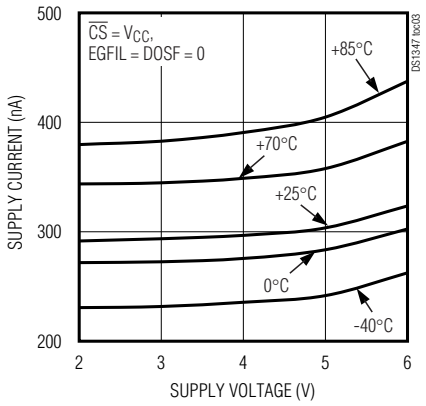
SUPPLY CURRENT vs. SUPPLY VOLTAGE



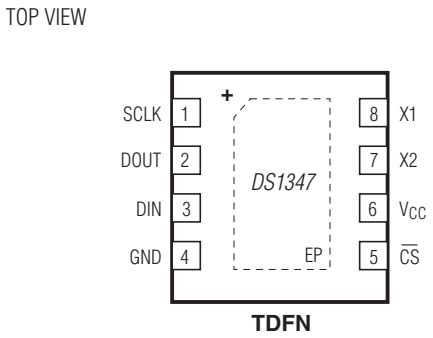
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



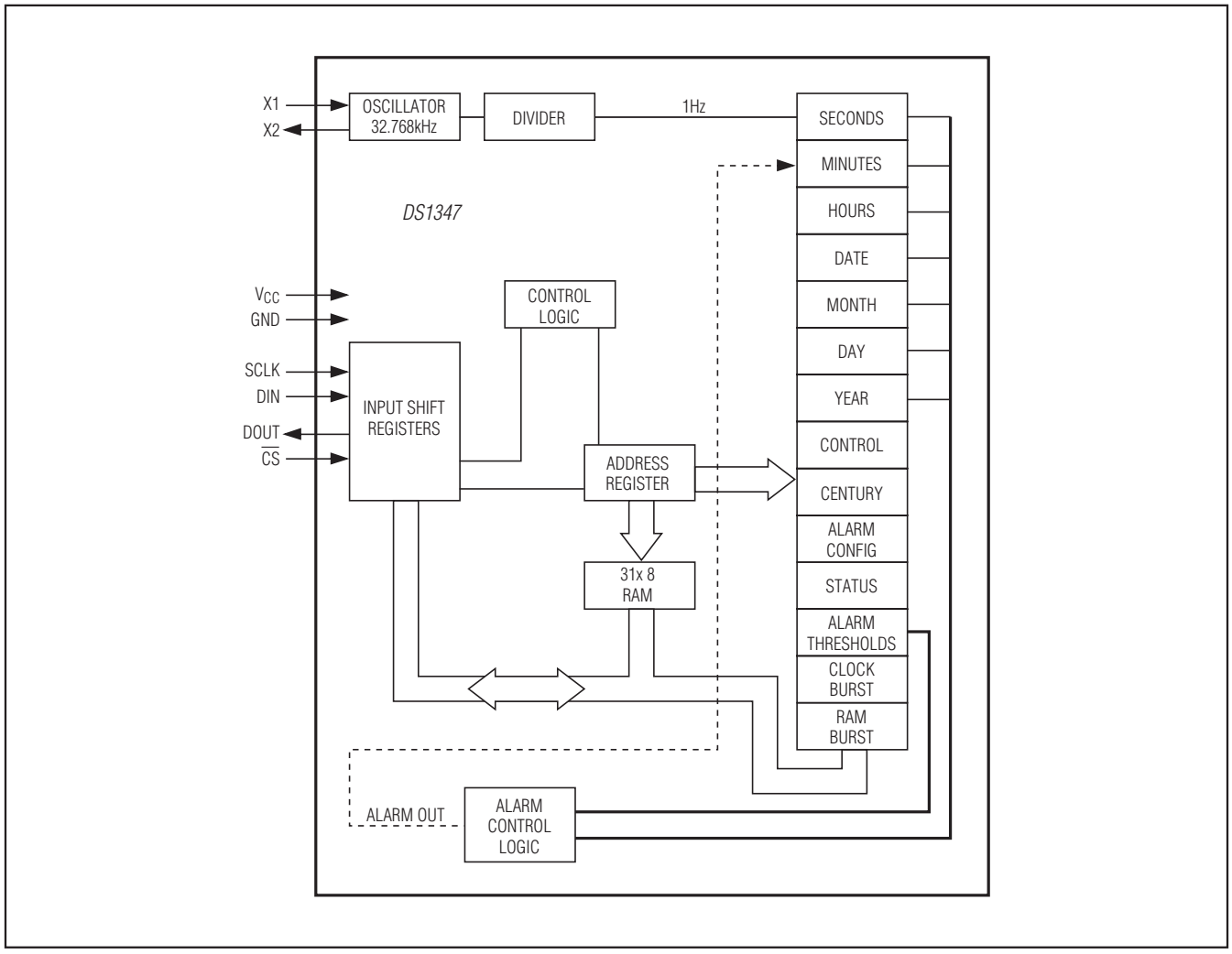
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	SCLK	Serial-Clock Input. SCLK is used to synchronize data movement on the serial interface for either 3-wire or SPI communications.
2	DOUT	Serial-Data Output. When SPI communication is enabled, the DOUT pin is the serial-data output for the SPI bus.
3	DIN	Serial-Data Input. When SPI communication is enabled, the DIN pin is the serial-data input for the SPI bus.
4	GND	Ground
5	$\overline{CS}$	Active-Low Chip Select. The chip-enable signal must be asserted low during a read or a write for SPI communications.
6	V_{CC}	Power-Supply Input
7	X2	Connections for Standard 32.768kHz Quartz Crystal (see the *Crystal Characteristics* table).
8	X1	
—	EP	Exposed Pad. Connect to GND or leave unconnected.

Functional Diagram



Detailed Description

The DS1347 is a real-time clock/calendar with an SPI-compatible interface and 31 x 8 bits of SRAM. It provides seconds, minutes, hours, day of the week, date of the month, month, and year information, held in seven 8-bit timekeeping registers (see the *Functional Diagram*). An on-chip 32.768kHz oscillator circuit requires only a single external crystal to operate. Table 1 shows the device's register addresses and definitions. Time and calendar data are stored in the registers in binary-coded decimal (BCD) format. A polled alarm function is included for scheduled timing of user-defined times or intervals.

Table 1. Register Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
01h	0	10 SECONDS			SECONDS				Seconds	00–59
03h	ALM OUT	10 MINUTES			MINUTES				Minutes	00–59
05h	12/$\overline{24}$	0	$\overline{AM}$/PM 20 HR	10 HR	HOUR				Hours	1–12+$\overline{AM}$/PM 00–23
07h	0	0	10 DATE		DATE				Date	01–31
09h	0	0	0	10 MO	MONTH				Month	01–12
0Bh	0	0	0	0	0	DAY			Day	1–7
0Dh	10 YEAR				YEAR				Year	00–99
0Fh	WP	0	0	0	0	0	0	ID	Control	00h or 81h
13h	1000 YEAR				100 YEAR				Century	00–99
15h	0	YEAR	DAY	MONTH	DATE	HOUR	MINUTE	SECOND	Alarm Configuration	00h–7Fh
17h	$\overline{EOSC}$	DOSF	EGFIL	0	0	OSF	1	1	Status	03h–E7h
19h	0	10 SECONDS			SECONDS				Alarm Seconds	00–59
1Bh	0	10 MINUTES			MINUTES				Alarm Minutes	00–59
1Dh	12/$\overline{24}$	0	$\overline{AM}$/PM 20 HR	10 HR	HOURS				Alarm Hours	1–12 + $\overline{AM}$/PM 00–23
1Fh	0	0	10 DATE		DATE				Alarm Date	1–31
21h	0	0	0	10 MO	MONTH				Alarm Month	1–12
23h	0	0	0	0	0	DAY			Alarm Day	1–7
25h	10 YEAR				YEAR				Alarm Year	00–99
3Fh	See the *Data Input (Burst Write)* section.								Clock Burst	—
41h	X	X	X	X	X	X	X	X	RAM 0	00h–FFh
43h	X	X	X	X	X	X	X	X	RAM 1	00h–FFh
45h	X	X	X	X	X	X	X	X	RAM 2	00h–FFh
47h	X	X	X	X	X	X	X	X	RAM 3	00h–FFh
49h	X	X	X	X	X	X	X	X	RAM 4	00h–FFh
4Bh	X	X	X	X	X	X	X	X	RAM 5	00h–FFh
4Dh	X	X	X	X	X	X	X	X	RAM 6	00h–FFh
4Fh	X	X	X	X	X	X	X	X	RAM 7	00h–FFh
51h	X	X	X	X	X	X	X	X	RAM 8	00h–FFh
53h	X	X	X	X	X	X	X	X	RAM 9	00h–FFh
55h	X	X	X	X	X	X	X	X	RAM 10	00h–FFh

Table 1. Register Map (continued)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
57h	X	X	X	X	X	X	X	X	RAM 11	00h–FFh
59h	X	X	X	X	X	X	X	X	RAM 12	00h–FFh
5Bh	X	X	X	X	X	X	X	X	RAM 13	00h–FFh
5Dh	X	X	X	X	X	X	X	X	RAM 14	00h–FFh
5Fh	X	X	X	X	X	X	X	X	RAM 15	00h–FFh
61h	X	X	X	X	X	X	X	X	RAM 16	00h–FFh
63h	X	X	X	X	X	X	X	X	RAM 17	00h–FFh
65h	X	X	X	X	X	X	X	X	RAM 18	00h–FFh
67h	X	X	X	X	X	X	X	X	RAM 19	00h–FFh
69h	X	X	X	X	X	X	X	X	RAM 20	00h–FFh
6Bh	X	X	X	X	X	X	X	X	RAM 21	00h–FFh
6Dh	X	X	X	X	X	X	X	X	RAM 22	00h–FFh
6Fh	X	X	X	X	X	X	X	X	RAM 23	00h–FFh
71h	X	X	X	X	X	X	X	X	RAM 24	00h–FFh
73h	X	X	X	X	X	X	X	X	RAM 25	00h–FFh
75h	X	X	X	X	X	X	X	X	RAM 26	00h–FFh
77h	X	X	X	X	X	X	X	X	RAM 27	00h–FFh
79h	X	X	X	X	X	X	X	X	RAM 28	00h–FFh
7Bh	X	X	X	X	X	X	X	X	RAM 29	00h–FFh
7Dh	X	X	X	X	X	X	X	X	RAM 30	00h–FFh
7Fh	See the *Data Input (Burst Write)* section.								RAM Burst	—

0 = Reads as logic 0, 1 = Reads as logic 1, X = Don't care.

Command and Control

Address/Command Byte

Each data transfer into or out of the device is initiated by an address/command byte. The address/command byte specifies which registers are to be accessed, and if the access is a read or a write. Table 1 shows the address/command bytes and their associated registers, and lists the hex codes for all read and write operations. The address/command bytes are input MSB (bit 7) first. Bit 7 specifies a write (logic 0) or read (logic 1). Bit 6 specifies register data (logic 0) or RAM data (logic 1). Bits 5–1 specify the designated register to be written or read. The LSB (bit 0) must be logic 1. If the LSB is a zero, writes to the device are disabled.

Clock Burst Mode

Sending the clock burst address/command (3Fh) specifies burst-mode operation. In this mode, multiple bytes are read or written after a single address/command. The first seven clock/calendar registers (Seconds, Minutes, Hours, Date, Month, Day, and Year) and the Control register are consecutively read or written, starting with the MSB of the Seconds register. When writing to the clock registers in burst mode, all seven clock/calendar registers and the Control register must be written in order for the data to be transferred. See the *Example: Setting the Clock with a Burst Write* section.

RAM Burst Mode

Sending the RAM burst address/command (7Fh) specifies burst-mode operation. In this mode, the 31 RAM locations can be consecutively read or written, starting at 41h. When writing to RAM in burst mode, it is not necessary to write all 31 bytes for the data to transfer; each complete byte written is transferred to RAM. When reading from RAM, data is output until all 31 bytes have been read, or until $\overline{CS}$ is driven high.

Setting the Clock

Writing to the Timekeeping Registers

The time and date are set by writing to the timekeeping registers (Seconds, Minutes, Hours, Date, Month, Day, Year, and Century). During a write operation, an input buffer accepts the new time data while the timekeeping registers continue to increment normally, based on the crystal counter. The buffer also keeps the timekeeping registers from changing as the result of an incomplete write operation, and collision-detection circuitry ensures that a time write does not occur coincident with a Seconds register increment. The updated time is loaded into the timekeeping registers after the rising edge of $\overline{CS}$, at the end of the SPI write operation. An incomplete write operation aborts the update procedure, and the contents of the input buffer are discarded. The timekeeping registers reflect the new time beginning with the first Seconds register increment after the rising edge of $\overline{CS}$.

Although both single writes and burst writes are possible, the best way to write to the timekeeping registers is with a burst write. With a burst write, the main timekeeping registers (Seconds, Minutes, Hours, Date, Month, Day, Year) and the Control register are written sequentially following the address/command byte. They must be written as a group of eight registers, with 8 bits each, for proper execution of the burst write function. All seven timekeeping registers are simultaneously loaded into the clock counters by the rising edge of $\overline{CS}$, at the end of the SPI write operation.

If single write operations are used to enter data into the timekeeping registers, error checking is required. If not writing to the Seconds register, begin by reading the Seconds register and save it as initial-seconds. Then write to the required timekeeping registers, and finally read the Seconds register again (final-seconds). Check to see that final-seconds is equal to initial-seconds. If not, repeat the write process. If writing to the Seconds register, update the Seconds register first, and then read it back and store its value (initial-seconds). Update the remaining timekeeping registers and then read the Seconds register again (final-seconds). Check to see that final-seconds is equal to initial-seconds. If not, repeat the write process.

AM/PM and 12Hr/24Hr Mode

Bit 7 of the Hours register selects 12hr or 24hr mode. When high, 12hr mode is selected. In 12hr mode, bit 5 is the $\overline{AM}$/PM bit, logic-high for PM. In 24hr mode, bit 5 is the 20hr bit, logic-high for hours 20 through 23.

Write-Protect Bit

Bit 7 of the Control register is the write-protect bit. When high, the write-protect bit prevents write operations to all registers except itself. After initial settings are written to the timekeeping registers, set the write-protect bit to logic 1 to prevent erroneous data from entering the registers during power glitches or interrupted serial transfers. The lower 7 bits (bits 0–6) are unusable, and always read zero. Any data written to bits 0–6 are ignored. Bit 7 must be set to zero before a single write to the clock, before a write to RAM, or during a burst write to the clock.

Example: Setting the Clock with a Burst Write

To set the clock to 10:11:31PM, Thursday July 4th, 2002, with a burst write operation, write 3Fh as the address/command byte, followed by 8 bytes, 31h, 11h, B0h, 04h, 07h, 05h, 02h, and 00h (Figure 2). 3Fh is the clock burst write address/command. The first data byte, 31h, sets the Seconds register to 31. The second data byte, 11h, sets the Minutes register to 11. The third data byte, B0h, sets the Hours register to 12hr mode, and 10PM. The fourth data byte, 04h, sets the Date register (day of the month) to the 4th. The fifth data byte, 07h, sets the Month register to July. The sixth data byte, 05h, sets the Day register (day of the week) to Thursday. The seventh data byte, 02h, sets the Year register to 02. The eighth data byte, 00h, clears the write-protect bit of the Control register to allow writing to the device. The Century register is not accessed with a burst write and therefore must be written to separately to set the century to 20. Note the Century register corresponds to the thousand and hundred digits of the current year and defaults to 19.

Reading the Clock

Reading the Timekeeping Registers

The main timekeeping registers (Seconds, Minutes, Hours, Date, Month, Day, Year) can be read with either single reads or a burst read. In the device, a latch buffers each clock counter's data. Clock counter data is latched by the SPI read command (on the falling edge of SCLK, after the address/command byte has been sent by the master to read a timekeeping register). Collision-detection circuitry ensures that this does not happen coincident with a Seconds counter increment to ensure accurate time data is read. The clock counters continue to count and keep accurate time during the read operation.

The simplest way to read the timekeeping registers is to use a burst read. In a burst read, the main timekeeping registers (Seconds, Minutes, Hours, Date, Month, Day, Year), and the Control register are read sequentially, in the order listed with the Seconds register first. They are read out as a group of eight registers, with 8 bits each. All timekeeping registers (except Century) are latched upon the receipt of the burst read command. The worst-case error between the "actual" time and the "read" time is 1s for a normal data transfer.

The timekeeping registers can also be read using single reads. If single reads are used, it is necessary to do some error checking on the receiving end, because it is possible that the clock counters could change during the read operations, and report inaccurate time data. The potential for error is when the Seconds register increments before all the registers are read. For example, suppose a carry of 13:59:59 to 14:00:00 occurs during single read operations. The net data read could be 14:59:59, which is erroneous. To prevent errors from occurring with single read operations, read the Seconds register first (initial-seconds) and store this value for future comparison. After the remaining timekeeping registers have been read, reread the Seconds register (final-seconds). Check that the final-seconds value equals the initial-seconds value. If not, repeat the entire single read process. Using single reads at a 100kHz serial speed, it takes under 2.5ms to read all seven of the timekeeping registers, including two reads of the Seconds register.

Example: Reading the Clock with a Burst Read

To read the time with a burst read, send BFh as the Address/Command byte. Then clock out 8 bytes, Seconds, Minutes, Hours, Date of the month, Month, Day of the week, Year, and finally the Control byte. All data is output MSB first. Decode the required information based on the register definitions listed in Table 1.

Using the Alarm

A polled alarm function is available by reading the ALM OUT bit. The ALM OUT bit is D7 of the Minutes timekeeping register. A logic 1 in ALM OUT indicates the Alarm function is triggered. There are eight registers associated with the alarm function—seven programmable alarm threshold registers and one programmable Alarm Configuration register. The Alarm Configuration register determines which alarm threshold registers are compared to the timekeeping registers, and the ALM OUT bit sets if the compared registers are equal. Table 1 shows the function of each bit of the Alarm Configuration register. Placing a logic 1 in any given bit of the Alarm Configuration register enables the respective alarm function. For example, if the Alarm Configuration register is set to 0000 0011, ALM OUT is set when both the minutes and seconds indicated in the alarm threshold registers match the respective timekeeping registers. Once set, ALM OUT stays high until it is cleared by reading or writing to the Alarm Configuration register, or by reading or writing to any of the alarm threshold registers. The Alarm Configuration register is located at address 15h, and is initialized to 00h on the first application of power.

Using the On-Board RAM

The static RAM is 31 x 8 bits addressed consecutively in the RAM Address/Command space. Table 1 details the specific hex address/commands for reads and writes to each of the 31 locations of RAM. The contents of the RAM are static and remain valid for V_{CC} down to 2V. All RAM data is lost if power is cycled. The write-protect bit (WP in the Control register), when high, disallows any writes to RAM. The RAM's power-on state is undefined.

Control Register (0Fh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WP	0	0	0	0	0	0	ID
0	0	0	0	0	0	0	0

BIT 7	**WP:** Write-Protect RAM. If the WP bit is logic one, writing to the 31 bytes of RAM is inhibited. This bit is cleared (0) when power is first applied.
BIT 0	**ID:** Device Identification Bit. The content of this bit does not alter the component functionality. This bit is cleared (0) when power is first applied.

Alarm Configuration Register (15h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	YEAR	DAY	MONTH	DATE	HOUR	MINUTE	SECOND
0	0	0	0	0	0	0	0

Status Register (17h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{\text{EOSC}}$	DOSF	EGFIL	0	0	OSF	0	0
0	0	0	0	0	1	1	1

BIT 7	**$\overline{\text{EOSC}}$:** Enable Oscillator. When the $\overline{\text{EOSC}}$ bit is logic 0, the oscillator is enabled. When this bit is logic 1, the oscillator is disabled. This bit is cleared (0) when power is first applied.
BIT 6	**DOSF:** Disable Oscillator Stop Flag. When the DOSF bit is set to 1, sensing of the oscillator conditions that would set the OSF bit is disabled. OSF remains at 0 regardless of what happens to the oscillator. This bit is cleared (0) on the initial application of power.
BIT 5	**EGFIL:** Enable Glitch Filter. When the EGFIL bit is 1, the 5µs glitch filter at the output of crystal oscillator is enabled. The glitch filter is disabled when this bit is 0. This bit is cleared (0) on the initial application of power.
BIT 2	**OSF:** Oscillator Stop Flag. If the OSF bit is 1, the oscillator either has stopped or was stopped for some period and could be used to judge the validity of the clock and calendar data. This bit is edge triggered and is set to 1 when the internal circuitry senses the oscillator has transitioned from a normal run state to a stop condition. This bit remains at logic 1 until written to logic 0. Attempting to write OSF to 1 leaves the value unchanged. The following are examples of conditions that can cause the OSF bit to be set: 1) The first time power is applied. 2) The voltage present on V_{CC} is insufficient to support oscillation. 3) The $\overline{\text{EOSC}}$ bit is set to logic 1. 4) External influences on the crystal (i.e., noise, leakage, etc.).

Alarm Seconds Register (19h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	10 SECONDS			SECONDS			
0	1	1	1	1	1	1	1

Alarm Minutes Register (1Bh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	10 MINUTES			MINUTES			
0	1	1	1	1	1	1	1

Alarm Hours Register (1Dh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
12/$\overline{24}$	0	$\overline{AM}$/PM 20 HR	10 HR	HOURS			
1	0	1	1	1	1	1	1

Alarm Date Register (1Fh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	10 DATE		DATE			
0	0	1	1	1	1	1	1

Alarm Month Register (21h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	10 MO	MONTH			
0	0	0	1	1	1	1	1

Alarm Day Register (23h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	DAY		
0	0	0	0	0	1	1	1

Alarm Year Register (25h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
10 YEAR				YEAR			
1	1	1	1	1	1	1	1

SPI-Compatible Serial Interface

Interface the device with a microcontroller using a serial, 4-wire, SPI interface. SPI is a synchronous bus for address and data transfer, and is used with Motorola or other microcontrollers that have an SPI port. Four connections are required for the interface: DOUT (serial-data out); DIN (serial-data in); SCLK (serial clock); and $\overline{CS}$ (chip select). In an SPI application, the device acts as a slave device and the microcontroller acts as the master. $\overline{CS}$ is asserted low by the microcontroller to initiate a transfer, and deasserted high to terminate a transfer. DIN transfers input data from the microcontroller to the device. DOUT transfers output data from the device to the microcontroller. A shift clock, SCLK, is used to synchronize data movement between the microcontroller and the device. SCLK, which is generated by the

microcontroller, is active only during address and data transfer to any device on the SPI bus. The inactive clock polarity is usually programmable on the microcontroller side of the SPI interface. In the device, input data is latched on the positive edge, and output data is shifted out on the negative edge. There is one clock cycle for each bit transferred. Address and data bits are transferred in groups of eight.

The SPI protocol allows for one of four combinations of serial clock phase and polarity from the microcontroller, through a 2-bit selection in its SPI Control register. The clock polarity is specified by the CPOL Control bit, which selects active-high or active-low clock, and has no significant effect on the transfer format. The clock phase control bit, CPHA, selects one of two different transfer formats. The clock phase and polarity must be identical for the master and the slave. For the device, set the control bits to CPHA = 1 and CPOL = 1. This configures the system for data out to be launched on the negative edge of SCLK and data in to be sampled on the positive edge. With CPHA equal to 1, $\overline{CS}$ can remain low between successive data byte transfers, allowing burst-mode data transfers to occur.

Address and data bytes are shifted MSB first into DIN of the device, and out of DOUT. Data is shifted out at the negative edge of SCLK, and shifted in or sampled at the positive edge of SCLK. Any transfer requires an address/command byte followed by one or more bytes of data. Data is transferred out of DOUT for a read operation, and into DIN for a write operation. DOUT transmits data only after an address/command byte specifies a read operation; otherwise, it is high impedance.

Data transfer write timing is shown in Figure 1. Data transfer read timing is shown in Figure 2. Detailed read and write timing is shown in Figure 3.

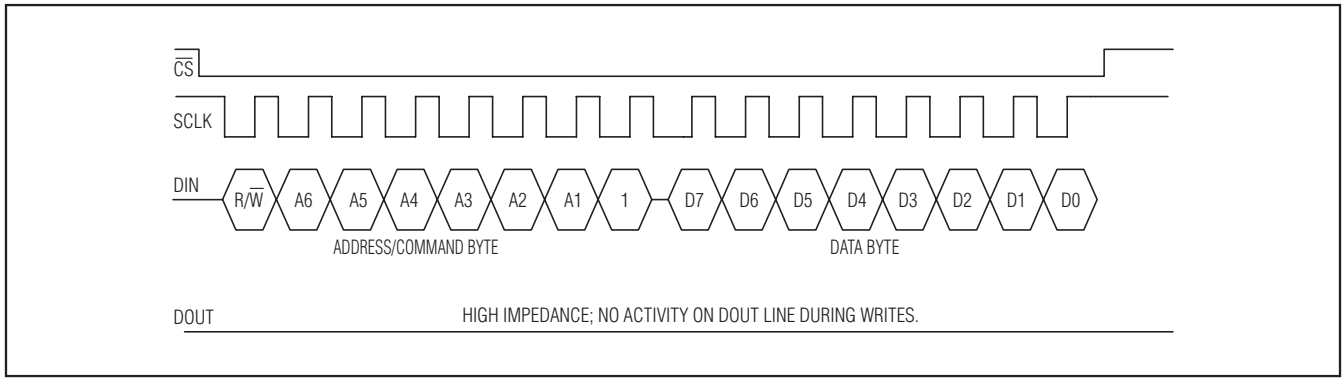


Figure 1a. Single Write

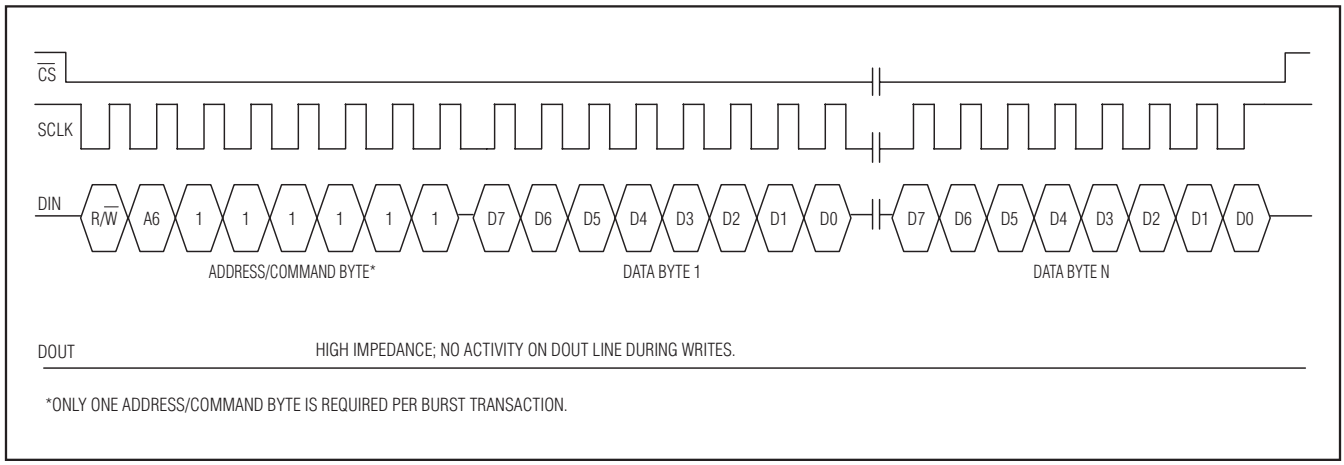


Figure 1b. Burst Write

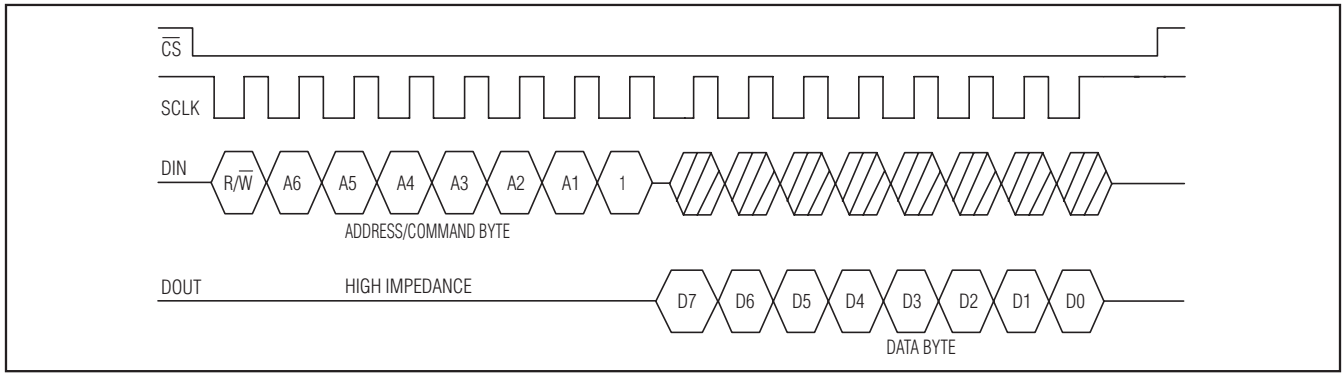


Figure 2a. Single Read

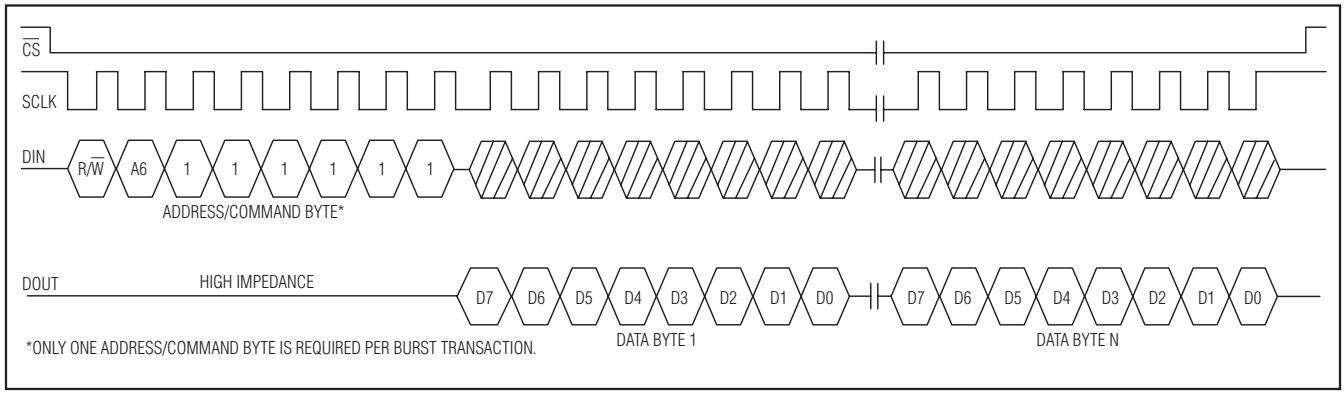


Figure 2b. Burst Read

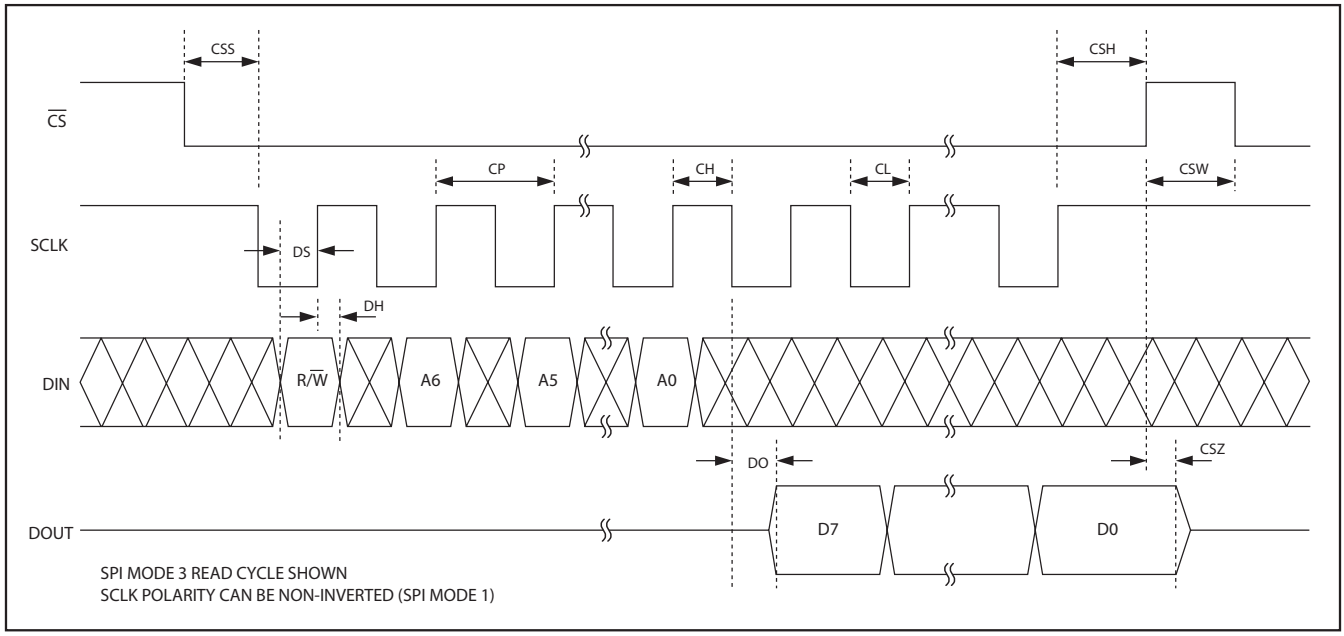


Figure 3. SPI Bus Timing Diagram

Chip Select

$\overline{CS}$ serves two functions. First, $\overline{CS}$ turns on the control logic that allows access to the Shift register for address/command and data transfer. Second, $\overline{CS}$ provides a method of terminating either single-byte or multiple-byte data transfers. All data transfers are initiated by driving $\overline{CS}$ low. If $\overline{CS}$ is high, then DOUT is high impedance.

Serial Clock

A clock cycle on SCLK is a rising edge followed by a falling edge. For data input, data must be valid at DIN before the rising edge of the clock. For data outputs, bits are valid on DOUT after the falling edge of the clock.

Data Input (Single-Byte Write)

Following the eight SCLK cycles that input a single-byte write address/command, data bits are input on the rising edges of the next eight SCLK cycles. Additional SCLK cycles are ignored. Input data MSB first.

Data Input (Burst Write)

Following the eight SCLK cycles that input a burst-write address/command, data bits are input on the rising edges of the following SCLK cycles. The number of clock cycles depends on whether the timekeeping registers or RAM are being written. A clock burst write requires 1 address/command byte, 7 timekeeping data bytes, and 1 control register byte. A burst write to RAM can be terminated after any complete data byte by driving $\overline{CS}$ high. Input data MSB first (Figure 1).

Data Output (Single-Byte Read and Burst Read)

A read from the device is initiated by an address/command Write from the microcontroller (master) to the device (slave). The address/command write portion of the data transfer is clocked into the device on rising clock edges. Following the eighth falling clock edge of SCLK, after t_{DO} (Figure 2) data begins to be output on DOUT of the device. Data bytes are output MSB first. Additional SCLK cycles transmit additional data bits, as long as $\overline{CS}$ remains low. This permits continuous burst-mode read capability.

Applications Information

Oscillator Start Time

The device's oscillator typically takes less than 2s to begin oscillating. To ensure the oscillator is operating correctly, the software should validate proper timekeeping. This is accomplished by reading the Seconds register. Any reading of 1s or more from the POR value of zero seconds is a validation of proper startup.

Power-On Reset

The device contains an integral POR circuit that ensures all registers are reset to a known state on power-up. Upon a POR, the time and date are set to 00:00:00 01/01/1970 (hh:mm:ss DD/MM/YYYY) and the day register is set to 01. Once V_{CC} rises, the POR circuit releases the registers for normal operation.

Power-Supply Considerations

For most applications, a 0.1µF capacitor from V_{CC} to GND provides adequate bypassing for the device. A series resistor can be added to the supply line for operation in extremely harsh or noisy environments.

PCB Considerations

The device uses a very low-current oscillator to minimize supply current. This causes the oscillator pins, X1 and X2, to be relatively high impedance. Exercise care to prevent unwanted noise pickup.

Connect the 32.768kHz crystal directly across X1 and X2 of the device. To eliminate unwanted noise pickup, design the PCB using these guidelines (Figure 4):

1) Place the crystal as close to X1 and X2 as possible and keep the trace lengths short.
2) Place a guard ring around the crystal, X1 and X2 traces (where applicable), and connect the guard ring to GND; keep all signal traces away from beneath the crystal, X1, and X2.
3) Finally, an additional local ground plane can be added under the crystal on an adjacent PCB layer. The plane should be isolated from the regular PCB ground plane, and connected to ground at the IC ground pin.
4) Restrict the plane to be no larger than the perimeter of the guard ring. Do not allow this ground plane to contribute significant capacitance between X1 and X2.

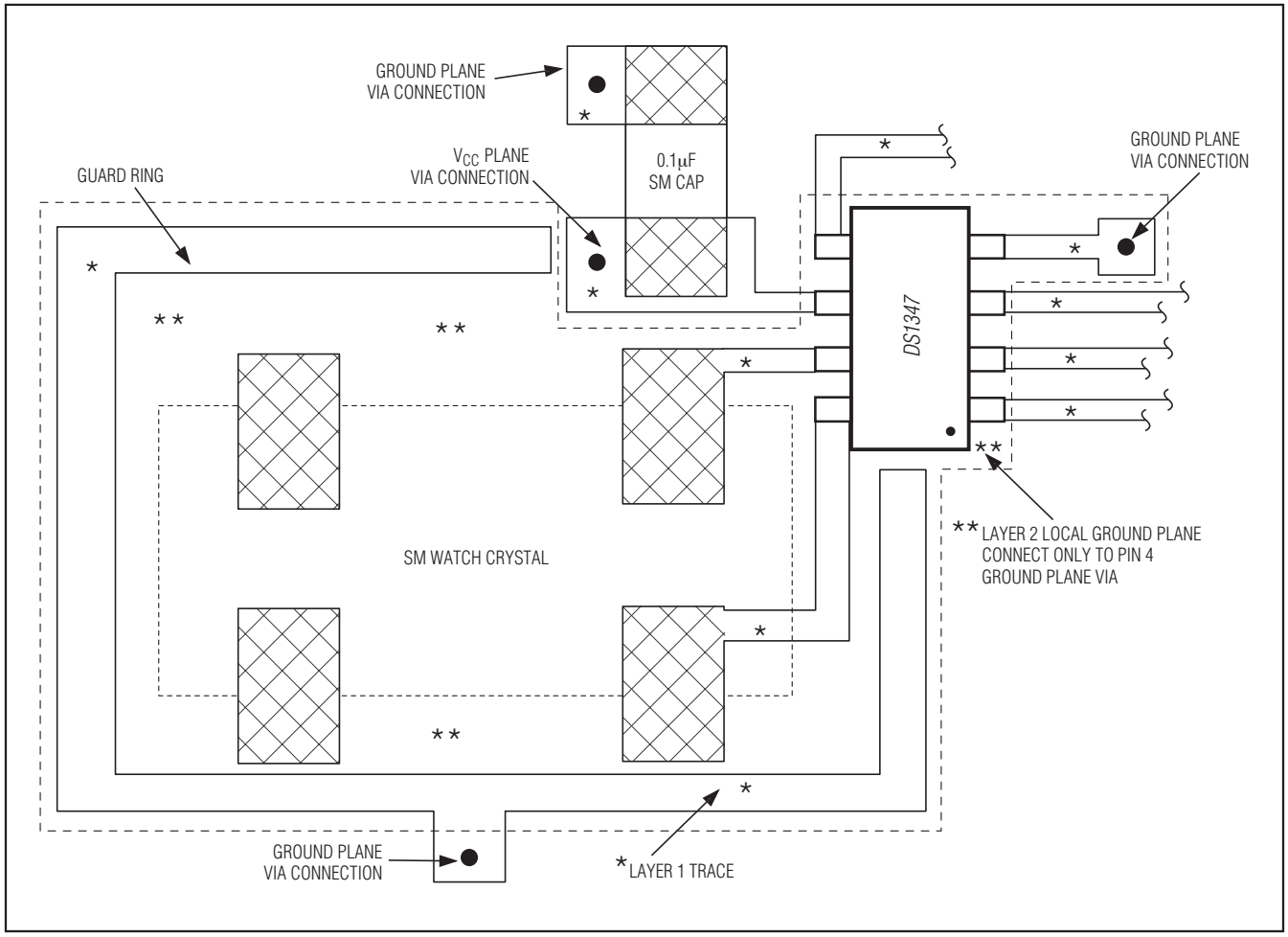


Figure 4. Crystal PCB Layout

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 TDFN-EP	T833+2	21-0137	90-0059

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/11	Initial release	—
1	1/12	Removed all references to the DS1346	All
2	2/12	Removed the external oscillator text from the X1 pin description in the *Pin Description* table	5
3	1/13	Moved *Crystal Characteristics* table below notes; added POR content for clock/calendar registers.	3, 15
4	11/13	Updated $\overline{CS}$ timing in Figures 1a, 1b, 2a, and 2b; replaced Figure 3	13, 14
5	4/15	Revised *Benefits and Features* section	1

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