DRV8886AT 2-A Stepper Motor Driver With Integrated Current Sense and Smart Tune Technology

1 Features

- PWM microstepping stepper motor driver
  - Up to 1/16 microstepping
  - Non-circular and standard ½ step modes
- Integrated current sense functionality
  - No sense resistors required
  - ±6.25% Full-scale current accuracy
- Smart tune adaptive decay technology, slow, and mixed decay options
- 8 to 37-V Operating supply voltage range
- Low $R_{DS(ON)}$: 550 mΩ HS + LS at 24 V, 25°C
- High current capacity
  - 3-A Peak per bridge
  - 2-A Full-scale per bridge
  - 1.4-A rms per bridge
- Dynamic and fixed off-time PWM current regulation
- Simple STEP/DIR interface
- Low-current sleep mode (20 μA)
- Small package and footprint
  - 24 HTSSOP PowerPAD™ package
  - 28 WQFN package
- Protection features
  - VM undervoltage lockout (UVLO)
  - Charge pump undervoltage (CPUV)
  - Overcurrent protection (OCP)
  - Thermal shutdown (TSD)
  - Fault condition indication pin (nFAULT)

2 Applications

- Bipolar stepper motors
- Multi-function printers and scanners
- Laser beam printers
- 3D printers
- Automatic teller and money handling machines
- Video security cameras
- Office automation machines
- Factory automation and robotics

3 Description

The DRV8886AT is a stepper motor driver for industrial and consumer end equipment applications. The device is fully integrated with two N-channel power MOSFET H-bridge drivers, a microstepping indexer, and integrated current sensing. The DRV8886AT is capable of driving up to 2-A full scale or 1.4-A rms output current (24-V and T_A = 25°C, dependent on PCB design).

The DRV8886AT uses an internal current sense architecture to eliminate the need for two external power sense resistors saving PCB area and system cost. The DRV8886AT uses an internal PWM current regulation scheme adjustable between smart tune adaptive decay technology, slow, and mixed decay options. Smart tune adaptive decay technology automatically adjusts for optimal current regulation performance and compensates for motor variation and aging effects.

A simple STEP/DIR interface allows an external controller to manage the direction and step rate of the stepper motor. The device can be configured in different step modes ranging from full-step to 1/16 microstepping. A low-power sleep mode is provided for very low standby quiescent standby current using a dedicated nSLEEP pin.

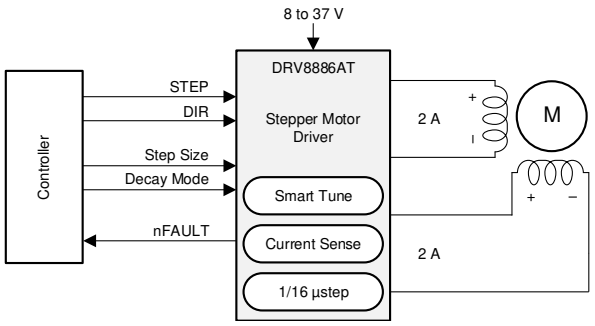
Device protection features are provided for supply undervoltage, charge pump faults, overcurrent, short circuits, and overtemperature. Fault conditions are indicated by the nFAULT pin.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8886AT	HTSSOP (24)	7.80 mm × 4.40 mm
	WQFN (28)	5.50 mm × 3.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 6
6.6 Indexer Timing Requirements ... 8
6.7 Typical Characteristics ... 9
7 Detailed Description ... 11
7.1 Overview ... 11
7.2 Functional Block Diagram ... 12
7.3 Feature Description ... 13
7.4 Device Functional Modes ... 33
8 Application and Implementation ... 34
8.1 Application Information ... 34
8.2 Typical Application ... 34
9 Power Supply Recommendations ... 37
9.1 Bulk Capacitance ... 37
10 Layout ... 38
10.1 Layout Guidelines ... 38
10.2 Layout Example ... 38
11 Device and Documentation Support ... 39
11.1 Documentation Support ... 39
11.2 Receiving Notification of Documentation Updates ... 39
11.3 Community Resources ... 39
11.4 Trademarks ... 39
11.5 Electrostatic Discharge Caution ... 39
11.6 Glossary ... 39
12 Mechanical, Packaging, and Orderable Information ... 39

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2018) to Revision C — **Page**

- Added Various Sources of Error and Application-Specific Error Calculations sections. ... 18

Changes from Revision A (July 2018) to Revision B — **Page**

- Changed device status from Advance Information to Production Data ... 1

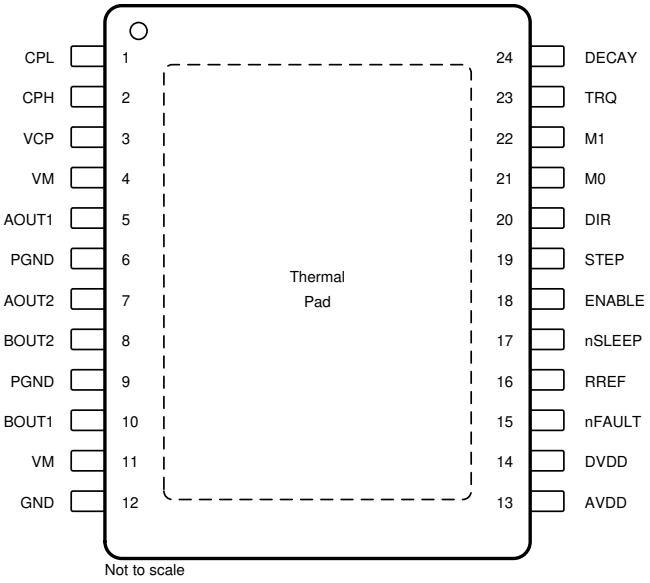
Changes from Original (January 2017) to Revision A — **Page**

- Added the WQFN package option ... 1
- Changed the units of the High-Side and Low-Side $R_{DS(ON)}$ axis labels from mΩ to Ω in the high-side and low-side $R_{DS(ON)}$ over VM and over temperature graphs ... 9

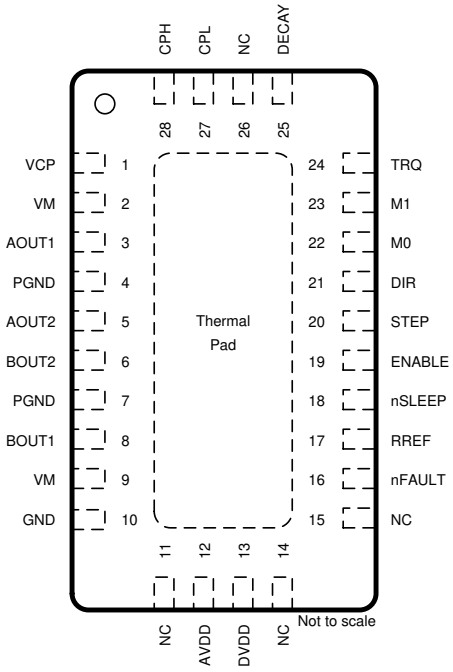
Copyright © 2017–2020, Texas Instruments Incorporated

5 Pin Configuration and Functions

PWP PowerPAD™ Package
24-Pin HTSSOP
Top View



RHR Package
28-Pin WQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	HTSSOP	WQFN		
AOUT1	5	3	O	Winding A output. Connect to stepper motor winding.
AOUT2	7	5		
AVDD	13	12	PWR	Internal regulator. Bypass to GND with a X5R or X7R, 0.47-µF, 6.3-V ceramic capacitor.
BOUT1	10	8	O	Winding B output. Connect to stepper motor winding.
BOUT2	8	6		
CPH	2	28	PWR	Charge pump switching node. Connect a X5R or X7R, 0.022-µF, VM-rated ceramic capacitor from CPH to CPL.
CPL	1	27		
DECAY	24	25	I	Decay-mode setting. Sets the decay mode (see the *Decay Modes* section). Decay mode is latched on device enable.
DIR	20	21	I	Direction input. Logic level sets the direction of stepping; internal pulldown resistor.
DVDD	14	13	PWR	Internal regulator. Bypass to GND with a X5R or X7R, 0.47-µF, 6.3-V ceramic capacitor.
ENABLE	18	19	I	Enable driver input. Logic high to enable device outputs; logic low to disable; internal pulldown resistor.
GND	12	10	PWR	Device ground. Connect to system ground.
M0	21	22	I	Microstepping mode-setting. Sets the step mode; tri-level pins; sets the step mode; internal pulldown resistor.
M1	22	23		
NC	—	11	—	No connect. No internal connection
		14		
		15		
		26		
PGND	6	4	PWR	Power ground. Connect to system ground.
	9	7		
RREF	16	17	I	Current-limit analog input. Connect resistor to ground to set full-scale regulation current.

(1) I = input, O = output, PWR = power, OD = open-drain

Copyright © 2017–2020, Texas Instruments Incorporated

Pin Functions (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	HTSSOP	WQFN		
STEP	19	20	I	Step input. A rising edge causes the indexer to advance one step; internal pulldown resistor.
TRQ	23	24	I	Current-scaling control. Scales the output current; tri-level pin.
VCP	3	1	PWR	Charge pump output. Connect a X5R or X7R, 0.22-µF, 16-V ceramic capacitor to VM.
VM	4	2	PWR	Power supply. Connect to motor supply voltage and bypass to GND with two 0.01-µF ceramic capacitors (one for each pin) plus a bulk capacitor rated for VM.
	11	9		
nFAULT	15	16	OD	Fault indication. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.
nSLEEP	17	18	I	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	40	V
Power supply voltage ramp rate (VM)	0	2	V/µs
Charge pump voltage (VCP, CPH)	–0.3	VM + 7	V
Charge pump negative switching pin (CPL)	–0.3	VM	V
Internal regulator voltage (DVDD)	–0.3	3.8	V
Internal regulator current output (DVDD)	0	1	mA
Internal regulator voltage (AVDD)	–0.3	5.7	V
Control pin voltage (STEP, DIR, ENABLE, nFAULT, M0, M1, DECAY, TRQ, nSLEEP)	–0.3	5.7	V
Open drain output current (nFAULT)	0	10	mA
Current limit input pin voltage (RREF)	–0.3	6.0	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–1.0	VM + 1.0	V
Transient 100 ns phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–3.0	VM + 3.0	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)	0	3	A
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Copyright © 2017–2020, Texas Instruments Incorporated

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Power supply voltage (VM)	8	37	V
V_I	Input voltage (DECAY, DIR, ENABLE, M0, M1, nSLEEP, STEP, TRQ)	0	5.3	V
f_{PWM}	Applied STEP signal (STEP)	0	100 (1)	kHz
I_{DVDD}	External load current (DVDD)	0	1 (2)	mA
I_{FS}	Motor full-scale current (xOUTx)	0	2 (2)	A
I_{rms}	Motor RMS current (xOUTx)	0	1.4 (2)	A
T_A	Operating ambient temperature	–40	125	°C

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load
(2) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC (1)		DRV8886		UNIT
		PWP (HTSSOP)	RHR (WQFN)	
		24 PINS	28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.8	33.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.0	23.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.7	12.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.8	12.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Copyright © 2017–2020, Texas Instruments Incorporated

6.5 Electrical Characteristics

at T_A = -40 to 125°C, V_{VM} = 8 to 37 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD, AVDD)						
VVM	VM operating voltage		8		37	V
I_{VM}	VM operating supply current	ENABLE = 1, nSLEEP = 1, No motor load		5	8	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0; T_A = 25°C			20	µA
		nSLEEP = 0; T_A = 125°C(1)			40	
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode		50	200	µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.85	1.5	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.85	1.5	ms
V_{DVDD}	Internal regulator voltage	0- to 1-mA external load	2.9	3.3	3.6	V
V_{AVDD}	Internal regulator voltage	No external load	4.5	5	5.5	V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage			VM + 5.5		V
LOGIC-LEVEL INPUTS (STEP, DIR, ENABLE, nSLEEP, M1)						
V_{IL}	Input logic-low voltage		0		0.8	V
V_{IH}	Input logic-high voltage		1.6		5.3	V
V_{HYS}	Input logic hysteresis			200		mV
I_{IL}	Input logic-low current	VIN = 0 V	–1		1	µA
I_{IH}	Input logic-high current	VIN = 5 V			100	µA
R_{PD}	Pulldown resistance	To GND		100		kΩ
t_{PD} (1)	Propagation delay	STEP to current change			1.2	µs
TRI-LEVEL INPUT (M0, TRQ)						
V_{IL}	Tri-level input logic low voltage		0		0.65	V
V_{IZ}	Tri-level input Hi-Z voltage		0.95	1.1	1.25	V
V_{IH}	Tri-level input logic high voltage		1.5		5.3	V
I_{IL}	Tri-level input logic low current	VIN = 0 V	–90			µA
I_{IH}	Tri-level input logic high current	VIN = 5 V			155	µA
R_{PD}	Tri-level pulldown resistance	VIN = Hi-Z, to GND		65		kΩ
R_{PU}	Tri-level pullup resistance	VIN = Hi-Z, to DVDD		130		kΩ
QUAD-LEVEL INPUT (DECAY)						
V_{I1}	Quad-level input voltage 1	Can set with 1% 5 kΩ to GND	0		0.14	V
V_{I2}	Quad-level input voltage 2	Can set with 1% 15 kΩ to GND	0.24		0.46	V
V_{I3}	Quad-level input voltage 3	Can set with 1% 44.2 kΩ to GND	0.71		1.24	V
V_{I4}	Quad-level input voltage 4	Can set with 1% 133 kΩ to GND	2.12		5.3	V
I_O	Output current	To GND	17	22	27.25	µA
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic-low voltage	I_O = 1 mA, R_{PULLUP} = 4.7 kΩ			0.5	V
I_{OH}	Output logic-high leakage	V_O = 5 V, R_{PULLUP} = 4.7 kΩ	–1		1	µA

(1) Specified by design and characterization data

Copyright © 2017–2020, Texas Instruments Incorporated

Electrical Characteristics (continued)

at T_A = -40 to 125°C, V_{VM} = 8 to 37 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ON)}$	High-side FET on resistance	VM = 24 V, I = 1.4 A, T_A = 25°C		290	346	mΩ
$R_{DS(ON)}$	Low-side FET on resistance	VM = 24 V, I = 1.4 A, T_A = 25°C		260	320	mΩ
t_{RISE} (1)	Output rise time			100		ns
t_{FALL} (1)	Output fall time			100		ns
t_{DEAD} (1)	Output dead time			200		ns
V_d (1)	Body diode forward voltage	I_{OUT} = 0.5 A		0.7	1	V
PWM CURRENT CONTROL (RREF)						
A_{RREF}	RREF transimpedance gain		28.1	30	31.9	kAΩ
V_{RREF}	RREF voltage	RREF = 18 to 132 kΩ	1.18	1.232	1.28	V
t_{OFF}	PWM off-time			20		µs
C_{RREF}	Equivalent capacitance on RREF				10	pF
t_{BLANK}	PWM blanking time	I_{RREF} = 2.0 A, 63% to 100% current setting		1.5		µs
		I_{RREF} = 2.0 A, 0% to 63% current setting		1		
ΔI_{TRIP}	Current trip accuracy	I_{RREF} = 1.5 A, 10% to 20% current setting, 1% reference resistor	–15%		15%	
		I_{RREF} = 1.5 A, 20% to 63% current setting, 1% reference resistor	–10%		10%	
		I_{RREF} = 1.5 A, 71% to 100% current setting, 1% reference resistor	–6.25%		6.25%	
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO	VM falling, UVLO report	7		7.8	V
		VM rising, UVLO recovery	7.2		8	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		200		mV
V_{CPUV}	Charge pump undervoltage	VCP falling; CPUV report		VM + 2		V
I_{OCP}	Overcurrent protection trip level	Current through any FET	3			A
t_{OCP} (1)	Overcurrent deglitch time		1.3	1.9	2.8	µs
t_{RETRY}	Overcurrent retry time		1		1.6	ms
T_{TSD} (1)	Thermal shutdown temperature	Die temperature T_J	150			°C
T_{HYS} (1)	Thermal shutdown hysteresis	Die temperature T_J		20		°C

Copyright © 2017–2020, Texas Instruments Incorporated

6.6 Indexer Timing Requirements

at T_A = -40 to 125°C, V_{VM} = 8 to 37 V (unless otherwise noted)

NO.			MIN	MAX	UNIT
1	f_{STEP} (1)	Step frequency		500	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	970		ns
3	$t_{WL(STEP)}$	Pulse duration, STEP low	970		ns
4	$t_{SU(DIR, Mx)}$	Setup time, DIR or USMx to STEP rising	200		ns
5	$t_{H(DIR, Mx)}$	Hold time, DIR or USMx to STEP rising	200		ns

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load.

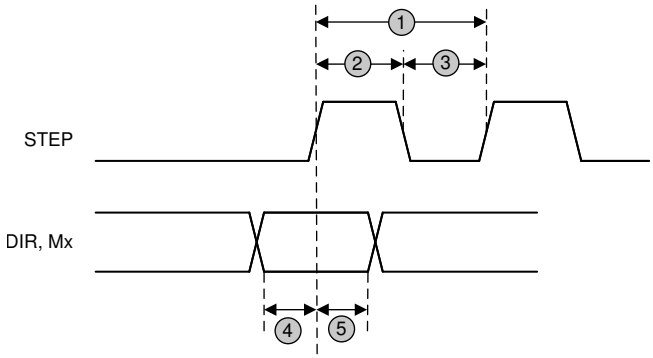


Figure 1. Timing Diagram

Copyright © 2017–2020, Texas Instruments Incorporated

6.7 Typical Characteristics

Over recommended operating conditions (unless otherwise noted)

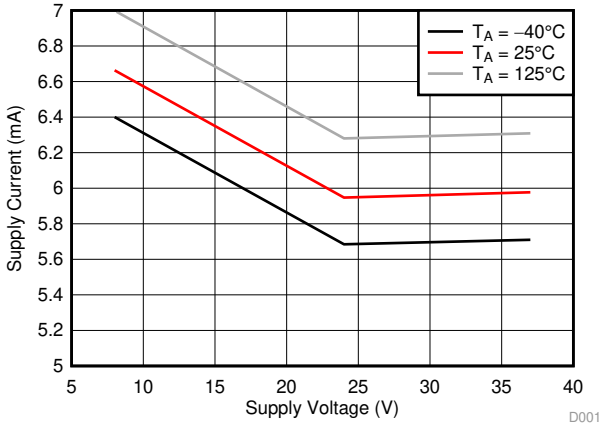


Figure 2. Supply Current over VM

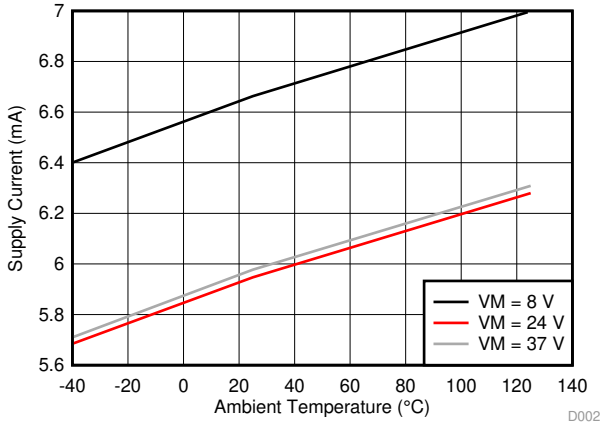


Figure 3. Supply Current over Temperature

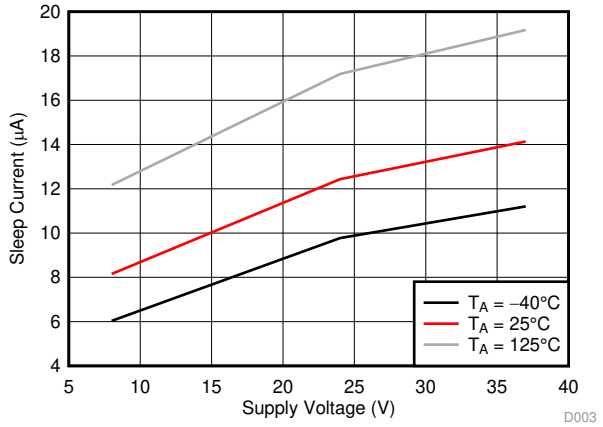


Figure 4. Sleep Current over VM

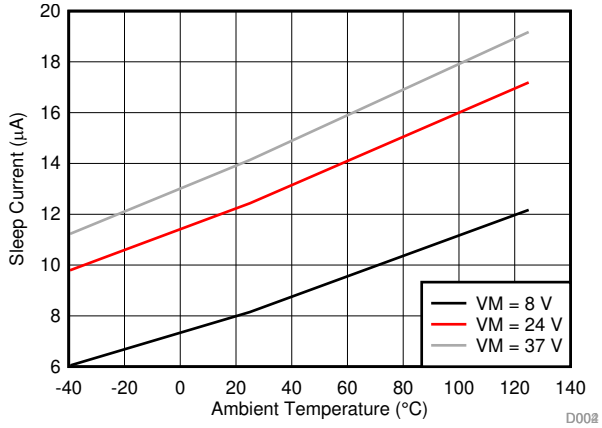


Figure 5. Sleep Current over Temperature

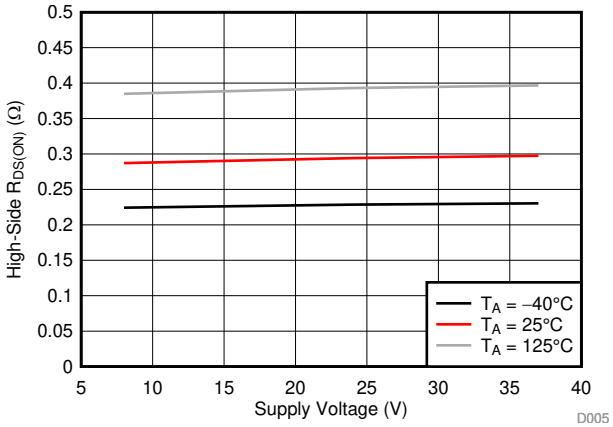


Figure 6. High-Side $R_{DS(ON)}$ over VM

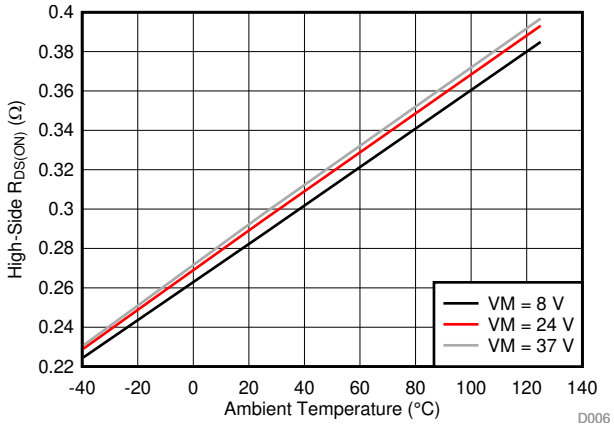


Figure 7. High-Side $R_{DS(ON)}$ over Temperature

Copyright © 2017–2020, Texas Instruments Incorporated

Typical Characteristics (continued)

Over recommended operating conditions (unless otherwise noted)

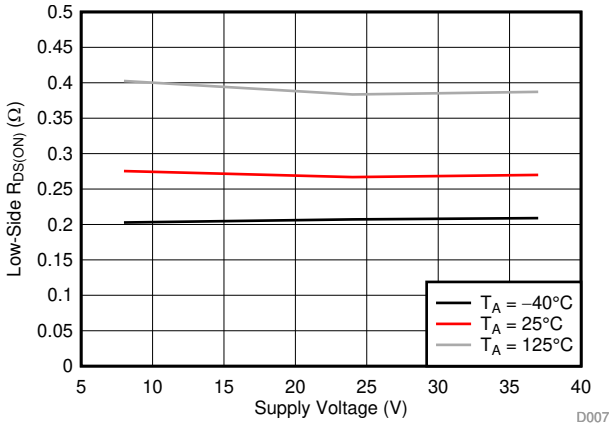


Figure 8. Low-Side $R_{DS(ON)}$ over VM

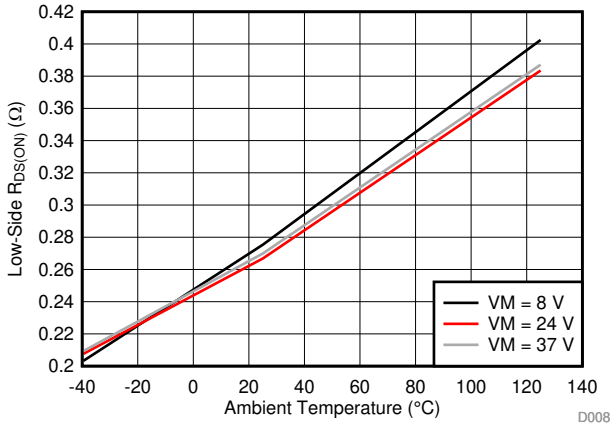


Figure 9. Low-Side $R_{DS(ON)}$ over Temperature

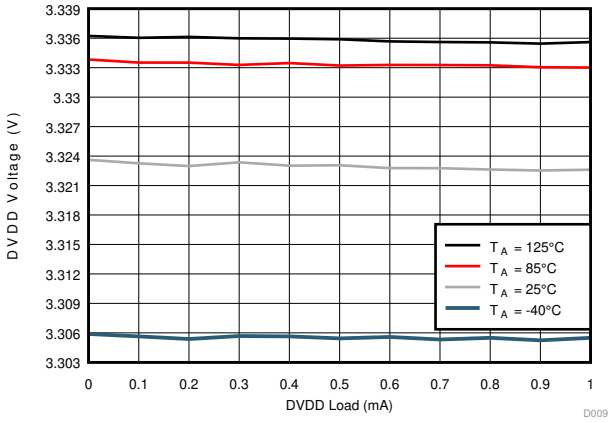


Figure 10. DVDD Regulator over Load (VM = 24 V)

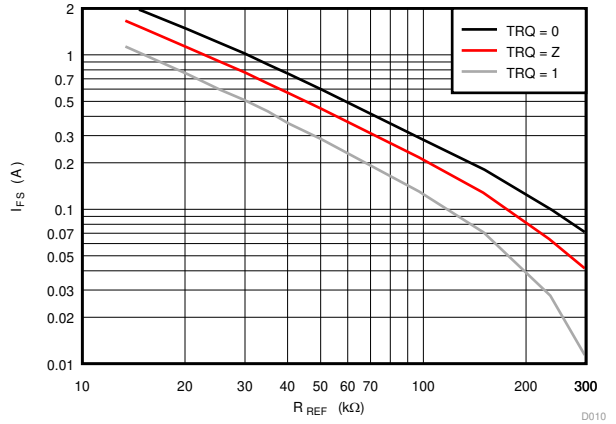


Figure 11. Full-Scale Current over RREF Selection

Copyright © 2017–2020, Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The DRV8886AT device is an integrated motor-driver solution for bipolar stepper motors. The device integrates two N-channel power MOSFET H-bridges, integrated current sense and regulation circuitry, and a microstepping indexer. The DRV8886AT device can be powered with a supply voltage from 8 to 37 V and is capable of providing an output current up to 3-A peak, 2-A full-scale, or 1.4-A root mean square (rms). The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal capability.

The DRV8886AT device uses an integrated current-sense architecture which eliminates the need for two external power sense resistors. This architecture removes the power dissipated in the sense resistors by using a current mirror approach and using the internal power MOSFETs for current sensing. The current regulation set point is adjusted with a standard low-power resistor connected to the RREF pin. This features reduces external component cost, board PCB size, and system power consumption.

A simple STEP/DIR interface allows for an external controller to manage the direction and step rate of the stepper motor. The internal indexer can execute high-accuracy microstepping without requiring the external controller to manage the winding current level. The indexer is capable of full step, half step, and 1/4, 1/8, 1/16 microstepping. In addition to a standard half stepping mode, a noncircular half stepping mode is available for increased torque output at higher motor RPM.

The current regulation is configurable between several decay modes. The decay mode can be selected as a slow-mixed, mixed decay, smart tune Ripple Control, or smart tune Dynamic Decay current regulation scheme. The slow-mixed decay mode uses slow decay on increasing steps and mixed decay on decreasing steps. The smart tune decay modes automatically adjust for optimal current regulation performance and compensate for motor variation and aging effects. smart tune Ripple Control uses a variable off-time, ripple control scheme to minimize distortion of the motor winding current. smart tune Dynamic Decay uses a fixed off-time, dynamic decay percentage scheme to minimize distortion of the motor winding current while also minimizing frequency content.

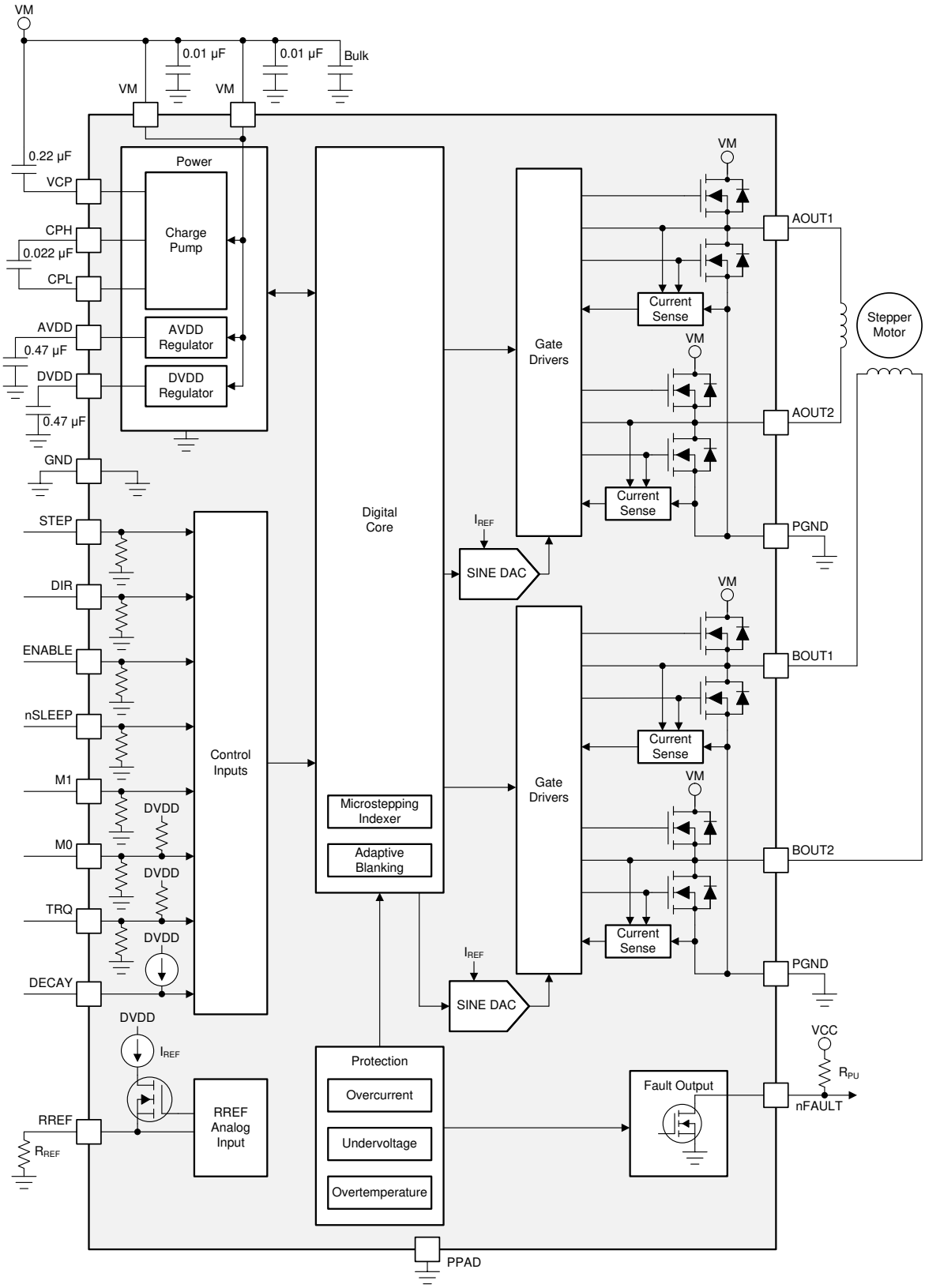
An adaptive blanking time feature automatically scales the minimum drive time with output current level. This feature helps alleviate zero-crossing distortion by limiting the drive time at low-current steps.

A torque DAC feature allows the controller to scale the output current without needing to scale the RREF reference resistor. The torque DAC is accessed using a digital input pin which allows the controller to save system power by decreasing the motor current consumption when high output torque is not required.

A low-power sleep mode is included which allows the system to save power when not actively driving the motor.

Copyright © 2017–2020, Texas Instruments Incorporated

7.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

7.3 Feature Description

Table 1 lists the recommended external components for the DRV8886AT device.

Table 1. DRV8886AT External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	Two X5R or X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM2}	VM	GND	Bulk, VM-rated capacitor
C_{VCP}	VCP	VM	X5R or X7R, 0.22-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X5R or X7R, 0.022-µF, VM-rated ceramic capacitor
C_{AVDD}	AVDD	GND	X5R or X7R, 0.47-µF, 6.3-V ceramic capacitor
C_{DVDD}	DVDD	GND	X5R or X7R, 0.47-µF, 6.3-V ceramic capacitor
R_{nFAULT}	VCC (1)	nFAULT	>4.7-kΩ resistor
R_{REF}	RREF	GND	Resistor to limit chopping current must be installed. See the *Typical Application* section for value selection.

(1) VCC is not a pin on the DRV8886AT device, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to DVDD

7.3.1 Stepper Motor Driver Current Ratings

Stepper motor drivers can be classified using three different numbers to describe the output current: peak, rms, and full-scale.

7.3.1.1 Peak Current Rating

The peak current in a stepper driver is limited by the overcurrent protection trip threshold I_{OCP}. The peak current describes any transient duration current pulse, for example when charging capacitance, when the overall duty cycle is very low. In general the minimum value of I_{OCP} specifies the peak current rating of the stepper motor driver. For the DRV8886AT device, the peak current rating is 3 A per bridge.

7.3.1.2 rms Current Rating

The rms (average) current is determined by the thermal considerations of the IC. The rms current is calculated based on the $R_{DS(ON)}$, rise and fall time, PWM frequency, device quiescent current, and package thermal performance in a typical system at 25°C. The actual operating rms current may be higher or lower depending on heatsinking and ambient temperature. For the DRV8886AT device, the rms current rating is 1.4 A per bridge.

7.3.1.3 Full-Scale Current Rating

The full-scale current describes the top of the sinusoid current waveform while microstepping. Because the sinusoid amplitude is related to the rms current, the full-scale current is also determined by the thermal considerations of the device. The full-scale current rating is approximately $\sqrt{2} \times I_{RMS}$. The full-scale current is set by the RREF pin and the torque DAC when configuring the DRV8886AT device, for details see the *Current Regulation* section. For the DRV8886AT device, the full-scale current rating is 2 A per bridge.

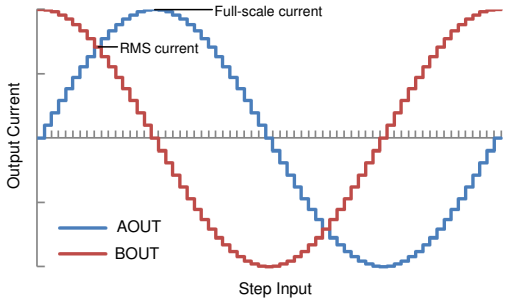


Figure 12. Full-Scale and rms Current

7.3.2 PWM Motor Drivers

The DRV8886AT device has drivers for two full H-bridges to drive the two windings of a bipolar stepper motor. Figure 13 shows a block diagram of the circuitry.

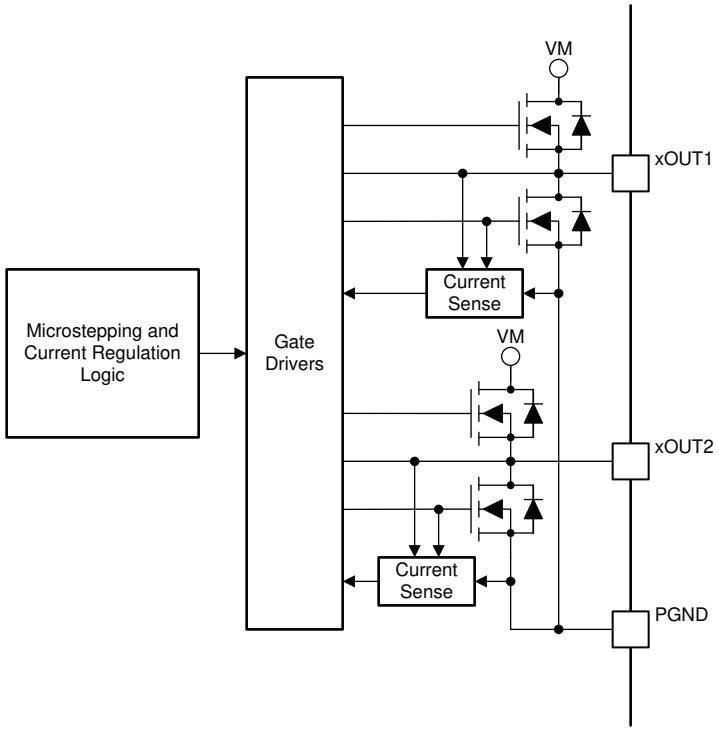


Figure 13. PWM Motor Driver Block Diagram

7.3.3 Microstepping Indexer

Built-in indexer logic in the DRV8886AT device allows a number of different step modes. The M1 and M0 pins are used to configure the step mode as shown in Table 2.

Table 2. Microstepping Settings

M1	M0	STEP MODE
0	0	Full step (2-phase excitation) with 71% current
0	1	1/16 step
1	0	1/2 step
1	1	1/4 step
0	Z	1/8 step
1	Z	Non-circular 1/2 step

Table 3 shows the relative current and step directions for full-step through 1/16-step operation. The AOUT current is the sine of the electrical angle and the BOUT current is the cosine of the electrical angle. Positive current is defined as current flowing from the xOUT1 pin to the xOUT2 pin while driving.

At each rising edge of the STEP input the indexer travels to the next state in the table. The direction is shown with the DIR pin logic high. If the DIR pin is logic low, the sequence is reversed.

On power-up or when exiting sleep mode, keep the STEP pin logic low, otherwise the indexer advances one step.

Copyright © 2017–2020, Texas Instruments Incorporated

NOTE

If the step mode is changed from full, 1/2, 1/4, 1/8, or 1/16 to full, 1/2, 1/4, 1/8, or 1/16 while stepping, the indexer advances to the next valid state for the new step mode setting at the rising edge of STEP. If the step mode is changed from or to noncircular 1/2 step the indexer goes immediately to the valid state for that mode.

The home state is an electrical angle of 45°. This state is entered after power-up, after exiting logic undervoltage lockout, or after exiting sleep mode. Table 3 lists the home state in red.

Table 3. Microstepping Relative Current Per Step (DIR = 1)

FULL STEP	1/2 STEP	1/4 STEP	1/8 STEP	1/16 STEP	ELECTRICAL ANGLE (DEGREES)	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)
	1	1	1	1	0.000°	0%	100%
				2	5.625°	10%	100%
			2	3	11.250°	20%	98%
				4	16.875°	29%	96%
		2	3	5	22.500°	38%	92%
				6	28.125°	47%	88%
			4	7	33.750°	56%	83%
				8	39.375°	63%	77%
1	2	3	5	9	45.000°	71%	71%
				10	50.625°	77%	63%
			6	11	56.250°	83%	56%
				12	61.875°	88%	47%
		4	7	13	67.500°	92%	38%
				14	73.125°	96%	29%
			8	15	78.750°	98%	20%
				16	84.375°	100%	10%
	3	5	9	17	90.000°	100%	0%
				18	95.625°	100%	–10%
			10	19	101.250°	98%	–20%
				20	106.875°	96%	–29%
		6	11	21	112.500°	92%	–38%
				22	118.125°	88%	–47%
			12	23	123.750°	83%	–56%
				24	129.375°	77%	–63%
2	4	7	13	25	135.000°	71%	–71%
				26	140.625°	63%	–77%
			14	27	146.250°	56%	–83%
				28	151.875°	47%	–88%
		8	15	29	157.500°	38%	–92%
				30	163.125°	29%	–96%
			16	31	168.750°	20%	–98%
				32	174.375°	10%	–100%
	5	9	17	33	180.000°	0%	–100%
				34	185.625°	–10%	–100%
			18	35	191.250°	–20%	–98%
				36	196.875°	–29%	–96%
		10	19	37	202.500°	–38%	–92%
				38	208.125°	–47%	–88%

Copyright © 2017–2020, Texas Instruments Incorporated

Table 3. Microstepping Relative Current Per Step (DIR = 1) (continued)

FULL STEP	1/2 STEP	1/4 STEP	1/8 STEP	1/16 STEP	ELECTRICAL ANGLE (DEGREES)	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)
			20	39	213.750°	–56%	–83%
				40	219.375°	–63%	–77%
3	6	11	21	41	225.000°	–71%	–71%
				42	230.625°	–77%	–63%
			22	43	236.250°	–83%	–56%
				44	241.875°	–88%	–47%
		12	23	45	247.500°	–92%	–38%
				46	253.125°	–96%	–29%
			24	47	258.750°	–98%	–20%
				48	264.375°	–100%	–10%
	7	13	25	49	270.000°	–100%	0%
				50	275.625°	–100%	10%
			26	51	281.250°	–98%	20%
				52	286.875°	–96%	29%
		14	27	53	292.500°	–92%	38%
				54	298.125°	–88%	47%
			28	55	303.750°	–83%	56%
				56	309.375°	–77%	63%
4	8	15	29	57	315.000°	–71%	71%
				58	320.625°	–63%	77%
			30	59	326.250°	–56%	83%
				60	331.875°	–47%	88%
		16	31	61	337.500°	–38%	92%
				62	343.125°	–29%	96%
			32	63	348.750°	–20%	98%
				64	354.375°	–10%	100%
	1	1	1	1	360.000°	0%	100%

Table 4 shows the noncircular 1/2–step operation. This stepping mode consumes more power than circular 1/2-step operation, but provides a higher torque at high motor RPM.

Table 4. Non-Circular 1/2-Stepping Current

NON-CIRCULAR 1/2-STEP	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	0	100	0
2	100	100	45
3	100	0	90
4	100	–100	135
5	0	–100	180
6	–100	–100	225
7	–100	0	270
8	–100	100	315

Copyright © 2017–2020, Texas Instruments Incorporated

7.3.4 Current Regulation

The current through the motor windings is regulated by an adjustable, fixed-off-time PWM current-regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. When the current hits the current regulation threshold, the bridge enters a decay mode for a fixed 20 μs, period of time to decrease the current. After the off time expires, the bridge is re-enabled, starting another PWM cycle.

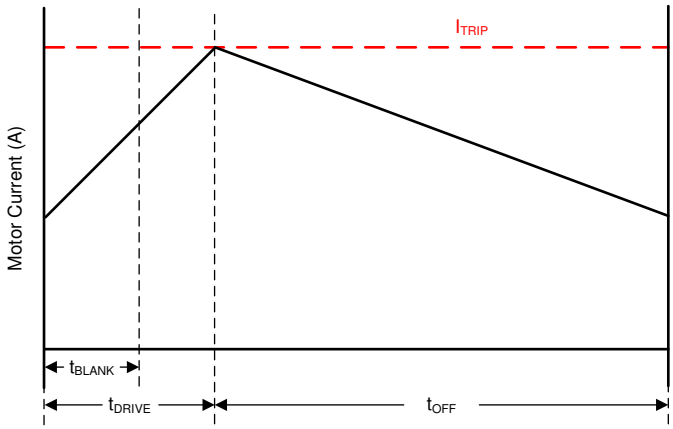


Figure 14. Current Chopping Waveform

The PWM regulation current is set by a comparator which monitors the voltage across the current sense MOSFETs in parallel with the low-side power MOSFETs. The current sense MOSFETs are biased with a reference current that is the output of a current-mode sine-weighted DAC whose full-scale reference current is set by the current through the RREF pin. An external resistor is placed from the RREF pin to GND to set the reference current. In addition, the TRQ pin can further scale the reference current.

Use Equation 1 to calculate the full-scale regulation current.

$$I_{FS}\,(A) = \frac{A_{RREF}\,(kA\Omega)}{RREF\,(k\Omega)} \times TRQ\,(\%) = \frac{30\,(kA\Omega)}{RREF\,(k\Omega)} \times TRQ\,(\%) \quad (1)$$

For example, if a 30-kΩ resistor is connected to the RREF pin, the full-scale regulation current is 1 A (TRQ at 100%).

The TRQ pin is the input to a DAC used to scale the output current. Table 5 lists the current scalar value for different inputs.

Table 5. Torque DAC Settings

TRQ	CURRENT SCALAR (TRQ)
0	100%
Z	75%
1	50%

Copyright © 2017–2020, Texas Instruments Incorporated

7.3.5 Controlling RREF With an MCU DAC

In some cases, the full-scale output current may need to be changed between many different values, depending on motor speed and loading. The reference current of the RREF pin can be adjusted in the system by tying the RREF resistor to a DAC output instead of GND.

In this mode of operation, as the DAC voltage increases, the reference current decreases and therefore the full-scale regulation current decreases as well. For proper operation, the output of the DAC should not rise above V_{RREF}.

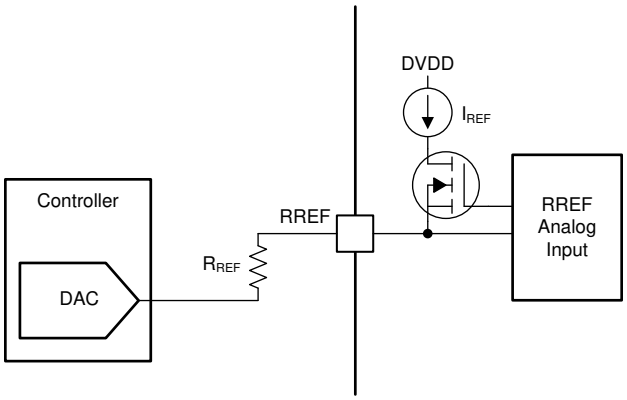


Figure 15. Controlling RREF with a DAC Resource

Use Equation 2 to calculate the full-scale regulation current as controlled by a controller DAC.

$$I_{FS}\ (A) = \frac{A_{RREF}\ (kA\Omega) \times \left[V_{RREF}\ (V) - V_{DAC}\ (V)\right]}{V_{RREF}\ (V) \times RREF\ (k\Omega)} \times TRQ\ (\%) \quad (2)$$

For example, if a 20-kΩ resistor is connected from the RREF pin to the DAC, and the DAC outputs 0.74 V, the chopping current is 600 mA (TRQ at 100%)

The RREF pin can also be adjusted using a PWM signal and low-pass filter.

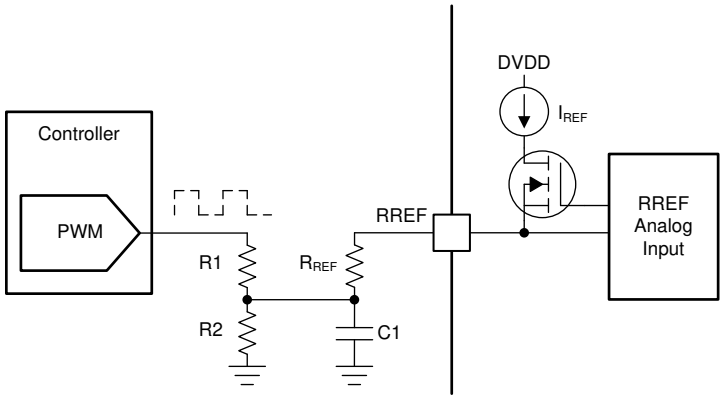


Figure 16. Controlling RREF With a PWM Resource

7.3.5.1 Various Sources of Error

When performing a design error calculation, the different variables that contribute the most to the error must be considered. To do so, first consider the typical values extracted from DRV8885 data sheet which are listed in Table 6 with a 20-kΩ 1% resistor .

Copyright © 2017–2020, Texas Instruments Incorporated

Table 6. DRV8885 Data Sheet Values

Parameter	Minimum	Typical	Maximum
A_{RREF}	28100	30000	31900
V_{RREF}	1.18	1.232	1.28
RREF	19800	20000	20200

Using and knowing the desired output current, the V_{DAC} value can be obtained. For example, the DRV8885EVM, which has a 20-kΩ resistor for RREF, was selected to operate at a 1-A, 400mA, and 200 mA current. Table 7 lists the calculated V_{DAC} values using typical A_{RREF} and V_{RREF} data sheet values

Table 7. V_{DAC} Calculation

Parameter	Minimum	Typical	Maximum
I_{FS}	1	0.4	0.2
A_{RREF}	30 000	30 000	30 000
V_{RREF}	1.232	1.232	1.232
R_{REF}	20 000	20 000	20 000
V_{DAC}	0.4107	0.9035	1.0677

Next, use Equation 3 and Equation 4 to calculate the worst case value for the minimum and maximum full scale current, respectively.

$$I_{FSmin}\ (A) = \frac{A_{RREFmin}\ (kA\Omega) \times [V_{RREFmin}\ (V) - V_{DACmax}\ (V)]}{V_{RREFmin}\ (V) \times RREF_{max}\ (k\Omega)} \times TRQ\ (\%) \quad (3)$$

$$I_{FSmax}\ (A) = \frac{A_{RREFmax}\ (kA\Omega) \times [V_{RREFmax}\ (V) - V_{DACmin}\ (V)]}{V_{RREFmax}\ (V) \times RREF_{min}\ (k\Omega)} \times TRQ\ (\%) \quad (4)$$

These two equations show that error contributions come from V_{DAC}, A_{RREF}, V_{RREF}, and RREF. The next sections will show how these different error contributors, affect the overall I_{FS} error and how they can be improved.

7.3.5.1.1 V_{RREF}, A_{RREF}, and RREF Error

To observe how V_{RREF}, A_{RREF}, and RREFV_{RREF} affect the I_{FS} error , Equation 3 and Equation 4 are used with the data sheet values from earlier while V_{DAC} voltage remains constant. Table 8, Table 9, and Table 10 list the results at different current levels (1 A, 400 mA, and 200 mA, respectively).

Table 8. Worst Case Calculation—I_{FS} Error at 1 A

Parameter	Minimum	Typical	Maximum
V_{DAC}	0.4107	0.4107	0.4107
A_{RREF}	28100	30000	31900
V_{RREF}	1.18	1.232	1.28
R_{REF}	19800	20000	20200
I_{FS} (mA)	906.95	1000	1094.21
Error (%)	–9.30		9.42

Table 9. Worst Case Calculation—I_{FS} Error at 400 mA

Parameter	Minimum	Typical	Maximum
V_{DAC}	0.9035	0.9035	0.9035
A_{RREF}	28100	30000	31900
V_{RREF}	1.18	1.232	1.28
R_{REF}	19800	20000	20200
I_{FS} (mA)	326.00	400	473.93
Error (%)	–18.50		18.48

Copyright © 2017–2020, Texas Instruments Incorporated

Table 10. Worst Case Calculation—I_{FS} Error at 200 mA

Parameter	Minimum	Typical	Maximum
V_{DAC}	1.0677	1.0677	1.0677
A_{RREF}	28100	30000	31900
V_{RREF}	1.18	1.232	1.28
R_{REF}	19800	20000	20200
I_{FS} (mA)	135.35	200	267.18
Error (%)	–33.83		33.59

These tables show that as the I_{FS} current level decreases, the overall error percentage increases due to increasing offset error from the internal signal chain. It is worthy to clarify that the V_{RREF} and A_{RREF} values in these tables are data sheet values which represent the characterization data variation across a wide range of temperatures and voltages with additional margin. For information on how to further minimize this percentage of error based on targeted characterization data for V_{RREF} and A_{RREF}, see Application-Specific Error Calculations .

7.3.5.1.2 V_{DAC} Error

Using the same methodology along with Equation 3 and Equation 4, the V_{DAC} error contribution to I_{FS} can be shown. This is done by removing the error from V_{RREF}, A_{RREF}, and RREF. The following examples show the V_{DAC} error value with a 3% and 10% variation.

Table 11. Worst Case Calculation—V_{DAC} 3% and 10%, I_{FS} Error at 1 A

Parameter	Minimum	Typical	Maximum
3% ERROR			
V_{DAC}	0.3983	0.4107	0.423
A_{RREF}	30000	30000	30000
V_{RREF}	1.232	1.232	1.232
R_{REF}	20000	20000	20000
I_{FS} (mA)	985.08	1000	1015.07
Error (%)	–1.50		1.50
10% ERROR			
V_{DAC}	0.3696	0.4107	0.4517
A_{RREF}	30000	30000	30000
V_{RREF}	1.232	1.232	1.232
R_{REF}	20000	20000	20000
I_{FS} (mA)	950.08	1000	1050.07
Error (%)	–5.00		5.00

Table 12. Worst Case Calculation—V_{DAC} 3% and 10%, I_{FS} Error at 400 mA

Parameter	Minimum	Typical	Maximum
3% ERROR			
V_{DAC}	0.8764	0.9035	0.9306
A_{RREF}	30000	30000	31 900
V_{RREF}	1.232	1.232	1.232
R_{REF}	20000	20000	20000
I_{FS} (mA)	367.18	400	433.17
Error (%)	–8.25		8.25
10% ERROR			
V_{DAC}	0.8131	0.9035	0.9938
A_{RREF}	30000	30000	30000

Copyright © 2017–2020, Texas Instruments Incorporated

Table 12. Worst Case Calculation—V_{DAC} 3% and 10%, I_{FS} Error at 400 mA (continued)

Parameter	Minimum	Typical	Maximum
V_{RREF}	1.232	1.232	1.232
R_{REF}	20000	20000	20000
I_{FS} (mA)	290.19	400	510.16
Error (%)	–27.48		27.48

Table 13. Worst Case Calculation—V_{DAC} 3% and 10%, I_{FS} Error at 200 mA

Parameter	Minimum	Typical	Maximum
3% ERROR			
V_{DAC}	1.0357	1.0677	1.0998
A_{RREF}	30000	30000	30000
V_{RREF}	1.232	1.232	1.232
R_{REF}	20000	20000	20000
I_{FS} (mA)	161.22	200	239.20
Error (%)	–19.48		19.48
10% ERROR			
V_{DAC}	0.9610	1.0677	1.1745
A_{RREF}	30000	30000	30000
V_{RREF}	1.232	1.232	1.232
R_{REF}	20000	20000	20000
I_{FS} (mA)	70.23	200	330.19
Error (%)	–64.92		64.92

These tables show that as the variation in V_{DAC} increases, the error percentage increases. Also, for very low currents, the error percentage increases greatly because of the V_{DAC} proximity to the V_{RREF} voltage.

7.3.5.2 Application-Specific Error Calculations

As described in the previous analysis, it is possible to obtain a tighter error calculations by using values for V_{RREF} and A_{RREF} for the specific application use case. The data sheet parameters represent limits based on design and characterization data across a wide range of temperatures and voltage with additional margin. For the following example, the operational voltage is limited to V_{VM} = 24 V, a common operating point for the DRV8884, DRV8885, DRV8886, and DRV8886AT.

Considering this use case, Table 14 provides updated values for V_{RREF} and A_{RREF}.

Table 14. Values For DRV8885 V_{VM}= 24-V

Parameter	Minimum	Typical	Maximum
A_{RREF}	28800	30000	31200
V_{RREF}	1.207	1.232	1.257
RREF	19800	20000	20200

Using values above and maintaining V_{DAC} constant, the error percentage is reduced as shown in the following tables.

Table 15. I_{FS} Error at 1 A, V_{DAC} Fixed and Application Values

Parameter	Minimum	Typical	Maximum
V_{DAC}	0.4107	0.4107	0.4107
A_{RREF}	28800	30000	31200
V_{RREF}	1.207	1.232	1.257
R_{REF}	19800	20000	20200

Copyright © 2017–2020, Texas Instruments Incorporated

Table 15. I_{FS} Error at 1 A, V_{DAC} Fixed and Application Values (continued)

Parameter	Minimum	Typical	Maximum
I_{FS} (mA)	940.79	1000	1060.8
Error (%)	–5.93		6.07

Table 16. I_{FS} Error at 400 mA, V_{DAC} Fixed and Application Values

Parameter	Minimum	Typical	Maximum
V_{DAC}	0.9035	0.9035	0.9035
A_{RREF}	28800	30000	31200
V_{RREF}	1.207	1.232	1.257
R_{REF}	19800	20000	20200
I_{FS} (mA)	358.54	400	443.18
Error (%)	–10.4		10.75

Table 17. I_{FS} Error at 200 mA, V_{DAC} Fixed and Application Values

Parameter	Minimum	Typical	Maximum
V_{DAC}	1.0677	1.0677	1.0677
A_{RREF}	28800	30000	31200
V_{RREF}	1.207	1.232	1.257
R_{REF}	19800	20000	20200
I_{FS} (mA)	164.51	200	267.26
Error (%)	–17.83		18.51

By keeping V_{DAC} value fixed or close to be fixed, yields much less error variation. The same calculation can be made using a V_{DAC} value with a ±3 % variation to compare error percentage difference as shown in the following tables.

Table 18. V_{DAC} 3%, V_{RREF} and A_{RREF} for 24-V Application at 1 A

Parameter	Minimum	Typical	Maximum
V_{DAC}	0.3983	0.4107	0.4230
A_{RREF}	28800	30000	31200
V_{RREF}	1.207	1.232	1.257
R_{REF}	19800	20000	20200
I_{FS} (mA)	926.09	1000	1076.39
Error (%)	–7.4		7.63

Table 19. V_{DAC} 3%, V_{RREF} and A_{RREF} for 24-V Application at 400 mA

Parameter	Minimum	Typical	Maximum
V_{DAC}	0.8764	0.9035	0.9306
A_{RREF}	28800	30000	31200
V_{RREF}	1.207	1.232	1.257
R_{REF}	19800	20000	20200
I_{FS} (mA)	326.52	400	477.16
Error (%)	–18.41		19.24

Copyright © 2017–2020, Texas Instruments Incorporated

Table 20. V_{DAC} 3%, V_{RREF} and A_{RREF} for 24-V Application at 200 mA

Parameter	Minimum	Typical	Maximum
V_{DAC}	1.0357	1.0677	1.0998
A_{RREF}	28800	30000	31200
V_{RREF}	1.207	1.232	1.257
R_{REF}	19800	20000	20200
I_{FS} (mA)	126.67	200	277.42
Error (%)	–36.73		38.56

Table 18, Table 19, and Table 20 show values closer to the typical values for both V_{DAC}, A_{RREF}, and V_{RREF}. From all these calculations, the error percentages for the 200 mA current are higher because at those very low values, the minimum change greatly affects the full current equation. One method to improve the low-value current accuracy is to use a combination of the MCU DAC and TRQ pin. This method can help improve the error by reducing the need to use only the DAC voltage to achieve the low full-scale current. An example of this method is to achieve 200 mA using the 400 mA DAC setting and the 50% TRQ setting.

Copyright © 2017–2020, Texas Instruments Incorporated

7.3.6 Decay Modes

The DRV8886AT decay mode is selected by setting the quad-level DECAY pin to the voltage range listed in Table 21. The decay mode setting is latched on device enable.

Table 21. Decay Mode Settings

DECAY	INCREASING STEPS	DECREASING STEPS
100 mV Can be tied to ground	Slow decay	Mixed decay: 30% fast
300 mV, 15 kΩ to GND	Mixed decay: 30% fast	Mixed decay: 30% fast
1.0 V, 45 kΩ to GND	smart tune Ripple Control	smart tune Ripple Control
2.9 V Can be tied to DVDD	smart tune Dynamic Decay	smart tune Dynamic Decay

Figure 17 defines increasing and decreasing current. For the slow-mixed decay mode, the decay mode is set as slow during increasing current steps and mixed decay during decreasing current steps. In full step mode the decreasing steps decay mode is always used. In noncircular 1/2-step mode the increasing step decay mode is used after a level transition (0% to 100% and 0% to –100%). When the level transition is to a similar level (100% to 100% and –100% to –100%), the decreasing step decay mode is used.

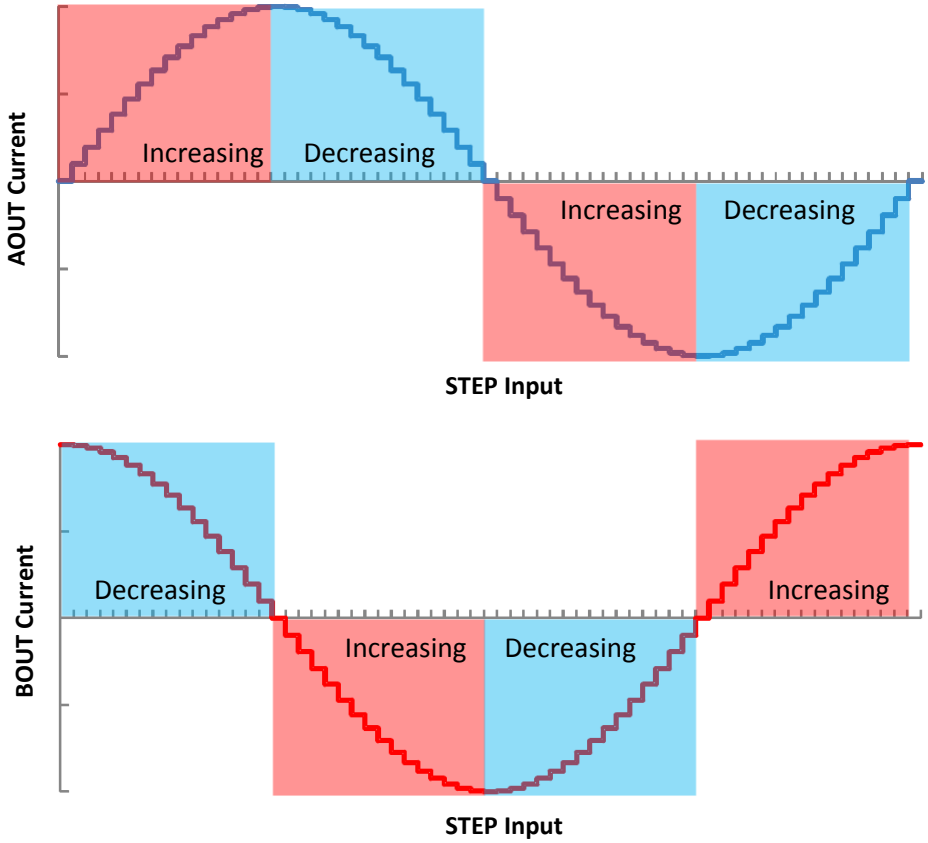


Figure 17. Definition of Increasing and Decreasing Steps

Copyright © 2017–2020, Texas Instruments Incorporated

7.3.6.1 Mode 1: Slow Decay for Increasing Current, Mixed Decay for Decreasing Current

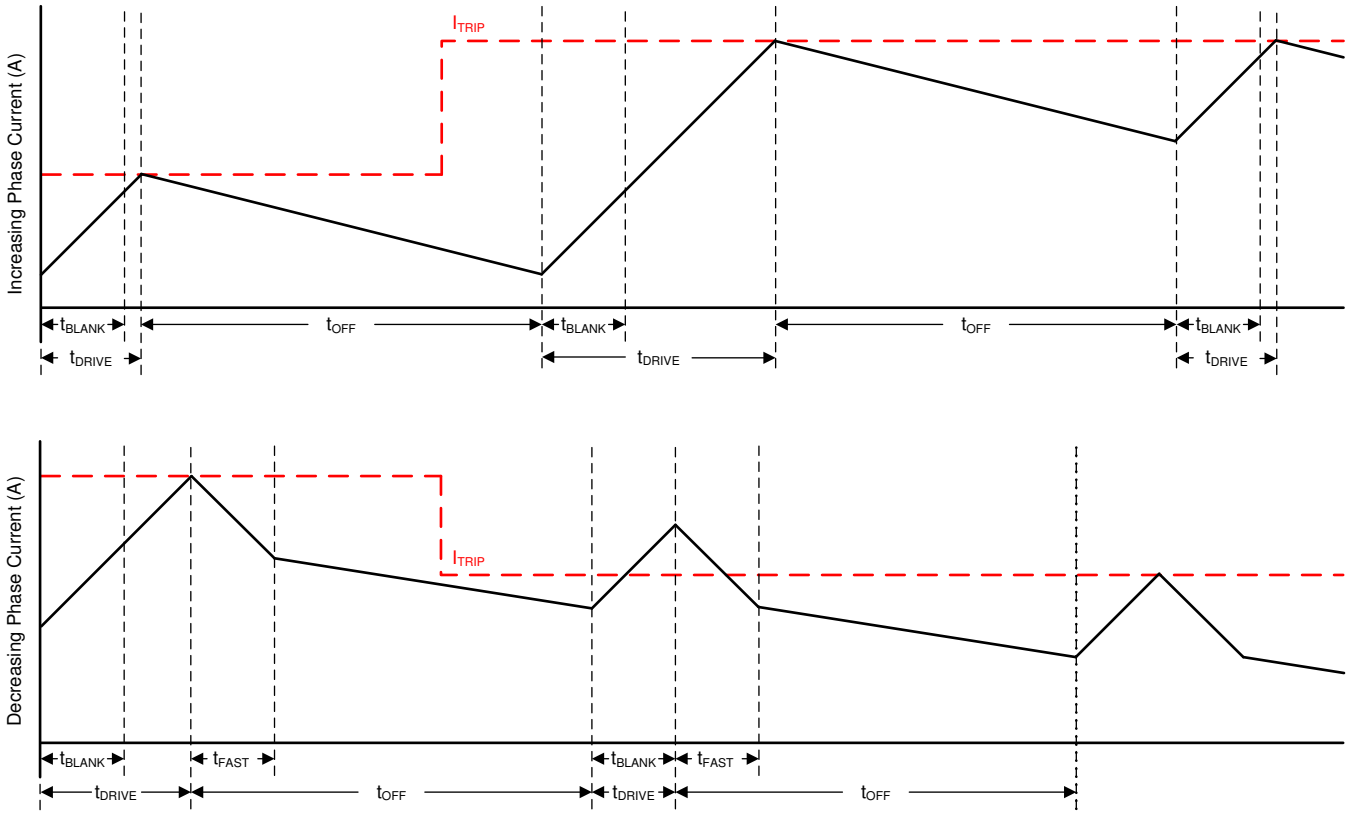


Figure 18. Slow-Mixed Decay Mode

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of the t_{OFF} time. In this mode, mixed decay only occurs during decreasing current. Slow decay is used for increasing current.

This mode exhibits the same current ripple as slow decay for increasing current, because for increasing current, only slow decay is used. For decreasing current, the ripple is larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

7.3.6.2 Mode 2: Mixed Decay for Increasing and Decreasing Current

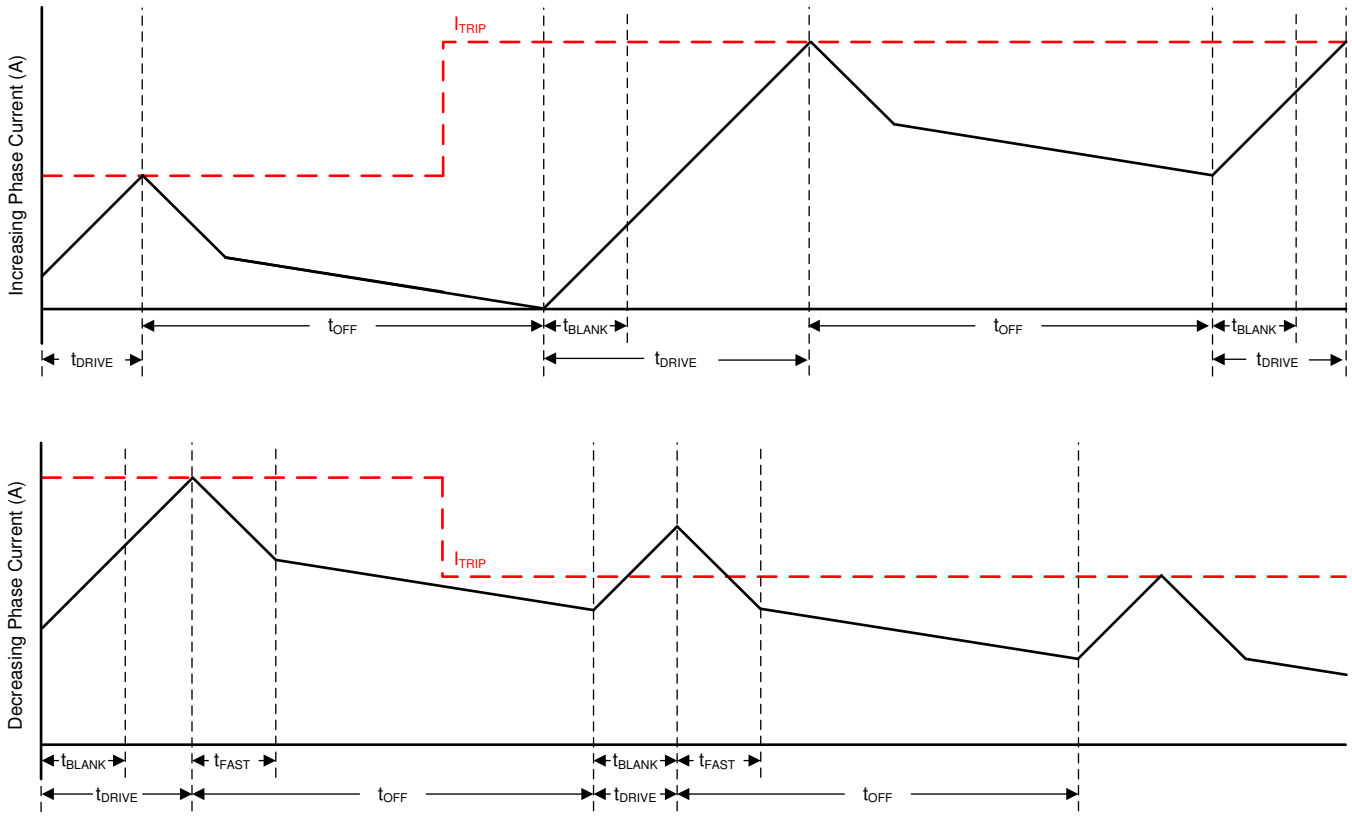


Figure 19. Mixed-Mixed Decay Mode

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of t_{OFF}. In this mode, mixed decay occurs for both increasing and decreasing current steps.

This mode exhibits ripple larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

In cases where current is held for a long time (no input in the STEP pin) or at very low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and requires an excessively large off-time. Increasing or decreasing mixed decay mode allows the current level to stay in regulation when no back-EMF is present across the motor windings.

Copyright © 2017–2020, Texas Instruments Incorporated

7.3.6.3 Mode 3: Smart Tune Ripple Control

The smart tune current regulation schemes are advanced current-regulation control methods that use additional components as compared to traditional fixed off-time current regulation schemes. Smart tune current regulation schemes help the stepper motor driver adjust the decay scheme based on operating factors such as the ones listed as follows:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Motor back-EMF difference on rising and falling steps
- Step transitions
- Low-current versus high-current dI/dt

The DRV8886AT device provides two different smart tune current regulation modes, named smart tune Ripple Control and smart tune Dynamic Decay.

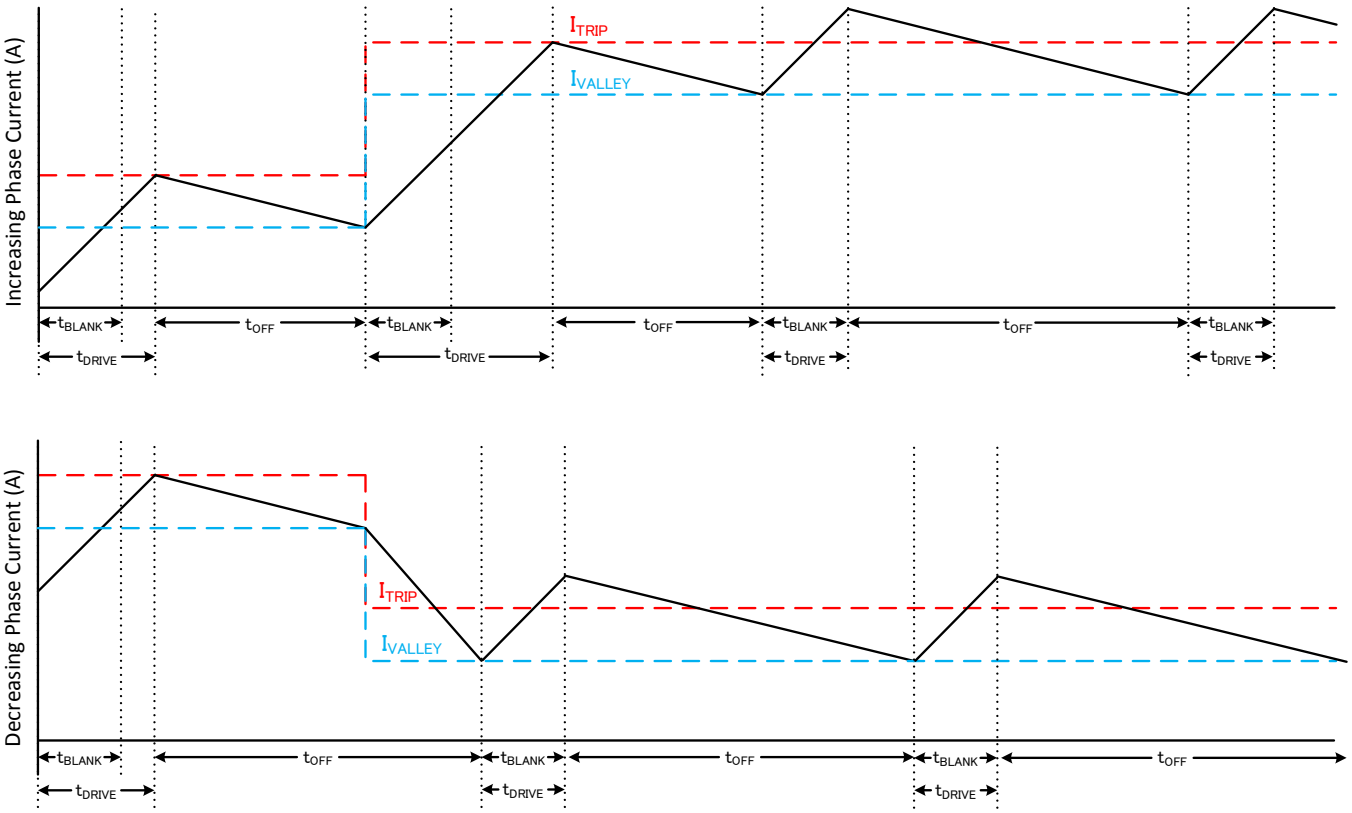


Figure 20. Smart Tune Ripple Control Decay Mode

Smart tune Ripple Control operates by setting an I_{VALLEY} level alongside the I_{TRIP} level. When the current level reaches I_{TRIP}, instead of entering slow decay until the t_{OFF} time expires, the driver enters slow decay until I_{VALLEY} is reached. Slow decay operates similar to mode 1 in which both low-side MOSFETs are turned on allowing the current to recirculate. In this mode, t_{OFF} varies depending on the current level and operating conditions.

This method allows much tighter regulation of the current level increasing motor efficiency and system performance. Smart tune Ripple Control can be used in systems that can tolerate a variable off-time regulation scheme to achieve small current ripple in the current regulation.

Copyright © 2017–2020, Texas Instruments Incorporated

7.3.6.4 Mode 4: Smart Tune Dynamic Decay

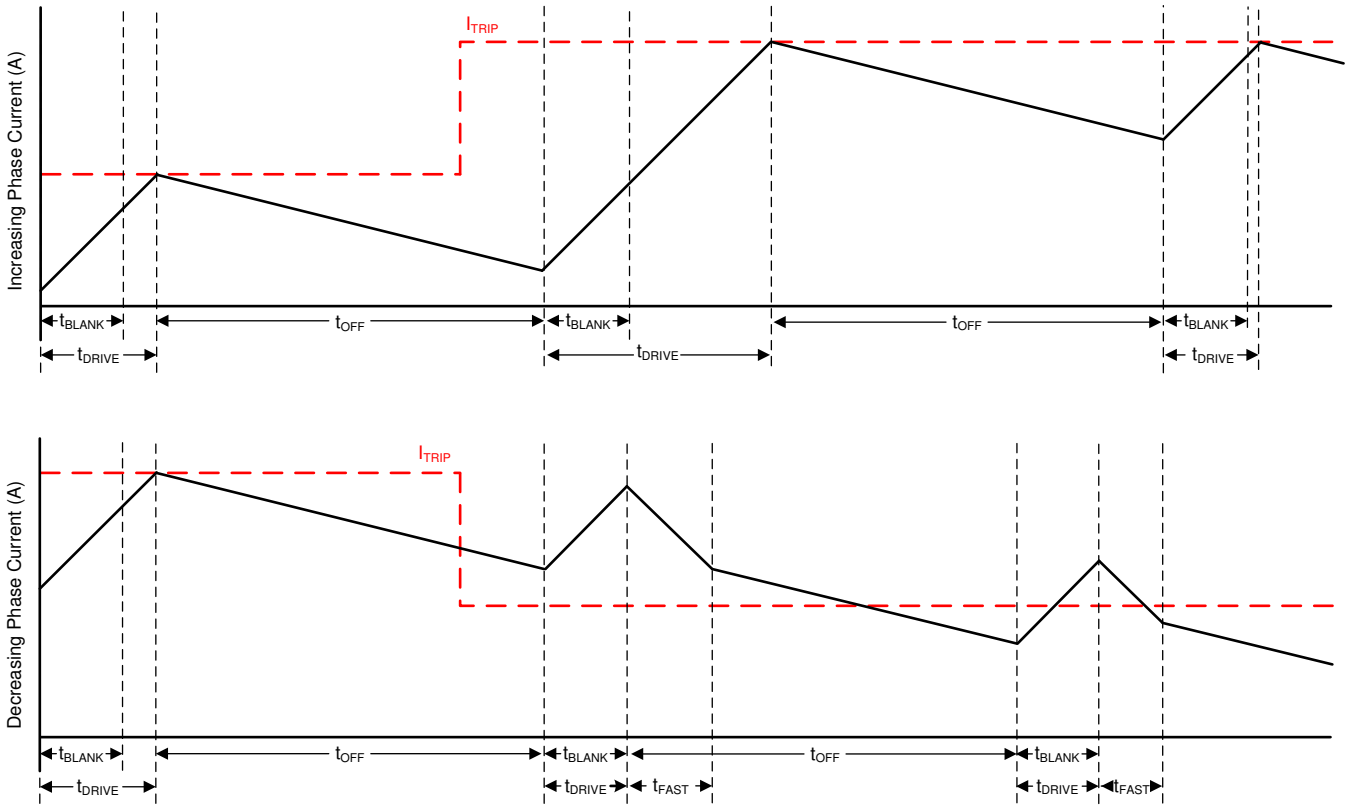


Figure 21. Smart Tune Dynamic Decay Mode

Smart tune Dynamic Decay greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

Smart tune Dynamic Decay is optimal for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.

Copyright © 2017–2020, Texas Instruments Incorporated

7.3.7 Blanking Time

After the current is enabled in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLANK}) before enabling the current-sense circuitry. The blanking time also sets the minimum drive time of the PWM. Table 22 shows the blanking time based on the sine table index and the torque DAC setting. In the smart tune current regulation modes the blanking time is fixed at 1.0 µs. Please note that the torque DAC index is not the same as one step as given in Table 3.

Table 22. Adaptive Blanking Time over Torque DAC and Microsteps

t_{blank} = 1.5 µs	t_{blank} = 1.0 µs

SINE INDEX	TORQUE DAC (TRQ)		
	100%	75%	50%
16	100%	75%	50%
15	98%	73.5	49%
14	96%	72%	48%
13	92%	69%	46%
12	88%	66%	44%
11	83%	62.3%	41.5%
10	77%	57.8%	38.5%
9	71%	53.3%	35.5%
8	63%	47.3%	31.5%
7	56%	42%	28%
6	47%	35.3	23.5%
5	38%	28.5	19%
4	29%	21.8%	14.5%
3	20%	15%	10%
2	10%	7.5%	5%
1	0%	0%	0%

Copyright © 2017–2020, Texas Instruments Incorporated

7.3.8 Charge Pump

A charge pump is integrated to supply a high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

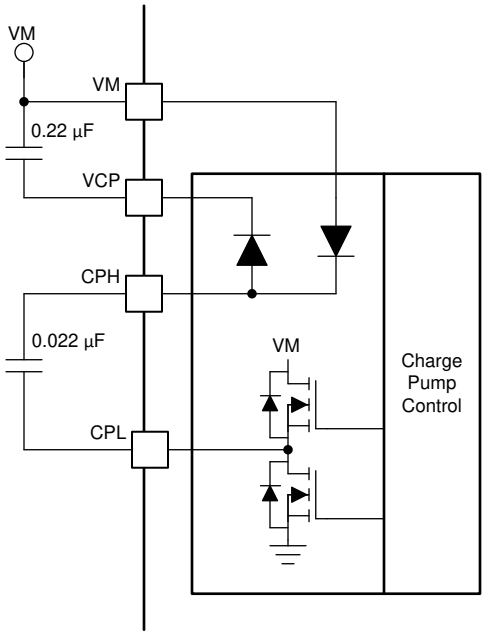


Figure 22. Charge Pump Block Diagram

Copyright © 2017–2020, Texas Instruments Incorporated

7.3.9 Linear Voltage Regulators

An linear voltage regulator is integrated into the DRV8886AT device. The DVDD regulator can be used to provide a reference voltage. For proper operation, bypass the DVDD pin to GND using a ceramic capacitor.

The DVDD output is nominally 3.3 V. When the DVDD LDO current load exceeds 1 mA, the output voltage drops significantly.

The AVDD pin also requires a bypass capacitor to GND. This LDO is for DRV8886AT internal use only.

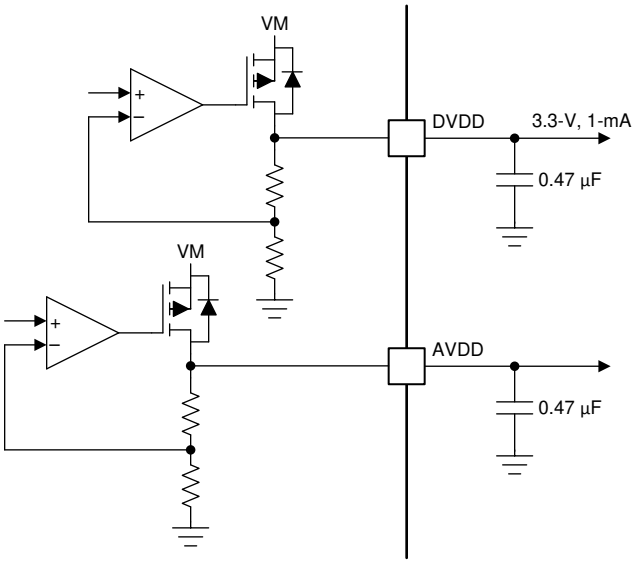


Figure 23. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high (that is, Mx, DECAY or TRQ), tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 100 kΩ, and tri-level inputs have a typical pulldown of 60 kΩ.

7.3.10 Logic and Multi-Level Pin Diagrams

Figure 24 shows the input structure for the logic-level pins STEP, DIR, ENABLE, nSLEEP, and M1.

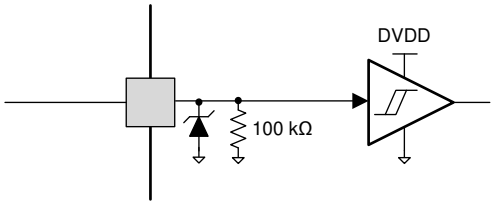


Figure 24. Logic-Level Input Pin Diagram

The tri-level logic pins, M0 and TRQ, have the structure shown in Figure 25.

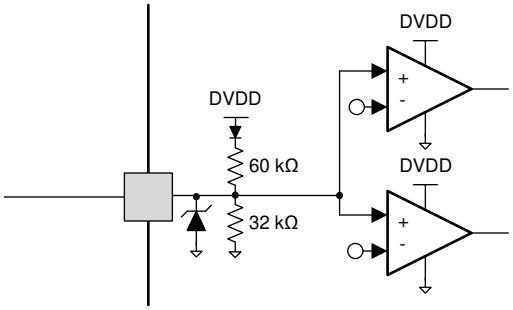


Figure 25. Tri-Level Input Pin Diagram

The quad-level logic pin, DECAY, has the structure shown in Figure 26.

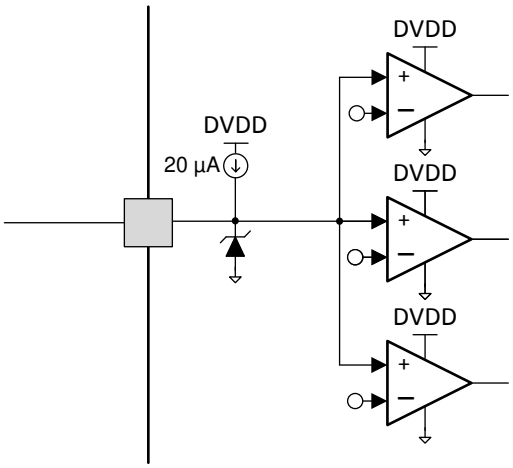


Figure 26. Quad-Level Input Pin Diagram

7.3.11 Protection Circuits

The DRV8886AT device is fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, and device overtemperature events.

7.3.11.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the VM undervoltage-lockout threshold voltage (V_{UVLO}), all MOSFETs in the H-bridge are disabled, the charge pump is disabled, the logic is reset, and the nFAULT pin is driven low. Operation resumes when the VM voltage rises above the V_{UVLO} threshold. The nFAULT pin is released after operation resumes. Decreasing the VM voltage below this undervoltage threshold resets the indexer position.

7.3.11.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the charge-pump undervoltage-lockout threshold voltage (V_{CPUV}), all MOSFETs in the H-bridge are disabled and the nFAULT pin is driven low. Operation resumes when the VCP voltage rises above the V_{CPUV} threshold. The nFAULT pin is released after operation resumes.

7.3.11.3 Overcurrent Protection (OCP)

An analog current limit circuit on each MOSFET limits the current through the MOSFET by removing the gate drive. If this analog current limit persists for longer than t_{OCP}, all MOSFETs in the H-bridge are disabled and the nFAULT pin is driven low.

Copyright © 2017–2020, Texas Instruments Incorporated

The driver is re-enabled after the OCP retry period (t_{RETRY}) has passed. The nFAULT pin becomes high again at after the retry time. If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes and nFAULT remains deasserted.

7.3.11.4 Thermal Shutdown (TSD)

If the die temperature exceeds the T_{TSD} level, all MOSFETs in the H-bridge are disabled and the nFAULT pin is driven low. When the die temperature falls below the T_{TSD} level, operation automatically resumes. The nFAULT pin is released after operation resumes.

Table 23. Fault Condition Summary

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	DVDD	AVDD	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO} (max 7.8 V)	nFAULT	Disabled	Disabled	Disabled	Operating	Disabled	VM > V_{UVLO} (max 8.0 V)
VCP undervoltage (CPUV)	VCP < V_{CPUV} (typ VM + 2.0 V)	nFAULT	Disabled	Operating	Operating	Operating	Operating	VCP > V_{CPUV} (typ VM + 2.7 V)
Overcurrent (OCP)	I_{OUT} > I_{OCP} (min 3 A)	nFAULT	Disabled	Operating	Operating	Operating	Operating	t_{RETRY}
Thermal Shutdown (TSD)	T_J > T_{TSD} (min 150°C)	nFAULT	Disabled	Disabled	Operating	Operating	Operating	T_J < T_{TSD} - T_{HYS} (T_{HYS} typ 20°C)

7.4 Device Functional Modes

The DRV8886AT device is active unless the nSLEEP pin is brought logic low. In sleep mode the charge pump is disabled, the H-bridge FETs are disabled Hi-Z, and the regulators are disabled.

NOTE

The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device is in sleep mode. The DRV8886AT device is brought out of sleep mode automatically if nSLEEP is brought logic high.

The t_{WAKE} time must elapse before the outputs change state after wake-up.

TI recommends to keep the STEP pin logic low when coming out of nSLEEP or when applying power.

If the ENABLE pin is brought logic low, the H-bridge outputs are disabled, but the internal logic is still active. A rising edge on STEP advances the indexer, but the outputs do not change state until the ENABLE pin is asserted.

Table 24 lists a summary of the functional modes.

Table 24. Functional Modes Summary

CONDITION		H-BRIDGE	CHARGE PUMP	INDEXER	DVDD	AVDD
Operating	8 V < VM < 40 V nSLEEP pin = 1 ENABLE pin = 1	Operating	Operating	Operating	Operating	Operating
Disabled	8 V < VM < 40 V nSLEEP pin = 1 ENABLE pin = 0	Disabled	Operating	Operating	Operating	Operating
Sleep mode	8 V < VM < 40 nSLEEP pin = 0	Disabled	Disabled	Disabled	Disabled	Disabled
Fault encountered	VM undervoltage (UVLO)	Disabled	Disabled	Disabled	Operating	Disabled
	VCP undervoltage (CPUV)	Disabled	Operating	Operating	Operating	Operating
	Overcurrent (OCP)	Disabled	Operating	Operating	Operating	Operating
	Thermal Shutdown (TSD)	Disabled	Disabled	Operating	Operating	Operating

Copyright © 2017–2020, Texas Instruments Incorporated

8 Application and Implementation

NOTE

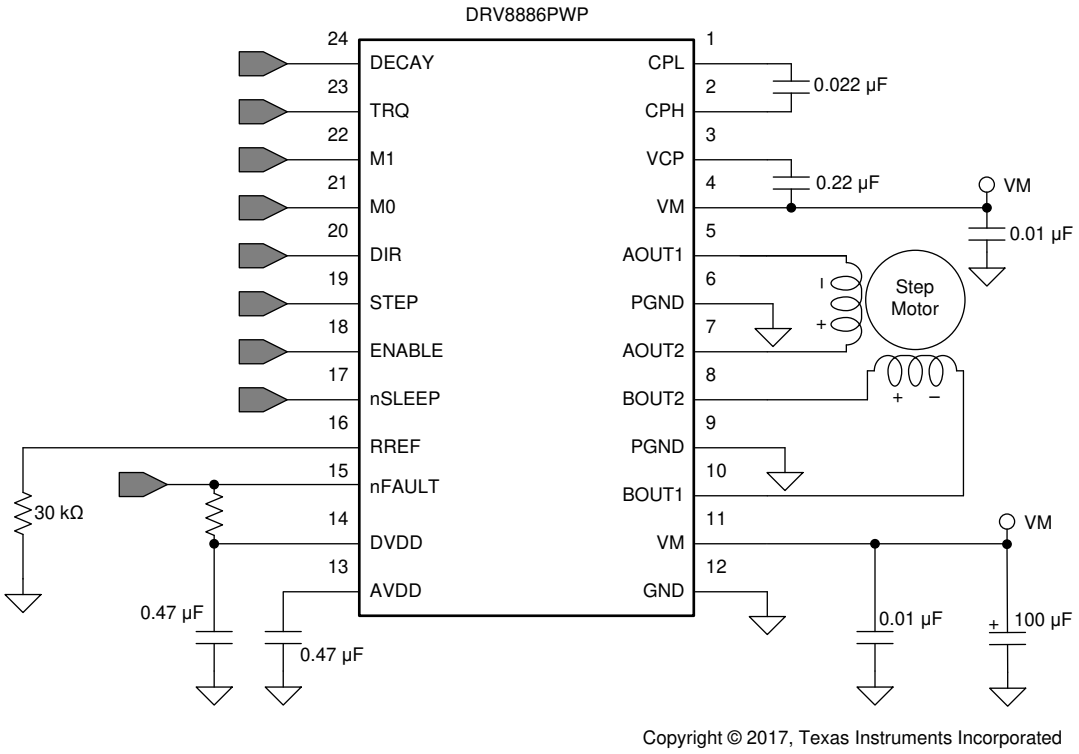
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8886AT device is used in bipolar stepper control.

8.2 Typical Application

The following design procedure can be used to configure the DRV8886AT device.



Copyright © 2017, Texas Instruments Incorporated

Figure 27. Typical Application Schematic

8.2.1 Design Requirements

Table 25 lists the design input parameters for system design.

Table 25. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	2.6 Ω/phase
Motor winding inductance	L_L	1.4 mH/phase
Motor full step angle	θ_{step}	1.8°/step
Target microstepping level	n_m	1/8 step
Target motor speed	v	120 rpm
Target full-scale current	I_{FS}	2.0 A

Copyright © 2017–2020, Texas Instruments Incorporated

8.2.2 Detailed Design Procedure

8.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8886AT device requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin.

If the target motor speed is too high, the motor does not spin. Make sure that the motor can support the target speed.

Use Equation 5 to calculate f_{step} for a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step})

$$f_{step}\ (\text{steps/s}) = \frac{\text{v (rpm)} \times 360\ (^\circ/\text{rot})}{\theta_{step}\ (^\circ/\text{step}) \times n_m\ (\text{steps/microstep}) \times 60\ (\text{s/min})} \quad (5)$$

The value of θ_{step} can be found in the stepper motor data sheet, or written on the motor.

For the DRV8886AT device, the microstepping level is set by the Mx pins and can be any of the settings listed in Table 26. Higher microstepping results in a smoother motor motion and less audible noise, but increases switching losses and requires a higher f_{step} to achieve the same motor speed.

Table 26. Microstepping Indexer Settings

M1	M0	STEP MODE
0	0	Full step (2-phase excitation) with 71% current
0	1	1/16 step
1	0	1/2 step
1	1	1/4 step
0	Z	1/8 step
1	Z	Non-circular 1/2 step

For example, the motor is 1.8°/step for a target of 120 rpm at 1/8 microstep mode.

$$f_{step}\ (\text{steps/s}) = \frac{120\ \text{rpm} \times 360^\circ/\text{rot}}{1.8^\circ/\text{step} \times 1/8\ \text{steps/microstep} \times 60\ \text{s/min}} = 3.2\ \text{kHz} \quad (6)$$

8.2.2.2 Current Regulation

In a stepper motor, the full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the RREF resistor and the TRQ setting. During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step.

$$I_{FS}\ (\text{A}) = \frac{A_{RREF}\ (\text{k}\Omega)}{\text{RREF}\ (\text{k}\Omega)} = \frac{30\ (\text{k}\Omega) \times \text{TRQ\%}}{\text{RREF}\ (\text{k}\Omega)} \quad (7)$$

NOTE

The I_{FS} current must also follow Equation 8 to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

$$I_{FS}\ (\text{A}) < \frac{\text{VM (V)}}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega)} \quad (8)$$

8.2.2.3 Decay Modes

The DRV8886AT device supports three different decay modes: slow decay, slow-mixed and all mixed decay. The current through the motor windings is regulated using an adjustable fixed-time-off scheme which means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8886AT places the winding in one of the three decay modes for t_{OFF}. After t_{OFF}, a new drive phase starts.

The blanking time, t_{BLANK}, defines the minimum drive time for the PWM current chopping. I_{TRIP} is ignored during t_{BLANK}, so the winding current may overshoot the trip level.

Copyright © 2017–2020, Texas Instruments Incorporated

8.2.3 Application Curves

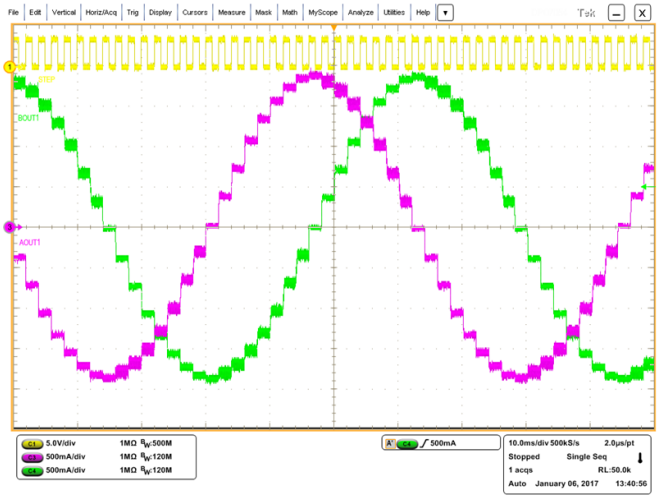


Figure 28. 1/8 Microstepping with Slow-Mixed Decay

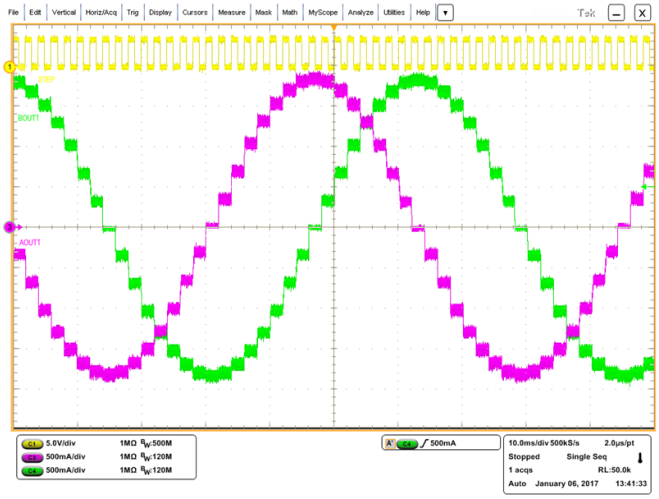


Figure 29. 1/8 Microstepping With Mixed30-Mixed30 Decay

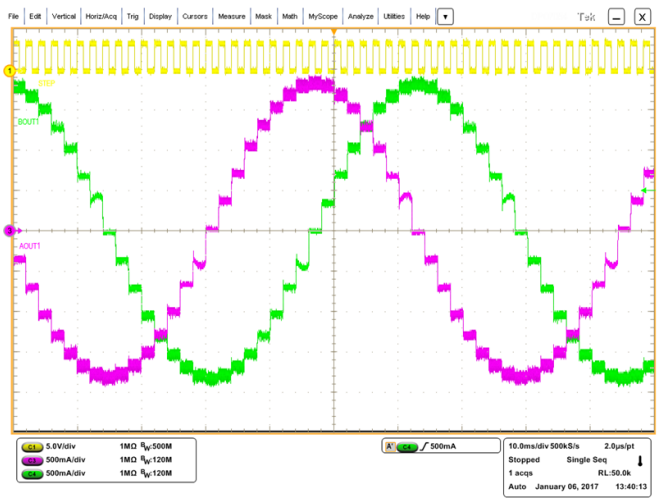


Figure 30. 1/8 Microstepping With Smart Tune Ripple Control

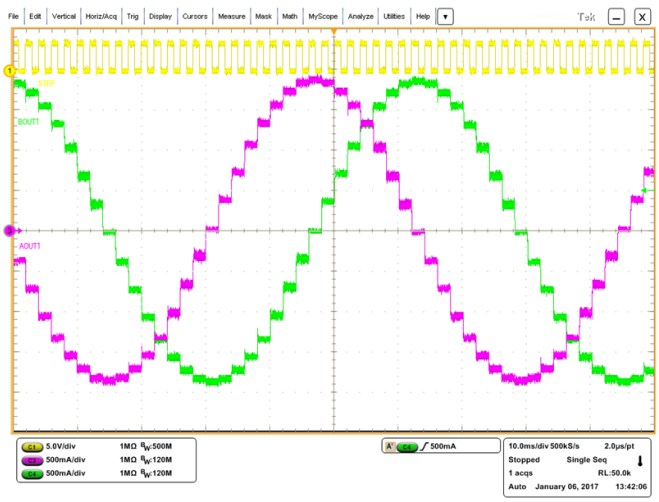


Figure 31. 1/8 Microstepping With Smart Tune Dynamic Decay

Copyright © 2017–2020, Texas Instruments Incorporated

9 Power Supply Recommendations

The DRV8886AT device is designed to operate from an input voltage supply (VM) range from 8 V to 37 V. A 0.01-µF ceramic capacitor rated for VM must be placed at each VM pin as close to the DRV8886AT device as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

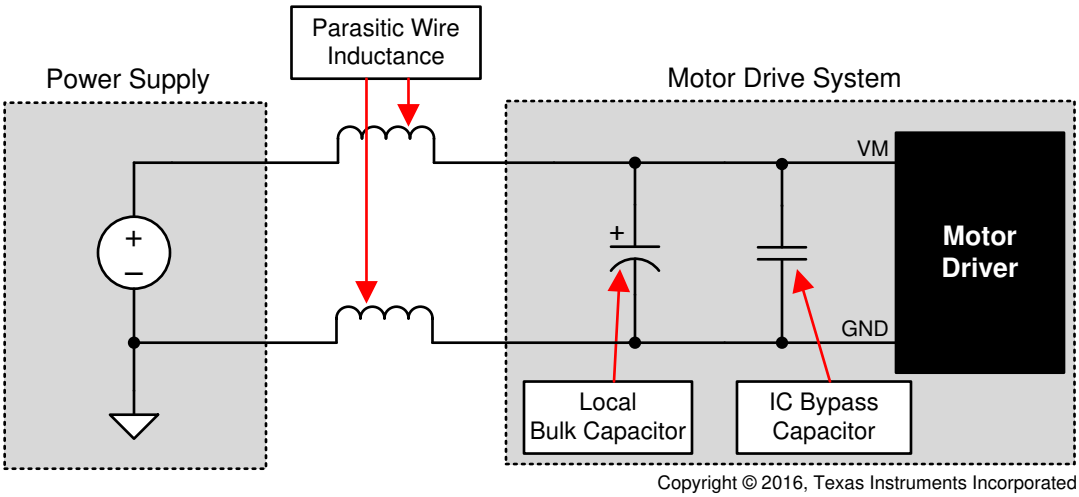


Figure 32. Example Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to GND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.022 µF rated for VM is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.22 µF rated for 16 V is recommended. Place this component as close to the pins as possible.

Bypass the AVDD and DVDD pins to ground with a low-ESR ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

10.2 Layout Example

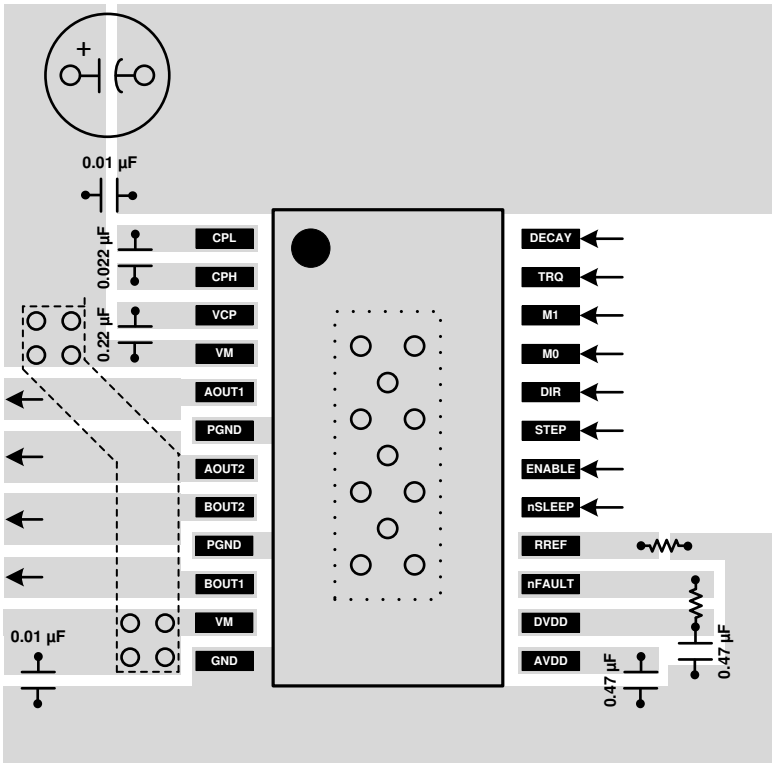


Figure 33. Layout Recommendation

Copyright © 2017–2020, Texas Instruments Incorporated

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *DRV8886AT Evaluation Module User's Guide*
- Texas Instruments, *Full-Scale Current Adjustment Using a Digital-to-Analog Converter (DAC)* application report
- Texas Instruments, *How smart tune regulates current in stepper motors* white paper
- Texas Instruments, *Industrial Motor Drive Solution Guide* white paper
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *Stepper motors made easy with smart tune* white paper
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2017–2020, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8886ATPWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	8886AT	Samples
DRV8886ATPWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	8886AT	Samples
DRV8886ATRHRR	ACTIVE	WQFN	RHR	28	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8886AT	Samples
DRV8886ATRHRT	ACTIVE	WQFN	RHR	28	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8886AT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

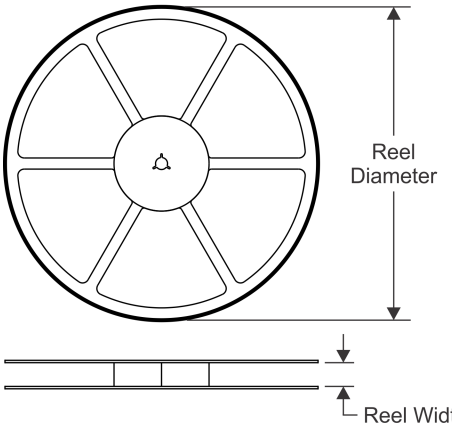
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

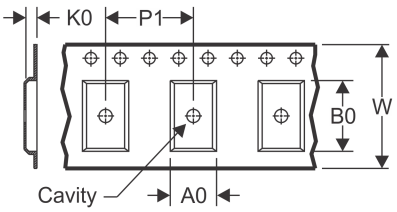
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

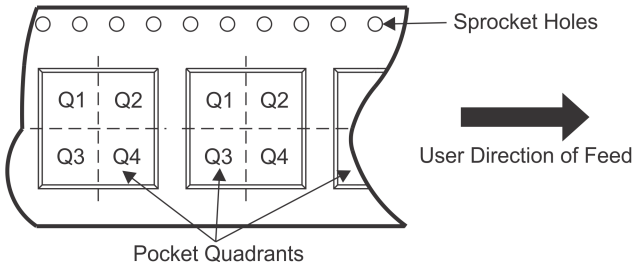


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

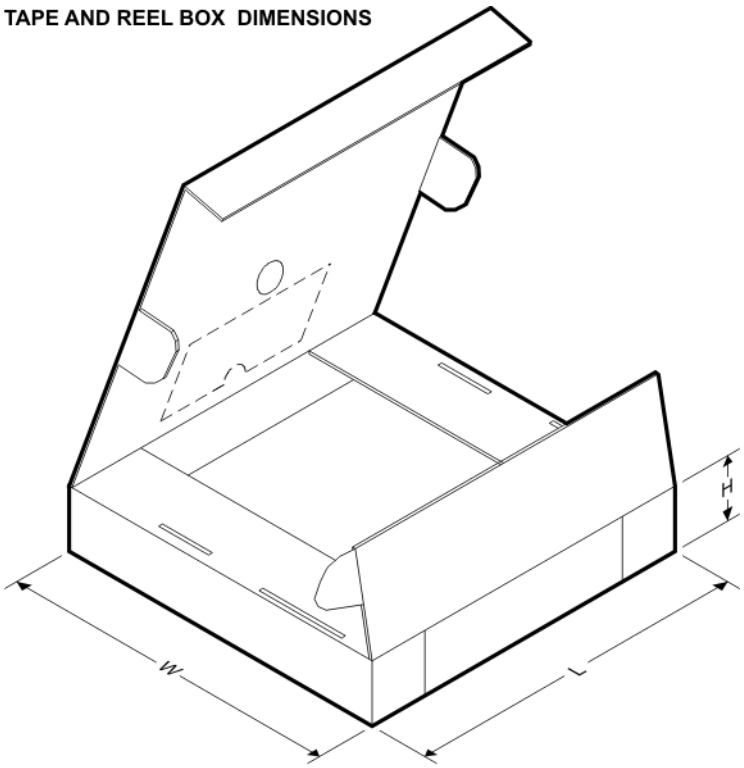
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8886ATPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DRV8886ATRHRR	WQFN	RHR	28	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
DRV8886ATRHRT	WQFN	RHR	28	250	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8886ATPWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0
DRV8886ATRHRR	WQFN	RHR	28	3000	367.0	367.0	35.0
DRV8886ATRHRT	WQFN	RHR	28	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

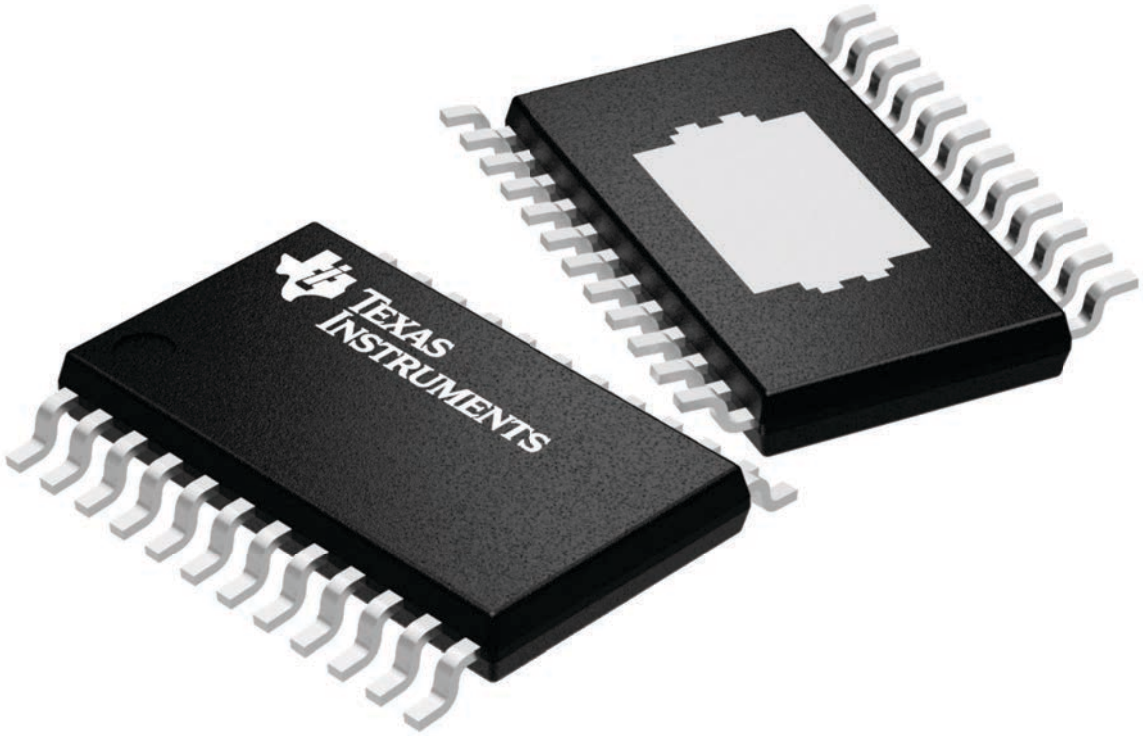
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B

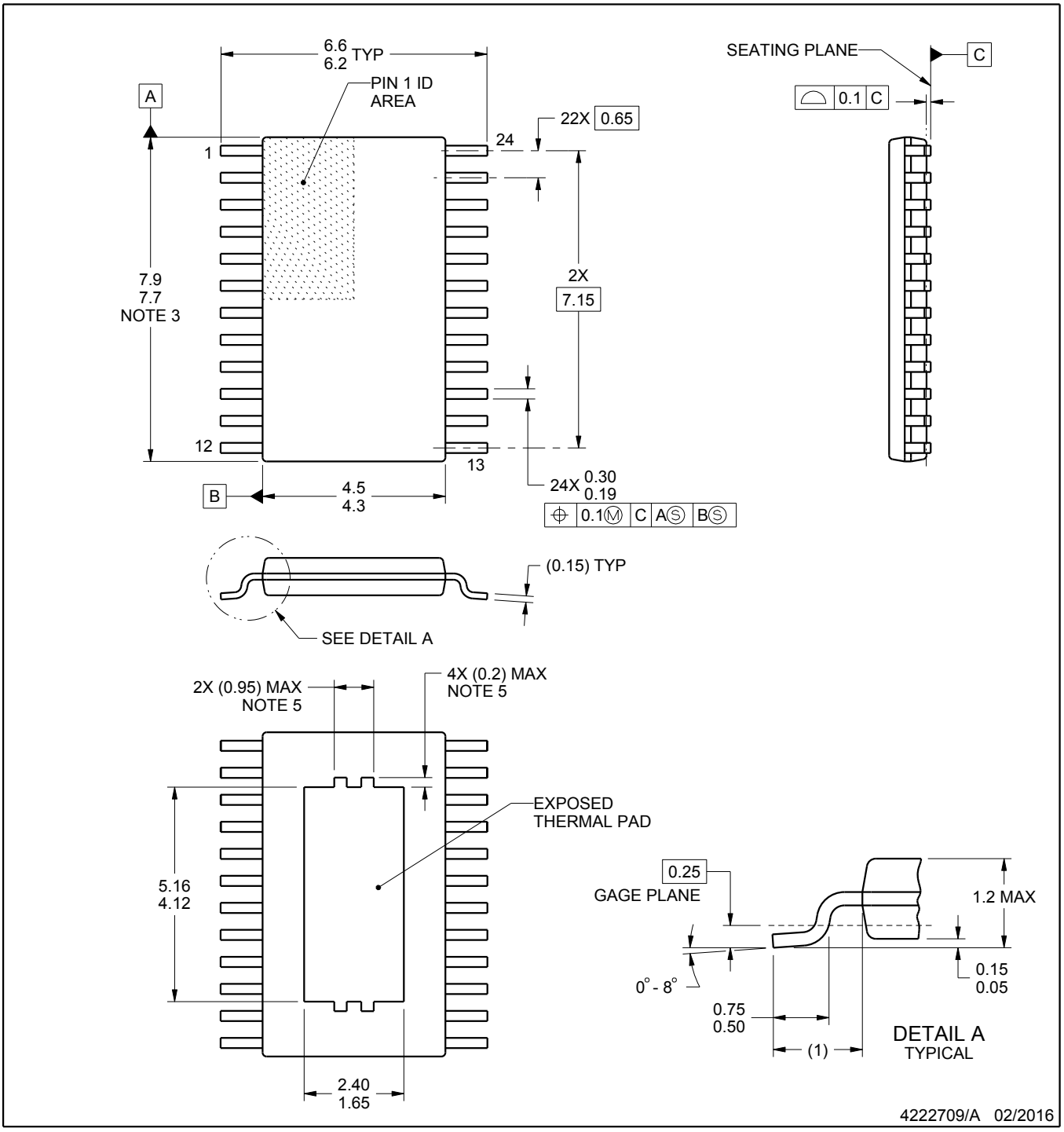


PACKAGE OUTLINE

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

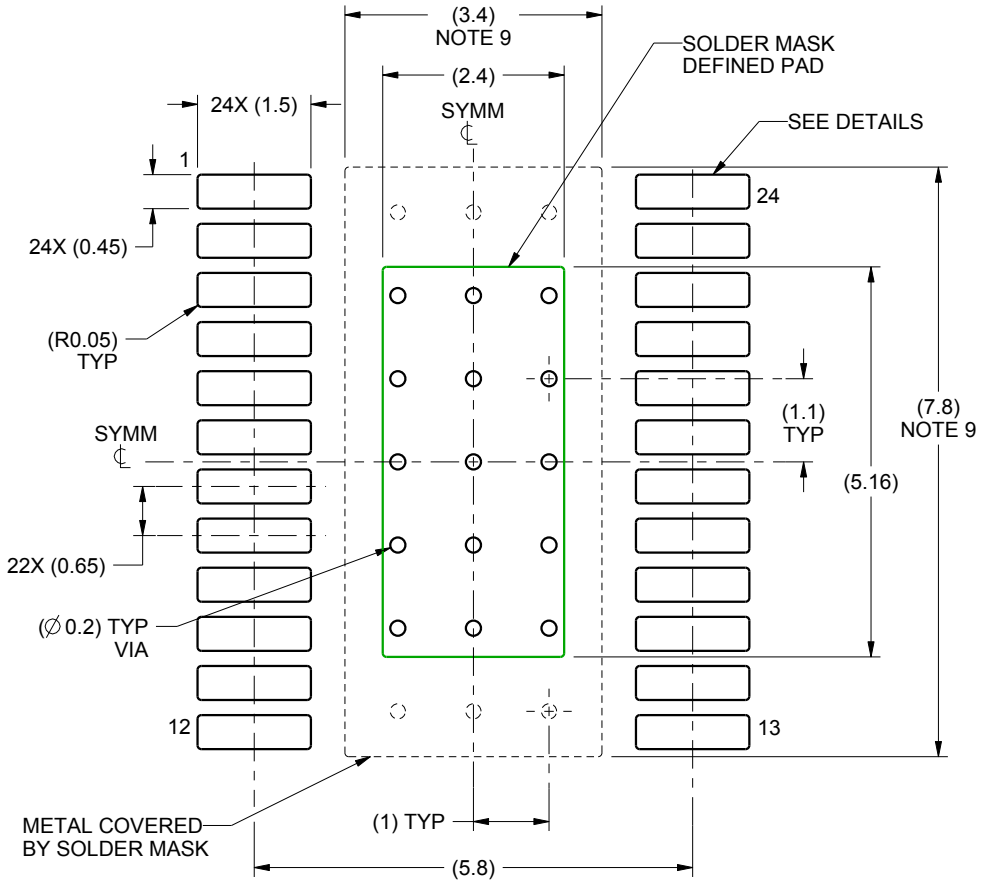
PLASTIC SMALL OUTLINE



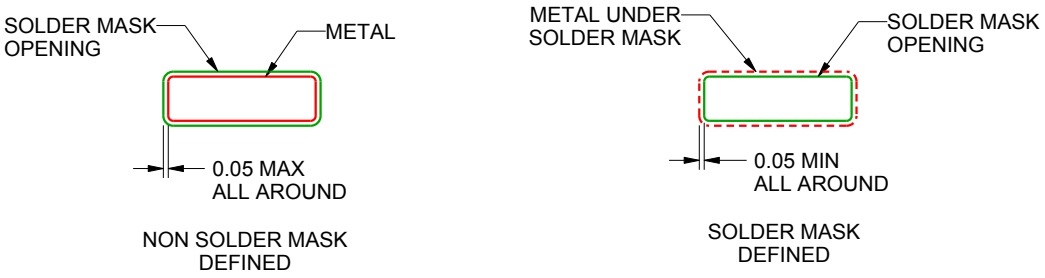
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.



LAND PATTERN EXAMPLE
SCALE:10X

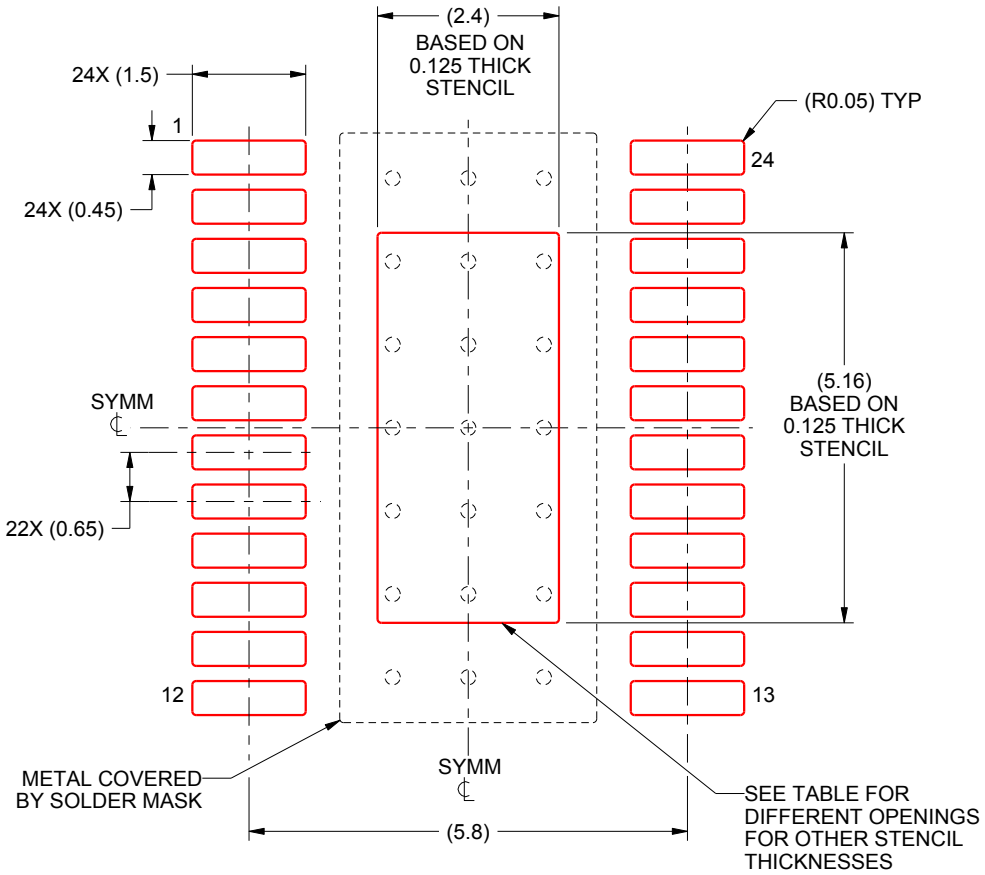


SOLDER MASK DETAILS
PADS 1-24

4222709/A 02/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

4222709/A 02/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

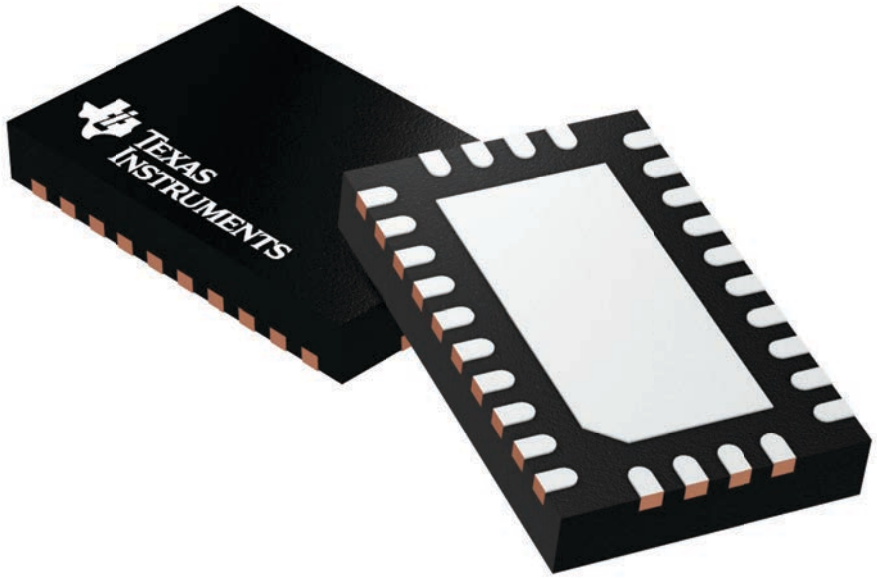
GENERIC PACKAGE VIEW

RHR 28

WQFN - 0.8 mm max height

3.5 x 5.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

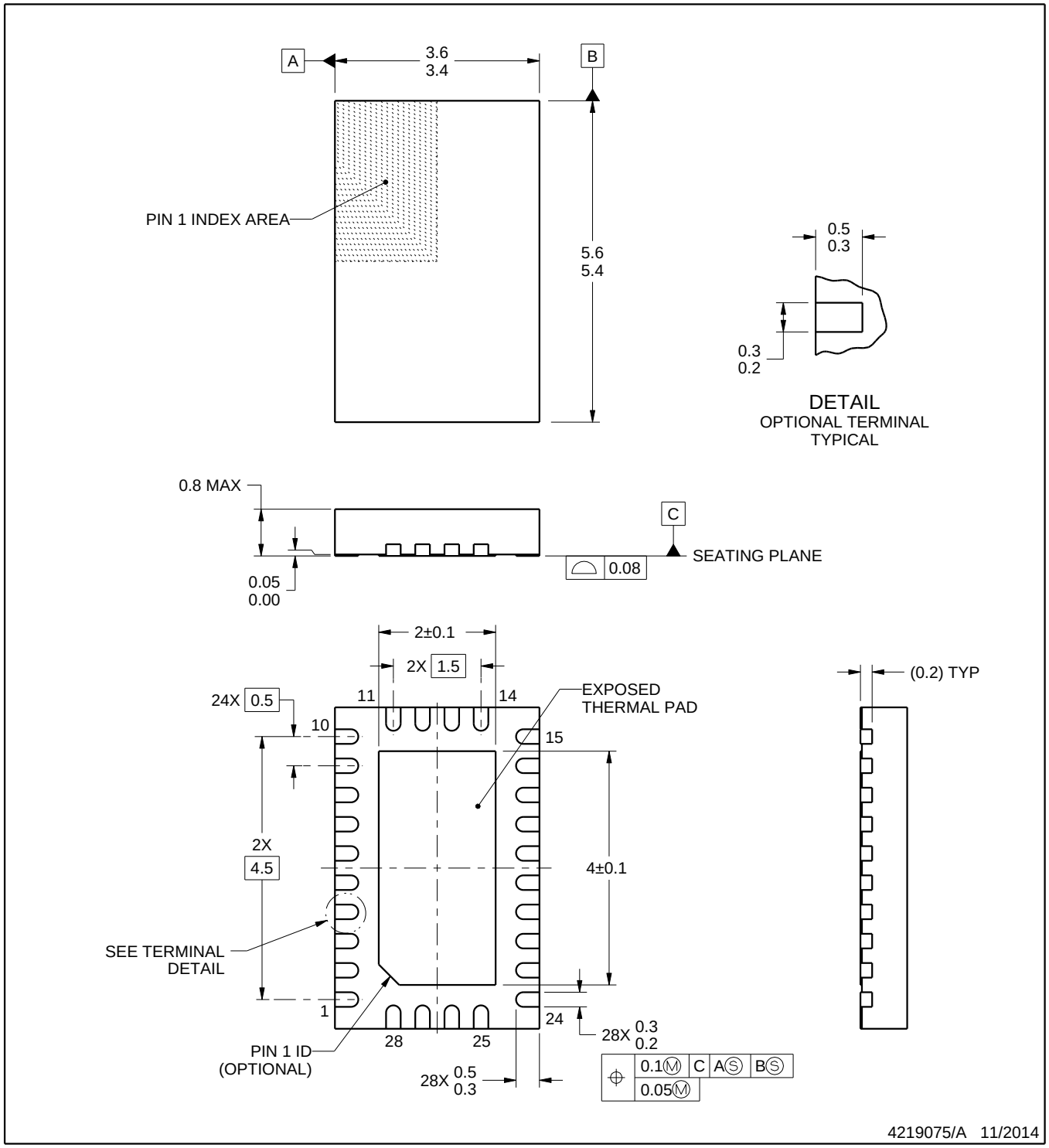
4210249/B

PACKAGE OUTLINE

RHR0028A

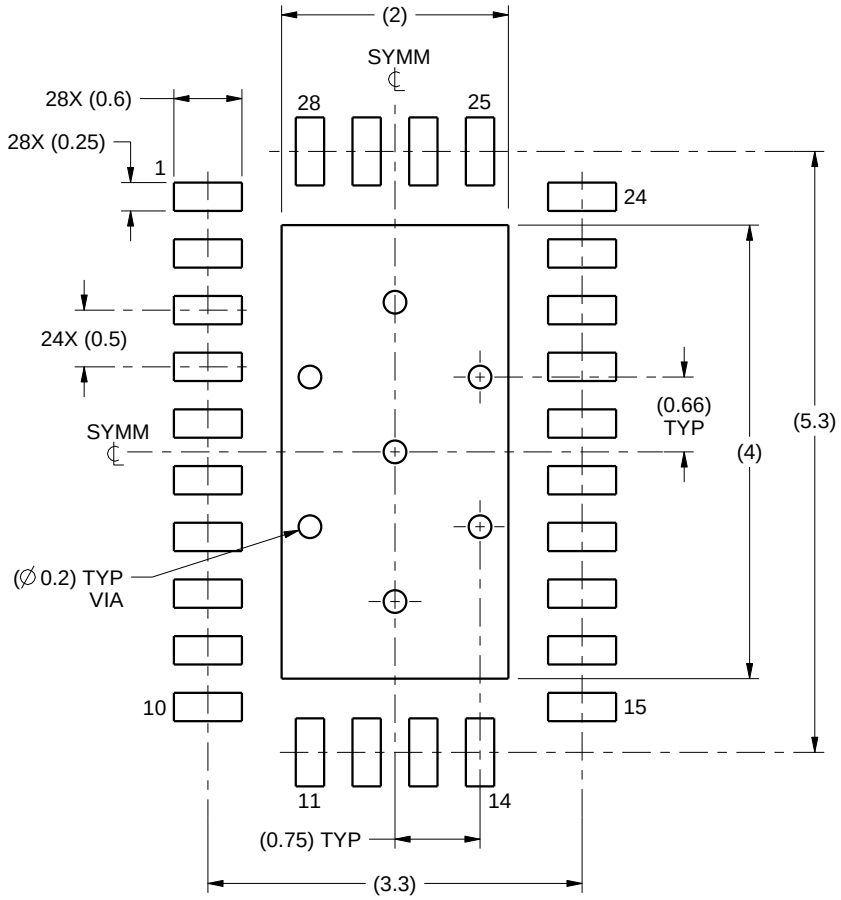
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

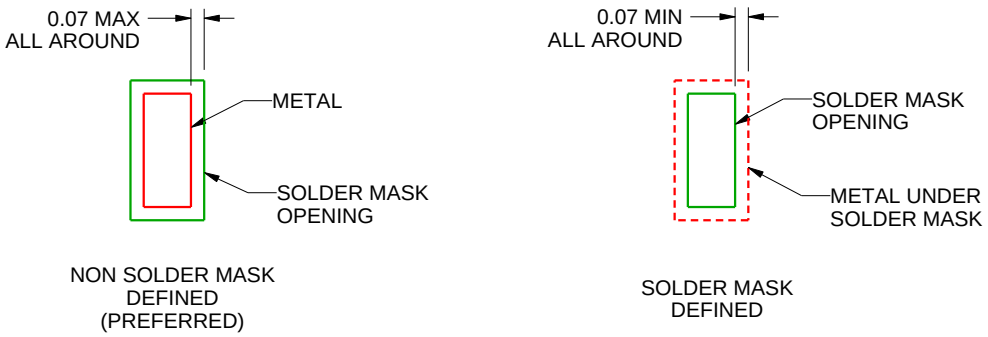


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

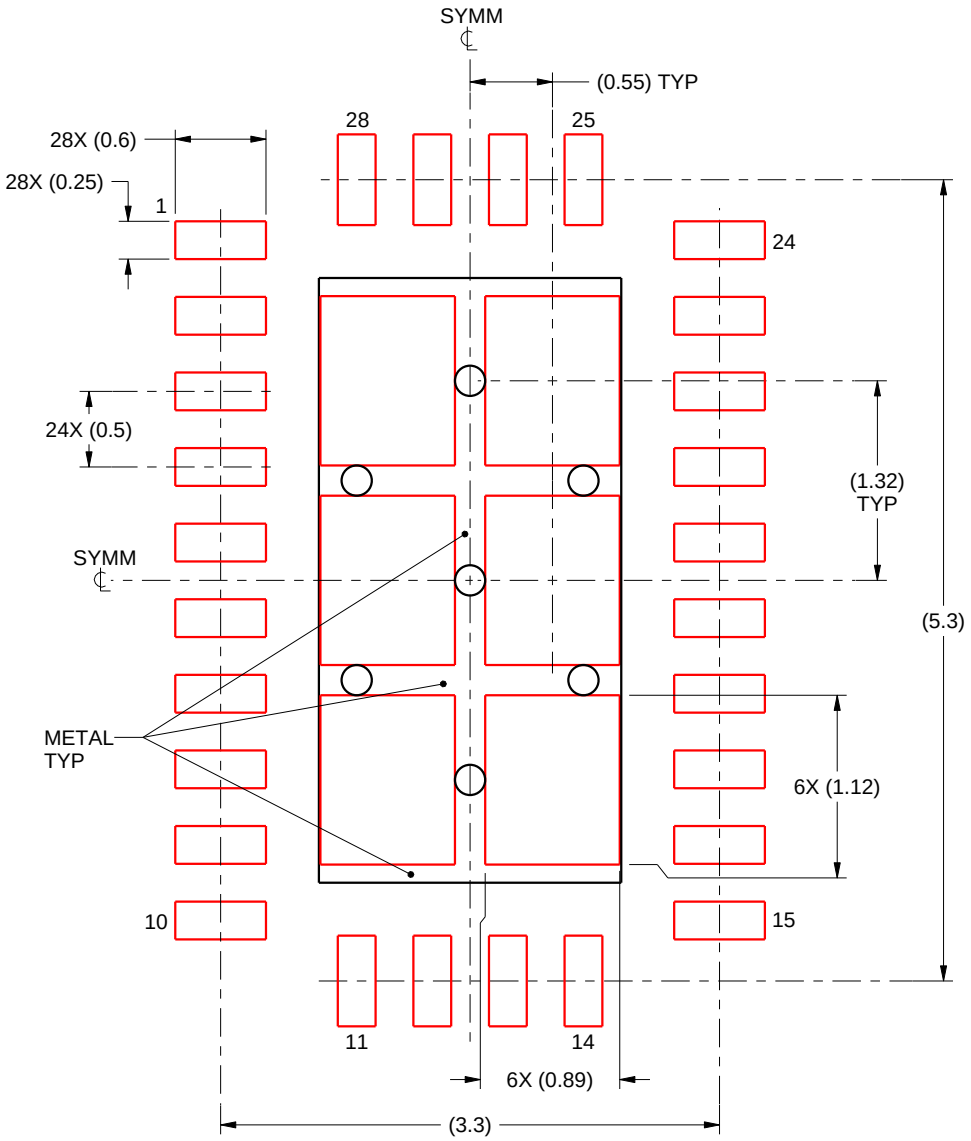


SOLDER MASK DETAILS

4219075/A 11/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219075/A 11/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated