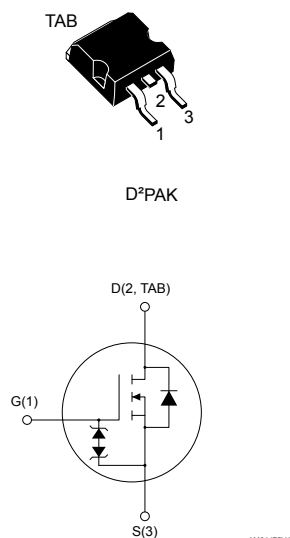


# N-channel 600 V, 115 mΩ typ., 25 A, MDmesh™ DM6 Power MOSFET in a D<sup>2</sup>PAK package



## Features

| Order code  | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> |
|-------------|-----------------|--------------------------|----------------|
| STB33N60DM6 | 600 V           | 128 mΩ                   | 25 A           |

- Fast-recovery body diode
- Lower R<sub>DS(on)</sub> per area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

## Applications

- Switching applications

## Description

This high-voltage N-channel Power MOSFET is part of the MDmesh™ DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge (Q<sub>rr</sub>), recovery time (t<sub>rr</sub>) and excellent improvement in R<sub>DS(on)</sub> per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

### Product status link

[STB33N60DM6](#)

### Product summary

|            |                    |
|------------|--------------------|
| Order code | STB33N60DM6        |
| Marking    | 33N60DM6           |
| Package    | D <sup>2</sup> PAK |
| Packing    | Tape and reel      |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter                                                         | Value      | Unit               |
|----------------|-------------------------------------------------------------------|------------|--------------------|
| $V_{GS}$       | Gate-source voltage                                               | $\pm 25$   | V                  |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$  | 25         | A                  |
|                | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$ | 16         | A                  |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                            | 80         | A                  |
| $P_{TOT}$      | Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$     | 190        | W                  |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                                 | 50         | V/ns               |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                                         | 100        | V/ns               |
| $T_{stg}$      | Storage temperature range                                         | -55 to 150 | $^{\circ}\text{C}$ |
| $T_J$          | Operating junction temperature range                              |            |                    |

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 25\text{ A}$ ,  $di/dt \leq 900\text{ A}/\mu\text{s}$ ,  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$
3.  $V_{DS} \leq 480\text{ V}$

**Table 2. Thermal data**

| Symbol              | Parameter                        | Value | Unit                        |
|---------------------|----------------------------------|-------|-----------------------------|
| $R_{thj-case}$      | Thermal resistance junction-case | 0.66  | $^{\circ}\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb  | 30    | $^{\circ}\text{C}/\text{W}$ |

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu.

**Table 3. Avalanche characteristics**

| Symbol   | Parameter                                                                                                              | Value | Unit |
|----------|------------------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )                                   | 4     | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 360   | mJ   |

## 2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

**Table 4. On/off states**

| Symbol        | Parameter                         | Test conditions                                                                                | Min. | Typ. | Max.    | Unit             |
|---------------|-----------------------------------|------------------------------------------------------------------------------------------------|------|------|---------|------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                                    | 600  |      |         | V                |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$                                                |      |      | 1       | $\mu\text{A}$    |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ ,<br>$T_C = 125\text{ }^{\circ}\text{C}^{(1)}$ |      |      | 100     | $\mu\text{A}$    |
| $I_{GSS}$     | Gate-body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$                                             |      |      | $\pm 5$ | $\mu\text{A}$    |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                             | 3.25 | 4    | 4.75    | V                |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 12.5\text{ A}$                                                 |      | 115  | 128     | $\text{m}\Omega$ |

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

| Symbol                     | Parameter                     | Test conditions                                                                                                                                 | Min. | Typ. | Max. | Unit     |
|----------------------------|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|----------|
| $C_{iss}$                  | Input capacitance             | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{GS} = 0\text{ V}$                                                                         | -    | 1500 | -    | pF       |
| $C_{oss}$                  | Output capacitance            |                                                                                                                                                 | -    | 115  | -    | pF       |
| $C_{rss}$                  | Reverse transfer capacitance  |                                                                                                                                                 | -    | 3    | -    | pF       |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$                                                                                     | -    | 225  | -    | pF       |
| $R_G$                      | Intrinsic gate resistance     | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$                                                                                                         | -    | 1.8  | -    | $\Omega$ |
| $Q_g$                      | Total gate charge             | $V_{DD} = 480\text{ V}$ , $I_D = 25\text{ A}$ ,<br>$V_{GS} = 0\text{ to }10\text{ V}$<br>(see Figure 14. Test circuit for gate charge behavior) | -    | 35   | -    | nC       |
| $Q_{gs}$                   | Gate-source charge            |                                                                                                                                                 | -    | 10   | -    | nC       |
| $Q_{gd}$                   | Gate-drain charge             |                                                                                                                                                 | -    | 15   | -    | nC       |

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions                                                                                                                                                                                                    | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 300\text{ V}$ , $I_D = 12.5\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$<br>(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | -    | 14   | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                                                                                                                    | -    | 9    | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |                                                                                                                                                                                                                    | -    | 7    | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                                                                                                                    | -    | 35   | -    | ns   |

**Table 7. Source drain diode**

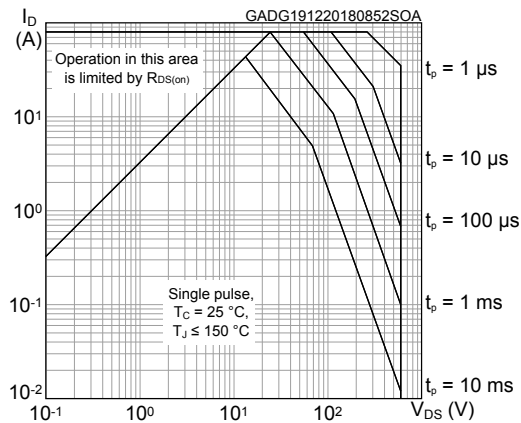
| Symbol          | Parameter                     | Test conditions                                                                                                                                                                                                    | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                                                                                    | -    |      | 25   | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                    | -    |      | 80   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $V_{GS} = 0\text{ V}$ , $I_{SD} = 25\text{ A}$                                                                                                                                                                     | -    |      | 1.6  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 25\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$<br>(see Figure 15. Test circuit for inductive load switching and diode recovery times)                                     | -    | 115  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                    | -    | 0.52 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                    | -    | 9    |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 25\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$<br>(see Figure 15. Test circuit for inductive load switching and diode recovery times) | -    | 210  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                    | -    | 1.68 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                    | -    | 16   |      | A             |

1. Pulse width is limited by safe operating area.

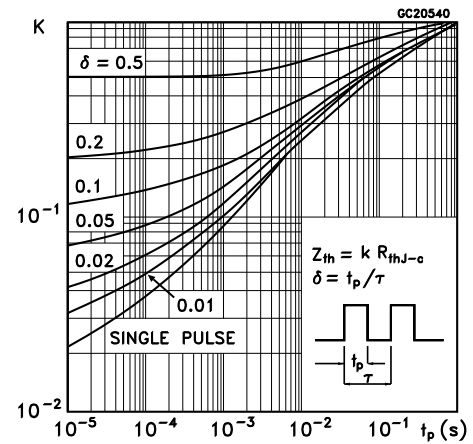
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

## 2.1 Electrical characteristics (curves)

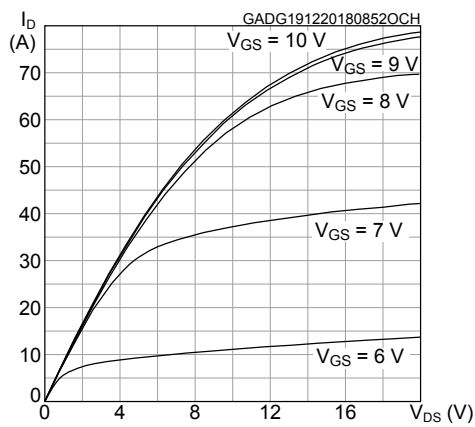
**Figure 1. Safe operating area**



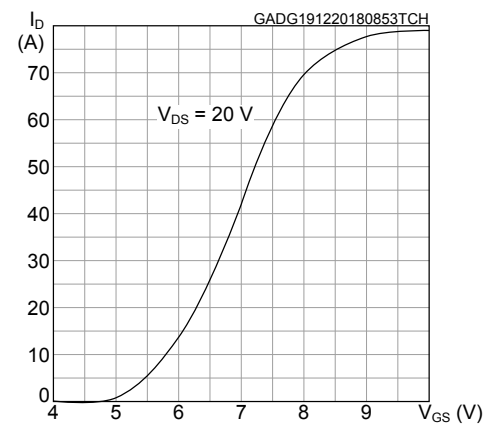
**Figure 2. Normalized thermal impedance**



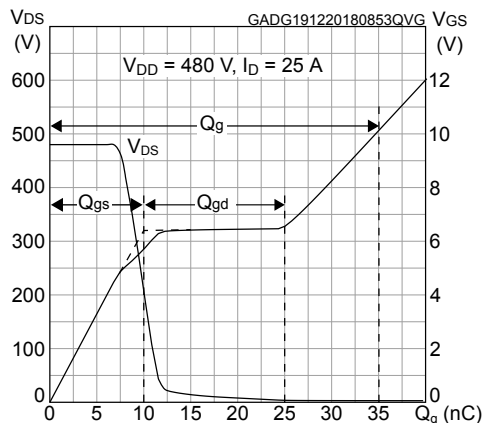
**Figure 3. Output characteristics**



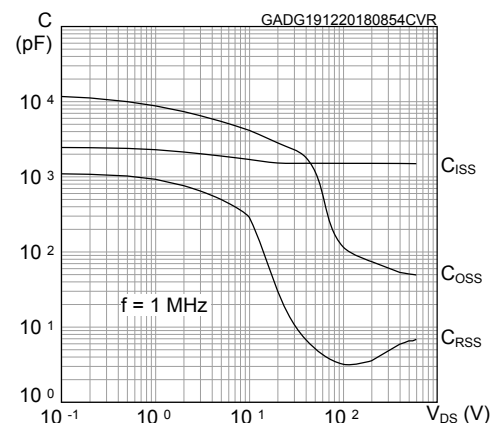
**Figure 4. Transfer characteristics**

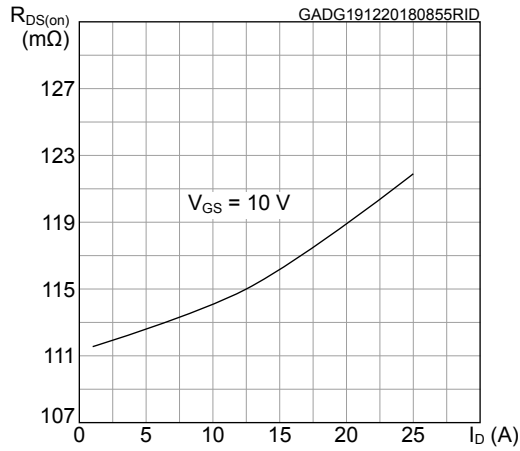
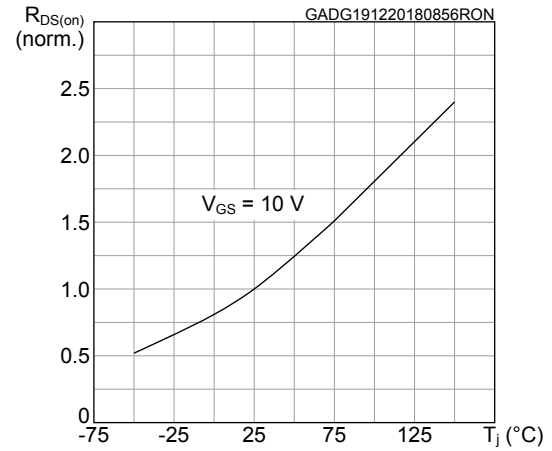
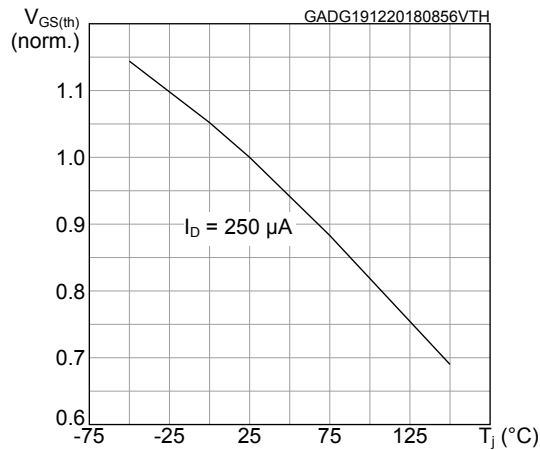
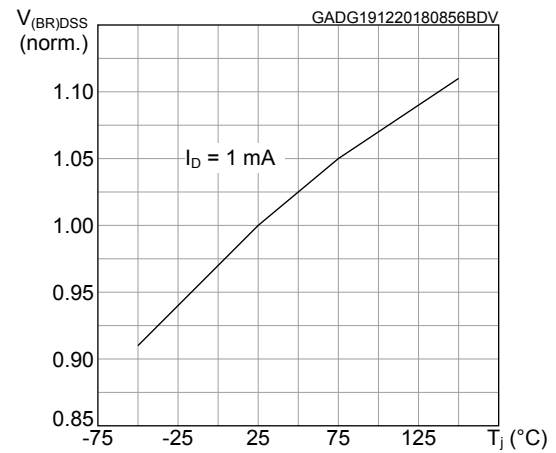
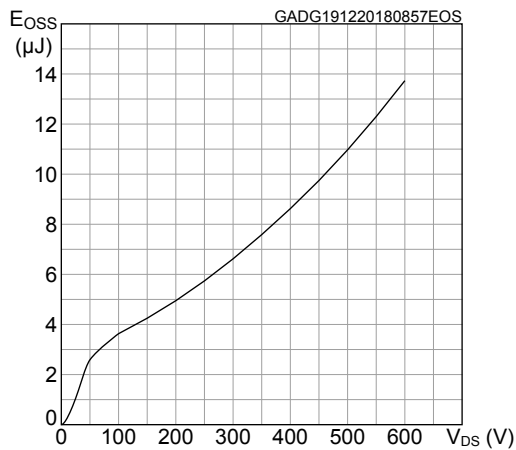
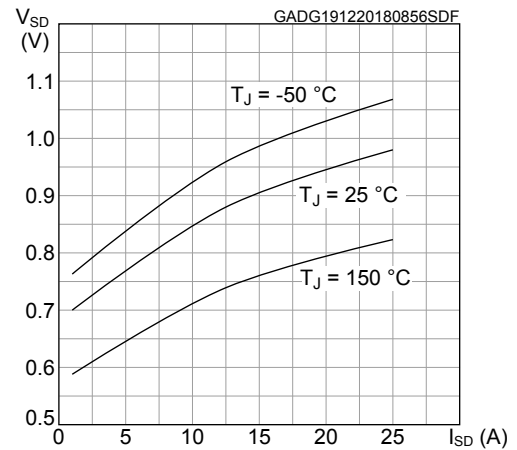


**Figure 5. Gate charge vs gate-source voltage**

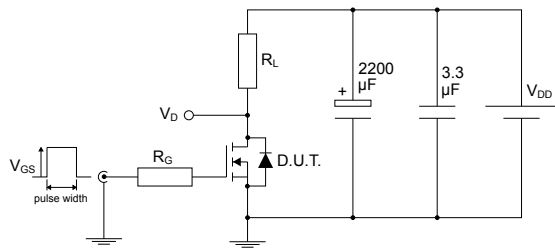


**Figure 6. Capacitance variations**

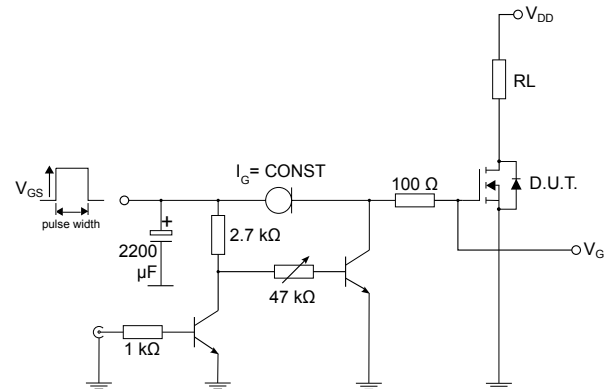


**Figure 7. Static drain-source on-resistance**

**Figure 8. Normalized on-resistance vs temperature**

**Figure 9. Normalized gate threshold voltage vs temperature**

**Figure 10. Normalized  $V_{(BR)DSS}$  vs temperature**

**Figure 11. Output capacitance stored energy**

**Figure 12. Source-drain diode forward characteristics**


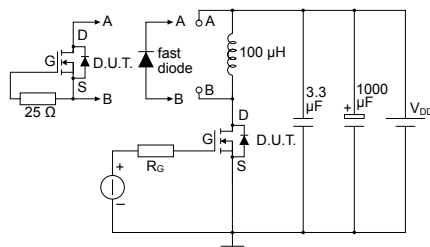
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


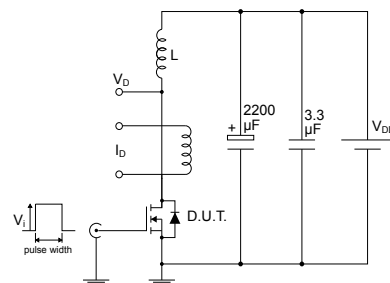
AM0146Bv1

**Figure 14. Test circuit for gate charge behavior**


AM0146Bv10

**Figure 15. Test circuit for inductive load switching and diode recovery times**


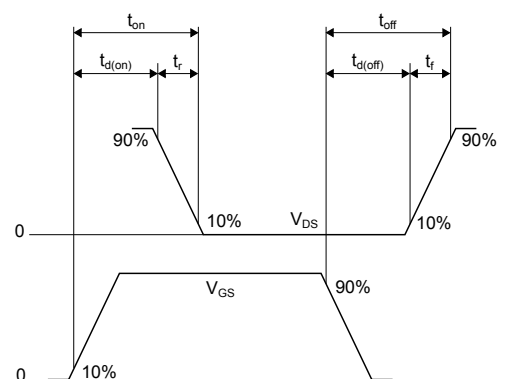
AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


AM01473v1

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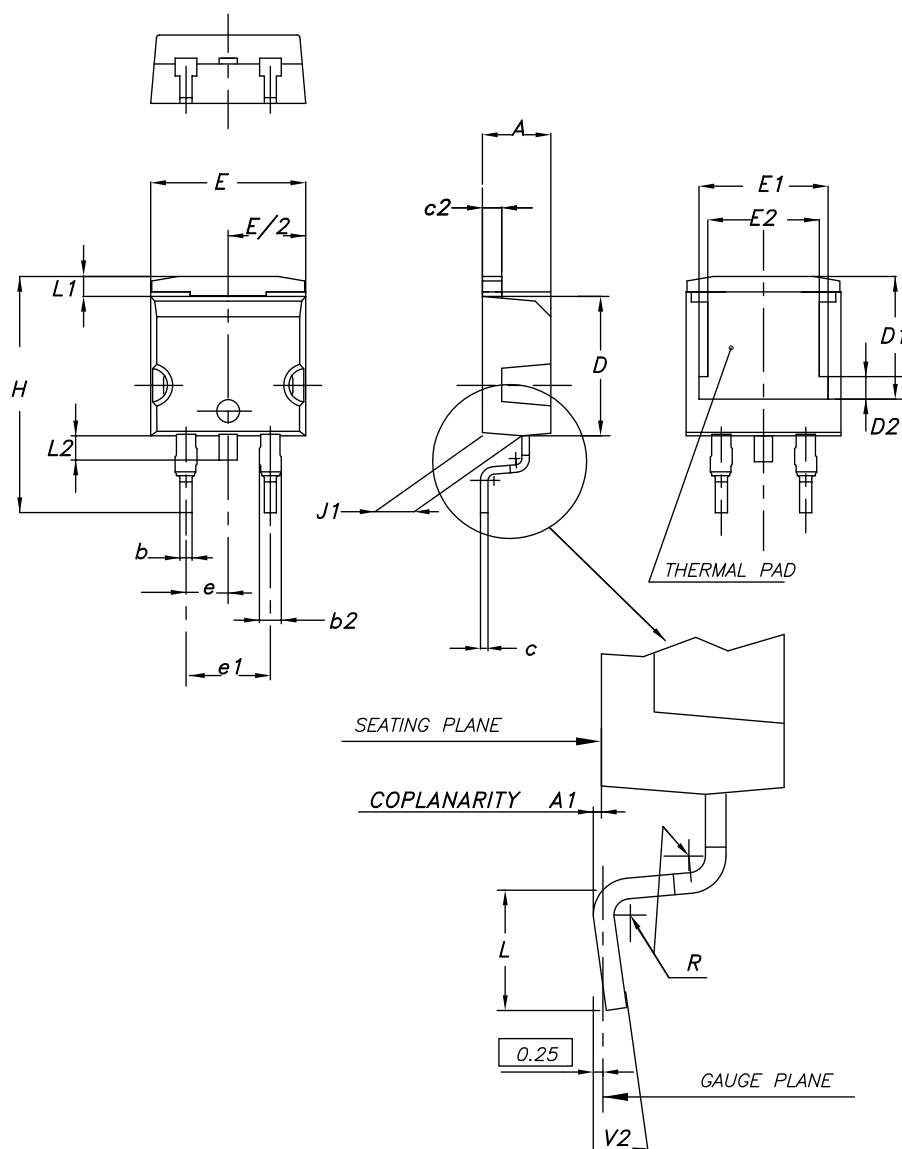
## 4 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

## 4.1 D<sup>2</sup>PAK (TO-263) type A2 package information

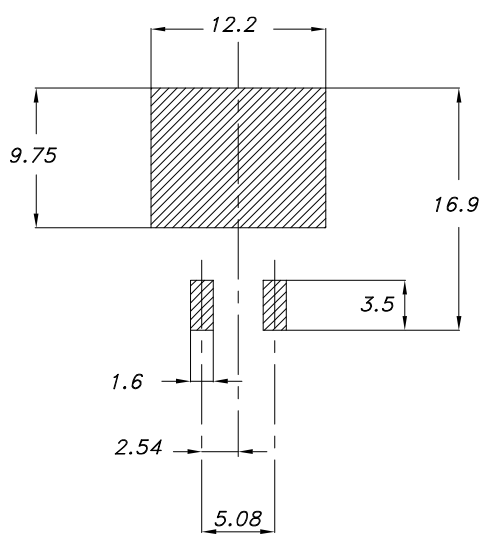
Figure 19. D<sup>2</sup>PAK (TO-263) type A2 package outline



0079457\_A2\_25

**Table 8. D<sup>2</sup>PAK (TO-263) type A2 package mechanical data**

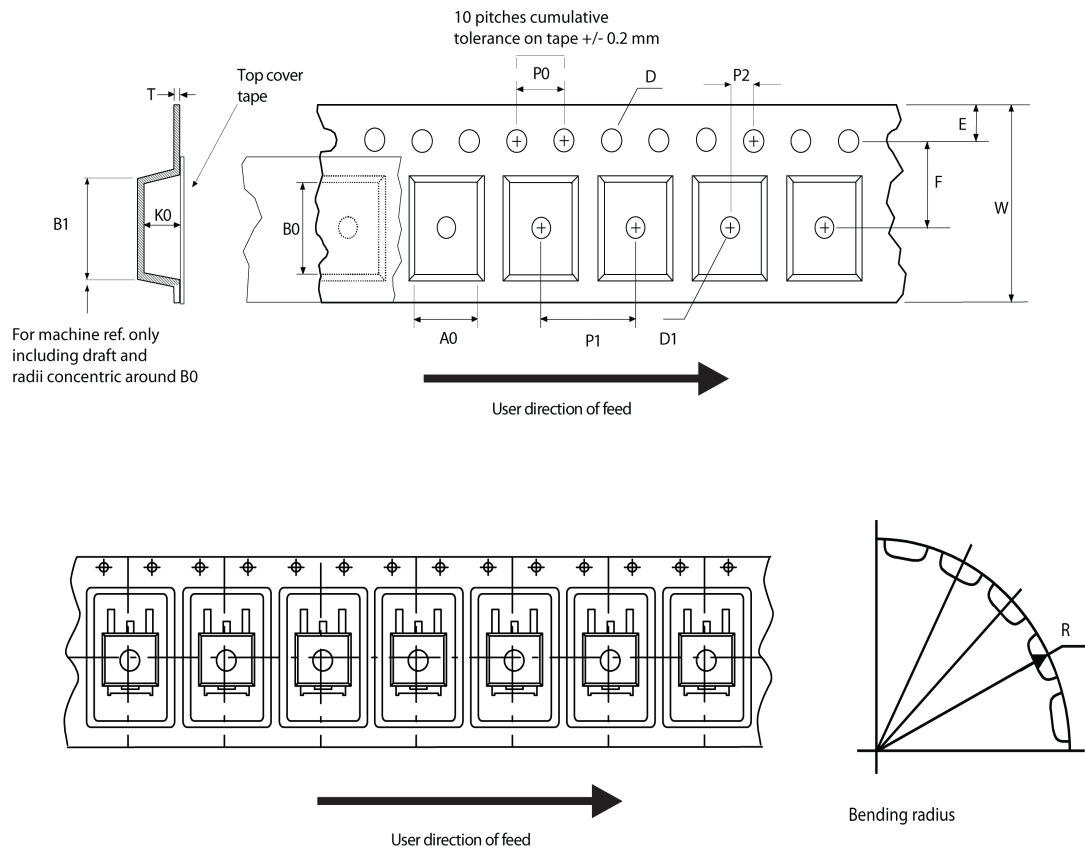
| Dim. | mm    |      |       |
|------|-------|------|-------|
|      | Min.  | Typ. | Max.  |
| A    | 4.40  |      | 4.60  |
| A1   | 0.03  |      | 0.23  |
| b    | 0.70  |      | 0.93  |
| b2   | 1.14  |      | 1.70  |
| c    | 0.45  |      | 0.60  |
| c2   | 1.23  |      | 1.36  |
| D    | 8.95  |      | 9.35  |
| D1   | 7.50  | 7.75 | 8.00  |
| D2   | 1.10  | 1.30 | 1.50  |
| E    | 10.00 |      | 10.40 |
| E1   | 8.70  | 8.90 | 9.10  |
| E2   | 7.30  | 7.50 | 7.70  |
| e    |       | 2.54 |       |
| e1   | 4.88  |      | 5.28  |
| H    | 15.00 |      | 15.85 |
| J1   | 2.49  |      | 2.69  |
| L    | 2.29  |      | 2.79  |
| L1   | 1.27  |      | 1.40  |
| L2   | 1.30  |      | 1.75  |
| R    |       | 0.40 |       |
| V2   | 0°    |      | 8°    |

**Figure 20. D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)**


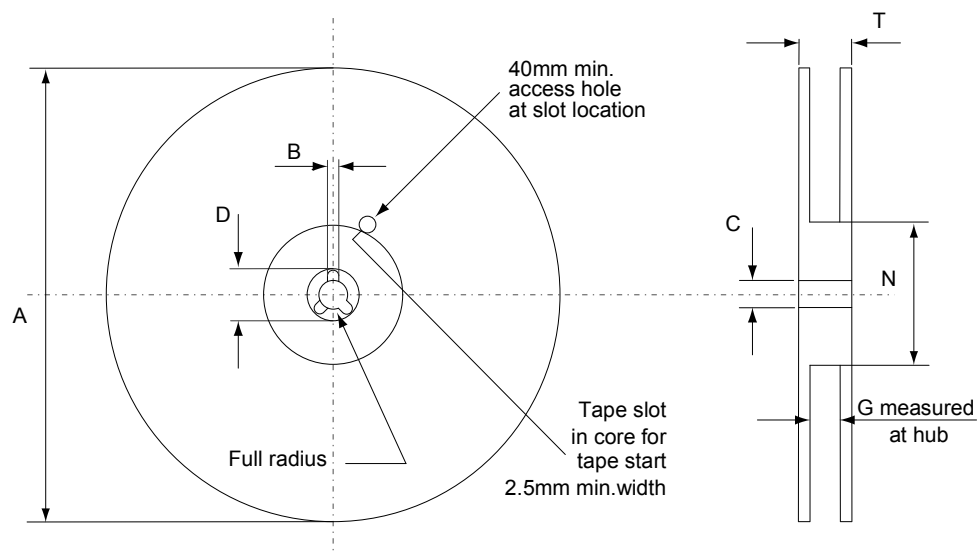
Footprint

## 4.2 D<sup>2</sup>PAK packing information

**Figure 21. D<sup>2</sup>PAK tape outline**



AM08852v1

**Figure 22. D<sup>2</sup>PAK reel outline**


AM06038v1

**Table 9. D<sup>2</sup>PAK tape and reel mechanical data**

| Tape |      |      | Reel          |      |      |
|------|------|------|---------------|------|------|
| Dim. | mm   |      | Dim.          | mm   |      |
|      | Min. | Max. |               | Min. | Max. |
| A0   | 10.5 | 10.7 | A             |      | 330  |
| B0   | 15.7 | 15.9 | B             | 1.5  |      |
| D    | 1.5  | 1.6  | C             | 12.8 | 13.2 |
| D1   | 1.59 | 1.61 | D             | 20.2 |      |
| E    | 1.65 | 1.85 | G             | 24.4 | 26.4 |
| F    | 11.4 | 11.6 | N             | 100  |      |
| K0   | 4.8  | 5.0  | T             |      | 30.4 |
| P0   | 3.9  | 4.1  |               |      |      |
| P1   | 11.9 | 12.1 | Base quantity |      | 1000 |
| P2   | 1.9  | 2.1  | Bulk quantity |      | 1000 |
| R    | 50   |      |               |      |      |
| T    | 0.25 | 0.35 |               |      |      |
| W    | 23.7 | 24.3 |               |      |      |

## Revision history

**Table 10. Document revision history**

| Date        | Version | Changes        |
|-------------|---------|----------------|
| 01-Feb-2019 | 1       | First release. |

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