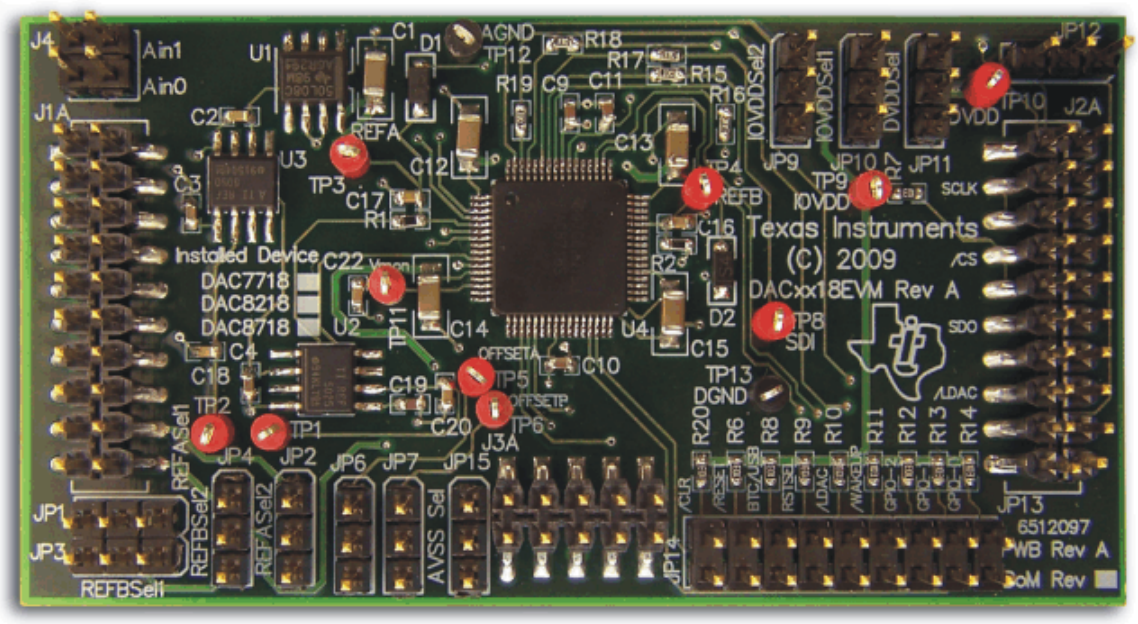
DAC8218EVM



DAC8218EVM

This user's guide describes the characteristics, operation, and use of the DAC8218EVM, an evaluation board for the DAC8218. The DAC8218 is a low-power, octal, 14-bit digital-to-analog converter (DAC). This device features low-power operation, good linearity, and low glitch. This evaluation module (EVM) allows evaluation of all aspects of the DAC8218 and gives control over every pin on the device. Complete circuit descriptions, schematic diagrams, and bills of material are included in this document.

The following related documents are available through the Texas Instruments web site at www.ti.com.

Related Documentation

Device	Literature Number
DAC8218	SBAS460
REF5025	SBOS410C
REF5050	SBOS410C
TL750L08	SLVS017T

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1 EVM Overview

1.1 Features

DAC8218EVM:

- Full-featured evaluation board for the DAC8218, a 14-bit, serial input, octal output digital-to-analog converter
- Onboard or external reference selection
- Configurable for single- or dual-supply operation
- Wide selection of digital and I/O voltages
- Hardware or software control of control logic

1.2 Introduction

The DAC8218 is a 14-bit, low-power, octal DAC that operates from independent AV_{DD}, AV_{SS}, and DV_{DD} supplies. It uses a high-speed serial peripheral interface, or SPI™ (up to 50MHz), to communicate with a DSP or a microprocessor using a compatible serial interface.

The DAC control logic can be controlled using onboard jumpers, or digitally through the J2 header.

The DAC8218EVM is designed for unipolar and bipolar (default) modes of operation. This flexibility allows for a wide range of supply voltages. Unipolar operation requires only a single analog voltage supply and bipolar operation requires two analog supplies.

The DAC8218EVM is an evaluation module built to the TI Modular EVM System specification. It can be connected to any modular EVM system interface card. The EVM ships in the TQFP-64 pin package.

Note that the DAC8218EVM has no microprocessor and cannot run software. To connect it to a computer, some type of interface is required.

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2 Analog Interface

For maximum flexibility, the DAC8218EVM can interface to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provides a 10-pin, dual-row, header at J1. This header provides access to the analog input and output pins of the DAC. An additional connector, J4, and test points are added to the evaluation module to allow access to all of the analog pins on the DAC. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options.

Table 1 summarizes the pinouts for analog interface J1.

Table 1. J1: Analog Interface Pinout

Pin Number	Signal	Description
J1.2	V_{OUT}-0	Analog output 0
J1.4	V_{OUT}-1	Analog output 1
J1.6	V_{OUT}-2	Analog output 2
J1.8	V_{OUT}-3	Analog output 3
J1.10	V_{OUT}-4	Analog output 4
J1.12	V_{OUT}-5	Analog output 5
J1.14	V_{OUT}-6	Analog output 6
J1.16	V_{OUT}-7	Analog output 7
J1.18	EXT-REFA	External reference source input for REF-A (V_{OUT}-0 to V_{OUT}-3)
J1.20	EXT-REFB	External reference source input for REF-B (V_{OUT}-4 to V_{OUT}-7)
J1.1-1.19 (odd)	GND	Analog ground connection

Table 2 summarizes the pinouts for analog interface J4.

Table 2. J4: Analog AIN Interface Pinout

Pin Number	Signal	Description
J4.2	AIN-0	Analog input 0
J4.4	AIN-1	Analog input 1
J4.1 and J1.3	GND	Analog ground connection

The analog interface is populated on the top and the bottom of the evaluation model. All of the output pins and the AIN-x pins are routed directly from the DAC8218 to the connector.

The GND pins of the DAC8218 are connected directly to the ground of the EVM board.

The DAC8218 has two auxiliary analog input pins, A_{IN}-0 and A_{IN}-1. These signals can be relayed to the V_{MON} output pin. Care must be taken to avoid overvoltage on these input pins. Make sure that the analog inputs do not exceed the Absolute Maximum Ratings found in the DAC8218 data sheet. The two A_{IN} pins can be accessed from the J4 header; see Table 2.

The DAC8218EVM has two external reference voltage options. J1.18 controls the external reference voltage for the REF-A input. J1.20 controls the reference for the REF-B input. When an external reference is used, jumpers JP1-JP4 must be configured properly. Test points TP3 and TP4 can be used to verify that the jumpers are configured properly and the correct reference voltage is applied to the DAC.

The output of the DAC8218 internal offset DAC is routed to test points TP5 and TP6. Jumpers JP6 and JP7 must be properly configured to route the OFFSET-A (TP5) and OFFSET-B (TP6) signals to the test points.

The V_{MON} output allows the user to relay any of the DAC outputs, as well as A_{IN}-0 or A_{IN}-1, to a single pin. V_{MON} is routed to test point TP11 and is connected to a 0.1µF capacitor.

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3 Digital Interface

The DAC8218EVM is a serial input data converter. The evaluation module is designed for interfacing to multiple control platforms.

3.1 Serial Data Interface

Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a 10-pin, dual-row, header/socket combination at J2. This header/socket provides access to the digital control and serial data pins from both J2A (top side) and J2B (bottom side) of the connector. The additional GPIO pins are connected to the JP13 header. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options.

Table 3 describes the serial interface pins.

Table 3. J2: Serial Interface Pins

Pin No.	Signal Name	I/O Type	Pull-Up	Function
J2.1, J2.7, J2.9	$\overline{CS}$	In	None	SPI bus chip select; pins are shorted together
J2.2	$\overline{CLR}$	In	High	Level trigger clear pin
J2.3, J2.5	SCLK	In	None	DAC8218 SPI clock; pins are shorted together
J2.4	DGND	In/Out	None	Digital ground
J2.6	$\overline{RESET}$	In	High	Input register reset
J2.8	BTC/USB	In	High	Data format for DAC input
J2.10	DGND	In/Out	None	Digital ground
J2.11	SDO/SDI	In/Out	None	DAC8218 SPI data in/out
J2.12	$\overline{WAKEUP}$	In	High	Wake up device from sleep mode
J2.13	Unused	—	—	—
J2.14	GPIO0	In/Out	High	DAC8218 GPIO0 signal
J2.15	$\overline{LDAC1}$	In	High	GPIO signal to control LDAC for DAC output latch update
J2.16	Unused	—	—	—
J2.17	$\overline{LDAC2}$	In	High	Alternate GPIO signal to control LDAC for DAC output latch update
J2.18	DGND	In/Out	None	Digital ground
J2.19	GPIO1	In/Out	High	DAC8218 GPIO1 signal
J2.20	Unused	—	—	—

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The SCLK signal and the $\overline{CS}$ signal can each be controlled by multiple pins on J2. Pins J2.3 and J2.5 have been shorted together to control SCLK. J2.1, 2.7 and J2.9 have been shorted together to control $\overline{CS}$.

Pins J2.2, J2.6, J2.8, J2.12, J2.14, J2.15, J2.17, and J2.19 have weak pull-up/-down resistors. These resistors provide default settings for many of the control pins. These signals can be controlled through the digital interface or jumpers found directly on the EVM. By default, these signals are pulled high through 10kΩ resistors. J2.1, J2.3, J2.5, J2.7, J2.9, J2.11 are the control line signals for the DAC8218. They are connected directly to the DAC through 33Ω resistors. The J2 header is the only way to access these pins. See the DAC8218 product data sheet for complete details on these pins.

The load DAC ($\overline{LDAC}$) pin is connected via jumper JP12 to either the J2.15 pin or the J2.17 pin. Updating the DAC registers can be completed in two different ways. First, the $\overline{LDAC}$ pin can be held low; in this approach, the input registers are immediately updated. Alternatively, the $\overline{LDAC}$ pin can be held high, and the DAC registers update when $\overline{LDAC}$ is taken low. By default, $\overline{LDAC}$ is pulled high through a 10kΩ resistor. A shunt can be placed across jumpers JP14.9 and JP14.10 to connect $\overline{LDAC}$ to the ground. See the DAC8218 data sheet for more information on updating the DAC.

GPIO signals GPIO0 and GPIO1 can be accessed at JP14 or the J2 header. GPIO2 can only be accessed at JP14. By default, these signals are each pulled high through a 10kΩ resistor. However, they can be tied to ground by vertically applying a shunt across the individual pins on JP14.

4 Power Supplies

Samtec part numbers SSW-105-22-F-D-VS-K and TSM-105-01-T-DV-P provide a 5-pin, dual-row, header/socket combination at J3. Table 4 lists the configuration details for J3. The voltage inputs to the DAC can be applied directly to the device. The DAC8218 requires multiple power supplies to operate. AV_{DD}, AV_{SS}, DV_{DD}, and IOV_{DD} are required to properly power the DAC. The power should be applied in the order: IOV_{DD}, DV_{DD}, then AV_{DD} and AV_{SS}, followed by reference voltage.

CAUTION

This sequence must be followed in order to prevent damage to the device.

Table 4. J3 Configuration: Power-Supply Input

Pin No.	Pin Name	Function	Required
J3.1	+VA	+4.75V to +24V analog supply	Yes
J3.2	–VA	-18V to -4.75V analog supply	Yes
J3.3	+5VA	+5V analog supply	No
J3.4	–5VA	–5V analog supply	No
J3.5	DGND	Digital ground input	Yes
J3.6	AGND	Analog ground input	Yes
J3.7	+1.8VD	1.8V digital supply	Optional
J3.8	VD1	Not used	No
J3.9	+3.3VD	3.3V digital supply	Optional
J3.10	+5VD	+5V	Optional

NOTE: To avoid damage to the DAC8218, DV_{DD} must stay greater than or equal to IOV_{DD}.

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The digital and analog ground inputs are short-circuited internally through a ground plane.

The digital supply voltage (DV_{DD}) for the DAC8218 is selectable between +5VD and +3.3VD via the JP11 jumper. Test point TP10 can be used to verify the digital supply voltage selected. Care must be taken to ensure that the EVM is not configured to be in a state where V_{REF} is greater than DV_{DD}. Diodes are put into place (D1 and D2) to add protection to the part.

The dc logic voltage for the DAC8218 (IOV_{DD}) is selectable between +5VD, +3.3 VD, or +1.8 VD using jumpers JP9 and JP10. These power-supply voltages are referenced to digital ground. Test point TP9 can be used to verify the selected IOV_{DD} voltage.

The DAC8218EVM is designed to work in either unipolar or bipolar mode. Each mode requires a different power-supply connection. In bipolar mode, AV_{SS} and AV_{DD} are powered through –VA and +VA directly. When unipolar mode is desired, JP15 allows AV_{SS} to be connected to the EVM board ground. AV_{DD} continues to be powered through +VA. Consult the DAC8218 data sheet for the restrictions on the power supplies for the two operating modes.

5 Voltage Reference

The DAC8218EVM has the ability to use two different reference voltages simultaneously for different output channels. REF-A and REF-B control the reference voltages for the DAC. Output channels V_{OUT}-0, V_{OUT}-1, V_{OUT}-2, and V_{OUT}-3 use REF-A as a reference. REF-B is used as a reference for output channels V_{OUT}-4, V_{OUT}-5, V_{OUT}-6, and V_{OUT}-7.

The evaluation module contains two different onboard reference sources and the option of using an external reference voltage. Jumpers JP1 through JP4 select the reference voltage from the REF5050(U3), REF5025(U2), or use an external reference. The REF5050 supplies 5.0V to the reference. The REF5025 supplies 2.5V to the reference. The outputs from the REF5025 and REF5050 can be accessed by test point TP1 and TP2, respectively. These reference voltages are additionally filtered through an RC filter before connected to the DAC8218. The TL751L08 is used to voltage regulate +VA to properly power the REF5025 and REF5050.

Jumpers JP2 (REF-A) and JP4 (REF-B) select between using an onboard reference or an external reference. If an onboard reference is selected, jumpers JP1 (REF-A) and JP3 (REF-B) are used to select between the 2.5V or the 5.0V reference. Pins J1.18 (REF-A) and J1.20 (REF-B) on header J1 are used to input an external reference. The reference voltages applied to the DAC can be observed at test points TP3 (REF-A) and TP4 (REF-B).

Note that if an external reference voltage is input to J1.18 or J1.20, it will be filtered through a RC filter with an 8Hz cutoff frequency. If the user desires to input his own reference signal without this filter, he can do so by connecting the reference signal directly to TP3 or TP4.

Figure 1 illustrates the reference test points.

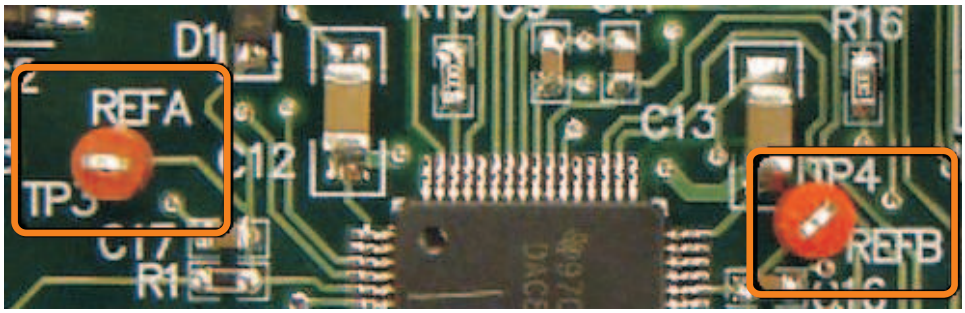


Figure 1. Reference Test Points

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6 EVM Operation

This section provides information on the analog input, digital control, and general operating conditions of the DAC8218EVM.

6.1 Analog Output

The DAC8218 has eight analog outputs that are available through the J1 header. Each of these output are referenced to the board ground.

The OFFSET-A and OFFSET-B analog outputs are routed to TP5 and TP6. The OFFSET feature can only be used in bipolar mode. A shunt must be placed across pins 1 and 2 to view the output on the test points. The pins must be shorted directly to ground for unipolar/single-supply operation. For this mode, apply shunts across pins 2 and 3 of JP6 and JP7 to short the OFFSET-A/-B pins to ground.

V_{MON} is the channel monitor output. It can relay any of the eight analog output signals, the OFFSET-A/-B, the Ref Buffer A/B, or either of the two A_{IN} signals. The output pin has a 0.1µF capacitor connected. By default, the V_{MON} pin is in 3-state mode.

6.2 Digital Control

The digital control signals can be applied directly to J1 (top or bottom side). The DAC8218EVM can also be connected directly to a DSP or microcontroller interface board.

No specific evaluation software is provided with this EVM; however, various code examples are available that show how to use this EVM with a variety of digital signal processors from Texas Instruments. Please check the specific device product folders or send an e-mail to dataconvapps@list.ti.com for a listing of available code examples. The EVM Gerber files are also available on request.

6.3 Default Jumper Settings and Switch Positions

The DAC8218EVM has the ability to operate in either bipolar or unipolar mode. The proper jumper conditions depend on which mode the evaluation module operates in. Table 5 summarizes the jumpers found on the EVM.

Table 5. DAC8218EVM Jumpers

Jumper	Name	Description
JP1	REFASel1	Reference A: Select between 2.5V and 5.0V onboard reference voltage
JP2	REFASel2	Reference A: Select between using the onboard ref (from JP1) or an external reference
JP3	REFBSel1	Reference B: Select between 2.5V and 5.0V onboard reference voltage
JP4	REFBSel2	Reference B: Select between using the onboard reference (from JP3) or an external ref
JP6	OFFSETA	OFFSET DAC A
JP7	OFFSETB	OFFSET DAC B
JP9	IOVDDSel2	IOV_{DD}: Select between 1.8V or the result from IOVDDSel1 (JP10)
JP10	IOVDDSel1	Routes 5.0V or 3.3V to JP9
JP11	DVDDSel	DV_{DD}: Select between 5.0V and 3.3V
JP12	LDAC Selection	Routes $\overline{LDAC}$ pin to either J2.15 or J2.17
JP14	Digital	Digital control pins: Pulled high by default; apply shunt to tie pins to ground
JP15	AVSS Sel	Tie AVSS to J3.1

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Figure 2 and Figure 3 show the default jumper conditions for bipolar and unipolar modes, respectively.

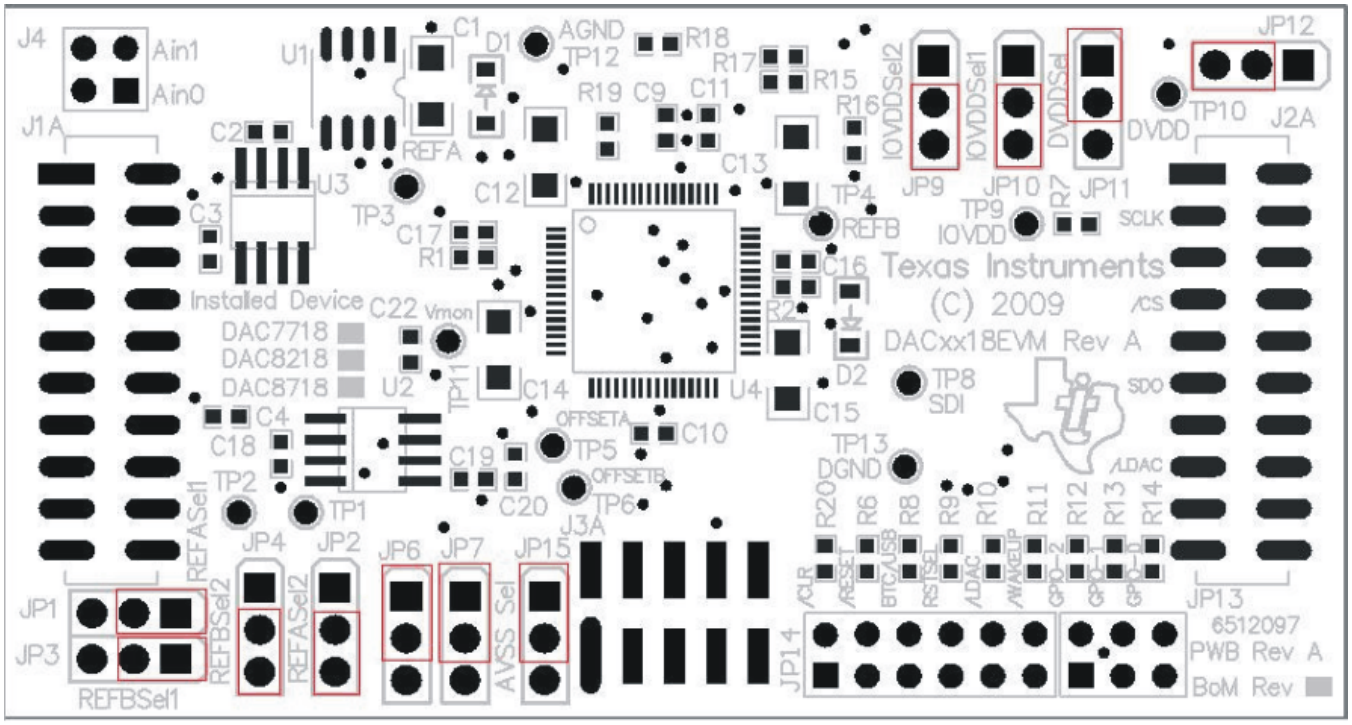


Figure 2. DAC8218EVM Default Jumper Locations for Bipolar Mode

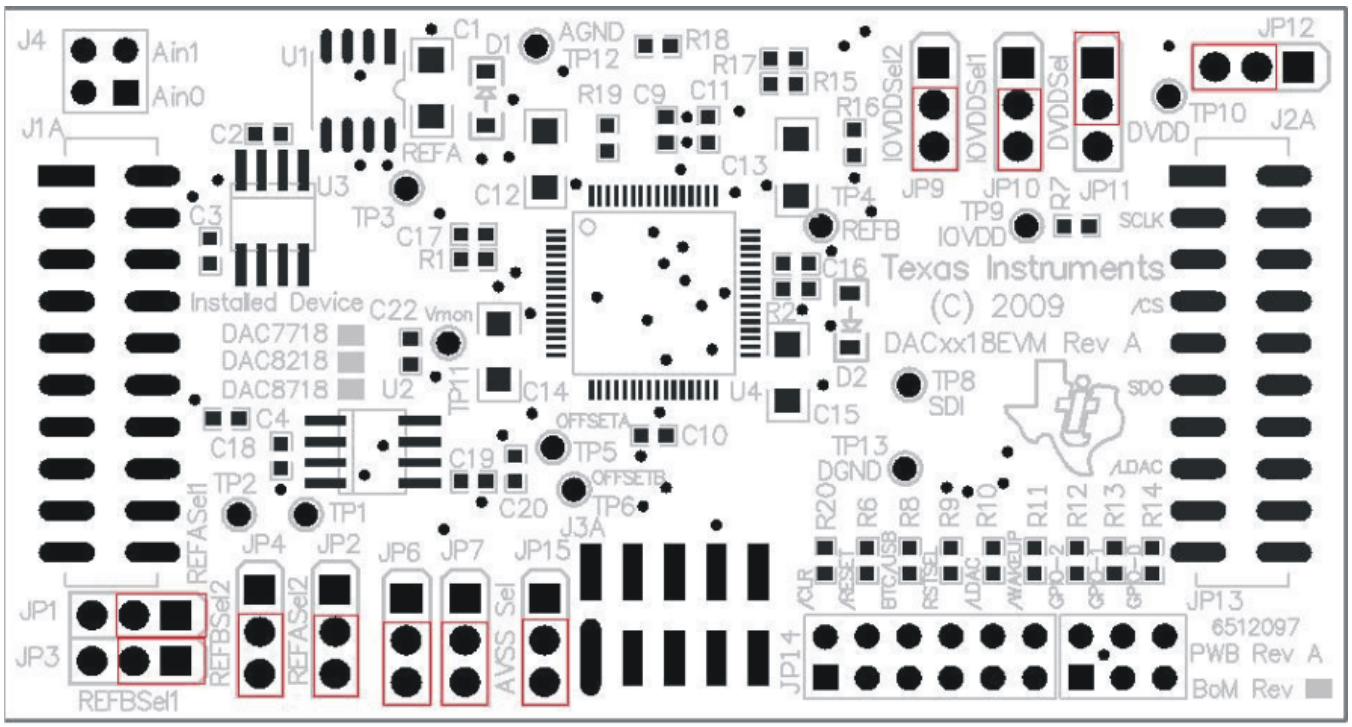


Figure 3. DAC8218EVM Default Jumper Locations for Unipolar Mode

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Jumpers JP1 and JP2 are used to control the reference voltage for group A. JP1 is selectable by connecting a jumper across pins 1 and 2 (2.5V) or 2 and 3 (5.0V). By default, a jumper is placed across pins 1 and 2 to enable the 2.5V reference. JP2 selects whether to use the onboard reference selected by JP1 (shunt pins 2 and 3) or use an external reference (shunt pins 1 and 2) from pin J1.18.

Jumper JP3 and JP4 are used to control the reference voltage for group B. JP3 is selectable by connecting a jumper across pins 1 and 2 (2.5V) or 2 and 3 (5.0V). By default, a jumper is placed across pins 1 and 2 to enable the 2.5V reference. JP4 selects whether to use the onboard reference selected by JP3 (shunt pins 2 and 3) or use an external reference (shunt pins 1 and 2) from pin J1.20. By default, the EVM is set to use the onboard 2.5V reference for REF-A and REF-B.

Jumpers JP6 and JP7 control the output signals OFFSET-A and OFFSET-B, respectively. When the evaluation board is used in unipolar mode, pins 2 and 3 (on JP6 and JP7) must be shorted together to connect OFFSET-A and OFFSET-B to ground. When the EVM board is used in bipolar mode, the shunt must be applied across pins 1 and 2 on the jumpers (default mode). The OFFSET-A and OFFSET-B signals are now routed to TP5 and TP6.

JP9 and JP10 set the IOV_{DD} for the DAC8218. The IOV_{DD} is selectable between 1.8V, 3.3V, or 5.0V. Jumper JP10 selects between 5.0V (shunt pins 1 and 2) or 3.3V (shunt pins 2 and 3). JP9 selects between the result from JP10 (shunt pins 2 and 3) or 1.8V (shunt pins 1 and 2). By default, IOV_{DD} is set to 3.3V. See the schematic (appended to the end of this document) for more information.

Jumper JP11 selects the DV_{DD} voltage. Shunting pins 1 and 2 enable DV_{DD} to be 5.0V (default). Shunting pins 2 and 3 set DV_{DD} to 3.3V.

Jumper JP12 selects where to route the $\overline{LDAC}$ signal. By default, pins JP12.2 and JP12.3 are connected to route the $\overline{LDAC}$ signal to J2.15. The shunt can be placed across JP12.1 and JP12.2 to route the $\overline{LDAC}$ signal to J2.17.

The DAC8218 digital control inputs can be accessed through JP14 or the J2 header. $\overline{CLR}$, $\overline{RESET}$, BTC/USB, $\overline{WAKEUP}$, and $\overline{LDAC}$ are all initially pulled high to IOV_{DD} through 10kΩ resistors. These signals can be tied to ground by applying a shunt across the corresponding pins on J14 or through the J2 header.

JP14 is also used to access the GPIO signals. By default, all of the signals are pulled high to IOV_{DD} through 10kΩ resistors. Placing a shunt vertically across the corresponding GPIO pin ties the GPIO signal to ground. GPIO-0 and GPIO-1 can also be controlled through the J2 header.

JP15 is the AV_{SS} selection for the DAC. AV_{SS} can be connected to ground (shunt pins 2 and 3) for unipolar operation mode or pin J3.1 (shunt pins 1 and 2) for bipolar operation. In bipolar mode, a voltage can be applied to J3.1 to power the AV_{SS} of the DAC8218.

7 Schematics and Layout

Schematics for the DAC8218EVM are appended to this user's guide. The bill of materials is provided in Table 6.

7.1 Bill of Materials

NOTE: All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, see the TI web site.)

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Table 6. DAC8218EVM Bill of Materials[1]

Item No.	Qty	Ref Des	Description	Manufacturer	Mfr Part Number
1	5	C1, C12, C13, C14, C15	Capacitor, ceramic, 10µF, 25V X5R 1206 10%	Panasonic	ECJ-3YB1E106K
2	2	C2, C22	Capacitor, ceramic, 0.1µF, 16V 0603 X7R 10%	Panasonic	ECJ-1VB1C104K
3	6	C3, C9, C10, C11, C18, C19	Capacitor, ceramic, 1.0µF, 16V X5R 10% 0603	TDK	C1608X5R1C105K
4	4	C4, C16, C17, C20	Capacitor, ceramic, 10µF, 10V 0603 X5R 20%	Panasonic	ECJ-1VB1A106M
5	2	D1, D2	Diode, Schottky, 40V, 350MA SOD123	Micro Commercial Co	SD103AW-TP
6	2	J1A, J2A (Top Side)	10-pin, dual row, SM Header (20 Pos.)	Samtec	TSM-110-01-T-DV-P
7	2	J1B, J2B (Bottom Side)	10 socket dual row, SM Header (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
8	1	J3A (Top Side)	5-pin, dual row, SM Header (10 Pos.)	Samtec	TSM-105-01-T-DV-P
9	1	J3B[2] (Bottom Side)	5 Socket, dual row, SM Header (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
10	1	J4	Header strip, 4 pin (2x2)	Samtec	TSW-102-07-L-D
11	11	JP1, JP2, JP3, JP4, JP6, JP7, JP9, JP10, JP11, JP12, JP15	Header strip, 3 pin (1x3)	Samtec	TSW-103-07-L-S
12	1	JP13	Header strip, 6 pin (2x3)	Samtec	TSW-103-07-L-D
13	1	JP14	Header strip, 12 pin (2x6)	Samtec	TSW-106-07-L-D
14	2	R1, R2	Resistor, 2.00kΩ 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF2001V
15	10	R6, R7, R8, R9, R10, R11, R12, R13, R14, R20	Resistor, 10kΩ 1/10W 5% 0603 SMD	Yageo	RC0603JR-0710KL
16	5	R15, R16, R17, R18, R19	Resistor, 33Ω 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ330V
17	10	TP1, TP2, TP3, TP4, TP5, TP6, TP8, TP9, TP10, TP11	Test Point - Single .025-pin, Red	Keystone	5000
18	2	TP12, TP13	Test Point - Single .025-pin, Black	Keystone	5001
19	1	U1	Single output, 8V voltage regulator	Texas Instruments	TL750L08CD
20	1	U2	Precision voltage reference 2.5V	Texas Instruments	REF5025AID
21	1	U3	Precision voltage reference 5.0V	Texas Instruments	REF5050AID
22	1	U4	Octal, 14-bit, High-Accuracy DAC, TQFP Package	Texas Instruments	DAC8218SPAG

(1) Manufacturer and part number for items may be substituted with electrically equivalent items.
(2) J3B parts are not shown in the schematic diagram. J3B is installed on the bottom side of the PWB opposite to J3A.

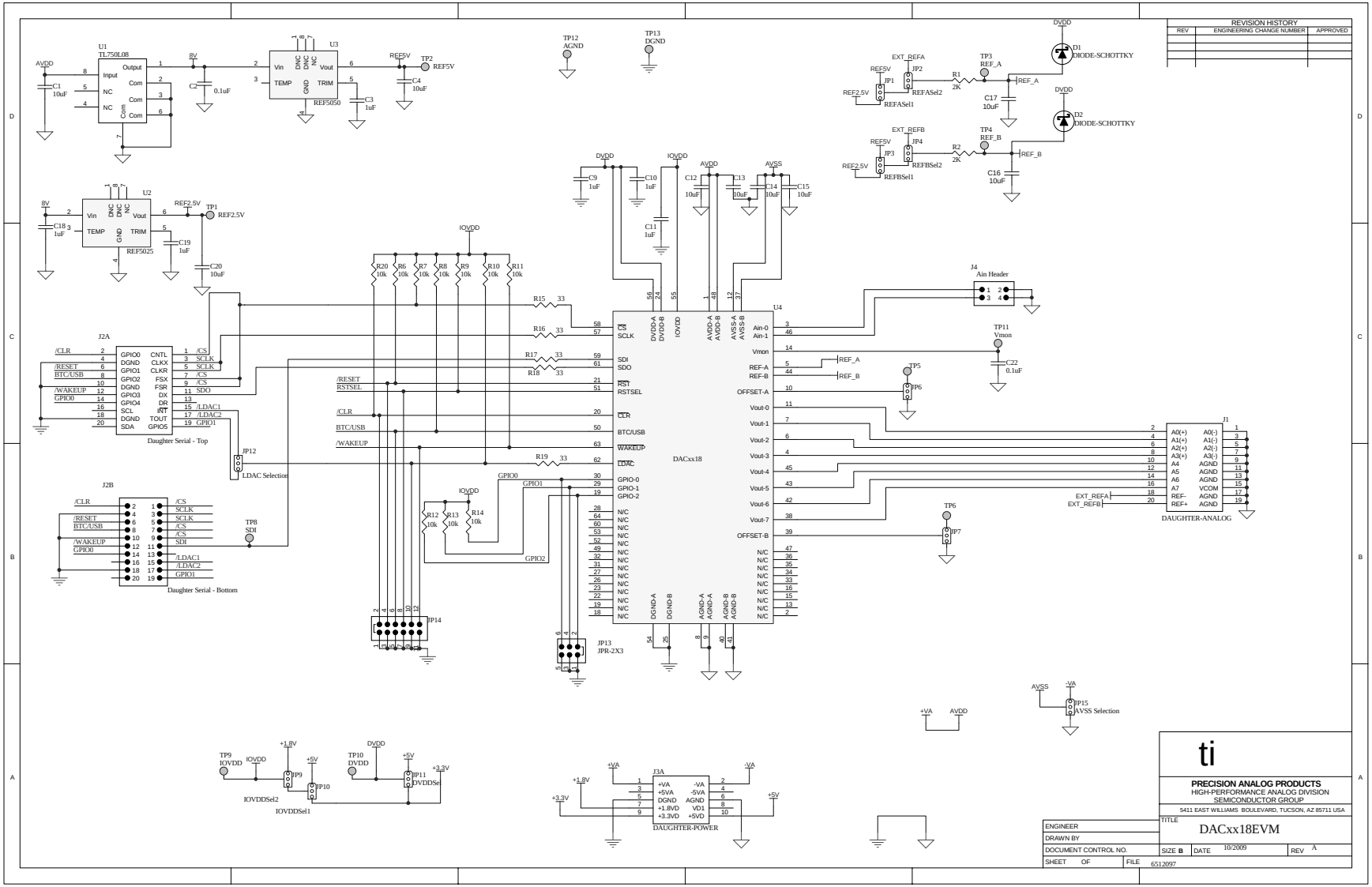
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Revision History

Changes from Original (February, 2010) to A Revision	Page
• Updated Table 4	5

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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REVISION HISTORY
REV
ENGINEERING CHANGE NUMBER
APPROVED
U1
TL750L08
U2
REF5025
U3
REF5050
U4
DACxx18
J1
DAUGHTER-ANALOG
J2A
Daughter Serial - Top
J2B
Daughter Serial - Bottom
J3A
DAUGHTER-POWER
J4
Ain Header
JP12
LDAC Selection
JP13
JPR-2X3
JP14
JP15
AVSS Selection
IOVDDSel1
IOVDDSel2
REFASel1
REFASel2
REFBSel1
REFBSel2
D1
DIODE-SCHOTTKY
D2
DIODE-SCHOTTKY
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During normal operation, some circuit components may have case temperatures greater than +30° C. The EVM is designed to operate properly with certain components above +60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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