

MAX14662

Beyond-the-Rails 8 x SPST

General Description

The MAX14662 is a serially controlled 8 x SPST switch for general purpose signal switching applications. The number of switches makes the device useful in a wide variety of applications while serial control maximizes flexibility with minimal pins. This part features Beyond-The-Rails™ capability so that $\pm 5.5\text{V}$ signals can be passed with any single supply between +1.6V and +5.5V.

The serial control is selectable between I²C and SPI. Both modes provide individual control of each independent switch so that any combination of switches can be applied. I²C mode provides two address select pins allowing for addressing up to four devices on a single bus. The SPI mode includes a DOUT pin that can be used to chain multiple devices together with a single select signal.

The MAX14662 is available in a 28-pin (4mm x 4mm) TQFN package and is specified over the -40°C to +85°C extended temperature range. The A₋ and B₋ pins provide $\pm 15\text{kV}$ Human Body Model (HBM) ESD protection.

Applications

- Audio Switching/Multiplexing
- Port Protection
- Power Management

Beyond-the-Rails™ is a trademark Maxim Integrated Products, Inc.

Features and Benefits

- 8 x SPST Switch
- Serial Control
 - I²C with Two Address-Select Pins
 - SPI with DOUT for Daisy Chain
 - Independent Control of Each Switch
- Beyond-the-Rails
 - $\pm 5.5\text{V}$ Signal Range Independent of Supply Voltage
- Low Distortion Switching
 - Total Harmonic Distortion + Noise 0.001% (typ)
 - R_{ON} Flatness 0.5m Ω (typ) Across Complete Signal Range
- Wide Supply Range
 - +1.6V to +5.5V Single Supply
- 0.425 Ω R_{ON} (typ)
- Compact Package
 - 4mm x 4mm, 28-Pin TQFN
- $\pm 15\text{kV}$ HBM ESD Protection on all A₋ and B₋ Pins

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX14662.related.

Ordering Information appears at end of data sheet.

Absolute Maximum Ratings

(All voltages referenced to GND.)

V_{CC}	-0.3V to +6.0V
$\overline{CS}/AD0$, $DOUT/AD1$, $SCLK/SCL$, DIN/SDA , $\overline{SD}$	-0.3V to +6.0V
SPI/I^2C	-0.3V to min ($V_{CC} + 0.3V$, 6V)
A_- , B_-	-6.0V to +6.0V
Continuous Current (A_- or B_- to any switch)	$\pm 200mA$
Peak Current (A_- or B_- to any switch) (pulsed at 1ms, maximum 10% duty cycle)	$\pm 400mA$

Continuous Power Dissipation	
28 TQFN (derate 28.6mW/°C above +70°C)	2285.7mW
Operating Temperature Range	-40°C to +85°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Package Thermal Characteristics (Note 1)

Junction-to-Case Thermal Resistance (θ_{JC})

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA})

TQFN

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

($V_{CC} = +1.6V$ to $+5.5V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Range	V _{CC}		1.6		5.5	V
Power-Supply Rejection Ratio	PSRR	R _A = R _B = 50Ω, V _{CC} = +3.3V ±0.1V, f = 10kHz		80		dB
V _{CC} Supply Current	I _{CC}	V _{CC} = +3.3V, all switches on		300	525	μA
		V _{CC} = +3.3V, 2 switches on		150	250	
		V _{CC} = +3.3V, $\overline{SD}$ = 0		0.01	1	
ANALOG SWITCH						
Analog Signal Range	V _{A-} , V _{B-}		-5.5		+5.5	V
On-Resistance	R _{ON}	V _{CC} > +1.8V		0.425	1	Ω
On-Resistance Match between Channels	ΔR _{ON}	V _{CC} = 3.3V		0.02		Ω
On-Resistance Flatness	R _{FLAT}	V _{CC} = 3.3V, I _{B-} = 10mA, V _{B-} = -5.5V to +5.5V		0.005		Ω
A ₋ , B ₋ Off-Leakage Current	I _{OFF}	V _{CC} = 3.3V, switch open, V _{A-} = -5.5V, +5.5V, V _{B-} = +5.5V, -5.5V, unconnected. See Figure 1. (Note 3)	-50		+50	nA
A ₋ , B ₋ On-Leakage Current	I _{ON}	V _{CC} = 3.3V, switch closed, V _{A-} = V _{B-} = ±5.5V See Figure 1. (Note 3)	-125		+125	nA

Electrical Characteristics (continued)

($V_{CC} = +1.6V$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$, $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Turn-Off Time	t_{OFF}	$V_{A_}$ or $V_{B_} = 3.0V$, $R_L = 100\Omega$, $C_L = 33pF$, open $A_$ & $B_$ together, see Figure 2.		5.5		μs
Break-Before-Make Time	t_{BBM}	$V_{A_}$ or $V_{B_} = 3.0V$, $R_L = 100\Omega$, $C_L = 33pF$, see Figure 2. (Note 4)	0			μs
Turn-On Time	t_{ON}	$V_{CC} = 3.3V$, $V_{A_}$ or $V_{B_} = 3.0V$, $R_L = 100\Omega$, $C_L = 33pF$, see Figure 2.			35	μs
		$V_{CC} = 1.6V$, $V_{A_}$ or $V_{B_} = 3.0V$, $R_L = 100\Omega$, $C_L = 33pF$, see Figure 2.			60	μs
Enable Time	t_{EN}	Time from when $\overline{SD}$ pin goes high to when the device is ready to listen for I ² C/SPI communications			300	μs
-3dB Bandwidth	BW	$R_S = R_L = 50\Omega$, $V_{B_} = 0.60V_{P-P}$. See Figure 3.		400		MHz
Total Harmonic Distortion Plus Noise	THD + N	$f = 20Hz$ to $20kHz$, $V_{A_}$ or $V_{B_} = 0.50V_{P-P}$, $R_S = R_L = 50\Omega$, DC bias = 0, see Figure 3.		0.001		%
Off-Isolation	V_{ISO}	$R_S = R_L = 50\Omega$, $V_{A_}$ or $V_{B_} = 0.60V_{P-P}$, $f = 1MHz$, see Figure 3.		-40		dB
Crosstalk	V_{CT}	$R_S = R_L = 50\Omega$, $V_{A_}$ or $V_{B_} = 0.60V_{P-P}$, $f = 1MHz$, see Figure 3.		-80		dB
Thermal Shutdown	T_{SDW}			150		$^{\circ}C$
Thermal Hysteresis	T_{HYST}			30		$^{\circ}C$
SPI TIMING CHARACTERISTICS (See Figure 10)						
SCLK Clock Period	$t_{CH} + t_{CL}$		95			ns
SCLK Pulse-Width High	t_{CH}		35			ns
SCLK Pulse-Width Low	t_{CL}		45			ns
$\overline{CS}$ Fall to SCLK Rise Time	t_{CSS}		15			ns
DIN Hold Time	t_{DH}		15			ns
DIN Setup Time	t_{DS}		15			ns
Output Data Propagation Delay	t_{DO}	$C_L = 15pF$, $V_{CC} \geq 2.7V$			40	ns
		$C_L = 15pF$, $V_{CC} < 2.7V$			80	
DOUT Rise and Fall Times	t_{FT}	$C_L = 15pF$		10		ns
$\overline{CS}$ Hold Time	t_{CSH}		60			ns

Electrical Characteristics (continued)

($V_{CC} = +1.6V$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$, $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C TIMING (See Figure 4)						
I ² C Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			μs
START Condition Setup Time	$t_{SU:STA}$		0.6			μs
START Condition Hold Time	$t_{HD:STA}$		0.6			μs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			μs
Clock Low Period	t_{LOW}		1.3			μs
Clock High Period	t_{HIGH}		0.6			μs
Data Valid to SCL Rise Time	$t_{SU:DAT}$	Write setup time	100			ns
Data Hold Time to SCL Fall	$t_{HD:DAT}$	Write hold time	0			ns
DIGITAL I/O						
Input Logic-High Voltage	V_{IH}		1.4			V
Input Logic-Low Voltage (DIN/SDA, SCLK/SCL, $\overline{CS}/AD0$)	V_{IL_FAST}				0.5	V
Input Logic-Low Voltage (DOUT/AD0, AD1, $\overline{SD}$)	V_{IL_SLOW}				0.4	V
Input Leakage Current	I_{IN}		-1		+1	μA
SPI/ $\overline{I^2C}$ I ² C Threshold	V_{I2C}				0.4	V
SPI/ $\overline{I^2C}$ SPI Threshold	V_{SPI}		1.5			V
Output Logic Low (I ² C mode)	V_{OL_I2C}	$I_{SINK} = 3mA$			0.4	V
SPI/ $\overline{I^2C}$ SPI Supply Voltage	V_{OVDD}		1.5	min (V_{CC} , 5.5)		V
Output Logic-Low (SPI Mode)	V_{OL_SPI}	$I_{SINK} = 200\mu A$			$0.15 \times V_{OVDD}$	V
Output Logic-High (SPI Mode)	V_{OH_SPI}	$I_{SOURCE} = 200\mu A$			$0.85 \times V_{OVDD}$	V
ESD PROTECTION						
All A and B Pins		Human Body Model (HBM)		± 15		kV
All Others Pins		Human Body Model (HBM)		± 2		kV

Note 2: All devices are 100% production tested at $T_A = +25^{\circ}C$. Specifications over temperature are guaranteed by design.

Note 3: Guaranteed by design.

Note 4: Time between the turn-off of one channel to the turn-on of another channel when updated together.

Test Circuits/Timing Diagrams

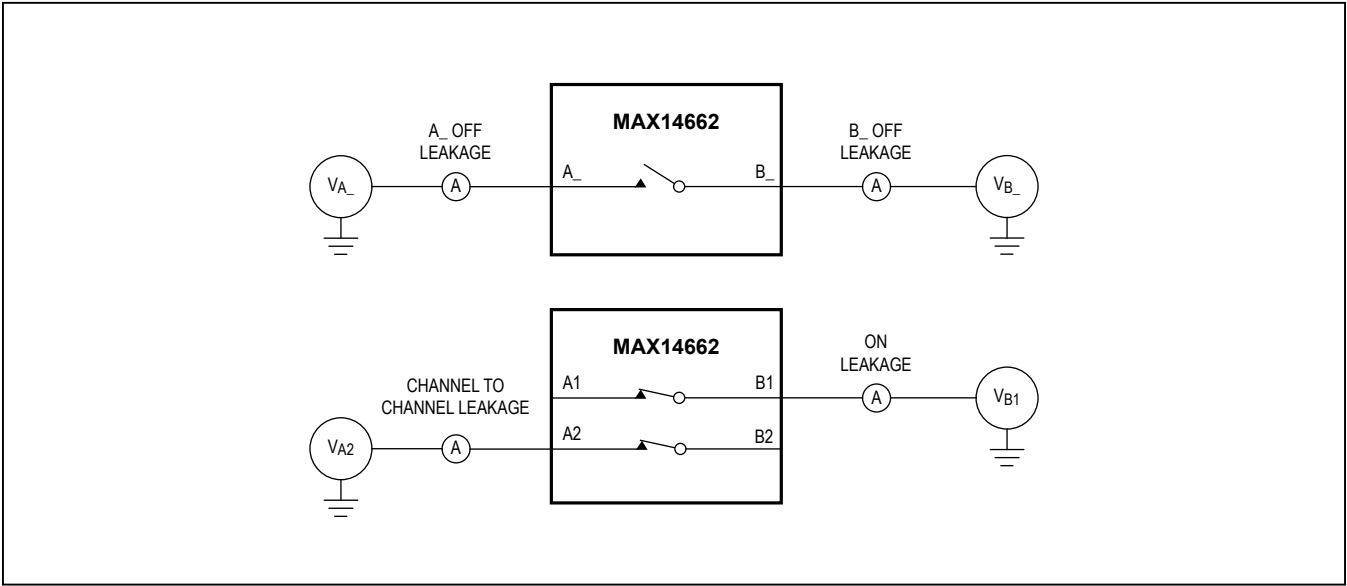


Figure 1. On-/Off-/Channel-to-Channel Leakage Current

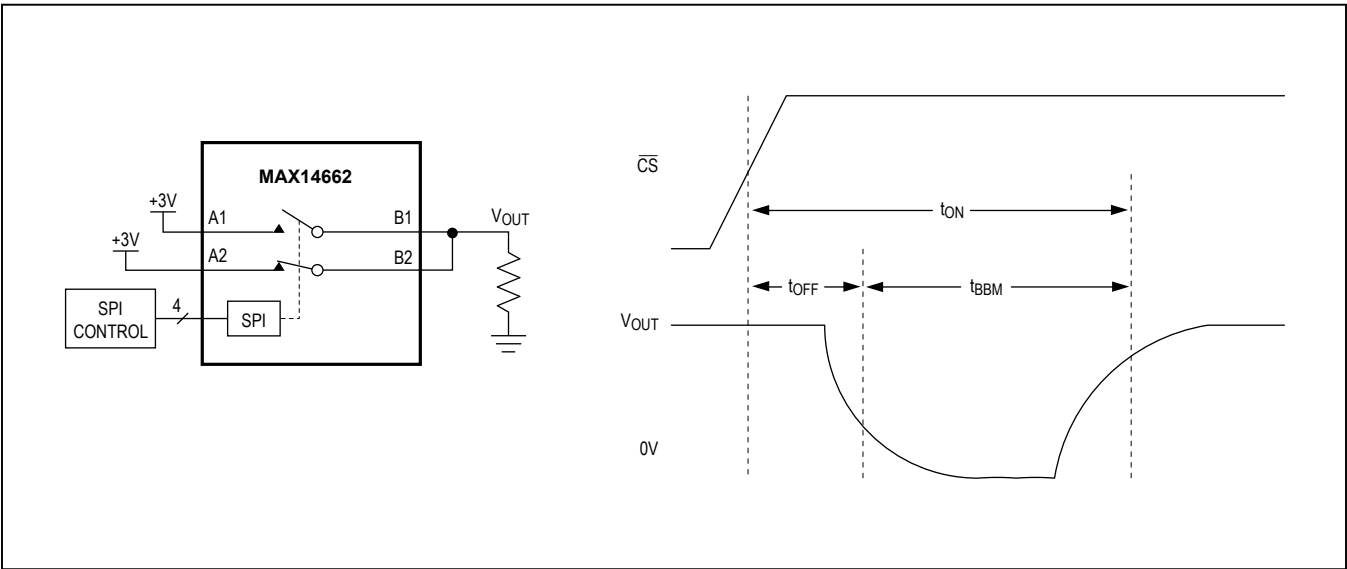


Figure 2. Turn-On/Turn-Off/Break-Before-Make

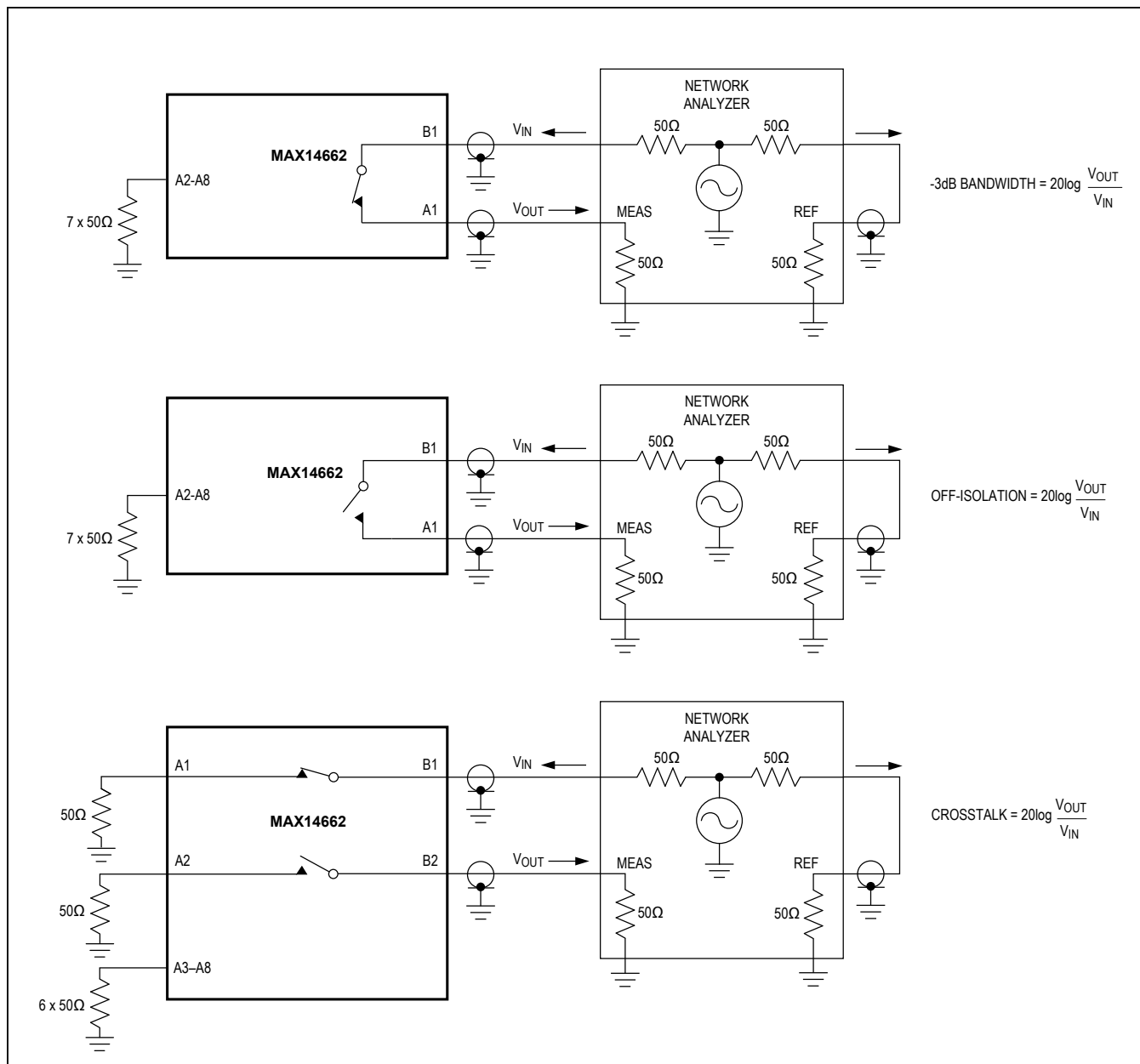
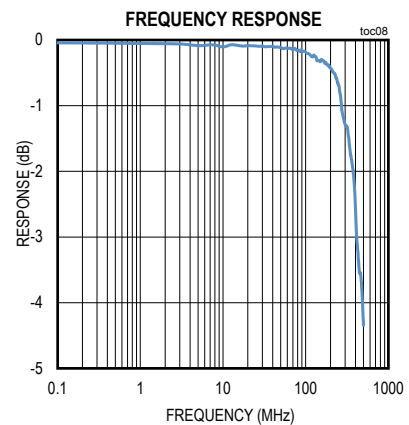
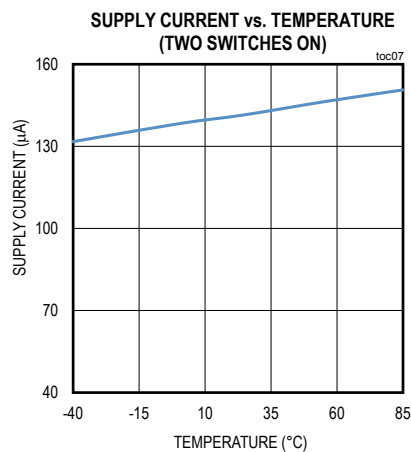
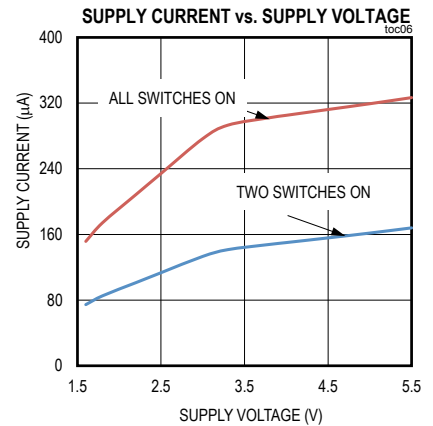
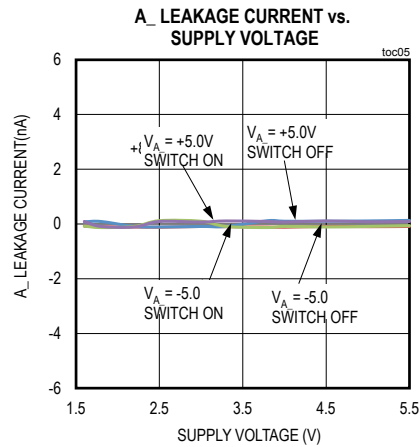
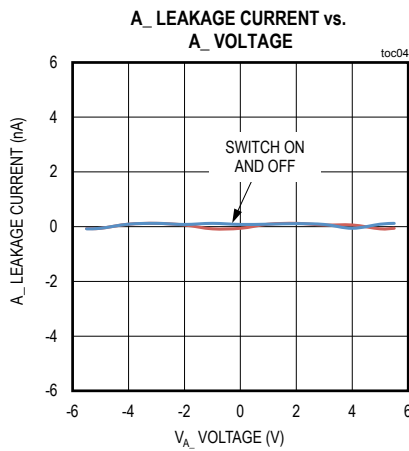
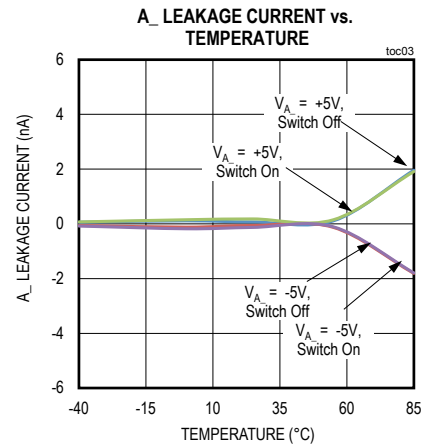
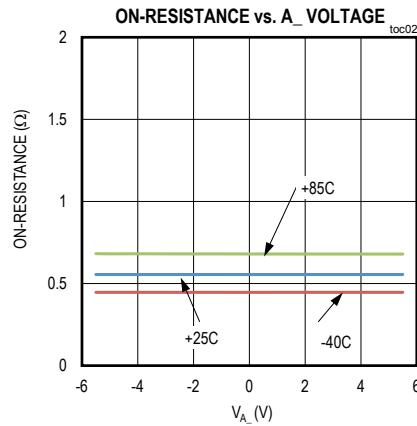
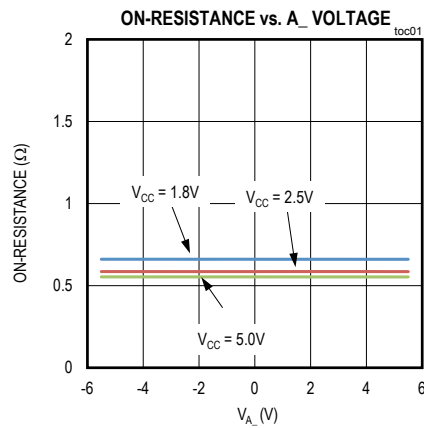


Figure 3. -3dB Bandwidth, Off-Isolation, and Crosstalk

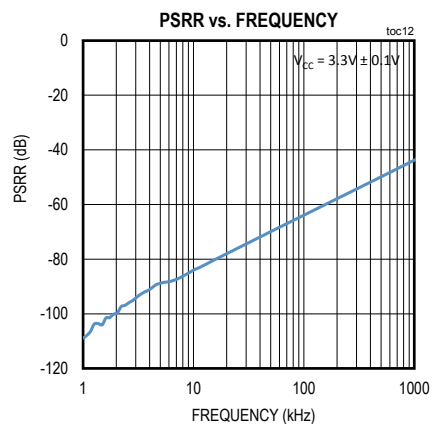
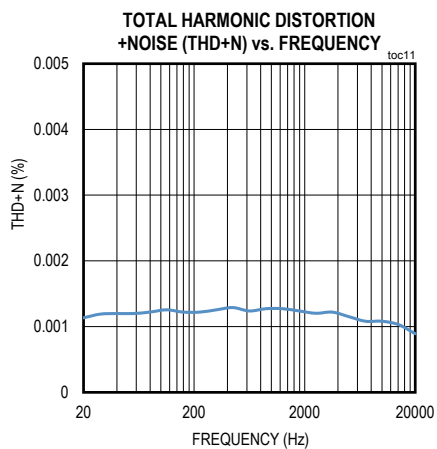
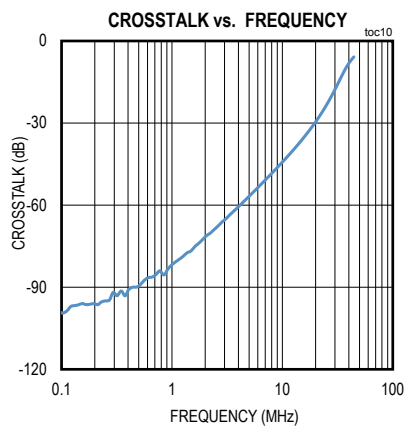
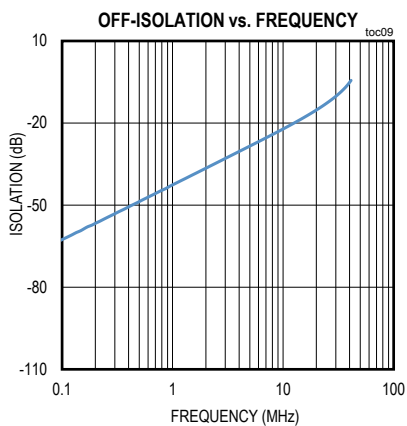
Typical Operating Characteristics

($V_{CC} = +1.6V$ to $+5.5V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

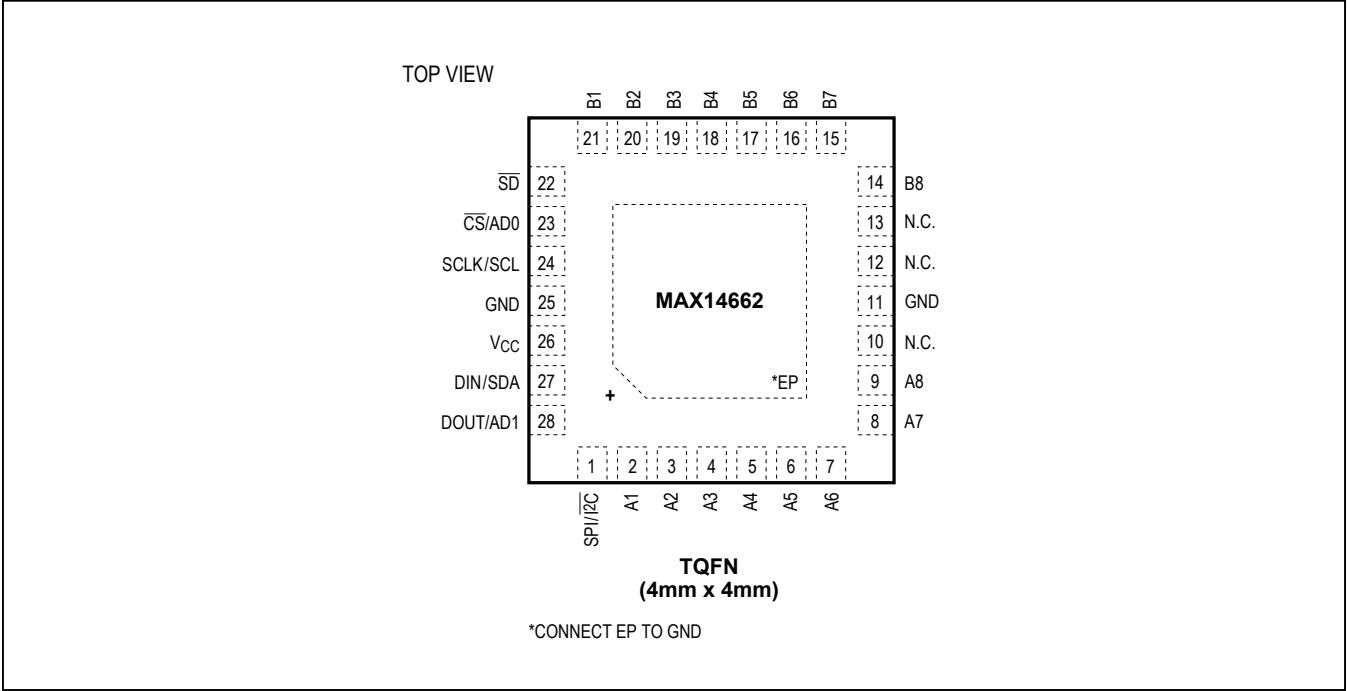


Typical Operating Characteristics (continued)

($V_{CC} = +1.6V$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$, $T_A = +25^{\circ}C$, unless otherwise noted.)



Pin Configurations



Pin Description

PIN	NAME	FUNCTION
1	SPI/ $\overline{\text{I2C}}$	Serial Mode Select. When SPI/ $\overline{\text{I2C}}$ is low, the device is in I^2C Mode. When SPI/ $\overline{\text{I2C}}$ is high, the device is in SPI mode. In SPI mode, SPI/ $\overline{\text{I2C}}$ also functions as supply input for DOUT.
2	A1	A Connection to Switch 1
3	A2	A Connection to Switch 2
4	A3	A Connection to Switch 3
5	A4	A Connection to Switch 4
6	A5	A Connection to Switch 5
7	A6	A Connection to Switch 6
8	A7	A Connection to Switch 7
9	A8	A Connection to Switch 8

Pin Description (continued)

PIN	NAME	FUNCTION
10	N.C.	Not Connected. Internally Not Connected.
11	GND	Ground
12	N.C.	Not Connected. Internally Not Connected.
13	N.C.	Not Connected. Internally Not Connected.
14	B8	B Connection to Switch 8
15	B7	B Connection to Switch 7
16	B6	B Connection to Switch 6
17	B5	B Connection to Switch 5
18	B4	B Connection to Switch 4
19	B3	B Connection to Switch 3
20	B2	B Connection to Switch 2
21	B1	B Connection to Switch 1
22	$\overline{SD}$	Active Low Shutdown. When $\overline{SD}$ is low, the device enters low power mode and turns all switches off.
23	$\overline{CS}/AD0$	SPI $\overline{CS}$ Signal/I2C Address Bit 0
24	SCLK/SCL	SPI Serial Clock/ I2C Serial Clock
25	GND	Ground
26	V_{CC}	Power-Supply Input
27	DIN/SDA	SPI Data Input/I2C Serial Data
28	DOUT/AD1	SPI Data Output/I2C Address Bit 1
—	EP	Exposed Pad. Internally connected to GND. Connect EP to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

Functional Diagram

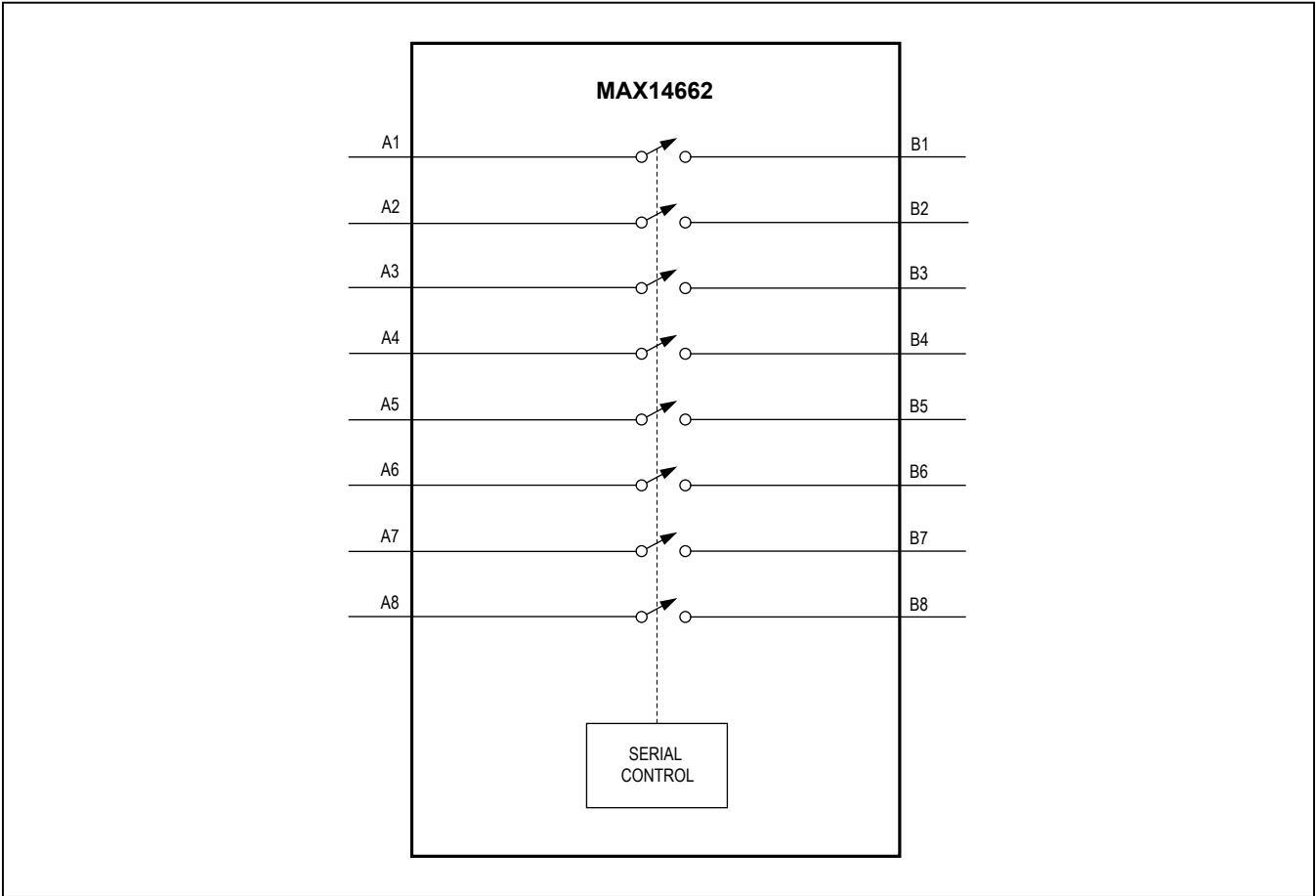


Table 1. Register Map

ADDRESS	NAME	TYPE	DEFAULT	DESCRIPTION
0x00	DIR0	RW	0x00	Switches 1-8 direct read/write access

Register Types: RW = Read/Write

Table 2. Detailed Register Map

DIR0 0x00								
BIT	7	6	5	4	3	2	1	0
BIT Name	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1
Reset Value	0	0	0	0	0	0	0	0
Description	Direct Register Data for SW8–1 0 = Switch open 1 = Switch closed							

Detailed Description

Low-Power Shutdown

The device includes an active-low shutdown pin ($\overline{SD}$). When $\overline{SD}$ is low, all registers are cleared and all switches are open. The serial interface is not functional when in shutdown. All switch connections are open and tolerant of the full $\pm 5.5V$ specified signal range. In this mode the part consumes minimal power.

SPI Output Supply

The $SPI/\overline{I^2C}$ pin has a dual purpose. In addition to selecting which serial protocol the part uses, it also functions as the I/O voltage power pin for the SPI DOUT signal. This allows the user to set the output voltage lower than the device supply voltage.

I²C Serial Interface

Direct Access

The direct access register (0x00) allows the user access to read or write the switches 8 at a time. The switches are updated after the last bit of the byte is clocked in.

Serial Addressing

When in I²C mode, the MAX14662 operates as a slave device that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX14662 and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open-drain output. A pullup resistor is required on SDA. The SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output. Each transmission consists of a START condition sent by a master, followed by the MAX14662 7-bit slave address plus R/W bit, a register address byte, one or more data bytes, and finally a STOP condition (Figure 4).

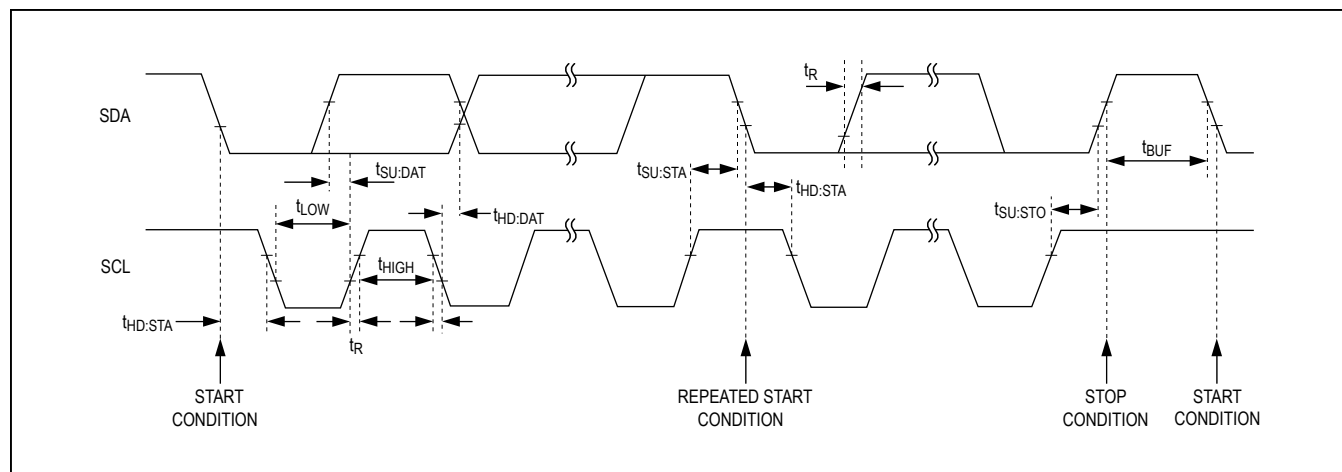


Figure 4. I²C Interface Timing Details

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (Figure 5). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 6). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 7), which the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9

bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX14662, it generates the acknowledge bit because the device is the recipient. When the device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. If the device did not pull SDA low, a not acknowledge is indicated.

Slave Address

The MAX14662 features a 7-bit slave address, configured by the AD0 and AD1 inputs. To select the slave address, connect AD0 and AD1 to GND or VCC, as indicated in Table 3. The MAX14662 has four possible addresses, allowing up to four MAX14662 devices to share the same interface bus. The bit following a 7-bit slave address is the R/W bit, which is low for a write command and high for a read command.

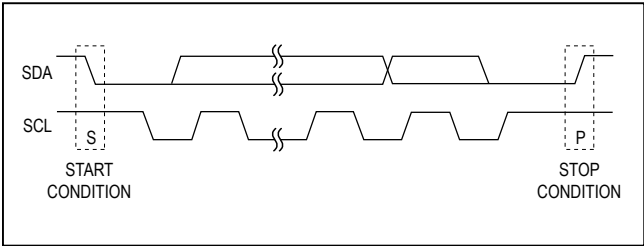


Figure 5. Start and Stop Conditions

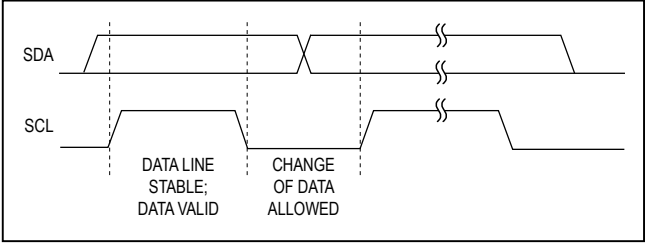


Figure 6. Bit Transfer

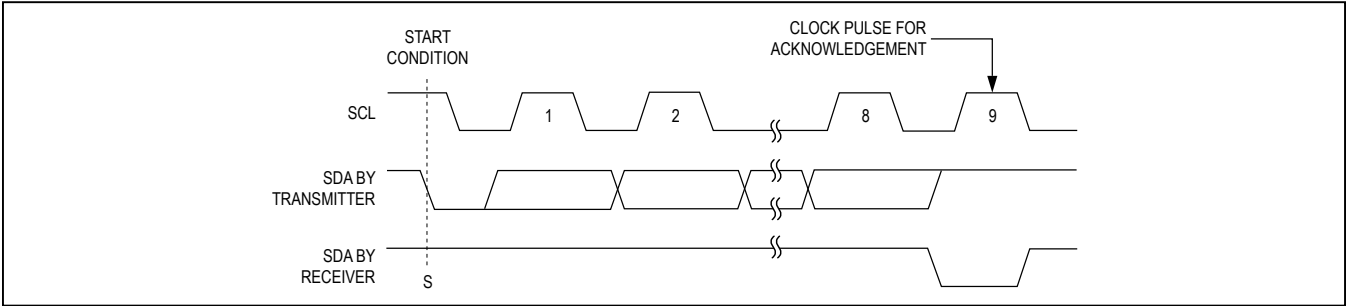


Figure 7. Acknowledge

Table 3. Slave Address Configuration

LOGIC INPUTS		I2C SLAVE ADDRESS									
AD1	AD0	A6	A5	A4	A3	A2	A1	A0	R/W	READ ADD	WRITE ADD
0	0	1	0	0	1	1	0	0	1/0	0X99	0X98
0	1	1	0	0	1	1	0	1	1/0	0X9B	0X9A
1	0	1	0	0	1	1	1	0	1/0	0X9D	0X9C
1	1	1	0	0	1	1	1	1	1/0	0X9F	0X9E

Bus Reset

The MAX14662 resets the bus with the I²C start condition for reads. When the $\overline{R/W}$ bit is set to 1, the device transmits data to the master, thus the master is reading from the device.

Format for Writing

A write to the MAX14662 comprises the transmission of the slave address with the $\overline{R/W}$ bit set to zero, followed by at least 1 byte of information. The first byte of information is the register address or command byte. The register address determines which register of the device is to be written by the next byte, if received. There is only one register in the MAX14662, so this byte should always be written to 0x00. If a STOP (P) condition is detected after

the register address is received, then the device takes no further action. The byte received after the register address is the data byte. The first data byte goes into the DIR register if it was preceded by the address 0x00 (Figure 8).

Format for Reading

Because the MAX14662 only has one register address, it always returns the data from this register. A register address can be selected by sending a 1-byte I²C write prior to the read, but it has no effect and is optional. To read, transmit the slave address with the $\overline{R/W}$ bit set to 1. If the slave address matches the address selected by pins AD0 and AD1, the MAX14662 will acknowledge the address and provide the 8 bits of data (Figure 9).

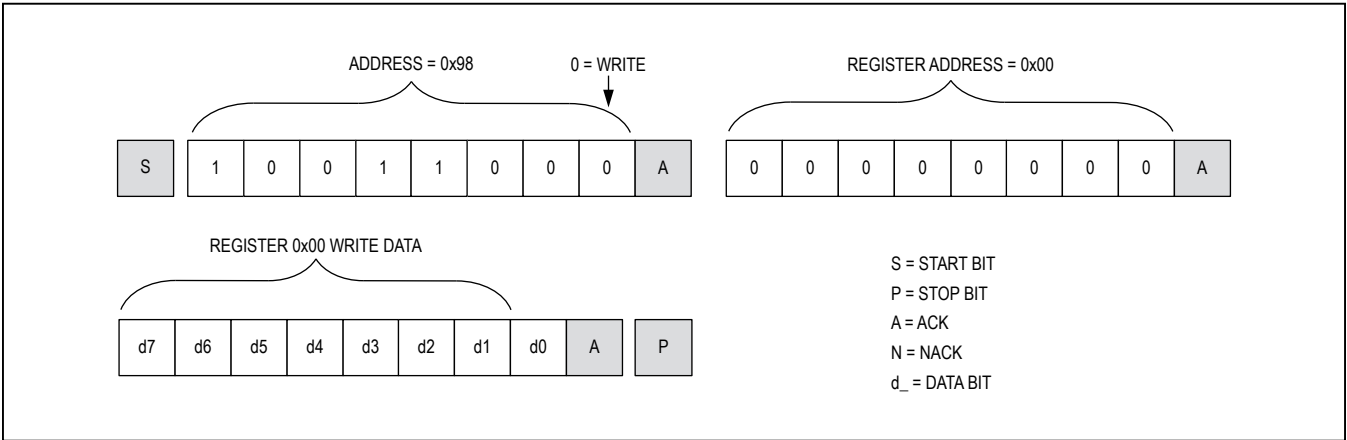


Figure 8. Format for I²C Write

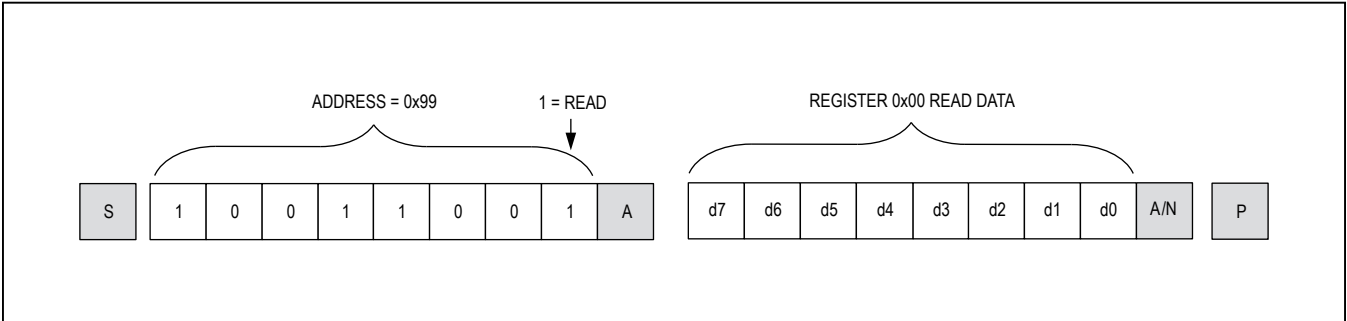


Figure 9. Format for Writing to Multiple Registers

SPI Interface

In SPI mode, the part will operate a shift register designed to work with common serial interfaces. The bits are shifted through so that a large serial chain can be made to minimize pins needed for a system with multiple devices. See [Figure 15](#). This shift register is also designed to be compatible with common microcontroller SPI type interfaces. The switches in the MAX14662 are all transitioned simultaneously. To update the switches in SPI mode, the user must shift in a bit with the desired state of each

switch. The switches are updated at the rising edge of $\overline{CS}$ with the last 8 bits of data shifted in only if the number of bits clocked in is greater than or equal to the number of switches (8). The data on the DOUT pin represents the end of the shift register. This will output the contents of the shift register followed by the data being shifted in on the DIN pin. Please note that the data in the shift register may not be the same as the state of the switches if there were insufficient clocks at the last rising edge of $\overline{CS}$. See [Figure 10](#) and [11](#) for the SPI timing diagrams.

Table 4. SPI Data Format

BYTE	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Data	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1

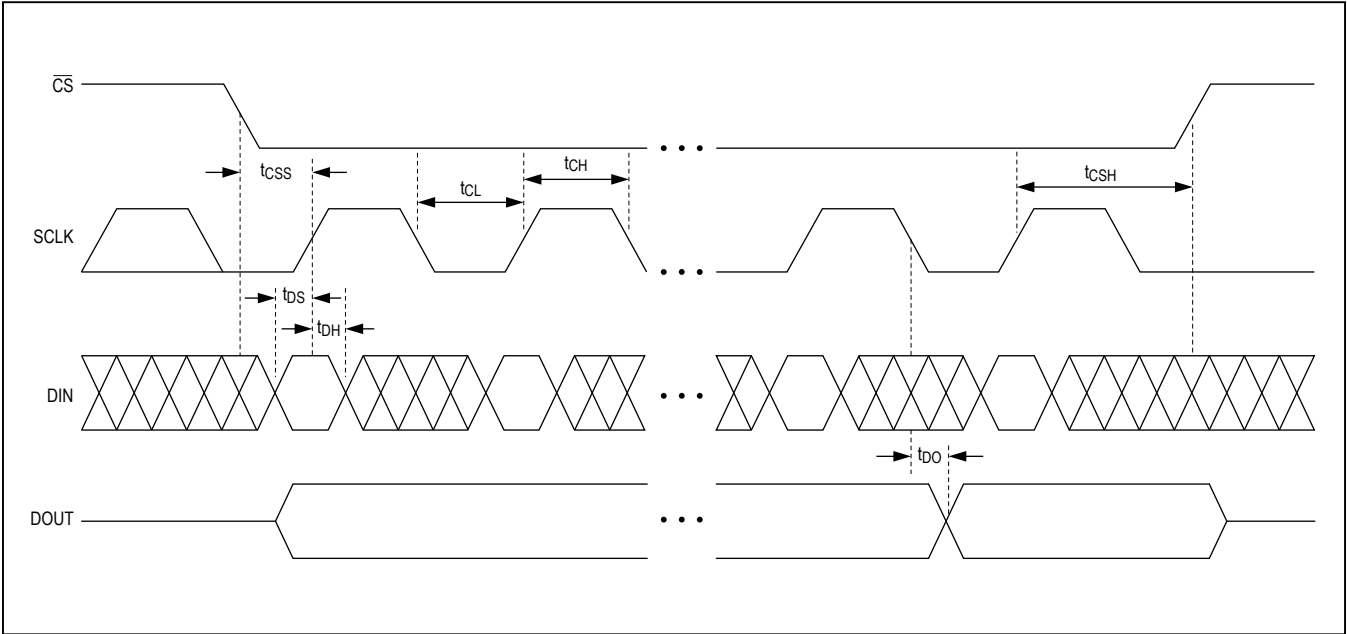


Figure 10. SPI Timing Details

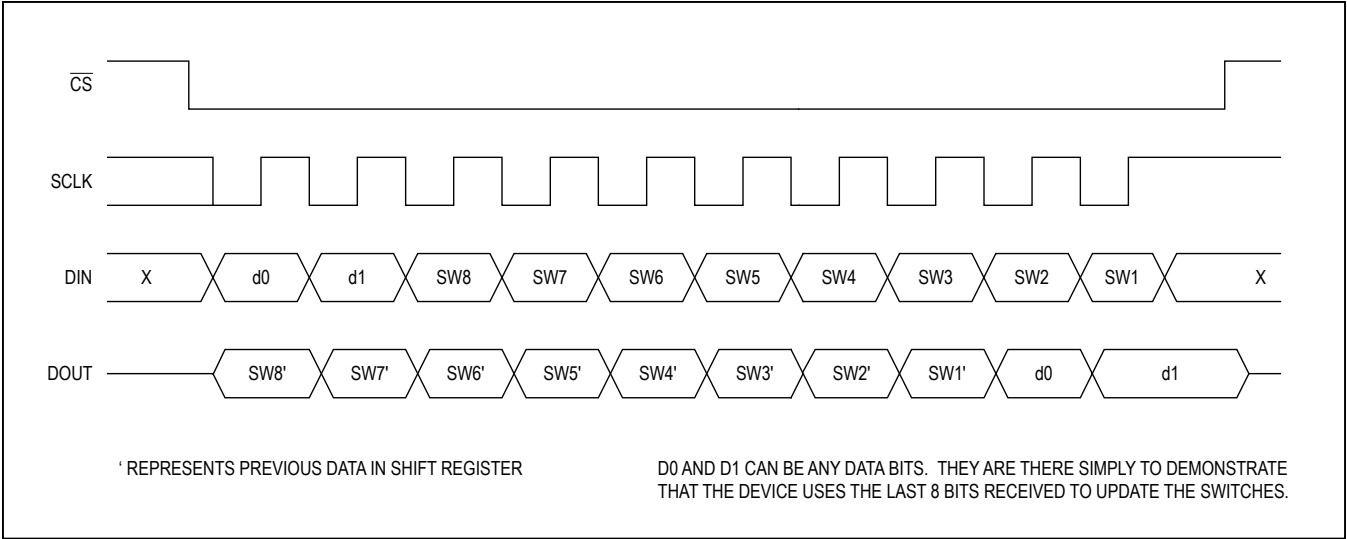


Figure 11. SPI Timing Diagram

Applications Information

Serial Bus Configurations

The MAX14662 is designed to support a wide variety of multiplexing applications. Multiple devices can be used in a system to expand the number of ports being multiplexed. With the two address-select pins provided in I²C mode, four devices can be attached to the same I²C bus simultaneously using only two pins. There are also several options for addressing multiple devices when using the SPI interface. Using only three pins on the microcon-

troller, as many devices as desired can be loaded by connecting all the CS and SCLK pins in parallel and chaining the DOUT pin from one device to the DIN pin on the next. It is also acceptable to provide a separate CS pin for each device so that they can be individually addressed and loaded. Alternatively a separate data line can be used for each device to reduce the time required to load all the devices. Some of the options and tradeoffs are listed in [Table 5](#), as well as example application diagrams in the [Typical Application Circuit](#).

Table 5. Benefits and Limitations of Different Serial-Bus Configurations

SERIAL BUS	PINS	BENEFITS	LIMITATIONS
I ² C (Figure 14)	2	Fewest Pins	Maximum four devices per bus, slow protocol, no simultaneous updates across all devices
SPI Daisy Chain (Figure 15)	3	Faster than I ² C with only one additional pin, simultaneous updates across all devices in chain	n x 8 clocks required to load all devices
SPI Separate CS (Figure 16)	n+2	Common SPI implementation, quick for single device updates	n x 8 clocks required to load all devices, requires an additional pin per device, no simultaneous updates across all devices
SPI Separate Data (Figure 17)	n+2	Fastest loading for multiple devices, simultaneous updates across all devices	Requires an additional pin per device, may not be supported by SPI controller

Extended ESD

ESD protection structures are incorporated on all pins to protect against electrostatic discharges up to $\pm 2\text{kV}$ (HBM) encountered during handling and assembly. A_{-} and B_{-} are further protected against ESD up to $\pm 15\text{kV}$ (HBM) without damage. The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the MAX14662 continues to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 12 shows the Human Body Model. Figure 13 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a $1.5\text{k}\Omega$ resistor.

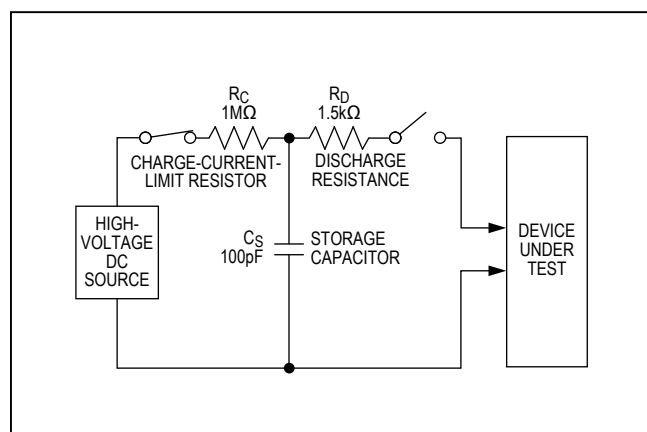


Figure 12. Human Body ESD Test Model

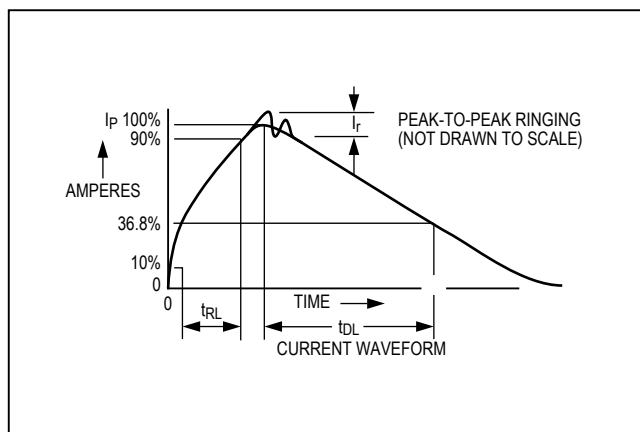
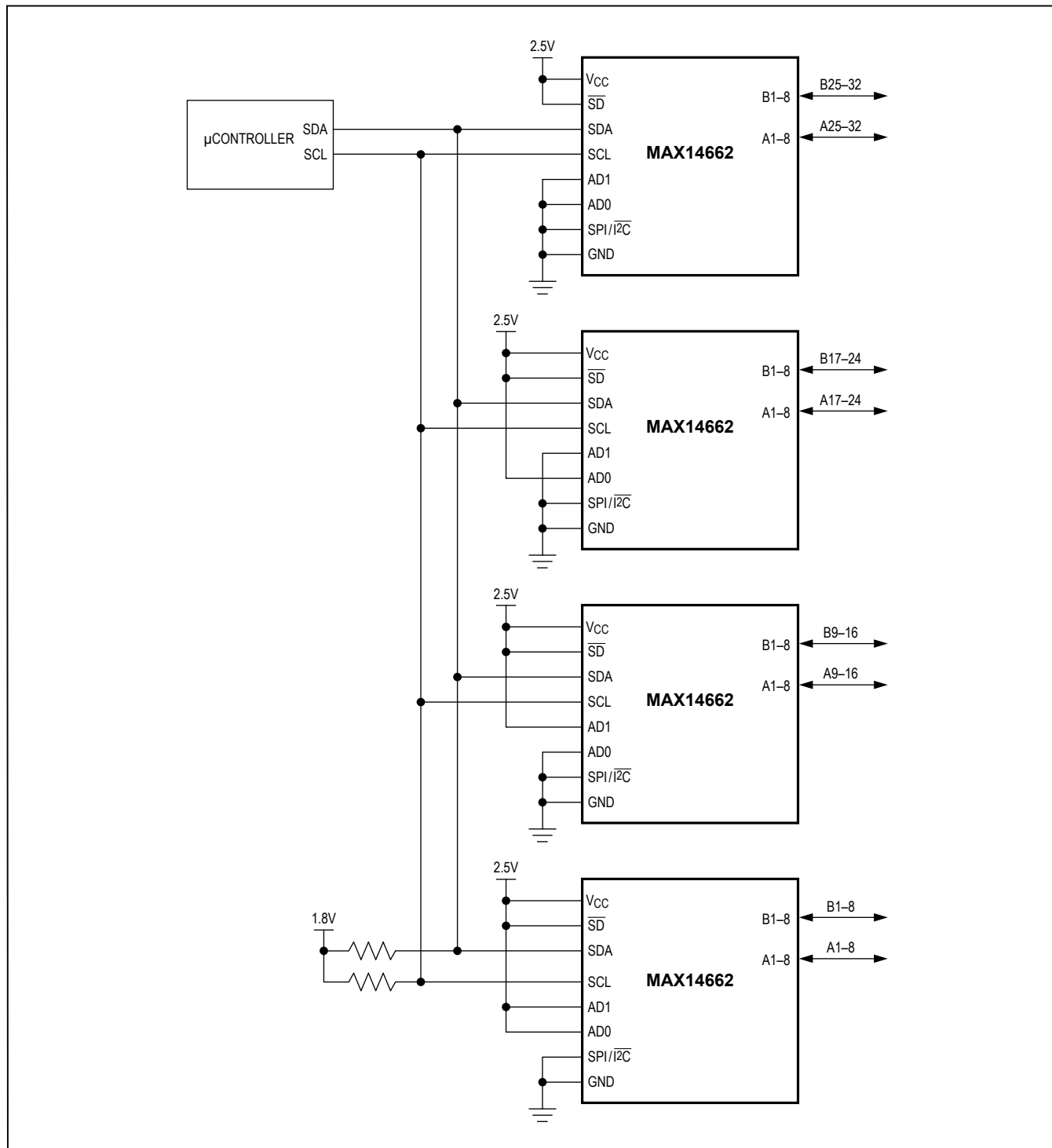


Figure 13. Human Body Current Waveform

Typical Application Circuit

Figure 14. I²C 32 Switches

Typical Application Circuit (continued)

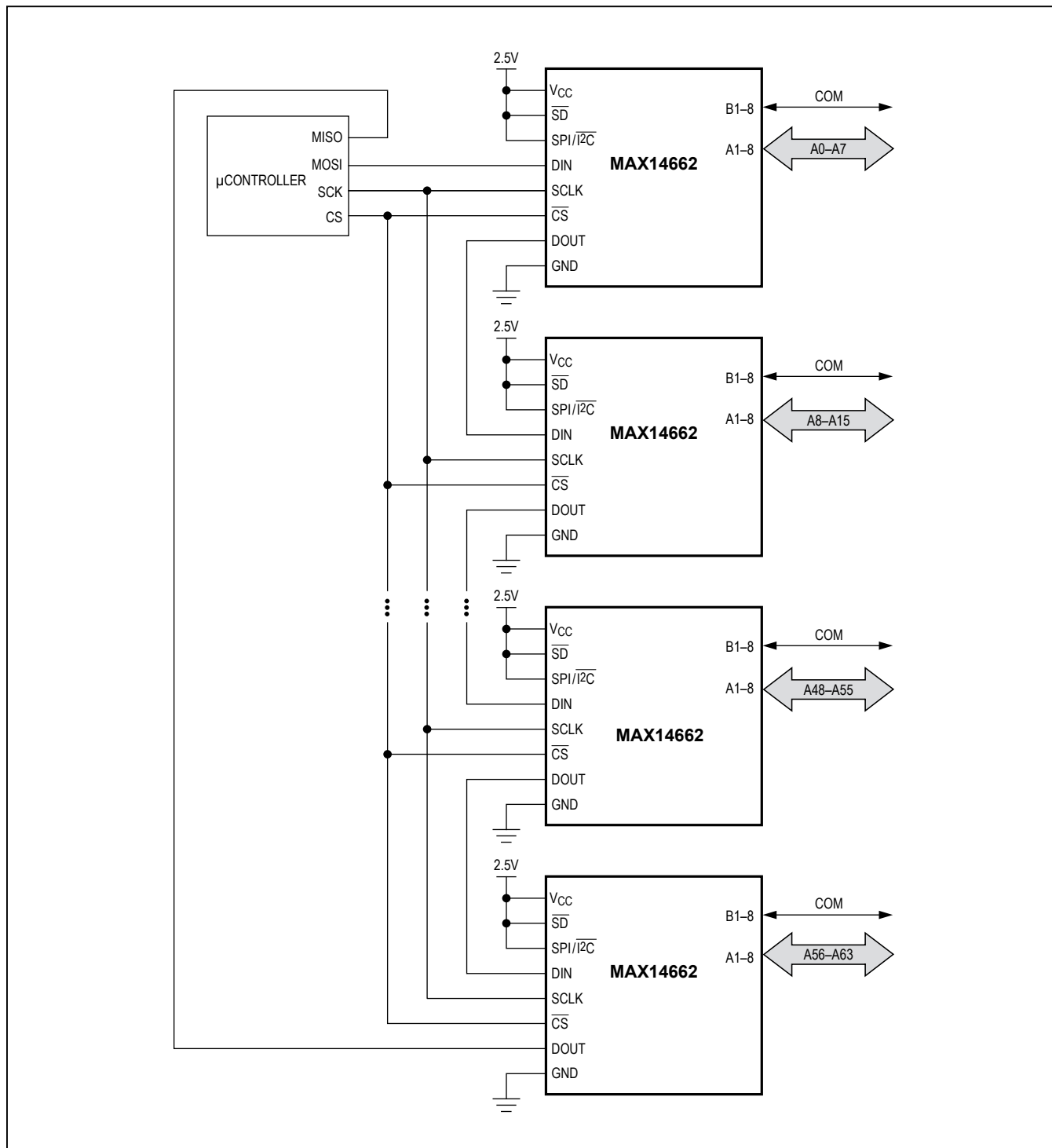


Figure 15. SPI Daisy Chain 64:1 MUX

Typical Application Circuit (continued)

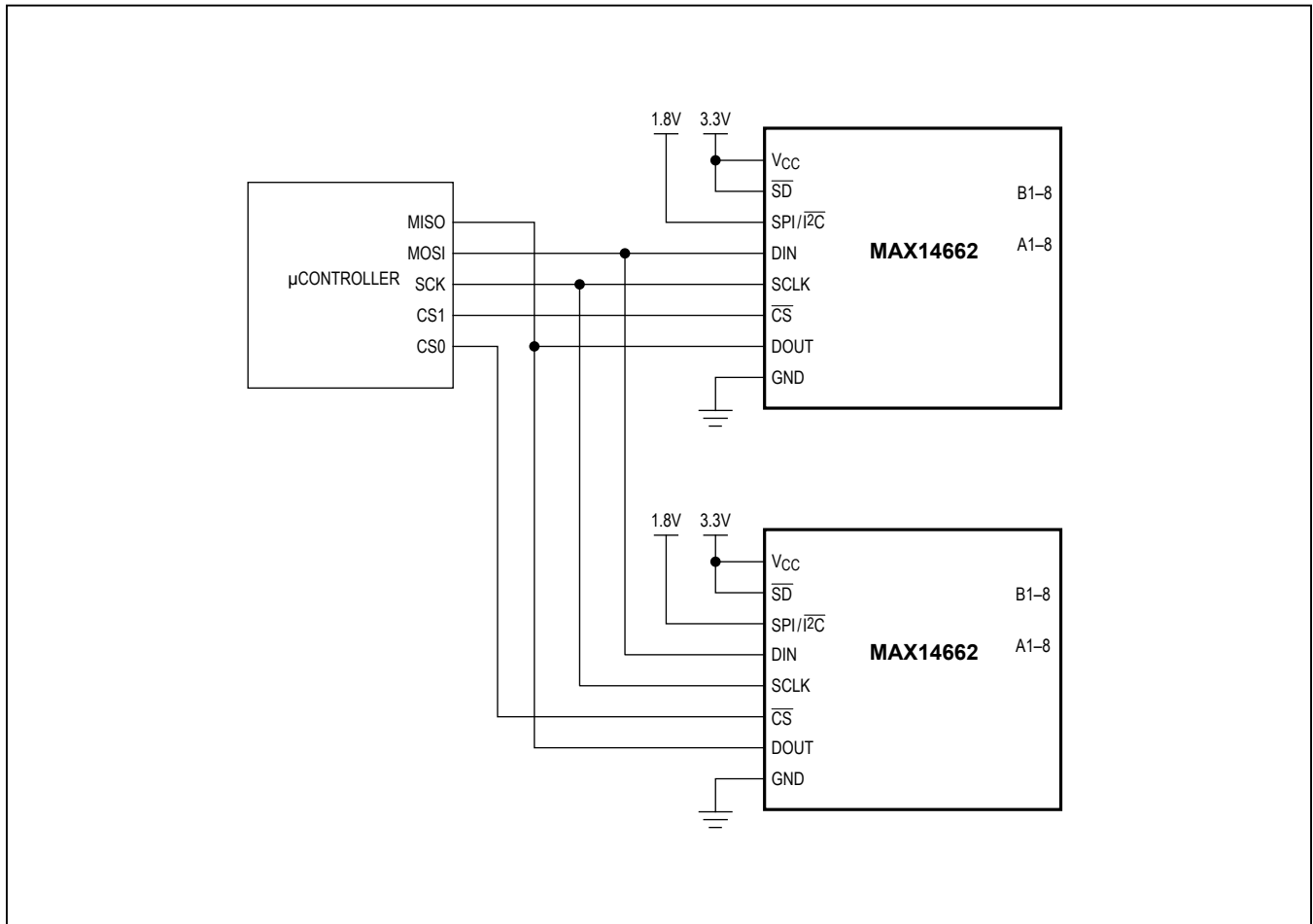


Figure 16. SPI Separate CS

The diagram illustrates a 4x8-bit parallel-to-serial converter using four MAX14662 shift registers. The registers are arranged in two columns of two. Each register has the following pins and connections:

- V_{CC}**: Connected to 3.3V.
- SPI/I²C**: Connected to 3.3V.
- SD**: Connected to 3.3V.
- DIN**: Connected to a common data bus (D7-D0).
- SCLK**: Connected to a common serial clock (SCK).
- CS**: Connected to a common chip select (CS).
- DOUT**: Connected to a common output bus (B7-B0).
- GND**: Connected to ground.

The output of each register is labeled B7, B6, B5, B4, B3, B2, B1, and B0, respectively. The common data bus (D7-D0) and serial clock (SCK) are connected to the DIN and SCLK pins of all registers. The common chip select (CS) is connected to the CS pin of all registers. The common output bus (B7-B0) is connected to the DOUT pin of all registers.

Figure 17. SPI Separate Data 8:8 crosspoint

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14662ETI+	-40°C to +85°C	28 TQFN-EP (4mm x4mm, 0.4mm)
MAX14662ETI+T	-40°C to +85°C	28 TQFN-EP (4mm x4mm, 0.4mm)

+Denotes lead(Pb)-free/RoHS-compliant package.

T = Tape and reel

*EP = Exposed Pad.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TQFN-EP	T2844+1C	21-0139	90-0035

Chip Information

PROCESS: CMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/14	Initial release	—
1	6/14	Correct x-axis on TOC 7	7

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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