TPS74x01EVM-118

This user's guide describes the characteristics, operation, and use of the TPS74x01EVM-118 evaluation module (EVM). This EVM contains either the TPS74201, TPS74301 or TPS74401 low dropout linear regulator IC. This user's guide includes EVM specifications, recommended test setup, test results, bill of materials (BOM), and a schematic diagram.

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1 Introduction

The Texas Instruments TPS74x01EVM-118 evaluation module uses either the TPS74201, TPS74301 or TPS74401 low-dropout linear regulator IC. These regulators require a low power bias voltage, V_{BIAS}, and a power input voltage, V_{IN}. All three regulators are capable of providing output voltages down to 0.8 V and have an integrated supervisory circuit with open drain output that goes to high impedance when the output voltage reaches regulation (power good or PG). The TPS74301 can provide up to 1.5 A dc current and has a TRACK pin which allows the user to input a ramp signal for the output voltage to follow, effectively implementing either simultaneous or ratiometric sequencing. The TPS74201 and TPS74401 can provide up to 1.5 A and 3.0 A dc current, respectively, and have a SS pin which allows the user to set the output voltage's linear ramp rate. The goal of the EVM is to facilitate evaluation of the TPS74x01 ICs.

1.1 Performance Specification Summary

Table 1 provides a summary of the TPS74x01EVM-118 performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Typical Performance Specification Summary

	CONDITION	VOLTAGE RANGE (V)			CURRENT RANGE (mA)		
		MIN	TYP	MAX	MIN	TYP	MAX
V_{BIAS} supply		2.62(1)	5.0	5.25		2	
V_{IN} supply	TPS74201 (HPA118-002), TPS74301 (HPA118-003)	1.31(1)	3.3	5.25(2)			1500
	TPS74401 (HPA118-001)	1.32(1)	3.3	5.25(2)			3000
V_{OUT}	TPS74201 (HPA118-002), TPS74301 (HPA118-003)	1.18(3)	1.20	1.22(3)			1500(2)
	TPS74401 (HPA118-001)	1.18(3)	1.20	1.22(3)			3000(2)

(1) This is the minimum voltage to provide the maximum output current in the table assuming the typical V_{BIAS} voltage is applied. Lower output currents are achievable with lower V_{IN} and V_{BIAS} voltages. See datasheet for V_{IN} to V_{OUT} and V_{BIAS} to V_{OUT} dropout data.

(2) Linear regulator power dissipation is computed as $P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$. As specified in the data sheet, the regulator's package has a finite power dissipation rating depending on the ambient temperature, board type and airflow. Using V_{IN} and/or V_{OUT} voltages other than the typical voltages recommended in the table or using the EVM in an environment with an ambient temperature higher than 25°C will significantly reduce the maximum allowed output current. See the datasheet for the regulator package's thermal resistance data and refer to application note SLVA118 entitled *Digital Designer's Guide to Linear Voltage Regulators and Thermal Management* for a full explanation.

(3) The EVM uses ±1% feedback resistors. Therefore, the EVM output tolerance is the ±1% internal reference tolerance plus $2 \times (1 - V_{REF}/V_{OUT}) \times TOL_{FBRES} = 2 \times (1- 0.8V/1.2V) \times \pm 1\% = 0.7\%$ or ±1.7%. For tigher output tolerance, tighter tolerance feedback resistors must be used.

1.2 Modifications

To aid user customization of the EVM, the board was designed with devices having 0603 or larger footprints. A real implementation would likely occupy less total board space.

Changing components can improve or degrade EVM performance. For example, adding a larger output capacitor will reduce output voltage undershoot but lengthen response time after a load transient event.

2 Input/Output Connector Descriptions

J1–VIN/GND This terminal block has both a positive and ground return connection to the power input (V_{IN}) supply. The leads to the input supply should be twisted and kept as short as possible.

J2–GND This header is the return connection for the bias (V_{BIAS}) supply.

J3–VIN This header is a positive connection to the power input supply (V_{IN}). Its use is recommended for low power (i.e., $I_{IN} = I_{OUT} < 1A$) evaluation or as a voltage test point.

J4–VBIAS This header is the positive connection for the bias (V_{BIAS}) supply.

J5–GND This header is a ground return connection to the power input (V_{IN}) supply. Its use is recommended for low power (i.e., $I_{IN} = I_{OUT} < 1A$) evaluation or as a ground test point.

J6–VOUT This header is the positive connection for the output load on V_{OUT}. Its use is recommended for low power (i.e., $I_{IN} = I_{OUT} < 1A$) evaluation only or as a voltage test point.

J7–GND This header is the ground return connection for the output load. Its use is recommended for low power (i.e., $I_{IN} = I_{OUT} < 1A$) evaluation or as a ground test point.

J8–VOUT/GND This terminal block has both a positive and ground return connection for the output load. The leads to the output load should be twisted and kept as short as possible.

J9–TRACK IN This header connects to top resistor of a resistor divider whose mid point connects to the TRACK IN pin of the TPS74301. An external voltage greater than 0.8 V must be applied to this pin for the TPS74301 to produce an output voltage. This header is not populated on the TPS74201 or TPS74401 EVM.

J10–EN This header is a connection to the enable pin (EN), which is also connected to the middle pin of S1. When S1 is OFF, the EN pin is pulled to ground through pull-down resistor.

J11–GND This header is a ground connection.

JP1– 1ms/Simult vs. 10ms/Ratio For the TPS74301, this jumper allows the user to select the appropriate resistor divider for either simultaneous or ratiometric sequencing. These resistors have been sized per the equations in datasheet Figure 5 assuming an external 3.3 V ramp signal is applied to J9 TRACK IN pin. Selecting SIMULTaneous results in the TPS74301 output voltage following the external ramp signal within a few millivolts until the TPS74301 reaches its regulated voltage. The TPS74301 output voltage will have the same ramp rate (dv/dt) as the external ramp signal but a different soft-start time. Selecting RATIOmetric results in the TPS74301 output voltage reaching its regulated voltage at the same time as the externally applied tracking signal reaches its maximum voltage (e.g., 3.3 V). Although the external ramp signal and the TPS74301 will have different ramp rates, they will have the same soft-start time. Leaving the jumper open and not applying the track signal results in no output voltage. Leaving the jumper open and applying a dc track signal greater than 0.8V results in the output voltage ramping up with default soft-start time of 500 us.

For the TPS74201 and TPS74401, this jumper allows the user to choose either 1 ms or 10 ms soft start time for the output voltage. Leaving the jumper open results in the output voltage ramping up with default soft-start time of 500 us.

S1 - This switch connects to the EN pin of the IC and allows the user to turn the IC ON or OFF by connecting enable to either V_{BIAS} or ground through a pull-down resistor.

TP1 - This is a Kelvin test point to V_{IN}.

TP2 - This is a Kelvin test point to IC ground.

TP3 - This is a Kelvin test point to V_{OUT}.

2.1 Test Setup

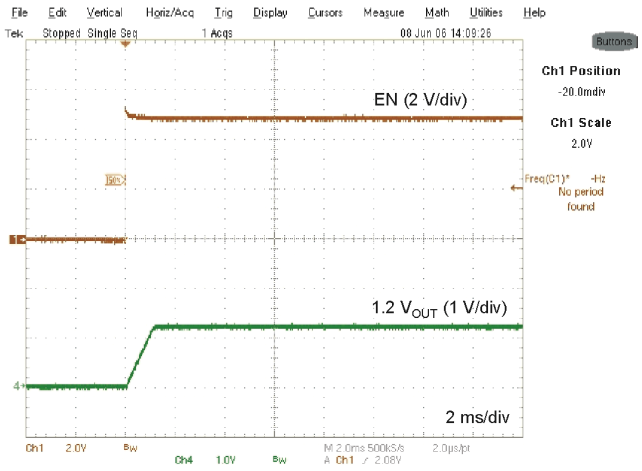
The absolute maximum voltage allowed on the BIAS, IN, EN or TRACK pins is 6 V. All three TPS74x01 devices are designed to operate with V_{IN} and V_{BIAS} less than or equal to 5.25 V. The TPS74201 and TPS74401 can have V_{IN}, V_{BIAS}, and V_{ENABLE} applied in any order without causing damage to the device. However, for the soft-start function to work as intended certain sequencing rules must be applied. With S1 in the OFF position, connecting the EN and IN pins through a jumper wire is acceptable for most applications as long as V_{IN} is greater than 1.1V and the ramp rate of both V_{IN} and V_{BIAS} is faster than the programmed soft-start ramp rate. If the ramp rate of the input sources is slower than the set soft-start time the output will track the slower supply minus the dropout voltage until it reaches the set output voltage. If EN is connected to BIAS (e.g., by placing S1 in the ON position on the EVM), the device will soft-start as programmed as long as V_{IN} is present before V_{BIAS}. Figure 5 in the datasheet shows the use of an RC delay circuit to hold off V_{EN} until V_{BIAS} has ramped. This technique can also be used to drive V_{EN} from V_{IN}.If V_{BIAS} > 2.375V and V_{EN} > 1.1V before V_{IN} is applied then V_{OUT} tracks the lower of V_{IN} or V_{SS} *(1+R1/R2), where V_{SS} is the voltage on the SS pin and is clamped to 0.8V. With S1 in the OFF position, an external control signal can also be used to enable the device after V_{IN} and V_{BIAS} are present.

The TPS74301 can also have V_{IN}, V_{BIAS}, V_{EN}, and V_{TRACK} sequenced in any order without causing damage to the device. However for the track function to work as intended certain sequencing rules must be applied. V_{BIAS} must be above 2.375 V and V_{EN} must be above 1.1V (e.g., S1 in the ON position tying the BIAS and EN pins together) before the externally applied track signal starts to ramp. V_{IN} should ramp up faster than the tracking signal so that the externally applied tracking signal does not drive the device into V_{IN} dropout as V_{OUT} ramps up. The preferred method to sequence the TPS74301 is for V_{IN}, V_{BIAS} and V_{EN} to be above their minimum required voltages before the tracking signal is applied and initates output voltage ramping. If the tracking feature is not needed, the TRACK pin should be connected to V_{IN}. Configured this way, the device starts up within 50us which may result in large inrush current that could cause the input supply to momentarily dip. Also, if the V_{IN} = V_{TRACK} ramps faster than 500 us, the output voltage may overshoot.

When connecting external loads above 1A, use short, twisted leads connected to the screw terminals in order to minimize DC drop at the connector and/or inductive voltage dip after a transient load is removed.

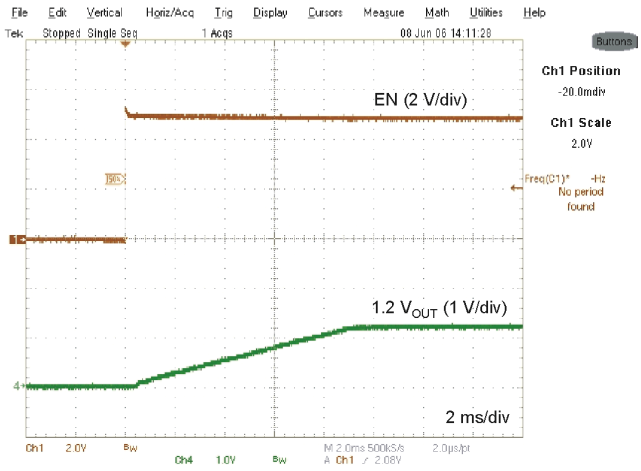
2.2 Test Results

Below are the test results at T_A = 25°C using this EVM:



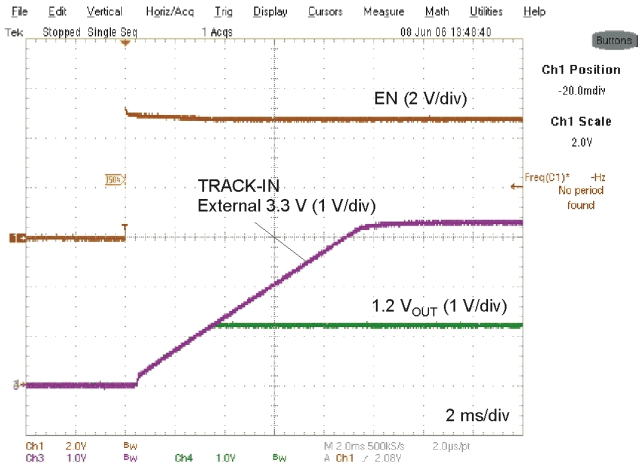
A V_{IN} = 5 V, V_{OUT}/I_{OUT} = 1.2 V / 1 A.

Figure 1. TPS74201 and TPS74401 Startup with 1-ms Soft Startup



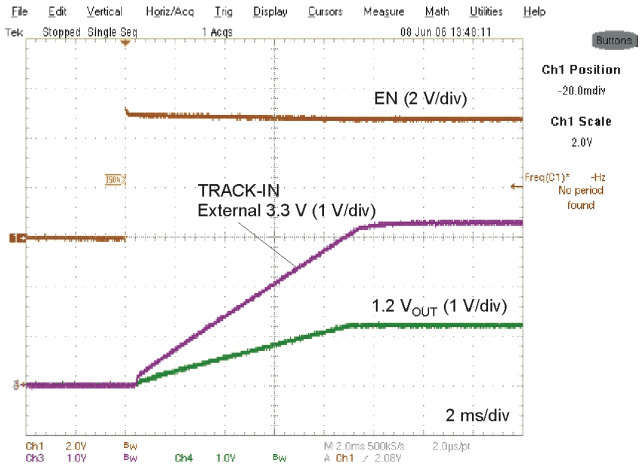
A V_{IN} = 5 V, V_{OUT}/I_{OUT} = 1.2 V / 1 A.

Figure 2. TPS74201 and TPS74401 Startup with 10-ms Soft Startup



A V_{IN} = 5 V, V_{OUT}/I_{OUT} = 1.2 V / 1 A with TRACK-IN signal provided by TPS74201 configured for 3.3 V and 10ms startup

Figure 3. TPS74301 Simultaneous Startup



A V_{IN} = 5 V, V_{OUT}/I_{OUT} = 1.2 V / 1 A with with TRACK-IN signal provided by TPS74201 configured for 3.3 V and 10ms startup

Figure 4. TPS74301 Ratiometric Startup

3 Board Layout

Board layout is critical for all switch mode power supplies. Figure 5, Figure 6, and Figure 7 show the board layout for the HPA118 PWB. The switching nodes with high-frequency noise are isolated from the noise-sensitive feedback circuitry, and careful attention has been given to the routing of high-frequency current loops. See the data sheet for more specific layout guidelines.

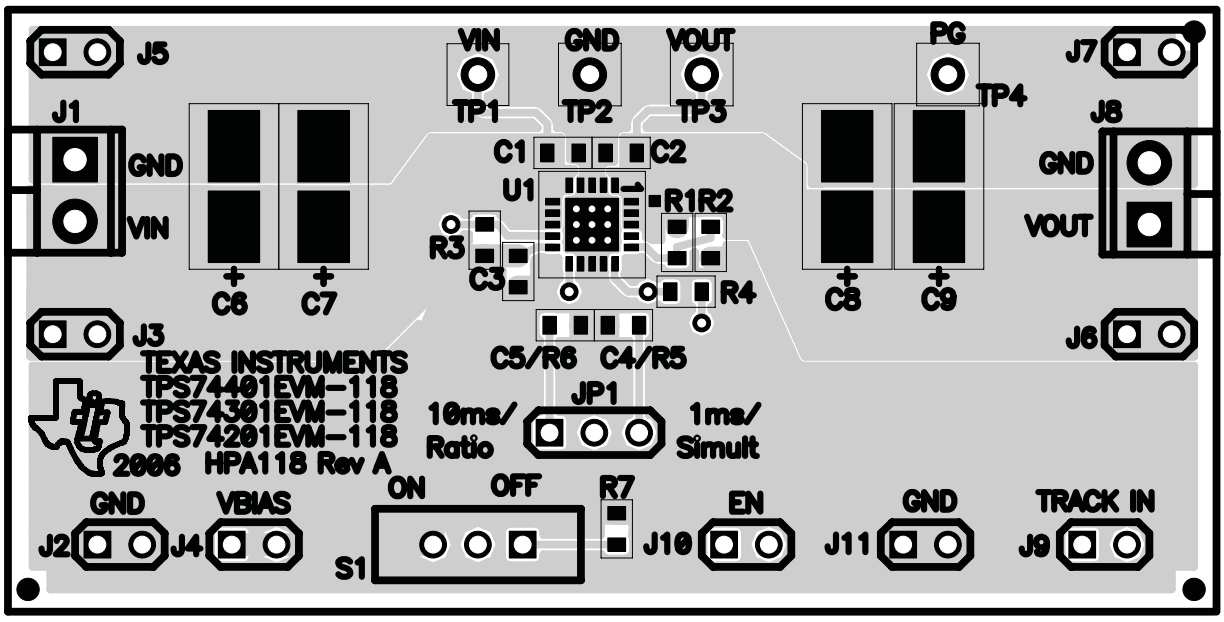


Figure 5. Top Assembly Layer

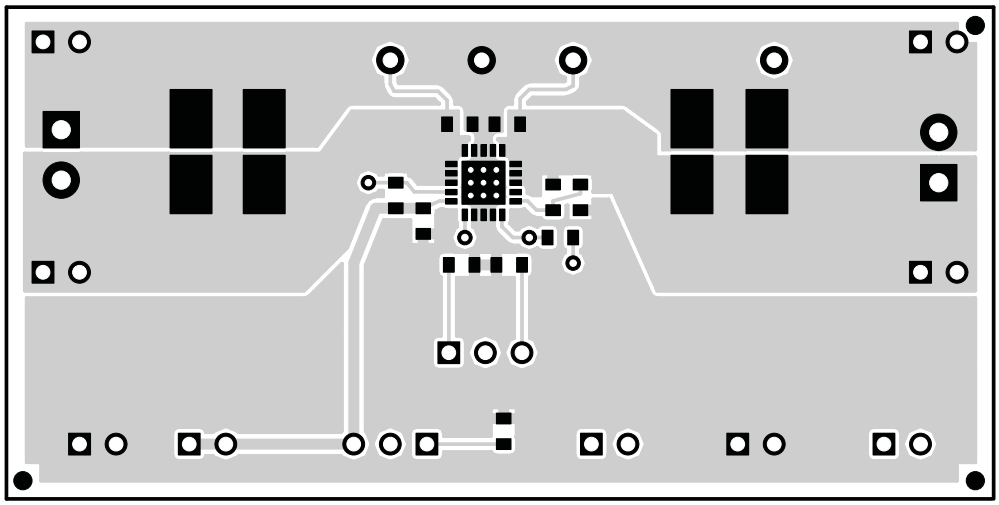


Figure 6. Top Layer

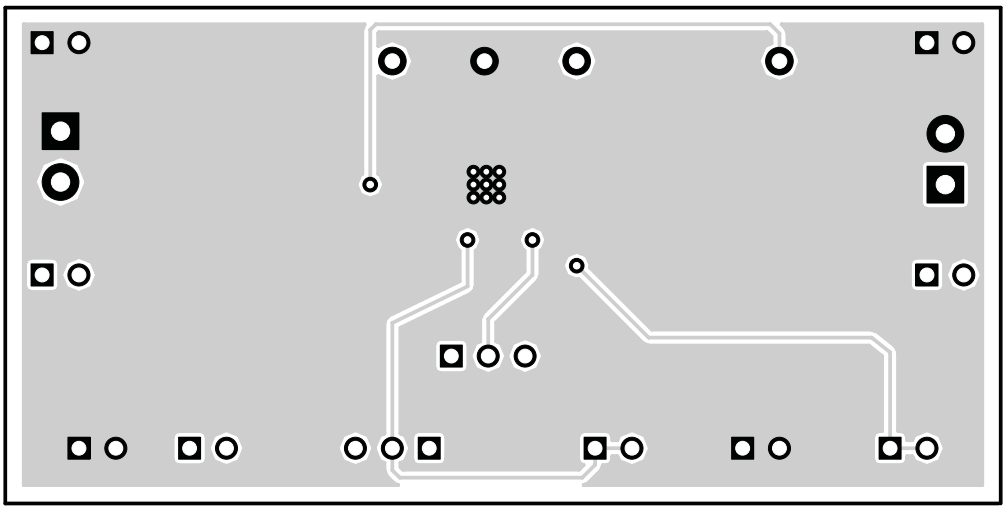
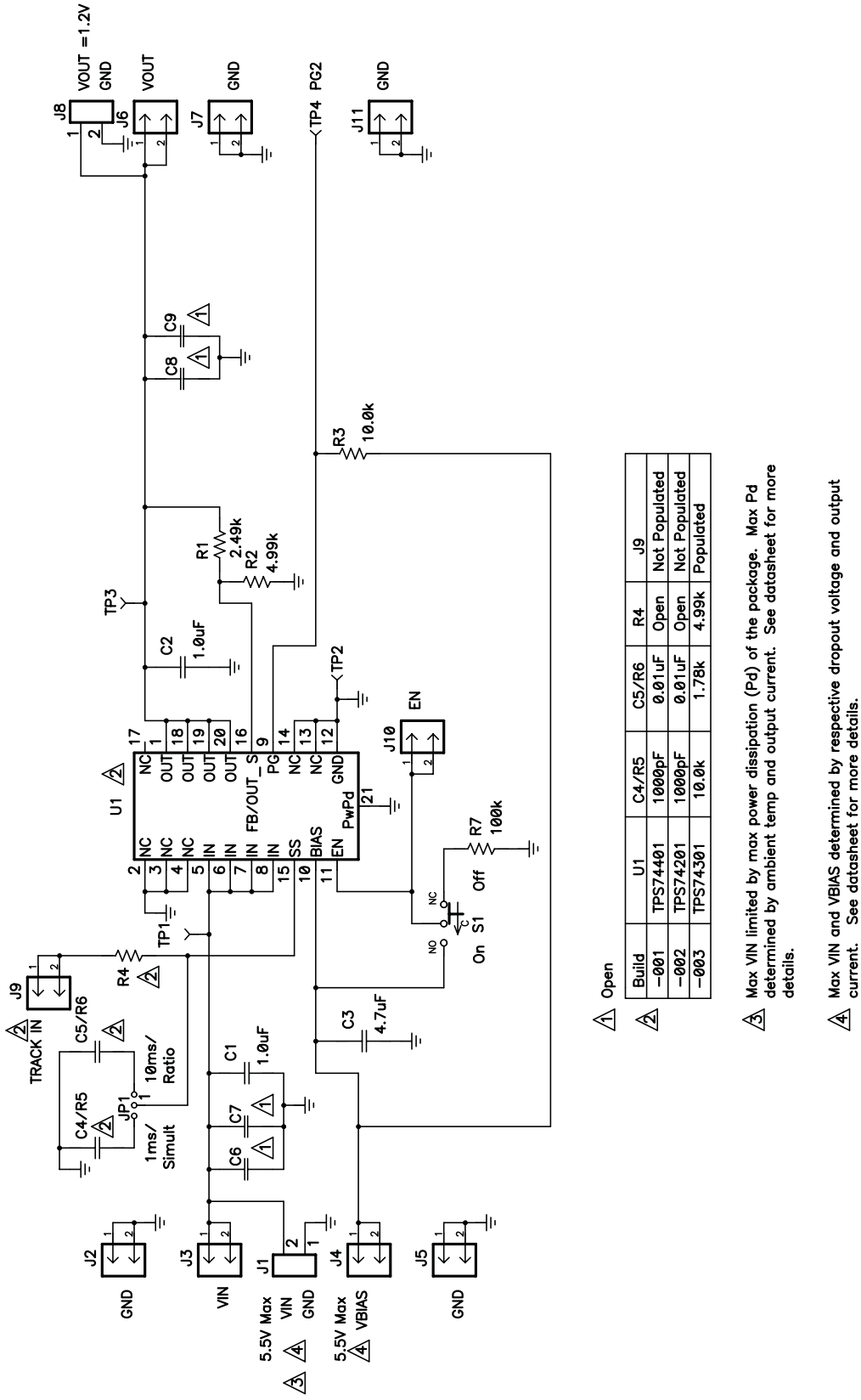


Figure 7. Bottom Layer



1 Open

Build	U1	C4/R5	C5/R6	R4	J9
-001	TPS74401	1000pF	0.01uF	Open	Not Populated
-002	TPS74201	1000pF	0.01uF	Open	Not Populated
-003	TPS74301	10.0k	1.78k	4.99k	Populated

2

3 Max VIN limited by max power dissipation (Pd) of the package. Max Pd determined by ambient temp and output current. See datasheet for more details.

4 Max VIN and VBIAS determined by respective dropout voltage and output current. See datasheet for more details.

Figure 8. Schematic

4 Bill of Materials and Schematic

4.1 Bill of Materials

Table 2. HPA118 Bill of Materials

Count			RefDes	Value	Description	Size	Part Number	MFR
-001	-002	-003						
2	2	2	C1, C2	1.0 µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	C1608X5R1E105K	TDK
1	1	1	C3	4.7 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	C1608X5R0J475K	TDK
1	1	0	C4	1000 pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H102JB	TDK
1	1	0	C5	0.01 µF	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H103KB	TDK
0	0	0	C6, C7, C8, C9	Open	Capacitor, Multi-pattern, 603-D case	7343 (D)		
2	2	2	J1, J8		Terminal Block, 2 pin, 6A, 3.5mm	0.27 x 0.25	ED1514	OST
8	8	8	J2 - J7, J10, J11		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins
0	0	1	J9		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins
1	1	1	JP1		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 x 3	PTC36SAAN	Sullins
1	1	1	R1	2.49 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	R2	4.99 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	R3	10.0 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	0	1	R4	4.99 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	0	1	R5	10.0 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	0	1	R6	1.78 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	R7	100 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	S1		Switch, 1P2T, Slide, PC mount, 200mA	0.46 x 0.16	EG1218	E_Switch
4	4	4	TP1 - TP4		Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100	5000	Keystone
1	0	0	U1		IC, 3.0A LDO With Programmable Soft Start	QFN-20	TPS74401RGW	TI
0	1	0			IC, 1.5A LDO With Programmable Soft Start	QFN-20	TPS74201RGW	TI
0	0	1			IC, 1.5A LDO With Programmable Sequencing	QFN-20	TPS74301RGW	TI
1	1	1	--		PCB, 2.7 In x 1.345 In x 0.062 In		HPA118	Any
1	1	1	--		Shunt, 100 mil, Black	0.100	929950-00	

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage of 5 V and the output voltage of 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 25°C. The EVM is designed to operate properly with certain components above 25°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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